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Master's Thesis

Interface trap and mobile charge density in dry oxidized 4H-SiC MOS structures in a wide temperature range

submitted at the Faculty of Electrical Engineering and Information Technology, TU Wien in partial fulfillment of the requirements for the degree of Master of Sciences

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Abstract

This master's thesis deals with the interface trap characterization of Si-face 4H-SiC (silicon-carbide) metal-oxide-semiconductor (MOS) structures realized by dry thermal oxidation. First, a detailed theoretical study of the 4H-SiC MOS structure in a wide temperature range is done to obtain theoretical capacitance-voltage (CV) curves. Experimentally, the D_{it} distribution is extracted using the high frequency Terman method, the low frequency capacitance method, the high-low frequency method and the conductance method in a temperature range from 150 to 600 K. Within this thesis a custom-built quasi-static (QS)-CV measurement circuit based on the improved feedback charge method is designed and realized and shows a high accuracy and a very low offset current. For a more detailed characterization mobile charge densities using the bias temperature stress (BTS) and the triangular voltage sweep (TVS) method are determined as well as breakdown measurements are performed. A very good agreement between the different interface trap characterization methods and rather low D_{it} values are extracted in a wide energy range of 0.05 eV up to 0.85 eV below the conduction band. Three different types of interface traps are identified. Besides the classic interface traps both near interface oxide traps (NIOTs) with a large response time constant and traps with a very short time constant are found additionally. The mobile charge density is measured to be in the $2 \cdot 10^{-12}$ cm^{-2} range. A large influence of pre-oxidation substrate cleaning to all investigated parameters is demonstrated.

Zusammenfassung

Diese Masterarbeit behandelt die Charakterisierung von Interface-Traps von trockenthermisch oxidierten Si-face 4H-SiC (Siliziumcarbid) 'metal-oxide-semiconductor' (MOS) Strukturen. In einem ersten Schritt wird eine detaillierte theoretische Untersuchung der MOS Struktur durchgeführt. Für den späteren Vergleich mit den experimentellen Daten wurden ideale capacitance-voltage (CV) Kurven in einem weiten Temperaturbereich berechnet. Die D_{it} Verteilung wird mithilfe der 'high frequency Terman' Methode, der 'low frequency capacitance' Methode, der 'high-low frequency' Methode und der 'conductance' Methode bestimmt. Eine Quasistatische (QS-)CV Messschaltung nach der 'improved feedback charge' Methode wurde speziell für diese Arbeit realisiert und überzeugt durch hohe Genauigkeit und niedrige Offsetströme. Ferner wird die Dichte an mobilen Ladungen mithilfe der 'bias temperature stress' (BTS) und der triangular voltage sweep' (TVS) Methode sowie die Durchbruchsspannung gemessen. Die extrahierten Werte der verschiedenen Interface-Trap Charakterisierungsmethoden stimmen sehr gut überein und generell wurden relativ niedrige D_{it} Konzentration in einem weiten Energiebereich von 0.05 eV bis 0.85 eV unter der Leitungsbandkante gemessen. Drei verschiedene Arten von Interface-Traps wurden gefunden: klassische Traps, 'near interface oxide traps' (NIOTs) mit einer sehr großen und Traps mit einer sehr kurzen Zeitkonstante. Die Dichte der mobilen Ladungen im Oxid liegt im Bereich von $2 \cdot 10^{-12}$ cm^{-2}. Grundsätzlich wurde ein starker Einfluss des gewählten Reinigungsschrittes vor der Oxidation auf die verschiedenen Messgrößen festgestellt.

Contents

1 Introduction

Silicon carbide (SiC), especially the polytype 4H is a promising semiconductor for high power and high temperatures devices and is already widely in use. For later device applications, however, dielectric layers such as oxides are needed on semiconductor substrates independent of the targeted application, being e.g. as gate oxide in MOSFETs or as insulator in micromachined, high temperature sensors and actuators. Especially in the case of gate oxides very low defect and trap concentrations are required both in the oxide and at the interface. SiC forms SiO_2 as native oxide like Si, but the oxidation kinetics and the quality of the oxide differ a lot.

To evaluate the oxidation process quality of 4H-SiC which can be achieved with our in-house technology this thesis uses several techniques to extract the interface trap concentration, the mobile charge density and the breakdown voltage.

Usually a metal oxide semiconductor (MOS) structure is used for the characterization of the oxide and the interface. Basically, capacitance-voltage (CV), conductance-voltage (GV) and conductance-frequency (Gω) curves are used for extracting the interface trap density D_{it} and the number of mobile ions N_m in the oxide.

These measurement techniques are used to compare oxides realized under different oxidation conditions and different pre- and post-oxidation treatments and to better understand the impact of process parameters on the origin and the density of defects. Performing the measurements in a wider temperature range allows to investigate trap properties in a larger part of the bandgap.

2 Fundamentals

2.1 Silicon carbide

SiC is a IV-IV compound semiconductor made of silicon and carbon and naturally occurs as the rare mineral moissanite. Depending on the polytype (crystal structure) of SiC it has a bandgap between 2.4 and 3.3 eV and therefore is called a wide bandgap semiconductor like GaN and ZnO. Table 1 shows the type and value of the bandgap of important semiconductor materials. Synthetic and natural silicon carbide has been used for many years due to its outstanding mechanical properties. Due to its hardness and high thermal resistivity it is widely used in abrasive machining processes. Its extreme high melting point opens a wide field of applications like in high temperature heating elements, isolation of fuel elements, and high performance breaks. Within the last decades, SiC has set foot as material in the electronic device industry. One of the first SiC products, apart from crystal radios, were LEDs and photo detectors. Today, GaN largely replaced SiC in the LED market because, in contrast to SiC, it is a direct bandgap semiconductor and thus has a much better optical efficiency. With the availability of cheaper wafers with less defects more and more devices based on SiC emerged. Due to its large bandgap and therefore low intrinsic carrier concentration, the high breakdown voltage and the excellent thermal conductivity, these devices are mainly used for high power or high frequency applications. Today, a wide variation of Schottky diodes, MOSFETs, JFETs, BJTs and more, with exceptional voltage and temperature properties are commercially available. [1]

Table 2 provides some important material parameters of the most common SiC polytypes and for comparison, also silicon as well-established standard. SiC differs from Si in most of the properties that are important for electronic devices. The up to 10 times higher breakdown field E_B allows for much larger voltage drops inside the semiconductor. Therefore ultra-high voltage devices with breakdown voltages > 10 kV are possible [2].

Table 1: Bandgaps of important semiconductors (d...direct, i...indirect). A bandgap of 4 eV is often used as characteristic number to distinguish between semiconductors and insulators.

	E_g [eV] (300 K)	Type
Ge	0.66	i
Si	1.12	i
GaAs	1.42	d
4H-SiC	3.26	i
GaN	3.45	d
Diamond	5.5	i

Table 2: Some material parameters of important SiC polytypes and silicon [5, 6, 7].

	3C-SiC	**6H-SiC**	**4H-SiC**	**Si**
Bandgap E_g[eV] at 300 K	2.36	3.03	3.26	1.12
Electron affinity χ [eV]	4	3.45	3.2	4.05
Breakdown field E_B [MV/cm] $@N_D = 10^{17}$ cm^{-3}	>1.5	$\parallel$ c-axis 3.2 $\perp$ c-axis >1	3	0.3
Permittivity ϵ_s	9.72	9.66	9.76	11.9
Density ρ [g/cm^3]	3.21	3.21	3.21	2.34
Electron mobility μ_n [cm^2/Vs] $@N_D = 10^{16}$ cm^{-3}	800	$\parallel$ c-axis 60 $\perp$ c-axis 400	$\parallel$ c-axis 900 $\perp$ c-axis 800	1430
Hole mobility μ_p [cm^2/Vs] $@N_A = 10^{16}$ cm^{-3}	40	90	115	480
Thermal conductivity κ [W/cm K]	3.4	4.9	3.7	1.5

The low-doped drift region in which the space-charge zone forms can also be reduced, which results in lower series resistance compared to silicon counterparts. The on resistance of high power devices is further reduced due to the two times higher saturation velocity of electrons. The about three times higher thermal conductivity compared to silicon allows for higher power dissipation in smaller areas. Impurities can be introduced into the crystal to change some of the electrical properties. In 4H-SiC nitrogen and phosphorus are used as donors with the energy levels $E_{N1} = 61$ meV, $E_{N2} = 115$ meV, $E_{P1} = 60$ meV and $E_{P1} = 120$ meV. For p-type doping aluminum is used with $E_{Al} = 200$ meV [3] [4]. Especially in p-type SiC not all acceptors become ionized at room temperature and below due to the deep energy level. Undoped SiC usually shows n-type behavior due to residual nitrogen atoms, which are present during growth in low concentrations. Doping can be done by incorporation of donors or acceptors during crystal growth or afterwards by ion implantation.

However, some of the outstanding properties of SiC complicate the manufacture of boles (single crystal ingots). Conventional semiconductors (e.g. Si and Ge) are usually grown out of the molten material. For SiC pressures higher than 10^5 atm and temperatures > 3200 °C are needed to create a stoichiometric melt. A production under these conditions is not profitable outside the laboratory [8]. Today the most commonly used technique for growing monocrystalline SiC is Physical Vapor Transport (PVT) which accounts for more than 90% of the supplied SiC wafers. In PVT, SiC powder is heated to temperatures > 2000 °C where it starts to sublimate. The vaporized SiC particles (Si, SiC_2 and Si_2C) condense on a cooler seed wafer at the top of the chamber. Other important technologies for SiC growth are High Temperature Chemical Vapor deposition (CVD), Liquid Phase Epitaxy and Sublimation Epitaxy [9]. Wafers up to 4 inch with low defect counts are

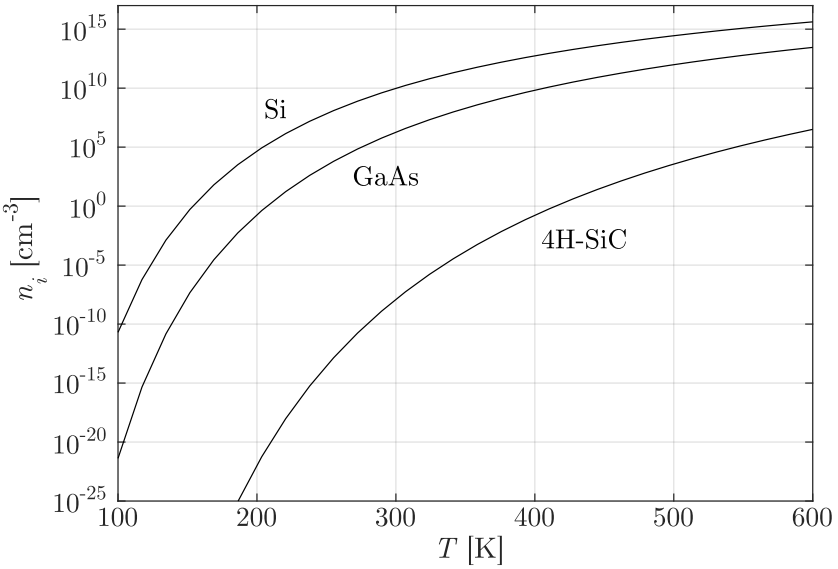

Figure 1: Intrinsic carrier concentration versus temperature [11, 12, 6].

available today. For comparison, silicon wafers are already available with 12-inch and 15-inch is on the rise.

2.1.1 High temperature semiconductor devices

The usage of semiconductors at high temperatures is limited due to many reasons [10]. The increasing intrinsic carrier concentration and the increasing junction leakage current with temperature are perhaps the two most limiting factors. An increase in the intrinsic carrier concentration n_i close to or above the dopant concentration N_D will dominate any doping profile as present in a e.g. p-n-junctions. This can lead to out of specification operation or in the worst case to a total failure of the device. Figure 1 shows the intrinsic carrier concentration n_i of Si, GaAs and 4H-SiC over a wide temperature range. In silicon n_i can already exceed low donor concentrations in the range of 10^{15} cm^{-3} at temperatures above 250 °C. Temperature induced carrier generation in reverse biased junctions is responsible for enhanced leakage current levels. Due to the exponential temperature dependence the leakage currents will quickly increase to intolerable values. As will be seen in a later chapter, both of these limitations are strongly related to the value of the bandgap. Therefore high bandgap semiconductors are suitable for high temperature operation, if other limiting properties like dopant diffusion, thermal conductivity and chemical reactivity are solved as well.

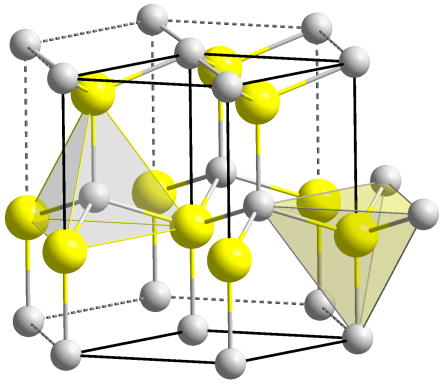

Figure 2: Lattice structure of α-moissanite, a naturally occurring silicon carbide. It has a wurtzite lattice structure which corresponds to the 2H polytype. The bilayers are along the (0001)-layer (horizontal plane). In this polytype they are stacked in A, B sequence. Si-atoms: big-yellow, C-atoms: small-grey.

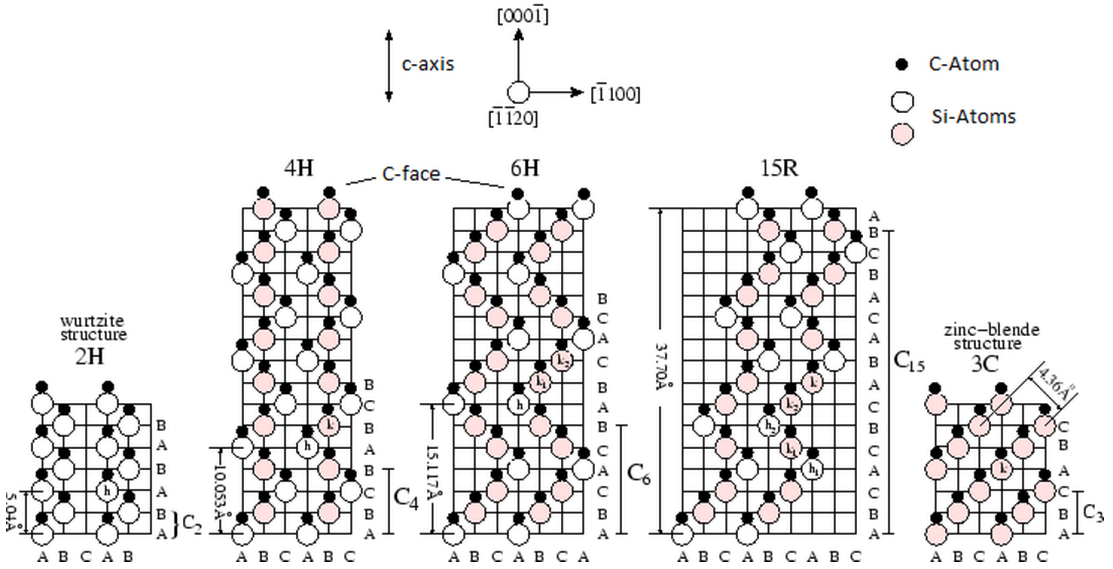

Figure 3: Stacking sequence of five different SiC polytypes. The coloring and the letters 'h' (quasi-hexagonal) and 'k' (quasi-cubic) in the Si atoms indicate the lattice type a Si-C bilayer forms with its immediate neighbors. Changed after [6].

2.1.2 Polytypism

Like many composite materials SiC crystallizes in many different lattice structures. This property is called polymorphism and a particular crystal structure is called a polytype. The uniqueness about SiC is that more than 200 different polytypes are already identified. Silicon carbide is composed out of stacked Si-C-bilayers. In figure 2 the bilayer structure can be seen on the example of a moissanite crystal, which corresponds to the 2H polytype. These bilayers are identical in two dimensions, but differ in the stacking sequence in the third dimension (along the c-axis). The variation of the three possible bilayer configurations A, B and C leads to one cubic polytype (3C-SiC or β-SiC), plenty of hexagonal polytypes (2H-, 4H-, 6H-,... or α-SiC) and rhombohedral polytypes (15H-, 21H-, 27H-SiC, etc.) [13]. In this notation the number stands for the count of layers until the stacking sequence repeats and the letter stands for the corresponding type of the crystallographic lattice. Figure 3 shows the stacking sequence for five important polytypes. The 2H hexagonal lattice structure with A,B sequence is called wurtzite crystal structure and the A,B,C sequence of the 3C polytype corresponds to a zinc-blende structure, where the Si and C atoms form two interpenetrating face-centered cubic lattices. All the other SiC polytypes consist of zinc-blende and wurtzite bonds. 4H-SiC has a cubic to hexagonal bond ratio of 1:1, 6H-SiC 2:1 and 15R-SiC a ratio of 3:2. Owing to the layered structure of the Si-C bilayers, all hexagonal polytypes show anisotropy of some material parameters normal to and parallel to the c-axis. Only the cubic 3C polytype is isotropic to directions normal to each other [6]. Because of the construction by Si-C bilayers along the c-axis the top plane (0001) is terminated with silicon atoms and is called Si-face and the opposite plane $(000\bar{1})$ is called C-face. The two faces have different properties like etching and oxidation rates and also differ in the amount of interface defects [14]. Commonly used SiC wafers for electronic devices are of 4H, 6H and 3C polytype and are usually cut a few degree off the c-axis to reveal the stacking order for growth processes.

2.2 Oxidation

Oxides and especially SiO_2 play a very important role in electronic devices. Important applications for oxides are as gate- and field-oxide in MOSFETs, as masking material during fabrication and as passivation layer. SiO_2 owes its multiple uses not only to its excellent insulating properties, but mainly to its ease of production by thermal oxidation of silicon. SiC is the only compound semiconductor that can be thermally oxidized to form SiO_2. That gives SiC a big advantage over other wide bandgap semiconductors for power device applications. Typically, two types of oxidation processes are distinguished, the dry oxidation under O_2 atmosphere and the wet oxidation under water vapor H_2O. At

first the oxidation process and kinetics of Si are discussed and afterwards the deviations of SiC oxidation are highlighted.

The Deal and Grove model on the general relationship for the thermal oxidation of silicon [15] is the most used and accepted model. Their model assumes that the species of oxidant (O_2 or H_2O) has to go through the following transport steps:

1. It is transported from the bulk of the oxidizing gas to the outer surface of oxide, where it is adsorbed.

2. It is transported across the oxide film towards silicon.

3. It reacts at the interface with silicon and form a new layer of SiO_2.

The overall flux of oxidants is equal to the partial fluxes of each of this three transport mechanisms and their influencing parameters

$$F = F_1 = F_2 = F_3 = \frac{kC^*}{1 + \frac{k}{h} + \frac{kx_0}{D_0}}. \tag{1}$$

The slowest transport mechanism determines the total flow. C^*, k, h and D_0 are process depending parameters like gas concentration and diffusion constant. The oxide growth rate is equal to the flux divided by the number of oxidant molecules per unit area and is given by

$$\frac{dx_0}{dt} = \frac{F}{N} = \frac{B}{A + 2x_0}. \tag{2}$$

The equation is simplified by introducing the parameters A and B

$$A = 2D_0 \left(\frac{1}{k} + \frac{1}{h} \right), \tag{3a}$$

$$B = 2D_0 \frac{C^*}{N}. \tag{3b}$$

B/A is called the linear rate coefficient and B the parabolic rate coefficient. Solving the differential equation 2 for the oxide thickness x_0 gives

$$x_0(t) = \frac{A}{2} \left(\sqrt{1 + \frac{4B}{A^2}(t + \tau)} - 1 \right), \tag{4}$$

where $\tau = (x_i^2 + Ax_i)/B$ is the time offset if the sample already has an oxide film with thickness x_i. Figure 4 shows the oxide thickness over oxidation time after Equation 4 for two different temperatures. Equation 4 can be split up in two regions, a linear and a parabolic region. For $t \gg \tau$ and $t \gg A^2/4B$ x_0 follows the parabolic relationship $x_0 \cong \sqrt{Bt}$. And for $t \ll A^2/4B$ a linear relationship describes the oxide thickness $x_0 \cong B/A \cdot (t + \tau)$. As can be seen from the plot in figure 4 the Deal and Grove model fails for very thin oxides < 30 nm. This was no problem in the middle of the 60's when the model was proposed,

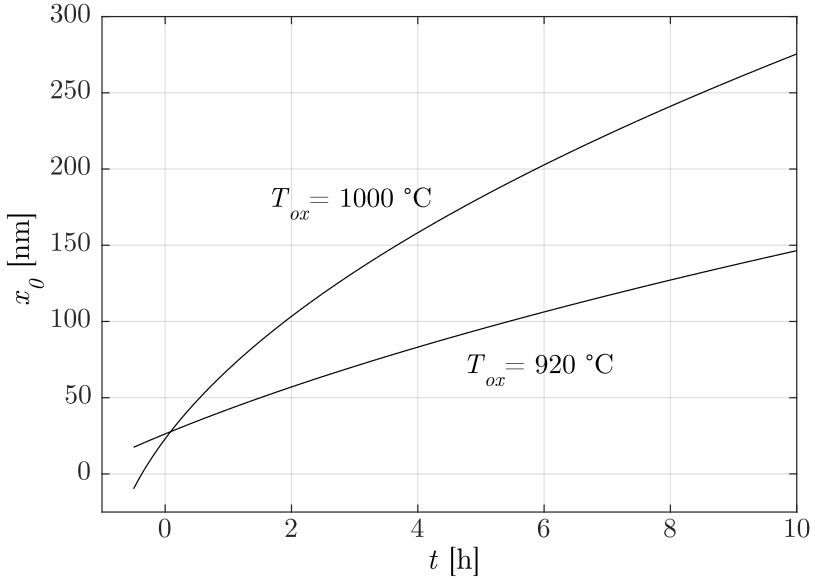

Figure 4: Calculated oxide thickness of dry oxidized (111)-silicon after the Deal and Grove model for two different temperatures.

because such thin oxides were not used. In the 80's Massoud *et al.* came up with a more comprehensive model for the oxidation kinetics, that also describes the faster oxidation of very thin oxide films [16, 17]. The physical process behind the empirical model of Massoud is explained by the stress induced emission of Si atoms into the oxide and is called "interfacial Si emission model" [18].
The Massoud's empirical model extends the Deal and Grove model to

$$\frac{dx_0}{dt} = \frac{B}{A + 2x_0} + C \exp\left(-\frac{x_o}{L}\right). \tag{5}$$

Two new coefficients are introduced. The initial enhancement parameter C and the characteristic length L. Like in the Deal and Grove model the temperature dependence of all parameters follows the Arrhenius equation

$$k = Z \exp\left(-\frac{E_a}{k_B T}\right), \tag{6}$$

where k is the rate constant ($B/A, B, C$ or L), Z a pre-exponential factor and E_a is the activation energy. This gives a set of eight parameters of the Massoud's empirical model, which can be fitted to experimental data.

When it comes to the oxidation of SiC the oxidation and transport mechanism of the containing carbon must be taken into account. A kinetic model called the "silicon and carbon (Si–C) emission model" was proposed by Hijikata *et al.* [19]. This model describes the oxidation of SiC on both C- and Si-face very well by taking the diffusion and oxidation

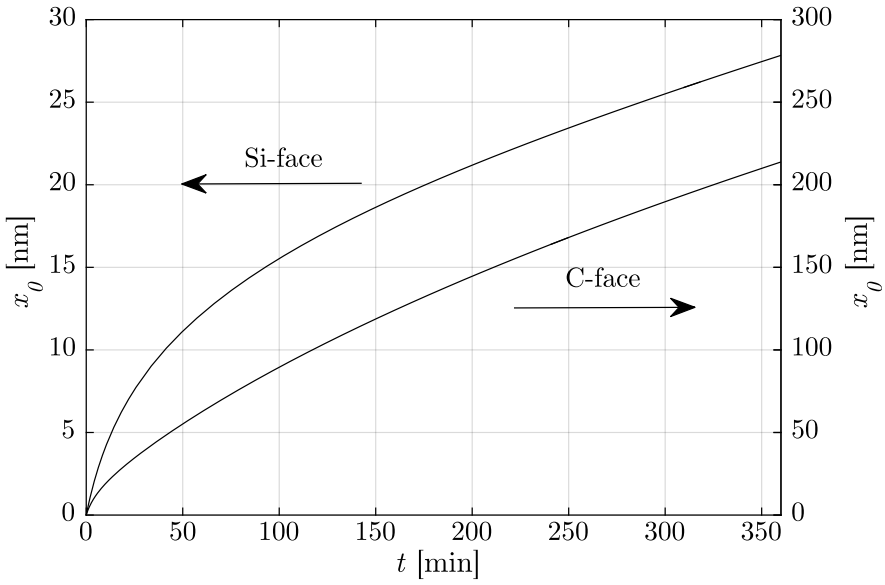

Figure 5: Calculated oxide thickness over oxidation time of 4H-SiC Si-face (left axis) and C-face (right axis) at 1100 °C.

of the carbon into account. The Si-face has a much lower oxidation rate than the C-face. The significantly higher activation energy of the Si-face is only one reason, but doesn't account for the huge difference in the oxidation rate in the parabolic regime. Numerical simulations predict, that the limiting process in Si-face SiC is the out-diffusion of CO_x (x=1 or 2) and not the oxygen in-diffusion like in Si, whereas the C-face oxidation seems to be limited by the oxygen diffusion [20]. Despite small deviations from the actual oxidation rate the Massoud's empirical model is often used to calculate the oxidation rate of SiC. A set of rate constants for 4H-SiC in different crystal orientations can be found in [21]. These values were used to create figure 5, which shows the oxide thickness over time at 1100 °C, being the temperature used to oxidize the SiC samples in this thesis.

2.3 MOS structure

The metal oxide semiconductor (MOS) structure or MOS capacitor is a straightforward device that allows to determine lots of information about the semiconductor, the oxide and their interface. Sometimes the more general name metal insulator semiconductor (MIS) is used because any type of dielectric material can be used instead of an oxide. In the following, oxide is used as a representative of all insulators. Apart from characterization, the MOS structure itself isn't of much use, but it is the main element of the MOSFET, the most important and most frequently produced semiconductor device. When talking about MOS, the terms nMOS and pMOS are often used, in which the 'n' and 'p' stands for the carrier type of the inversion layer. For example a pMOS is made out of an n-type

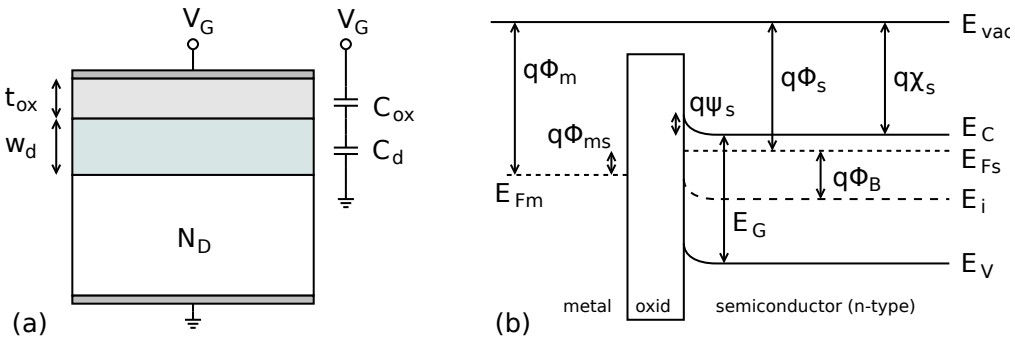

Figure 6: (a) Cross-section of a MOS structure with depletion layer, (b) energy band diagram of a pMOS in depletion condition.

substrate, which forms a p-inversion layer at the interface when biased beyond threshold. To get a better understanding and to have a comparison for the analytical calculations, a simulation of an ideal MOS structure is done prior to the analytical approach to get a deeper understanding of the band alignment.

A cross-section of an ideal MOS structure with depletion layer is depicted in figure 6a. From top to bottom a MOS structure consists of a metal or highly doped semiconductor gate, an insulator (e.g. an oxide), the bulk semiconductor and an ohmic back contact. The oxide between gate and bulk forms a capacitor C_{ox}. Under certain bias condition a capacitor C_d arises when a depletion region is built up under the oxide. For the theoretical part the ohmic contact on the back will be considered as ideal.

Most MOS capacitor characterization methods are based on the capacitance-voltage (CV) and the current-voltage (IV) curves of the device. The following part is devoted to the analytical and numerical characterization of the CV curve of an ideal MOS capacitor. In an ideal MOS there are no oxide charges, no interface traps and no carrier transport inside the oxide; furthermore the ohmic contact has zero resistance. Also the work function difference between gate and the semiconductor Φ_{ms} is zero in an ideal case.

The CV characteristic of an ideal MOS can be divided into three regions, depending on the applied gate voltage V_G. In case of an n-type MOS capacitor these regions are accumulation ($V_G > 0$ V) where majority carriers are attracted towards the semiconductor surface, depletion ($V_G < 0$ V) where the majority carriers are depleted near the surface, and inversion ($V_G << 0$ V) where an inversion layer of minority carriers builds up at the surface. Figure 6b shows the energy band diagram of a pMOS in depletion condition. The metal work function Φ_m and the semiconductor work function Φ_s are the potential differences between the Fermi levels and the vacuum level. Multiplication with the elementary charge q gives the energy required to lift an electron from the Fermi level to vacuum level. The electron affinity $q\chi_s$ is defined as the energy difference between the conduction band

Table 3: Work functions of important metals [24].

Metal	Mo	Au	Pt	W	Al
$q\Phi_m[eV]$	4.19	4.83	5.66	4.57	4.2

edge E_C and the vacuum energy level. The band banding at the surface of the semiconductor is designated as surface potential ψ_s. In flatband condition the energy bands are flat, hence $\psi_s = 0$ and the semiconductor charge $Q_s = 0$. The potential $\psi_p(x)$ is the band bending inside the semiconductor and is defined as the difference between the intrinsic Fermi level $E_i(x)/q$ and the intrinsic Fermi level deep in the bulk $E_i(\infty)/q$

$$\psi_s = \psi_p(0), \qquad (7a) \qquad \psi_p(x) = \frac{E_i(x) - E_i(\infty)}{q}. \qquad (7b)$$

A MOS is in the so-called flatband condition when it is biased at the flatband voltage $V_G = V_{FB}$. In case of an ideal MOS the flatband voltage is zero. Taking into account the work functions of the gate material and the semiconductor the flatband voltage depends on the work function difference Φ_{ms}. In case of a metal gate the work functions Φ_m are well known and table 3 lists values of often used metals. Due to band alignment between gate and oxide the effective work function of the gate material is reduced (for e.g. an Al gate to about 4.1 to 4.14 eV [22] [23]). Because the semiconductor work function Φ_s depends on the position of the Fermi level E_{Fs} it needs to be calculated using equation 8. A look at the band diagram shows that one needs the election affinity χ_s, the intrinsic Fermi level E_i and the Fermi potential Φ_B to obtain Φ_s. χ_s is a measurable quantity and is the energy difference between vacuum level and conduction band edge, E_i is the intrinsic Fermi level of an undoped semiconductor and can be calculated by equation 9, and Φ_B is the difference between the Fermi level E_{Fs} of a doped semiconductor and the intrinsic level. Values for different semiconductors can be found in table 2.

$$q\Phi_s = q\chi_s + E_i - q\Phi_B. \qquad (8)$$

The intrinsic level lies very close to the middle of the bandgap. At elevated temperatures it is slightly shifted due to different effective densities of states of electrons in the conduction band N_c and holes in the valence band N_v. The densities of states are calculated using equation 10a and 10b [25] and require the density of states effective masses for electrons m_n^* and holes m_p^*. Lots of different publications about the density of states effective mass in 4H-SiC can be found [26] [27] [28]. In this work m_n^*= $0.4m_e$ and m_p^*= $0.8m_e$ is used, which is a good average of the published values. m_e is the electron mass. Using these

values and M_c= 3 [6] gives N_c= $1.9 \cdot 10^{19}$ cm^{-3} and N_v= $1.8 \cdot 10^{19}$ cm^{-3} at $T = 300$ K.

$$E_i = \frac{E_G}{2} + \frac{k_B T}{2} \cdot \ln\left(\frac{N_v}{N_c}\right). \tag{9}$$

$$N_c = 2M_c \left(\frac{2\pi m_n^* k_B T}{h^2}\right)^{\frac{3}{2}} \tag{10a}$$

$$N_v = 2 \left(\frac{2\pi m_p^* k_B T}{h^2}\right)^{\frac{3}{2}} \tag{10b}$$

With the 4H-SiC bandgap of $E_G = 3.235$ eV and $T = 300$ K this gives $E_i = 1.62$ eV using the valence band edge as reference level. At room temperature the Fermi level of an intrinsic 4H-SiC semiconductor is practically in the middle of the forbidden band. A doping concentration of N_D or N_A shifts the Fermi level by Φ_B according to

$$\mathrm{n-type:}\ \ \Phi_B = \frac{k_B T}{q} \ln\left(\frac{N_D}{n_i}\right) \qquad \mathrm{p-type:}\ \ \Phi_B = \frac{k_B T}{q} \ln\left(\frac{n_i}{N_A}\right). \tag{11}$$

To calculate the Fermi potential Φ_B the intrinsic carrier concentration n_i is needed

$$n_i = \sqrt{N_c N_v} \cdot \exp\left(-\frac{E_G}{2k_B T}\right). \tag{12}$$

Solving these equations for N_D= $1 \cdot 10^{16}$ cm^{-3} gives n_i= $1.26 \cdot 10^{-8}$ cm^{-3} and Φ_B= 1.42 V. This finally gives a work function difference for an aluminum gate of $\Phi_{ms,Al}$= 0.81 V at room temperature. The following calculations of an ideal CV curve will assume $V_{FB} = 0$.

2.3.1 Calculations of an ideal CV curve

To numerically calculate a CV curve of an ideal MOS, the one dimensional Poisson equation has to be solved for the potential distribution in the oxide and the semiconductor.

$$\frac{d^2\psi}{dx^2} = -\frac{\rho(x)}{\epsilon_s} \tag{13}$$

At the boundary between the oxide and the semiconductor an interface condition is needed because of the different permittivities ($\epsilon_{ox} E_{ox} - \epsilon_s E_s = 0$). The total space charge density inside the semiconductor is given by

$$\rho(x) = q(N_D^+ - N_A^- + p(x) - n(x)), \tag{14}$$

assuming all donors are ionized. The electron and hole concentrations inside the semiconductor are given by

$$n(x) = n_0 \cdot \exp(\beta\psi_p(x)), \tag{15a}$$

$$p(x) = p_0 \cdot \exp(-\beta\psi_p(x)). \tag{15b}$$

In case of an n-type semiconductor $n_0 = N_D$ and $p_0 = n_i^2/N_D$ with $\beta = q/k_BT$.

This is done in a numerical simulation for several gate voltages V_G. Figure 7 shows the simulated energy band diagram of a pMOS at four different bias conditions. It clearly reveals that the energy bands start to bend upwards for negative gate voltages and a depletion region builds up. If V_G is negative enough, the valence band edge at the surface comes close to or even move above the Fermi level. Because $np = n_i^2$ needs to be maintained an inversion layer of minority carriers starts to build up. The minority carriers can be generated thermally or by optical generation. Although the generation lifetime τ_g in SiC is up to 4 orders of magnitude lower than in Si [29] [30], the generation rate G is still extremely low, because the intrinsic carrier concentration n_i of 4H-SiC is about 19 orders of magnitude lower compared to silicon. Therefore it would take years to build up an inversion layer in SiC at room temperature. In the best case the time constant to build up the inversion layer by thermal generation follows the relation $\tau_{inv} \propto 2\tau_g/n_i$ [23]. Figure 8 shows the carrier concentrations inside the semiconductor at the same gate voltages as in Figure 7. The two top graphs distinguish the case of deep depletion (blue dashed) and inversion (black dashed). The resulting CV curve of this simulation is depicted in Figure 9 and also shows the two cases of deep depletion and inversion. The blue CV curve must be used at room temperature, only after almost infinitely long time or strong UV radiation the black line would be measured. The actual measured curve also depends on the measurement frequency. If a MOS capacitor is in inversion, the measured capacitance depends on the measurement frequency, because the minority carrier recombination-generation must be able to follow the measurement signal. Therefore quasi-static (QS) or low-frequency (LF) capacitance measurement methods are used to measure the inversion capacitance.

An analytical approach to calculate the CV curve is given in [25]. At first the potential $\psi_p(x)$ inside the semiconductor needs to be calculated using the Poisson equation from equation 13. Integrating the Poisson equation once and using only the potential at the surface $\psi_p = \psi_s$ gives an equation for the electric field at the surface $E_s = \frac{d\psi_s}{dx}$. The space charge density at the surface Q_s than follows by

$$Q_s = -\epsilon_s E_s = \mp \frac{\sqrt{2}\epsilon_s kT}{qL_D} \sqrt{[\exp(\beta\psi_s) - \beta\psi_s - 1] + \frac{p_0}{n_0}[\exp(-\beta\psi_s) + \beta\psi_s - 1]}. \qquad (16)$$

For negative surface potentials Q_s is positive and *vice versa*. The capacitance of the depletion layer $C_d(\psi_s)$ follows by differentiation of the surface charge via

$$C_d = \frac{dQ_s}{d\psi_s} = \frac{\epsilon_s}{\sqrt{2}L_D} \frac{1 - \exp(\beta\psi_s) + \frac{p_0}{n_0}[\exp(-\beta\psi_s) - 1]}{\sqrt{[\exp(\beta\psi_s) - \beta\psi_s - 1] + \frac{p_0}{n_0}[\exp(-\beta\psi_s) + \beta\psi_s - 1]}}. \qquad (17)$$

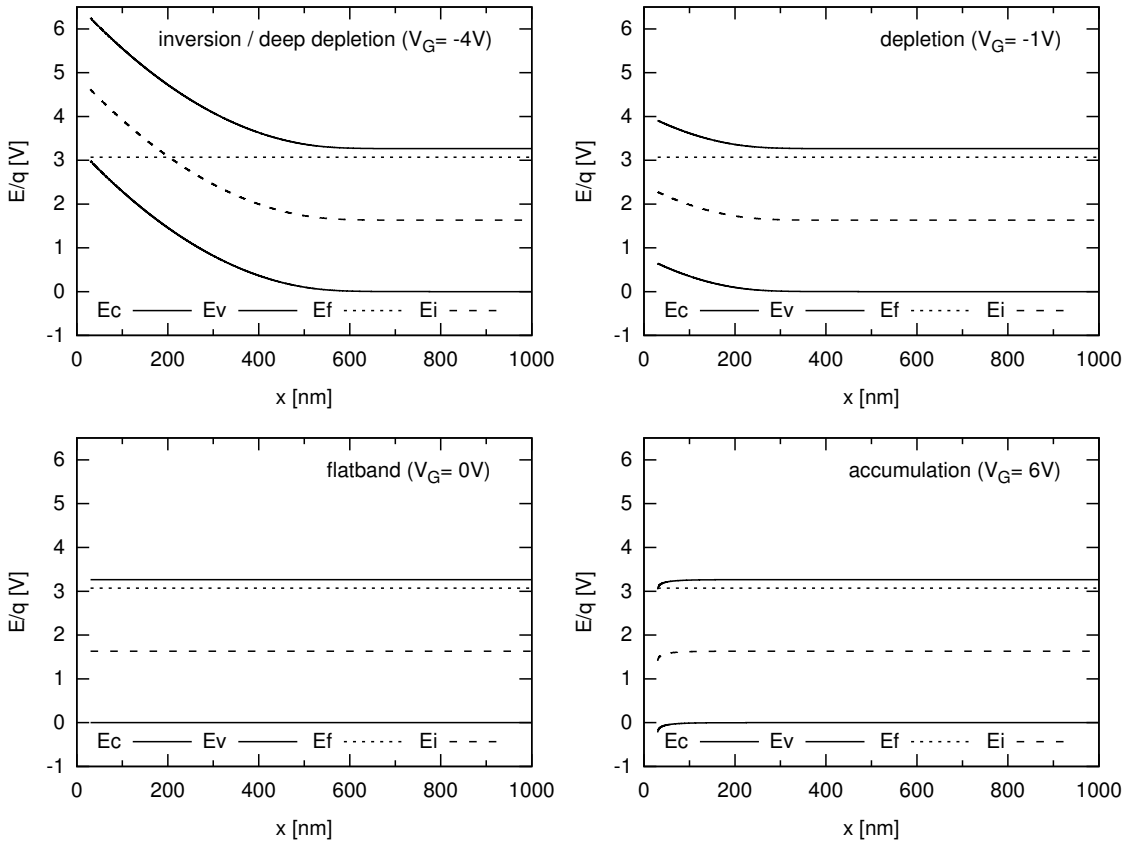

Figure 7: Numerical simulation of the energy bands of an ideal 4H-SiC pMOS at four different bias conditions, using $N_D = 1 \cdot 10^{16}$ cm^{-3}, $t_{ox} = 30$ nm, $T = 300$ K.

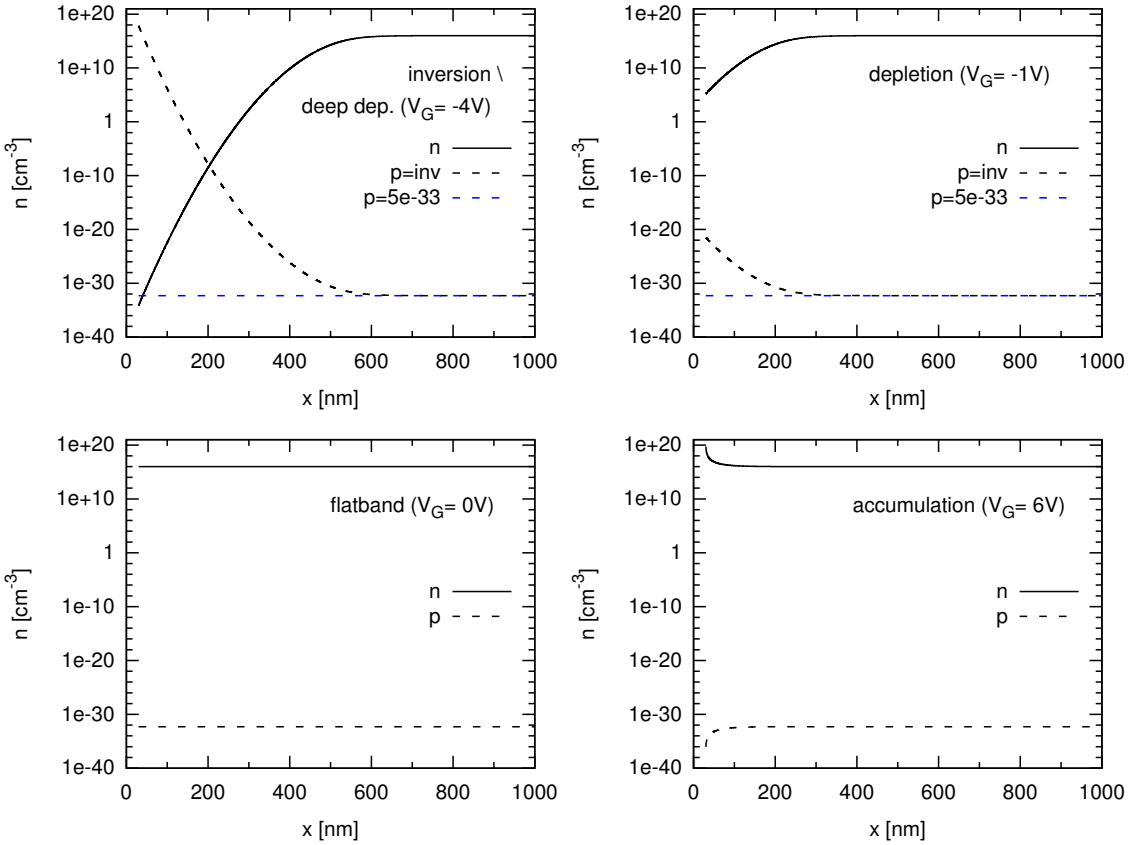

Figure 8: Numerical simulation of the carrier concentrations in an ideal 4H-SiC pMOS at four different bias conditions. The top graphs with negative gate voltage also show the case if no inversion layer is built up and the minority carrier concentration remains at the bulk value (blue lines). Using $N_D = 1 \cdot 10^{16}$ cm^{-3}, $t_{ox} = 30$ nm, $T = 300$ K.

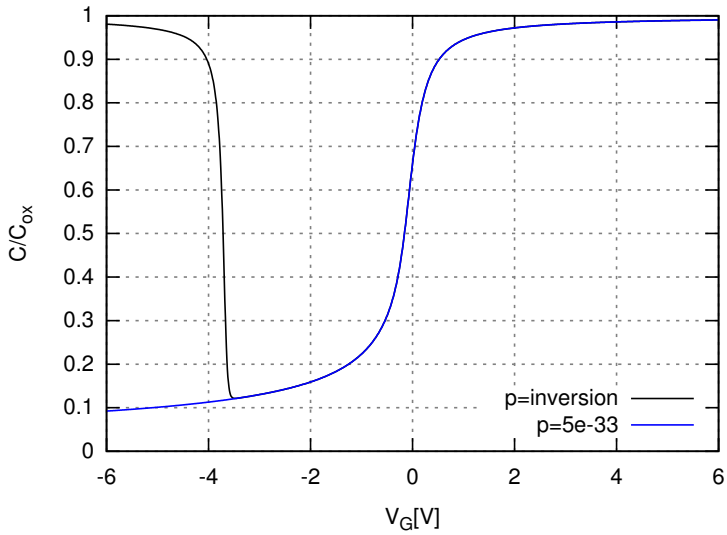

Figure 9: Numerical simulation of the CV curve of an ideal 4H-SiC pMOS with inversion (black) and deep depletion (blue). Using $N_D = 1 \cdot 10^{16}$ cm^{-3}, $t_{ox} = 30$ nm, $T = 300$ K.

The abbreviation L_D is the Debye length for electrons

$$L_D = \sqrt{\frac{kT\epsilon_s}{n_0 q^2}}. \tag{18}$$

Equations 16 and 17 assume the carriers to be in thermal equilibrium and therefore will give Q_s and C_d for the inversion case. If the deep depletion curves are wanted p_0 must be set to zero. In order to obtain the dependency of the total capacitance of the gate voltage one needs to use the relation that the gate voltage is the sum of the voltage across the oxide plus the surface potential $V_G = V_{ox} + \psi_s$ by

$$V_{ox} = \frac{-Q_s t_{ox}}{\epsilon_{ox}} = -\frac{Q_s}{C_{ox}}, \tag{19}$$

with the oxide thickness t_{ox} and its permittivity ϵ_{ox}. The total capacitance of the MOS structure is a series connection of C_d and C_{ox}:

$$C = \frac{C_{ox} C_d}{C_{ox} + C_d}. \tag{20}$$

A more comprehensive explanation with all equations can be found in [25, Chap. 4]. The CV curve was calculated using this analytical approach with the same parameters as in the numerical simulation. The CV curve isn't depicted separately because it exactly matches figure 9.

2.3.2 Temperature dependencies

In the previous section the ideal CV curve has been calculated at room temperature ($T = 300$ K). In order to determine certain properties, such as the interface trap density in a larger energy range, CV measurements are done at temperatures above or below room temperature. Therefore the ideal CV curve and the location of the Fermi level needs to be calculated for a wider temperature range. At first, the temperature dependency of the bandgap needs to be considered when investigating a temperature interval of several hundred Kelvin. The bandgap of all semiconductors decreases with increasing temperature due to thermally induced expansion of the lattice and temperature-dependent electron lattice interaction [31]. The bandgap of 4H-SiC has been measured to be 3.265 eV at 4.2 K. At a temperature of 600 K, it gets reduced to 3.147 eV. Also the effective densities of states N_c and N_v depend on T according to equations 10a and 10a [6]. The density of states effective masses m_n^*, p are considered to be rather temperature independent in the range of 150 to 600 K. The position of the Fermi level depends on the doping concentration

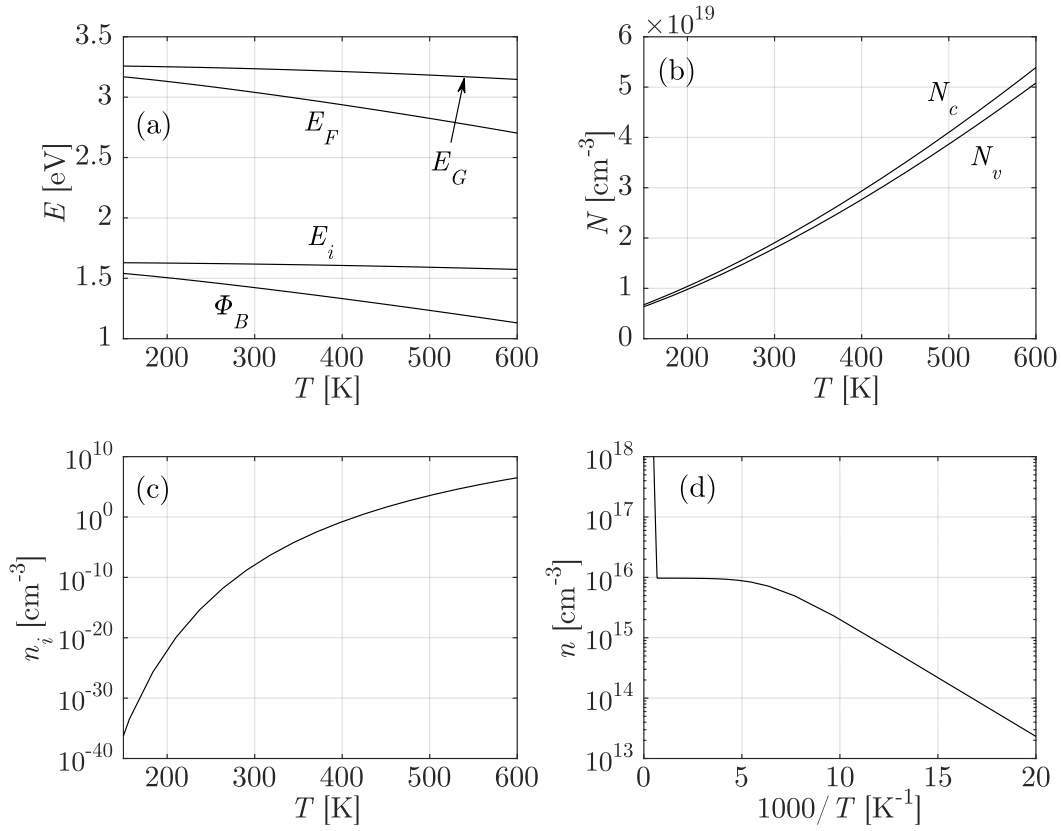

Figure 10: Calculated values of 4H-SiC with $N_D = 10^{16}$ cm^{-3} versus temperature for a) the bandgap E_G, the Fermi level E_F, the intrinsic Fermi level E_i and the Fermi potential $q\Phi_B$, b) the density of states N_c and N_v, c) the intrinsic electron concentration n_i and d) the electron concentration n.

N_D and the energy level of the dopants according to

$$N_c \exp\left(-\frac{E_C - E_F}{kT}\right) \approx \frac{N_D}{1 + 2\left[(E_F - E_D)/kT\right]}. \tag{21}$$

Figure 10 shows the most important semiconductor parameters over a wide temperature range. Furthermore the ideal CV curve has been calculated for several temperatures in this range. The result is depicted in figure 11. As shown in this figure, the temperature dependence of the CV curve primarily occurs in accumulation and around flatland voltage. This part is of special interest when using the ideal curves to determine D_{it} with the Terman method. Also the Fermi level Φ_B is reduced by about 27% in the observed temperature range from 150 to 600 K. Basically, this value is of importance to precisely determine the energy position of a trap.

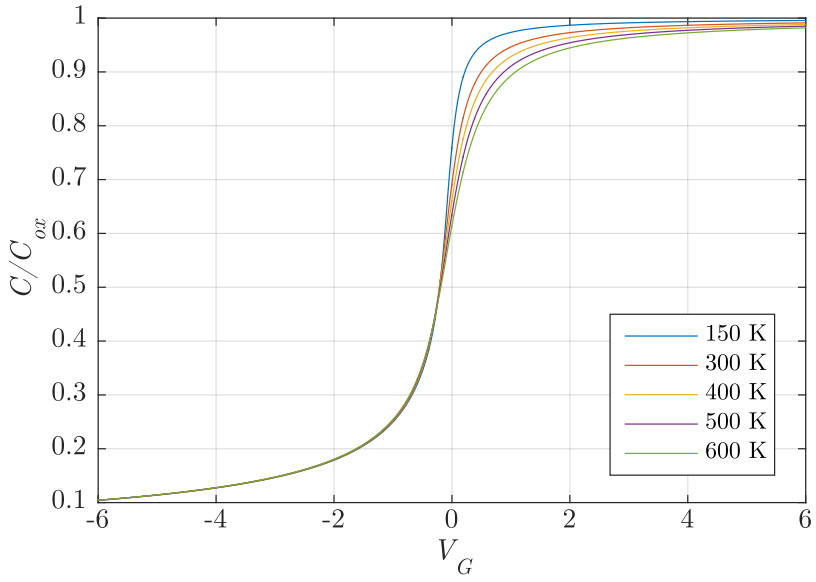

Figure 11: Ideal CV curves with deep depletion at five different temperatures of 4H-SiC MOS capacitors with $N_D = 10^{16}$ cm^{-3} and $C_{ox} = 102$ nF/cm^2.

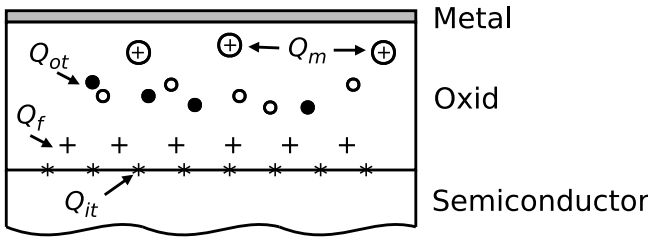

Figure 12: Charges inside a typical silicon MOS capacitor.

2.4 Oxide and interface defects

2.4.1 Charge and defect types

In the calculations and simulations presented in the previous section the MOS structure was considered to be ideal. In reality there are of course deviations from the model discussed above. This section is devoted to electrically active charges and traps inside the oxide and at the oxide-semiconductor interface. The following designations are used to classify the charges and traps. Q is the net effective charge per unit area [C $\cdot$ cm^{-2}], N is the net effective number of charges or defects per unit area [cm^{-2}] and D is the trap density per unit area per unit energy in [cm$^{-2} \cdot$ eV^{-1}]. Generally four different types of charges are found in $SiO_2 - Si$ and $SiO_2 - SiC$ MOS systems. Figure 12 schematically depicts the charges and their typical location.

Mobile Oxide Charges Q_m: This charge type is the only one that is mobile in the oxide and origins from ionic and heavy metal impurities during fabrication. They are usually located near the metal gate and drift towards the semiconductor interface with positive gate voltages. Mobile oxide charges are usually Na^+, K^+ and Li^+ ions and carry a positive charge. In a MOSFET mobile charges can lead to instabilities and a change of the threshold voltage over time [32].

Oxide Trapped Charges Q_{ot}: This charge type can be either positive or negative and is distributed inside the oxide. Origins of such charges are electrons or holes trapped inside the oxide which are created, for example, by X-ray radiation, avalanche injection or Fowler-Nordheim tunneling [33].

Fixed Oxide Charges Q_f: These positive charges are located at or near the interface where the oxide is non-stoichiometric and under stress due to the different lattice constants between the underlying semiconductor and the SiO_2. Therefore the amount of fixed oxide charges depend on the type and crystal orientation of the underlying semiconductor as well as on the growth condition like heating and cooling rates and oxygen pressure. Higher oxidation temperatures or post annealing in inert atmospheres after the "Deal Triangle" [34] lowers Q_f significantly. The origin of the positive fixed charges may be ionic silicon that is left near the interface. In wet oxidized SiC the fixed oxide charge appears to be negative [35] due to negative CO_3^{2-} ions and a large number of incorporated H atoms.

Interface Trap Density D_{it}: Interface traps can capture electrons or holes at a specific energy level. These traps are located at the interface and the energy positions of the traps are usually distributed in the whole bandgap. Most likely every interface consists of two kinds of interface traps. Acceptor like traps, which are neutral and become negatively charged by accepting an electron, and donor like traps, which are neutral and become positively charged by donating an electron. Like illustrated in Figure 13 it is assumed that acceptor states are more densely distributed near the conduction band edge and donor states at the valence band edge [32]. Conveniently the sum of traps per unit energy is designated as D_{it}. The neutral level E_0 marks the energy above which traps are mostly acceptor type and beyond which traps are mostly donor type. Although the traps are very close together in energy they do not form any kind of energy band and they do not influence each other because trap sites are spaced too far apart on the interface plane [32]. Every trap acts isolated and only exchanges charges with the semiconductor. In silicon MOS structures, most of the interface states are due to dangling bonds, oxygen vacancies, metal impurities or radiation defects. With clean fabrication processes and

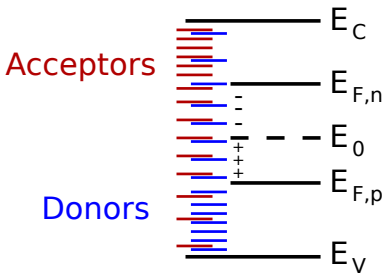

Figure 13: Distribution of interface states in the bandgap. Any interface consists of traps of both types. At the neutral level E_0 they cancel each other out. Above E_0 there are more acceptor states and beyond more donor states. The position of the Fermi level E_F in respect to E_0 defines whether the net charge is positive (below) or negative (above).

post oxidation annealing in hydrogen the interface trap density can be reduced to the low 10^{10} cm^{-2}eV^{-1} range [32]. In thermally oxidized SiC the interface density can be more than an order of magnitude higher and hydrogen annealing has to be performed at much higher temperatures to achieve a reduction of D_{it} [36]. Bassler *et al.* [37] [38] suggested carbon clusters as the reason for the higher interface trap densities in oxidized SiC. The interface traps are of special interest because they effect the charge transport inside the semiconductor. Inside a MOSFET interface traps reduce the carrier mobility of the channel and also leads to random telegraph signal (RTS) noise due to the random occupancy of the states with carriers from the channel.

2.4.2 Flatband voltage

All this charges influence the ideal CV characteristic of a MOS capacitor. In the previous section the flatband voltage V_{FB} was introduced as the voltage at which the energy bands are flat and the surface potential $\psi_s = 0$. This voltage does not only shift due to the work function differences between gate and semiconductor, but also strongly depends on the charges inside the oxide. The closer the location of the charges is to the semiconductor the stronger is the shift of the flatband voltage, because the charge is imaged into the semiconductor and needs to be compensated with a higher or lower gate voltage. The total voltage shift due to all charge types is given by

$$V_{qox} = \frac{Q_f}{C_{ox}} + \frac{Q_{it}(\psi_s)}{C_{ox}} + \frac{1}{C_{ox}} \int_0^{t_{ox}} \frac{x}{t_{ox}} \rho_m(x)\, \mathrm{d}x + \frac{1}{C_{ox}} \int_0^{t_{ox}} \frac{x}{t_{ox}} \rho_{ot}(x)\, \mathrm{d}x. \tag{22}$$

The fixed oxide charges Q_f and the interface charges Q_{it} are directly mirrored into the semiconductor because they are near the interface, whereas the oxide trapped charges Q_{ot} and the mobile oxide charges Q_m are usually distributed in the oxide and their influence on the flatband voltage is weighted by their distance from the interface. If substrates with

an epi-layer are used for MOS capacitors a shift of the flatband voltage due to the work function difference of the two differently doped regions also needs to be taken into account. For an n-type semiconductor with $N_{bulk} = 10^{19}$ cm^{-3} and $N_{epi} = 10^{16}$ cm^{-3} this results in a shift of $\Phi_{epi} = +90$ mV [39]. The total flatband voltage becomes

$$V_{FB} = \Phi_{ms} - V_{qox} + \Phi_{epi}. \tag{23}$$

The capacitance at the flatband voltage is called flatband capacitance $C(V_{FB}) = C_{FB}$. It follows from solving equation 17 at $\psi_s = 0$ which gives $C_d(0) = \epsilon_s / L_D$. The total capacitance is C_d in series with C_{ox} which gives

$$C_{FB} = \frac{C_d C_{ox}}{C_d + C_{ox}} = \frac{\epsilon_{ox}\epsilon_s}{\epsilon_s t_{ox} + \epsilon_{ox} L_D}. \tag{24}$$

One could now erroneously assume that one can simply obtain the flatband voltage at the C_{FB} point of a CV curve. But unfortunately this won't give the correct value due to the deviation of the CV curve from the ideal case due to interface traps. The influence of the interface traps on the CV curve will be discussed later. But it still is a good estimation especially if the trap concentration is low.

2.4.3 Interface trap time constant

Important parameters of interface traps are their capture and emission time constants τ_c and τ_e. For acceptor like traps, these are the mean times needed to capture or emit an electron from or to the conduction band. Capture and emission times are usually in the same order of magnitude. The emission time constant τ_e is often called trap time constant τ_{it}. For acceptor like traps it can be calculated using

$$\tau_e = \tau_{it} = \frac{1}{\sigma_n v_{th} N_c} \cdot \exp\left(\frac{\Delta E}{k_B T}\right). \tag{25}$$

Here σ_n is the capture cross section for electrons, v_{th} is the thermal velocity for electrons and $\Delta E = E_C - E_T$ is the energy position of the trap referenced to the conduction band. For donor traps N_v and $E_T - E_V$ are used. The capture cross section is material dependent an also varies with the energy level of the trap [40, 41, 42]. An explanation of the temperature and activation energy dependency of the capture cross section can be made using the nonradiative multiphonon emission theory [43]. For n-type 4H-SiC σ_n is in the range of 10^{-20} to 10^{-14} cm^2. The thermal velocity is given by

$$v_{th} = \sqrt{\frac{3 k_B T}{m_n^*}}, \tag{26}$$

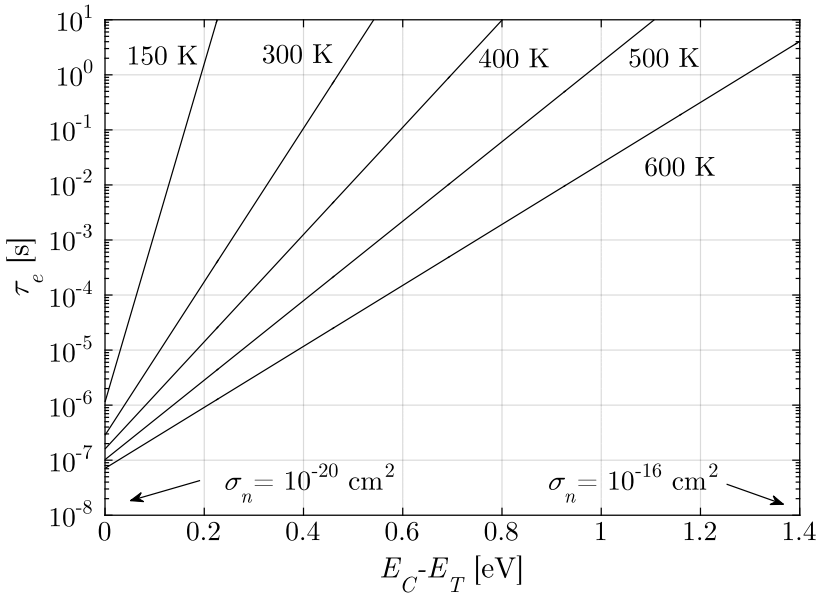

Figure 14: Emission time constant τ_e for electrons in n-type 4H-SiC for various temperatures. The capture cross section σ_n is assumed to increase logarithmically with ΔE from 10^{-20} cm^2 at the conduction band edge to 10^{-16} cm^2 at $\Delta E = 1.4$ eV.

with the density of state effective mass m_n^* as described in section 2.3. At T= 300 K $v_{th} = 1.85\text{x}10^7$ cm/s;

A visualization of the emission time constants for various temperatures is provided in figure 14. The used capture cross-sections are only estimated values out of their usual range to provide a good illustration. The plot can also be used to estimate the covered energy range of the used trap characterization method. Techniques like the conductance and Terman method (will be discussed later) use superimposed AC signals to measure the capacitance or conductance. The lower limit of the Terman method is the sweep rate of the DC bias and that of the conductance method is the lowest AC signal that can give an accurate measurement of the capacitance. The upper limit of the AC signal is mostly due to the losses and inductance of the wiring of the measurement setup. Usual values are 0.5 V/s or 100 Hz up to 1 MHz. This frequency range can be mapped to an emission time range which gives an observable energy range for a certain operation temperature. This very rough estimate gives a range of 0.1 to 0.5 eV at room temperature. Performing measurements at lower temperatures allows characterizing traps closer to the conduction band (or valence band for p-type). Measurements at elevated temperatures allow trap characterization towards mid-band.

2.4.4 Mobile oxide charge and CV

As mentioned above mobile oxide charges are primarily Na^+, K^+ and Li^+ ions. Sodium is usually the most dominant ion species. Critical sources of sodium are gate metallization, oxidation and high temperature annealing in sodium contaminated quartz furnaces, photoresist bake, sodium containing chemical reagent and improper handling by humans [32]. Vacuum pump oil is a known source of lithium [33]. Despite this so called extrinsic source of contamination, intrinsic generation during the oxidation process is possible and reported for SiC [44, 45]. The mobile charge density is usually measured in N_{ions}/cm^2. Values in the 5×10^9 to 10^{10} cm^{-2} range are acceptable for integrated circuits [33]. The influence of the mobile charges on the device behavior and the CV curve is via the flatband voltage V_{FB}. As can be seen in equation 22 the flatband voltage shift depends not only on the amount of mobile charges but also on their position inside the oxide. Because the ions are positively charged they are able to drift due to the applied gate voltage and therefore change the flatband voltage. This influence is observable in a shift of the CV curve depending on the bias polarity prior measurement. If the amount of mobile charge is high enough and the sweep rate is rather slow, an offset between two CV curves with different sweep directions can be observed. The time an ion needs to drift from one side of the oxide to the other depends on the ion mobility μ and the electric field $E = V_G/t_{ox}$ inside the oxide. The temperature dependence of the ion mobility follows the exponential relation

$$\mu = \mu_0 \exp\left(\frac{-E_A}{k_B T}\right), \tag{27}$$

with the pre-exponential factor μ_0 and the activation energy E_A. The drift time t_d can be calculated using

$$t_d = \frac{t_{ox}^2}{\mu_0 V_G} \exp\left(\frac{E_A}{k_B T}\right). \tag{28}$$

Experimentally determined values for three important contaminants Na: $\mu_0 = 3.5 \cdot 10^{-4}$ $\mathrm{cm}^2/\mathrm{Vs}$ and $E_A = 0.44 \pm 0.09$ eV, Li: $\mu_0 = 4.5 \cdot 10^{-4}$ $\mathrm{cm}^2/\mathrm{Vs}$ and $E_A = 0.47 \pm 0.08$ eV and K: $\mu_0 = 2.5 \cdot 10^{-3}$ $\mathrm{cm}^2/\mathrm{Vs}$ and $E_A = 1.04 \pm 0.1$ eV after [46] are used to generate figure 15. With an oxide thickness of 30 nm and a gate voltage of 2 V only a couple of milliseconds are needed to transfer Na and Li ions through the oxide.

Ways to reduce mobile ion contamination depend on their source. Samples should only be handled with new and clean gloves. For cleaning and etching processes de-ionized water and chemicals with high purity should be used. If oxidation or annealing furnaces are suspected as sources of contamination, high temperature annealing under HCl-O_2 atmosphere can reduce the ion concentration in the furnace [47]. The use of high purity metals and sodium free filaments (in case of evaporation) can rule out the gate metallization as a source of contamination. Furthermore phosphosilicate glass layer grown on the SiO_2 can

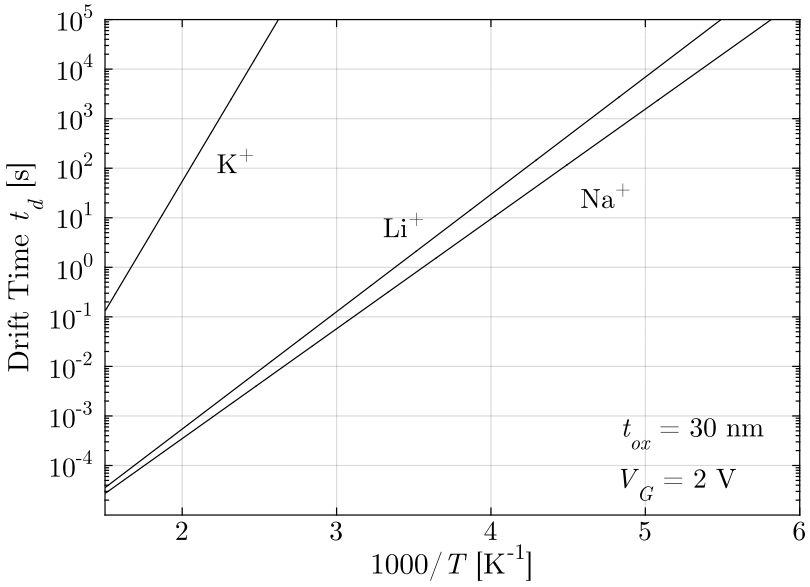

Figure 15: Drift times of the three most common mobile ions in SiO_2 for an oxide thickness of 30 nm and a gate voltage of 2 V calculated using equations 27 and 28.

getter ions and chemically bind them in a neutral state [48]. Also oxidation in HCl diluted oxygen is known to reduce the number of mobile ions in the oxide [47, 49, 50]. In case of an intrinsic ion source, post deposition annealing under argon atmosphere at 1100 °C has led to a reduction of the mobile ion concentration in 4H-SiC [44]. Measuring methods for determining the mobile charge concentration are discussed in the next chapter.

2.5 Ohmic contact

Virtually every semiconductor device needs at least one ohmic contact. In a MOS capacitor one ohmic contact usually on the back side of the semiconductor is used. When a metal and a semiconductor are brought into contact two types of contacts can arise. A rectifying Schottky contact and an ohmic contact. The ohmic contact has a linear and symmetric IV characteristic and its contact resistance is small compared to the total resistance of the semiconductor device. The band diagrams of both types are depicted in figure 16. Which type of contact arises depends on the difference between the metal work function Φ_s and the semiconductor work function Φ_s. If $\Phi_m > \Phi_s$ like on the left hand side of figure 16 electrons from the n-type semiconductor will flow into the metal, where they find free states at lower energies. This leaves behind positively charged donors in the semiconductor which cause the formation of a depletion layer with width W and the bands bend upwards creating a barrier with height $\Phi_B = \Phi_m - \chi_s$. The barrier height depends only negligibly on the doping, but the width of the barrier depends on the doping concentration by $W \propto 1/\sqrt{N_D}$. In the other case, if $\Phi_m < \Phi_s$ electrons will flow from the

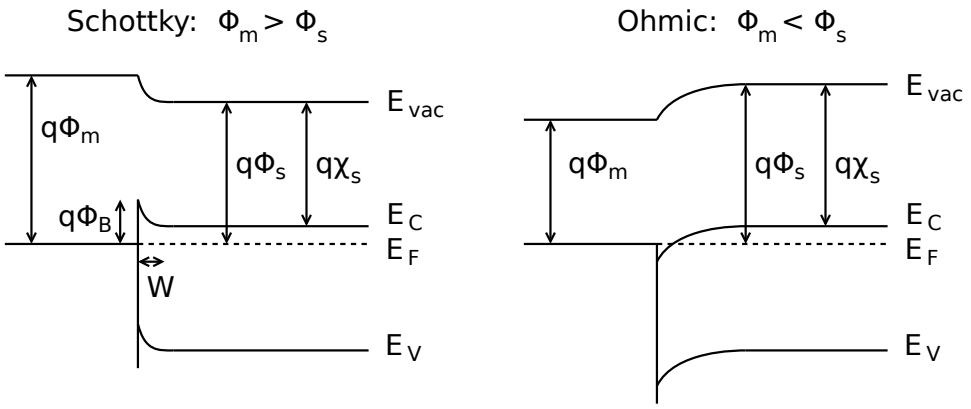

Figure 16: Energy band diagrams of a Schottky contact (left) and an ohmic contact (right) between metal and n-type semiconductor.

metal into the semiconductor, that also results in a band bending to align the Fermi levels. The now arising band diagram does not contain a barrier for carriers in either direction.

The problem is that the majority of metals have a work function in the range of 4-6 eV and the electron affinity of semiconductors is 4 eV or even lower for those with a wide bandgap. Values can be found in tables 2 and 3. Therefore, almost every electrical contact made on SiC is rectifying and hence, non-linear in the IV characteristics. But there are ways to form low resistance contacts between metal and SiC. One method is to use very high doping concentrations near the contact. This can be done by implanting, diffusion or epitaxial growth of a highly doped layer. As described above, the barrier height Φ_B does not change with doping concentration, but the width of the barrier does. That means that with sufficiently high doping concentration $N > 10^{19}$ cm^{-3} the depletion width and as a consequence, the barrier width becomes very narrow. With decreasing barrier width the dominant charge transport mechanism of the Schottky contact changes from thermionic emission (TE) to thermionic field emission (TFE). In the TE transport regime carriers must have a high enough thermal energy to surmount the barrier and in the TFE regime carriers do not need to overcome the barrier, but tunnel through it at elevated energies over the conduction band when it is sufficiently thin. For even higher doping concentrations the barrier becomes so thin, that carriers are able to tunnel through it without additional thermal energy. This conduction mechanism is called field emission (FE) and the associated contacts are called tunnel ohmic contacts.

Another way to form ohmic contacts on wide bandgap semiconductors even with low doping concentration is the use of a heterojunction with smaller bandgap like silicides and carbides. Widely used metals which alloy with the silicon and carbon at high temperature annealing are Ti and Al/Ti [51] and Ni [52]. A good overview of recent studies with different materials and annealing temperatures can be found in [53]. Due to the high

temperatures needed for low ohmic contact formation a compromise in thermal budget has to be found for enhanced device performance as in parallel, the oxide quality is reduced above a certain characteristic temperature value [54, 55]. Usually both, a high doping concentration and an annealing process to form low bandgap interlayers are used. With these techniques ohmic contacts in the range of $10^{-6}\ \Omega \cdot \mathrm{cm}^2$ are possible on 4H-SiC.

3 Measurement Theory

3.1 Small-signal steady-state capacitance methods

All small signal steady state methods are based on capacitance measurements. Usually impedance analyzers are used to measure the capacitance by applying a small AC voltage to the device under test (DUT) and measure the current and phase shift. With this information the impedance Z of the DUT can be calculated. Depending on the used equivalent circuit of the DUT the analyzer can convert the impedance into several measurement parameters e.g. capacitance with parallel conductance. The frequency f of the measurement signal and a DC offset can be adjusted in a wide range. (Note: for capacitors in the low pF-range the lowest frequency for acceptable accuracy is a few hundred Hz). Another method to measure a capacitance is based on quasi-static (QS) measurements. These methods usually measure the transferred charge when a small voltage step is applied to the DUT. QS-measurement devices can measure small capacitors with effectively $f = 0$ Hz. As will be seen soon, the frequency of the measurement is important for the various methods. Multiple measurements at different DC offsets will give a CV curve.

Interface traps and CV Curve:
The presence of interface traps in a MOS capacitor result in a stretchout of the measured CV curve compared to an ideal CV curve. Interface traps change their charge depending on their filling state and can be seen as interface charge Q_{it}. Acceptor like traps are negative when filled and neutral when empty, and donor like traps are neutral when filled and positive when empty. Inside the MOS an overall charge neutrality between the gate, the semiconductor surface and the interface has to be maintained mathematically expressed by

$$Q_G + Q_s + Q_{it} = 0. \tag{29}$$

Any change of the gate charge δQ_G has to be compensated by other charges. Gate charge and gate voltage are related by the total capacitance of the MOS via

$$\delta Q_G \ = C \cdot \delta U_G. \tag{30}$$

Because the interface traps behave like a voltage-dependent charge, they can be treated as a capacitor C_{it}. The interface trap capacitance C_{it} and the semiconductor surface capacitance C_s are functions of the surface potential ψ_s

$$C_{it}(\psi_s) = \frac{dQ_{it}}{d\psi_s}, \tag{31a}$$

$$C_s(\psi_s) = \frac{dQ_s}{d\psi_s}. \tag{31b}$$

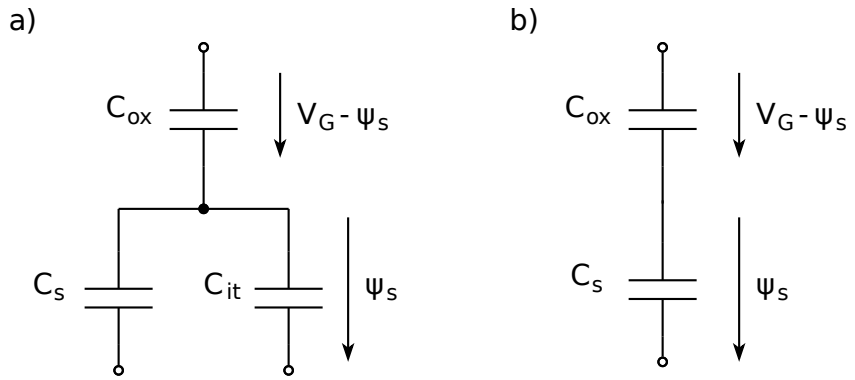

Figure 17: (a) Low frequency and (b) high frequency equivalent circuit of a MOS capacitor.

To maintain the notation of standard literature the capacitance of the semiconductor due to the semiconductor charge is designated as semiconductor surface capacitance C_s. Except in inversion the semiconductor capacitance equals the depletion capacitance $C_s = C_d$. And inversion usually does not occur in 4H-SiC due to the large band gap.

Using the oxide capacitance the charge neutrality eq. 29 can be rewritten as

$$C_{ox}(V_G - \psi_s) = -Q_{it} - Q_s. \tag{32}$$

A look at figure 17a should clarify the procedure. Now the relation of a slow, infinitesimal change of the gate voltage to the surface potential can expressed via

$$\frac{dV_G}{d\psi_s} = \frac{C_{ox} + C_{it} + C_s}{C_{ox}}. \tag{33}$$

As can be seen in the equation above the presence of interface traps and therefore an interface capacitance C_{it} influences the change of the surface potential (=band bending) with gate bias. Therefore a stretchout of the CV curve is observed when interface traps are present.

If the capacitance of a MOS structure is measured quasi static or with a low frequency all interface traps have enough time to respond and the equivalent circuit of figure 17a applies with the total capacitance

$$C_{LF} = (C_s + C_{it})\frac{C_{ox}}{C_{ox} + C_s + C_{it}}. \tag{34}$$

If the capacitance is measured with a gate voltage with superimposed AC frequency $dV_G(\omega)$ the total charge of the MOS is supposed to vary with this frequency. Not all interface traps are able to capture and emit electrons fast enough and therefore $dQ_{it}(\omega)$ and $C_{it}(\omega)$ become functions of the frequency. For high enough frequencies the contribution of the interface traps to the total capacitance disappears $\delta Q_{it}(\omega \to \infty) = 0 \ \to \ C_{it} = 0$. In this

case figure 17b applies as equivalent circuit and the total capacitance becomes

$$C_{HF} = \frac{C_s C_{ox}}{C_{ox} + C_s}. \tag{35}$$

For intermediate frequencies only the traps with response times between the sweep rate and $1/\omega$ participate. See section 2.4.3 for more details about interface trap time constant.

3.1.1 High frequency capacitance method (Terman)

The high frequency capacitance method, often called Terman method was one of the first methods for interface trap characterization developed 1962 by Terman [56]. In the Terman method the CV curve of a MOS structure is measured with a slowly sweeping gate voltage with a superimposed AC signal to measure the capacitance. Usually frequencies between 100 kHz and 1 MHz are used. As discussed above only a minority of the interface traps can follow this fast AC signal and therefore the high frequency capacitance from equation 35 is measured. This is the same capacitance as in an ideal MOS capacitor with $D_{it} = 0$. The interface traps can not follow the fast superimposed AC signal, but they can easily follow the slowly varying gate voltage. Because of the change in interface occupancy and therefore interface charge during the slow gate bias sweep the surface charge has to adjust to maintain charge neutrality, as discussed above. The presence of interface traps result in a strechout of the CV curve as described in equation 33. Using this equation the $dV_G/d\psi_s$ relation of an ideal MOS with the same doping concentration and oxide thickness as the sample under test can be calculated. Figure 18 compares an ideal MOS with that having $D_{it} = 1 \cdot 10^{12}$ cm^{-2}eV^{-1} uniformly distributed across the forbidden energy band. A strechout of the curve can be seen over the entire voltage range. If the interface traps were concentrated in a certain energy range, a much slower change in capacitance would be observed when the surface potential passes this region.

To obtain D_{it} from a measured CV curve one needs to have a model of an ideal MOS with the same properties. Using equations 16 to 20 the capacitance versus surface potential of an ideal MOS can be calculated. In figure 19 both the ideal and the measured curve are depicted. Now, for each capacitance value one can get the corresponding ψ_s and V_G values like illustrated with the dashed lines. For this particular case, a gate voltage of $V_G = -2$ V corresponds to a surface potential of $\psi_s = -0.4$ V. Doing this for every capacitance value gives a ψ_s versus V_G curve like in figure 20. In this type of visualization, the influence of the interface traps is easy to see. Having this relation and rewriting equation 33 to

$$C_{it}(\psi_s) = C_{ox}\left(\frac{dV_G}{d\psi_s} - 1\right) - C_s(\psi_s), \tag{36}$$

the interface trap capacitance can easily be calculated. The interface trap density D_{it} is

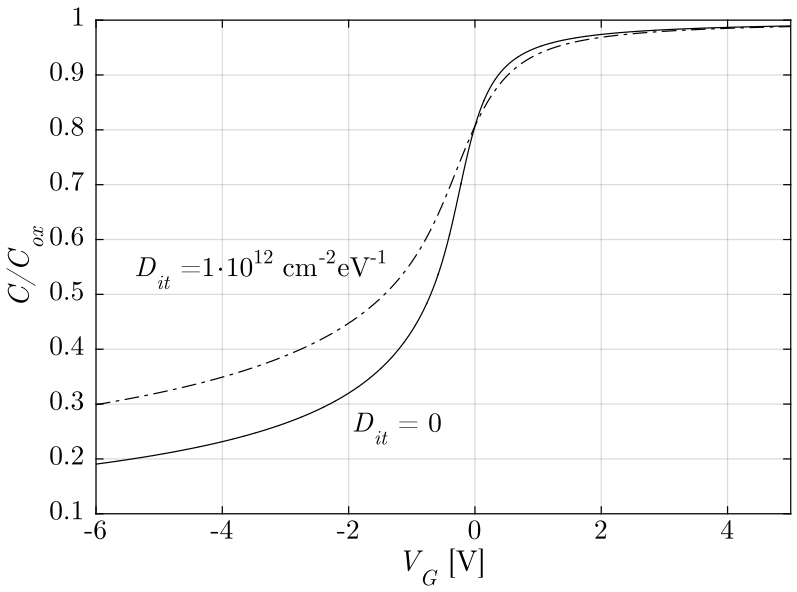

Figure 18: Calculated CV curves of a 4H-SiC MOS structures with $N_D = 1 \cdot 10^{16}$ cm^{-3} and $C_{ox} = 55$ nF/cm^2. One curve with $D_{it} = 0$ and one with $D_{it} = 1 \cdot 10^{12}$ cm^{-2}eV^{-1} uniformly distributed across the forbidden energy band.

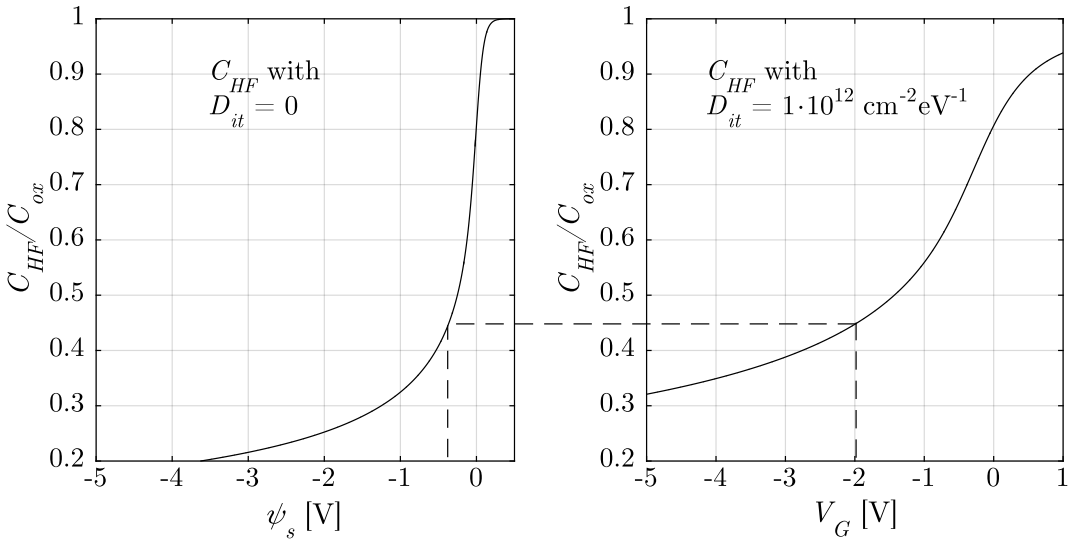

Figure 19: Theoretical trap free HF capacitance versus surface potential ψ_s (left) and HF capacitance versus gate voltage V_G of a MOS structure with $D_{it} = 1 \cdot 10^{12}$ cm^{-2}eV^{-1} uniformly distributed across the forbidden energy band (right). Reprinted for 4H-SiC MOS after [32].

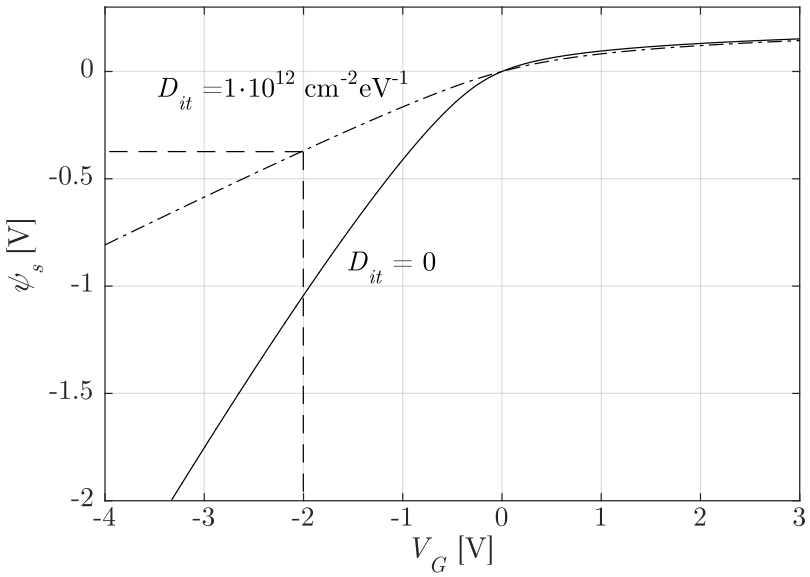

Figure 20: Calculated ψ_s versus V_G plot of a trap free MOS and one with $D_{it} = 1 \cdot 10^{12}$ cm^{-2}eV^{-1}.

the number of traps per unit area and unit energy. One trap can take the elementary charge q, it follows $dQ_{it} = qD_{it}dE$. In combination with equation 31a it follows

$$D_{it}(\psi_s) = \frac{C_{it}(\psi_s)}{q}. \tag{37}$$

Note: This equation applies if the energy is measured in eV and the surface potential(=band bending) in V. The energy position of a trap level E_T in the bandgap can be calculated using

$$(E_C - E_T) = E_i - q\Phi_B - q\psi_s. \tag{38}$$

The conduction band edge is used as reference level.

The Terman method is also criticized because of some disadvantages [57]. One criticism is that the used measurement frequency of 1 MHz or in some cases less does not exclude all interface traps from the measured capacitance C_{HF}, because some, especially near the band edges, have very fast emission times and are able to follow this frequency. Also the lower limit of detection in the $5 \cdot 10^9$ to 10^{10} cm^{-2}eV^{-1} range is a point for criticism. Lower trap concentration are not detectable with regular capacitance measurement devices, because C_{it} becomes very small compared to C_s and C_{ox} and therefore the strechout of the CV curve is so weak that it is not detectable. Good quality Si-SiO_2 interfaces have such low interface trap densities that they can no longer be measured with the Terman method. Due to its simplicity and the fact that only the high frequency capacitance needs to be measured the Terman method is still widely used to characterize MOS structures with

insulators other than SiO_2 or to make quantitative measurements to compare different treatments.

3.1.2 Low frequency capacitance method

Berglund [58] developed an interface trap characterization method based on the low frequency capacitance of a MOS structure. The CV curve is measured with a low frequency AC signal or with quasi static techniques to allow most of the interface traps to respond. The measured capacitance C_{LF} follows from figure 17b and equation 34. Additionally the strechout is observed, because the interface traps can also follow the slow sweep of the gate voltage. Equation 34 can be rearranged to

$$C_{it} = \left[\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right]^{-1} - C_s. \tag{39}$$

To calculate C_{it} the measured $C_{LF}(V_G)$ values and calculated $C_s(V_G)$ values are needed. With the equations in section 2.3 $C_s(V_G)$ is obtained. To determine the energy position of the traps, C_{it} and hence C_s must be known as functions of ψ_s. Therefore the ψ_s - V_G relationship needs to be known. Berglund suggests using the integral

$$\psi_s = \psi_{s0} + \int_{V_{G0}}^{V_G} \left[1 - \frac{C_{LF}(V_G)}{C_{ox}}\right] dV_G \tag{40}$$

to calculate the ψ_s - V_G relation out of the measured C_{LF} values. This relationship can be used to calculate $C_s(\psi_s)$ and $C_{LF}(\psi_s)$. The integration constant $\psi_{s0}(V_{G0})$ is not known. Usually a value of V_{G0} in accumulation, where ψ_{s0} is small, is used to solve the integral to minimize uncertainties. Using $V_{G0} = V_{FB}$ would give $\psi_{s0} = 0$ and therefore no error, but an exact determination of V_{FB} is difficult. D_{it} versus E_T values can be obtained same as above using equations 37 and 38. The accuracy of the low frequency capacitance method depends on the ability to measure the quasi static capacitance with high precision and on the error in determining V_{FB} or guessing V_{G0}.

3.1.3 High-low frequency method

The high-low frequency method was first described by Castagné and Vapaille [59]. This method eliminates the need to have a theoretical CV curve. Instead of an ideal curve, the CV curve of the MOS capacitor is measured twice. With a low frequency or quasi static and with a high frequency. Rearranging the C_{HF} equation 35 and inserting it into equation 39 gives

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1}. \tag{41}$$

This equation gives $C_{it}(V_G)$ only from measured values. To calculate the energetic position of a trap, $C_{it}(\psi_s)$ and hence the ψ_s - V_G relationship is needed. Equation 40 can be used again. A big advantage of this method is that devices with non-uniform or unknown doping profile can be characterized where a theoretical calculation is difficult to impossible. The uncertainties in calculating the ψ_s - V_G relation define the accuracy of this method.

3.1.4 Surface potential - depletion capacitance ($C - \psi_s$) method

In 2012 Yoshioka *et al.* [60] introduced a new method for interface trap characterization using measured high and low frequency CV curves. The method uses the measured C_{LF} and equation 39 to determine the interface trap density and the high frequency CV curve to determine the integration constant $\psi_{s0}(0)$ from the Berglund integral 40. It is suggested that SiC-MOS capacitors have very fast interface traps, that measurement frequencies of about 100 MHz would be needed to measure a true HF CV curve. At the usual 1 MHz, the evaluation of the ψ_s - V_G relation in the Therman method, or the extraction of the flatband voltage via the flatband capacitance is faulty. To overcome this problem a method to determine $\psi_{s0}(0)$ exactly is presented. When a MOS is in deep depletion ($\psi_s < 2\psi_B$) frequencies of 1 MHz are sufficient to assume $(C_s + C_{it}) \approx C_d$. In deep depletion the depletion capacitance is given by [25]

$$\frac{1}{(C_s + C_{it})^2} \approx \frac{1}{C_d^2} = -\frac{2\psi_s}{qA^2\epsilon_s N_D}, \tag{42}$$

with A being the surface area of the MOS. Having the measured C_{HF} values one can calculate $C_s = (C_{HF}C_{ox})/(C_{HF} - C_{ox})$ and $\psi_s = C_{HF}V_G/C_s$. A plot of $1/C_d^2$ versus ψ_s is shown in figure 21. A linear fit of the curve in deep depletion gives the integration constant $\psi_{s0}(0)$ at the y-axis intersection. With this constant the Berglund integral can be solved starting at $V_{G0} = 0$. Using the thus obtained ψ_s - V_G relationship $C_{LF}(\psi_s)$ and $C_s(\psi_s)$ can be calculated and used in equation 39 to determine the interface trap capacitance. The doping concentration N_D can also be extracted using the slope of the linear fit. The accuracy in determining $\psi_{s0}(0)$ depends on the validity of the approximation $C_s \approx (C_s + C_{it})$. The fit should only be done in the deep depletion region ($\psi_s < 2\psi_B$). This method only works for wide band gap semiconductors that can be biased in deep depletion without the presence of minority carriers.

3.2 Conductance method

The conductance method [61] is a more complex method, but provides more information about interface traps than just their quantity and energetic position. This method does not require a measured CV curve, instead an admittance measurement over a large

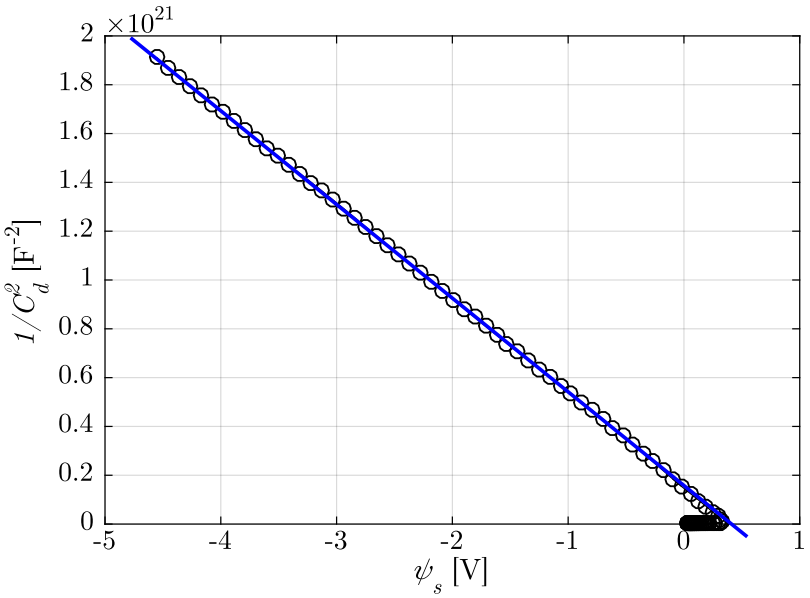

Figure 21: A typical plot of measured $1/C_d^2$ over ψ_s data with linear fit in the deep depletion region. Intercept with the ψ_s-axis equals the integration constant ψ_{s0}.

frequency range $\omega = 2\pi f$ at different gate voltages is needed. The admittance is the inverse of the impedance and can be split up in a conductance with a parallel capacitance $Y_P = 1/Z = G_p + j\omega\, C_p$.

Now consider a MOS with interface defects distributed in energy. At a gate voltage with superimposed AC signal ($V_G + v_{AC}(\omega)$) the surface potential (surface Fermi level) is at a level defined by the DC part of the gate voltage and it varies a few meV around this position due to the AC part. Interface traps in this range of energy will capture and emit charges due to the varying Fermi level if they can follow the change. A charge movement out of phase results in an energy loss that is supplied by the AC signal. Now the frequency is swept from low to high frequencies. At low frequencies the majority of traps can easily follow the AC signal and the losses are small. With increasing frequency more and more traps cannot follow the AC signal immediately and the capture and emission process is lagging behind the Fermi potential change. This results in losses and an increase in conductivity. At even higher frequencies most of the traps are not able to follow the changing Fermi level at all and no charge movements occur. The losses decline at high frequencies. These losses can be measured as an equivalent parallel conductance $G_p(\omega)$. Each frequency sweep at a specific gate voltage gives the density D_{it}, the emission time constant τ_e and the surface fluctuation σ_s for one energy position. Many measurements at different gate voltages are required to get a dense coverage in the energy spectrum.

To get a better understanding of what is measured and what is calculated figure 22 shows three equivalent circuits of a MOS with interface traps at a specific gate voltage V_G.

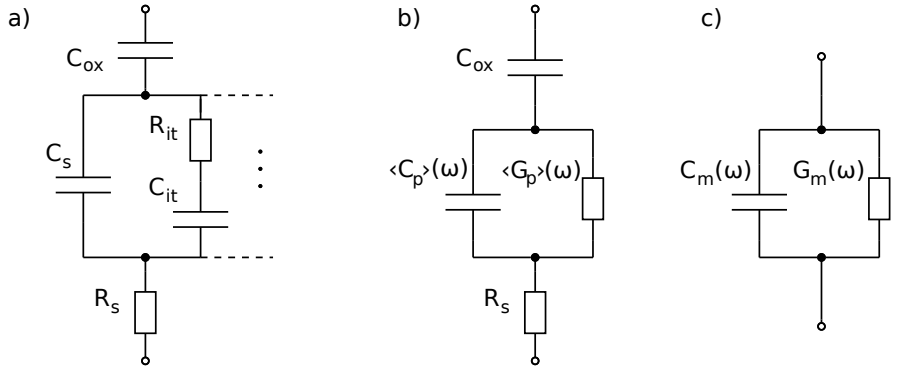

Figure 22: Equivalent circuits of a MOS at a gate voltage V_G. All shown quantities are functions of V_G and hence ψ_s. (a) full equivalent circuit, (b) combined to a parallel capacitance and conductance and (c) measurement equivalent circuit.

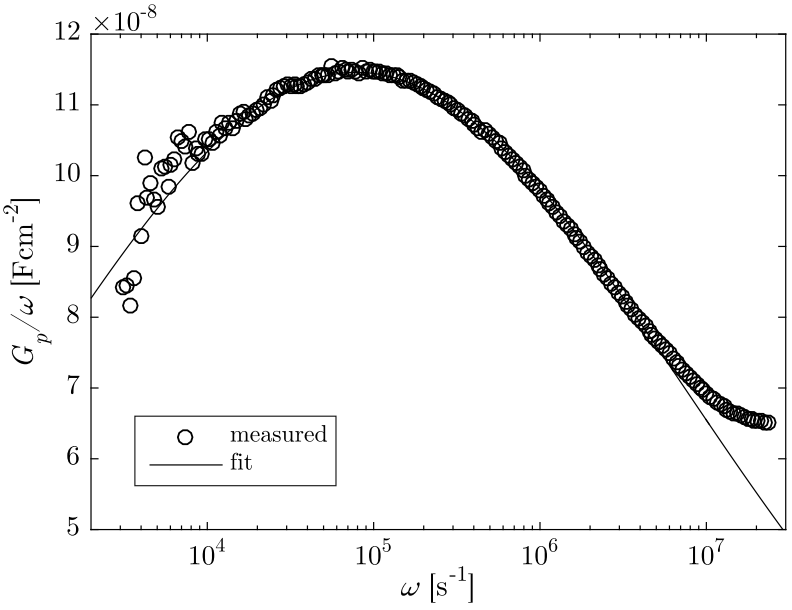

Figure 23: Measured and corrected conductance versus ω and best fit of equation 44.

Circuit (a) shows the most detailed representation with separate oxide and semiconductor capacitance and series resistance. The branch representing the interface trap can be seen as parallel combination of patches with an RC combination, each represents a trap with time constant $\tau_{it,n} = R_{it,n}C_{it,n}$. All together have an average time constant τ_{it}. This effect is called time constant dispersion. If all traps were on a single energy level, then there would only be one branch and one time constant. In (b) all parallel components are combined to the admittance $\langle Y_P \rangle = \langle G_p \rangle + j\omega\langle C_p \rangle$. Circuit (c) shows the equivalent circuit when measuring the MOS with an impedance analyzer giving a parallel capacitance C_m and a parallel conductance G_m. C_{ox} and R_s can be measured separately by measuring the impedance (C in series with R) in accumulation.

The equivalent circuit (b) follows from (a) by calculating the equivalent parallel conductance and capacitance using

$$\frac{\langle G_p \rangle}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}}\ln(1 + (\omega^2\tau_{it}^2)), \qquad (43a) \qquad \langle C_p \rangle = C_s + \frac{qD_{it}}{\omega\tau_{it}}\arctan(\omega\tau_{\mathrm{it}}). \qquad (43b)$$

In addition to the time constant dispersion a phenomenon called surface potential fluctuations must be considered when real MOS capacitors are measured. This is due to a random distribution of charges in the oxide, doping inhomogeneities and a distribution of capture cross sections. This effect is considered using a Gaussian distribution of the potential around the Fermi level. A more detailed explanation about this effect can be found in [32]. This gives the new equations

$$\frac{\langle G_p \rangle}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}} \frac{1}{\sqrt{2\pi\sigma_s^2}} \int_{-\infty}^{\infty} \mathrm{e}^{\eta} \ln(1 + \omega^2\tau_{it}^2\,\mathrm{e}^{-2\eta}) \exp\left(-\frac{\eta^2}{2\sigma_s^2}\right) d\eta, \qquad (44)$$

$$\langle C_p \rangle = C_s + \frac{qD_{it}}{\omega\tau_{it}} \frac{1}{\sqrt{2\pi\sigma_s^2}} \int_{-\infty}^{\infty} \mathrm{e}^{\eta} \arctan(\omega^2\tau_{it}^2\,\mathrm{e}^{-\eta}) \exp\left(-\frac{\eta^2}{2\sigma_s^2}\right) d\eta. \qquad (45)$$

where $\eta = q/(k_BT)(\psi_s - \langle\psi_s\rangle)$ is the normalized difference between the surface potential to its mean value, and σ_s the standard deviation of the surface potential due to fluctuation in units of k_BT/q.

In the evaluation process the equivalent circuit (b) is derived from (c). The first step is to compensate for the series resistance using

$$C'_m = \frac{(G_m^2 + \omega^2C_m^2)C_m}{a^2 + \omega^2C_m^2}, \qquad (46a) \qquad G'_m = \frac{(G_m^2 + \omega^2C_m^2)a}{a^2 + \omega^2C_m^2}. \qquad (46b)$$

With $a = G_m - (G_m^2 + \omega^2C_m^2)R_s$, G_m and C_m are the measured values. The compensated values are used to calculate the equivalent parallel conductance according to

$$\frac{\langle G_p \rangle}{\omega} = \frac{\omega C_{ox}^2 G'_m}{G'^2_m + \omega^2(C_{ox} - C'_m)^2}. \qquad (47)$$

Now equation 44 can be fitted to the measured $\langle G_p \rangle / \omega$ values using the three fitting parameters (D_{it}, τ_{it}, σ_s). An example of measured points and the best fit is provided in figure 23. The time constant dispersion and the surface potential fluctuation account for a broadening and lowering of the $\langle G_p \rangle / \omega$ peak. To get the energetic position of the fitted data the ψ_s - V_G relationship is needed to map the used gate voltage to an energy positions. Equation 38 gives the position in the bandgap.

One big advantage of this method is the ability to measure interface trap densities of 10^9 cm^{-2}eV^{-1} and below. Also the time constant and using equation 25 the capture cross section of a trap can be obtained as a function of energy. The disadvantages are the need of many measurements and the complex evaluation.

3.3 Mobile charge measurement

Mobile charges can lead to sever problems during devices operation and also can interfere with D_{it} measurements. Therefore two methods are presented to measure the amount of mobile charges in a MOS structure. The theoretical background is presented in section 2.4.4. The charge density Q_m and the ion density N_m are related via $Q_m = qN_m$ assuming that an ion carries the elementary charge q.

3.3.1 Bias temperature stress

As discussed above, the amount and position of mobile charges inside the oxide influences the flatband voltage V_{FB} of a MOS device. A straightforward way to estimate the amount of mobile charges is the bias temperature stress (BTS) method. The MOS structure is biased with a positive gate voltage and held at elevated temperature (200 to 300 °C) for a few minutes to allow all mobile ions to drift to one side of the oxide. Then the device is cooled to room temperature or below under bias. When the temperature is reached the charges are 'frozen' at their current position. Next a high frequency CV curve is measured. The same procedure is repeated with opposite bias polarity. The two CV curves are shifted by a voltage ΔV_{FB} due to the different positions of the mobile ions in the oxide. Figure 24 shows the shift in the curves. The amount of mobile charge follows from this voltage shift by

$$N_m = \frac{C_{ox} \Delta V_{FB}}{q}. \tag{48}$$

The BTS method works for charge densities of about 10^9 C $\cdot$ cm^{-2} and above [33]. Caution is advised not to apply too high electric field strengths to allow charge injection or to damage the oxide at the elevated temperature.

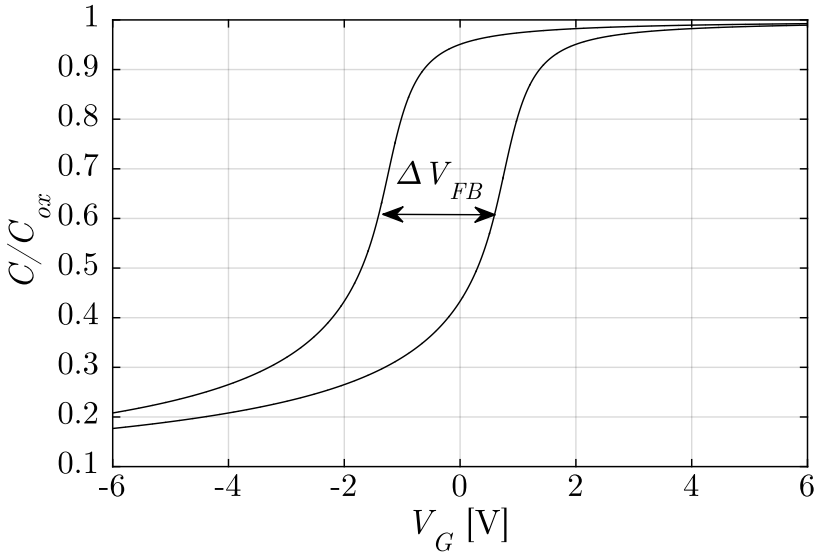

Figure 24: CV curve shift due to mobile charges.

3.3.2 Triangular voltage sweep

The triangular voltage sweep (TVS) method [62] detects mobile charges by measuring a displacement current instead of a capacitance. The MOS is held at elevated temperatures (200 to 350 °C) while a linear voltage ramp is applied to the device. At these elevated temperatures most of the ions are mobile and will travel through the oxide in a certain gate bias range, resulting in a current. Usually QS capacitance meters are used in the TVS method. QS meters measure the charge transfer through the device. The gate current is defined as the change of gate charge in time

$$I_G = \frac{dQ_G}{dt}. \tag{49}$$

Inside the MOS structure charge neutrality must be maintained $Q_G = Q_s - Q_{it} - Q_m - Q_{ot} - Q_f$. The measured current becomes [32]

$$I_G = C_{LF}\frac{dV_G}{dt} - C_{LF}\frac{dV_{FB}}{dt}. \tag{50}$$

Where $C_{LF}(V_G)$ is the low frequency capacitance after equation 34 of a mobile charge free device. Note: $C_{LF} = C_{ox}$ as often found in literature does not apply for wide bandgap semiconductors at the used measurement temperatures. The measured gate current I_G of equation 50 is composed out of two parts: the displacement current on the left and the charge transfer due to the mobile ions on the right. Integrating both sides of equation 50 from $-V_G$ to V_G and assuming that all mobile charges are at the gate-oxide interface at

$-V_G$ and at the oxide-semiconductor interface at V_G gives

$$N_m = \frac{C_{ox}}{\alpha q} \int_{-V_G}^{V_G} \left(\frac{I_G}{C_{LF}} - \alpha \right) dV_G. \tag{51}$$

Because linear voltage ramps are used $\alpha = dV_G/dt$. Some QS-CV methods like the improved feedback charge method discussed below directly give the capacitance instead of the current over gate voltage. Than the mobile charge density follows from the area between the measured C_{QS} curve and the charge free C_{LF} curve via

$$N_m = \frac{1}{q} \int_{-V_G}^{V_G} (C_{QS} - C_{LF})\, dV_G. \tag{52}$$

Advantages of this method are the higher resolution of about 10^9 C $\cdot$ cm^{-2}, the possibility to distinguish between different mobile ions species and the immunity against changes in interface trap density with temperature. The evaluation process, however, is much more complicated than in the BTS method.

3.4 Quasi-Static CV measurement circuit

As can be seen above, many characterization techniques require a low frequency CV curve. The best way to get such a curve is a quasi-static CV measurement. To be able to perform such measurements a QS-CV measurement circuit according to the improved feedback charge method [63] has been constructed and used for measurements. Figure 25 shows a schematic of this method. The DUT, labeled as C_x, is connected between a precision voltage source and a feedback charge amplifier (integrator). The feedback loop of the OpAmp is built of a reference (integration) capacitor C_r in parallel with a high impedance relay S. In the initial state of the circuit, S is closed and therefore C_r is discharged and the voltage source sources V_0. At t_0 the relay S opens and any current flowing through the DUT is integrated by the OpAmp and stored as charge in C_r. The amount of transferred charge can be measured as $\Delta V_{out} = -\Delta Q/C_r$. When a voltage step $V_0 + \Delta V$ is applied to the DUT at t_1, the charge $\Delta Q = C_x \Delta V$ must be transferred and results in a change of the output voltage of $-\Delta V_{out}$. By measuring V_{out} before and after the step of the input voltage the capacitance of the DUT follows by

$$C_x = \frac{\Delta Q}{\Delta V} = -C_r \frac{\Delta V_{out}}{\Delta V}. \tag{53}$$

Afterwards at the time t_2 the relay S is closed again, and the procedure starts from the beginning, with $V_1 = V_0 + \Delta V$ being the new start voltage. ΔV can have both polarities allowing ramps in either direction. The time between t_1 and t_2 will be designated as

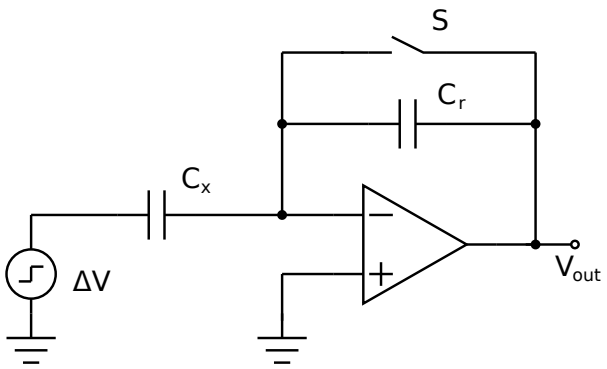

Figure 25: Schematic of improved feedback QS-CV measurement circuit after [63].

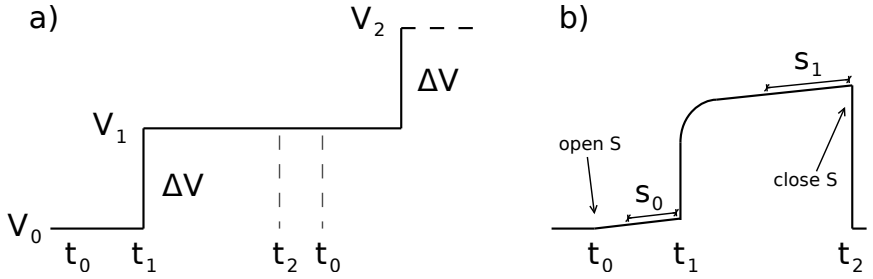

Figure 26: Timing sequence of (a) the voltage source and (b) the measured charge.

measurement time $t_m = t_2 - t_1$.

A timing diagram of the sequence is depicted in figure 26. The left figure shows the output of the voltage source connected to the DUT. On the right the measured charge $Q = -V_{out}C_r$ is displayed. After S is opened the charge Q slowly increases due to the leakage current through the DUT. When the voltage step is applied Q quickly increases while the slope due to the leakage current is still present. After the time t_2 the relay is closed again. The slope of the Q-t curve is measured before and after the step and is averaged in the designated regions s_0 and s_1. Out of the slopes the amount of leakage current can be calculated ($I = dQ/dt$). By compensating the measured Q-t curve for the leakage current the exact height of the step ΔQ and hence C_x can be calculated. The shape of the measured Q-t curve depends on the DUT. An ideal capacitor would have no leakage and the response wound be a perfect step function. In case of a leaky MOS the Q-t curve looks more like in figure 26b with a rounded edge due to the settling time of minority carrier generation-recombination or interface trap response. Therefore the slope s_1 and the corresponding charge is measured near the end close to t_2. In long lifetime semiconductors this settling time could be hundreds of seconds depending on the step height and the temperature and therefore longer measurement times should be used to avoid errors.

In the past alternative QS-CV measurement methods like the ramp method [64, 65, 66]

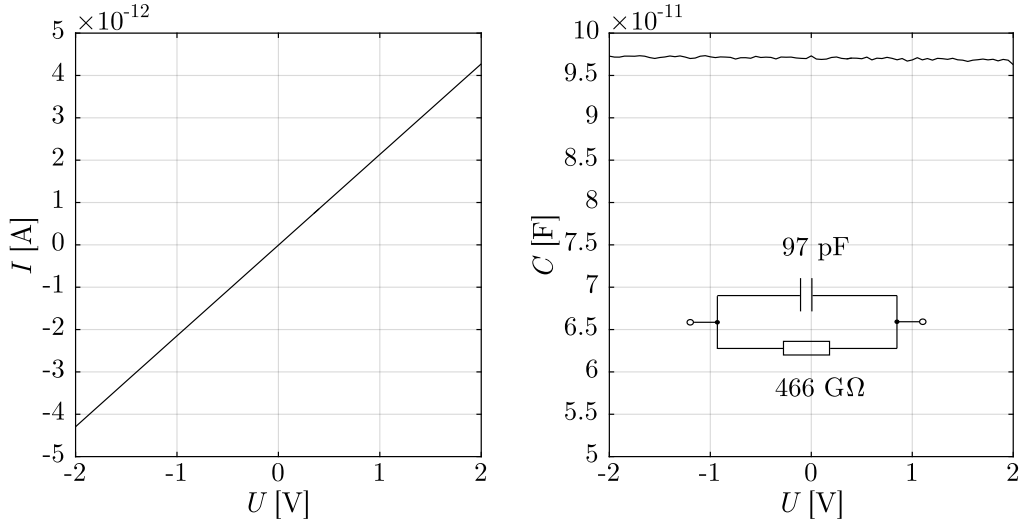

Figure 27: Current and capacitance measurements of a capacitor in parallel with a high value resistor. $\Delta V = 50$ mV, $t_m = 6.67$ s.

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and the Static and QV method [67, 68] were proposed. However, the improved feedback QS-CV method used here has some advantages over the other two. Due to the used feedback loop the node at the non-inverting input is at virtual ground potential, which reduces the requirements for high impedance insulation. Furthermore, the used method makes it easy to distinguish between leakage currents and displacement currents. Also the signal-to-noise ratio is much higher compared to the ramp method.

Results: In the following a few measurement results of the custom-built QS measurement circuit are presented. A Keithley high precision SMU and an Agilent 34410a DMM are used as voltage source and to measure the output signal, respectively. As reference capacitor C_r a value of 105 pF is used to cover a measurement range of about 20 to 500 pF. The circuit was built only with ultra-low leakage components and with sufficient insulation between the components. The whole setup is placed inside a shielded metal box. For testing and calibration several different capacitors have been measured. To illustrate the performance of the built circuit a capacitor with a high value resistor in parallel to simulate leakage are used as DUT. Figures 27 and 28 show the results of the these pre-investigations with known components. The DUT has been characterized prior the measurement to calculate the measurement error of the circuit. The accuracy of the capacitance measurement is measured to be within 1%. The accuracy of the current measurement is hard to determine because all available instruments have a large error in this low current range. But due to the high level symmetry and an offset of only -28 fA the current measurement should be very accurate as well. Figure 28 shows the measured output voltage of the OpAmp as a

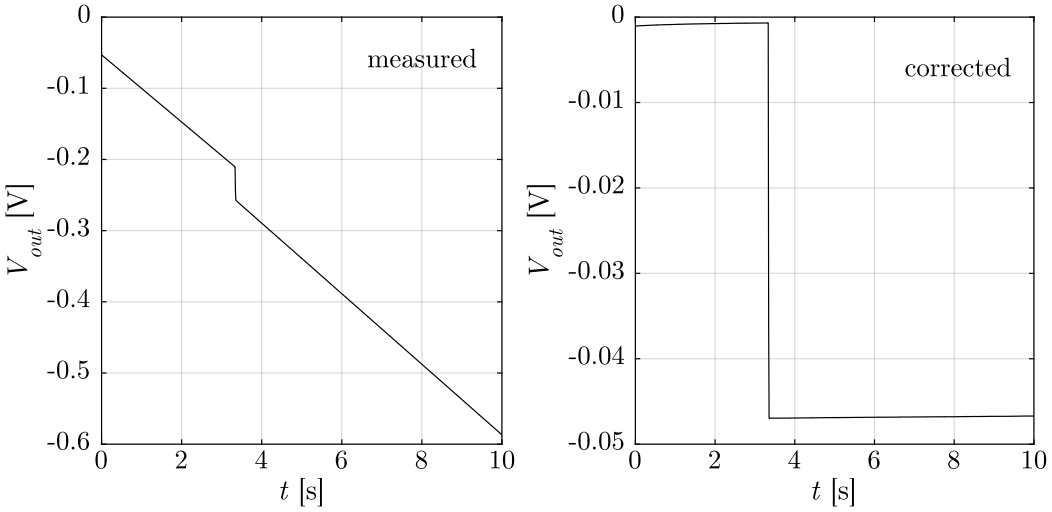

Figure 28: (left) Measured voltage V_{out} at the step from 1.00 to 1.05 V from the measurement in figure 27. At $t = 0$ the relay S is opened and at $t = 3.33$ s the voltage step is applied. (right) Output voltage corrected for leakage currents.

function of time before and after compensating the impact of the leakage current. The resolution and the accuracy strongly depend on the shielding and the used instrument for the voltage step. With the used setup and offset compensation the smallest resolvable current is about 5 fA.

3.5 Breakdown voltage measurement

The breakdown voltage of an insulator is one of the most important parameters, especially when insulators become thinner and thinner. Instead of the breakdown voltage the dielectric strength is often used because it is related to the thickness. Usually the dielectric strength is defined as the electric field at which the insulator is irreversibly damaged. Several different measurement techniques are used to determine the dielectric strength. The most widely used method is the voltage ramp method, where a voltage ramp is applied to the insulator while the current is measured. The breakdown voltage is the voltage at which a predefined current density J_l is reached. Another often used technique is the time-dependent gate oxide breakdown (TDDB) method, where a relatively low electric field is applied to the insulator and the time until a pre-set current limit J_l is reached is measured. The results of both methods are related through the concept of charge to breakdown Q_{BD}. The actual breakdown mechanism can be divided in two types, the intrinsic breakdown and the defect-related breakdown. The intrinsic breakdown occurs due to damaging of the oxide due to electron or hole injection, impact ionization or energy dissipation at the metal-dielectric interface leading to breaking bonds and free ions creating a conductive path over time. The defect-related breakdown usually occurs before the

intrinsic breakdown and can be related to metal and inorganic impurities inside the oxide or an uneven surface, that creates metal hence, electric field spikes into the oxide. Because of the different breakdown mechanisms and generally slight differences between individual samples the breakdown voltage has a strong statistical nature. Therefore usually a large number of samples is measured and the probability of breakdown in a certain electric field strength range is calculated out of the measured data. This distribution is visualized using a Weibull plot. [69]

4 Device Fabrication

As substrate a nitrogen doped (0001) Si-face 4° off axis 4H-SiC wafer from SiCrystal is used. The wafer has a thickness of 350 µm with a doping density of 10^{19} cm^{-3} and a 5 µm thick epitaxially grown drift layer with $N_D = 10^{16}$ cm^{-3} on top. The wafer is cut into $0.5 \cdot 0.5$ cm^{-2} pieces. A "Von Ardenne" (LS 730) sputtering machine with 2 AC/DC and 1 DC magnetron sputtering units and one AC-ISE unit is used for the deposition of the top contact metallization.

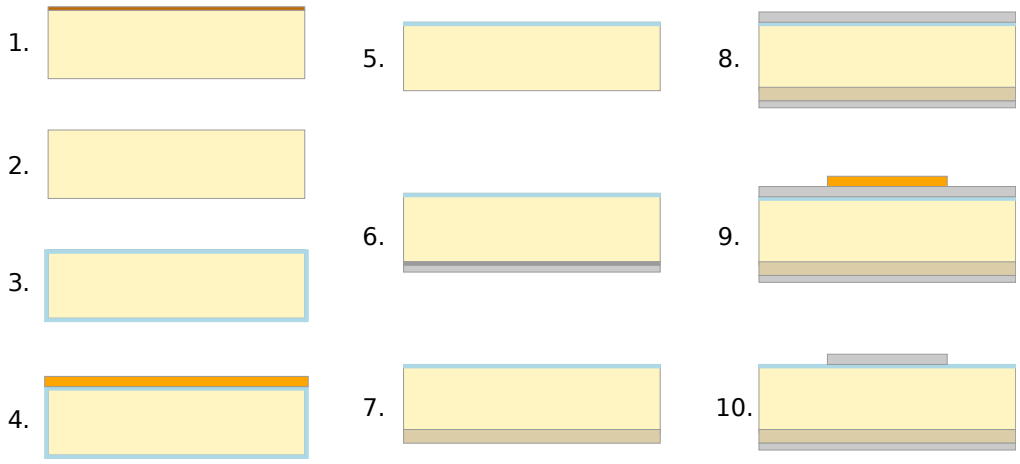

Figure 29: Different fabrication steps of a MOS structure. Substrate: 4H-SiC, orange: photoresist, light blue: SiO_2, gray: metals.

All following processes are performed under cleanroom conditions. In figure 29 the cross-section of a sample in all important fabrication steps is depicted schematically. The sequence starts with a SiC sample with a thin layer of photo-resist, a very thin layer of native oxide and some dirt from cutting and handling. The epitaxial layer is on the top side, but not shown for simplicity. To obtain a MOS device the SiC sample undergoes the following procedures:

1. - 2.: The first and perhaps most important step is the cleaning procedure. At first, the SiC sample is placed in an ultrasonic bath with acetone for a few minutes to remove the photoresist film and organic contaminations from the surface followed by a rinse with isopropyl alcohol (IPA). The next step is a RCA clean [70]. The RCA clean consists of two solutions SC-1 and SC-2. SC-1 is made out of H_2O, $NH_4OH(29\%)$, $H_2O_2(30\%)$ in a ratio of 5:1:1 and effectively removes organic residues and insoluble particles. SC-2 is made out of H_2O, $H_2O_2(30\%)$, $HCl(37\%)$ in a ratio of 5:1:1 and removes the remaining traces of metallic (ionic) contaminants. Electronic-grade chemicals and deionized (DI)-water has been used. Both solutions are heated to 70-75 °C. The sample is placed in SC-1 for 10 minutes

followed by a rinse in DI-water, a dip in diluted HF and another DI-water rinse. Then it is placed in SC-2 for 10 minutes, again followed by a water rinse.

2. - 3.: The cleaned sample is immediately loaded into the oxidation furnace and is oxidized at 1100 °C under pure O_2 for 5 hours followed by an annealing step in Ar atmosphere at 1000 °C for 1 h.

3. - 4.: The top surface of the sample gets covered with photoresist.

4. - 5.: The sample is dipped in a buffered oxide etch (BOE) solution (H_2O, NH_4F, HF) for 2-3 minutes to remove any oxide from the exposed surfaces. Afterwards the resist is stripped using acetone and IPA.

5. - 6.: 100 nm Ti and 400 nm Al are sputter deposited on the backside.

6. - 7.: The sample is annealed at 1000 °C under Ar atmosphere for 10 minutes to allow the formation of an ohmic contact.

7. - 8.: 500 nm Al is sputter deposited on the top side to act as gate electrode and 100 nm Pt is sputtered on the back side as protective layer of the ohmic contact.

8. - 9.: Circular photoresist pads of 500 µm in diameter are applied using photolithography.

9. - 10.: Phosphoric acid (H_3PO_4) heated to 60-65 °C is used to etch the Al layer. Afterwards the photoresist is stripped using acetone and IPA.

5 Results and Discussion

Several SiC samples have been prepared to collect experience with the oxidation process and to get familiar with the measurement techniques. In the following section the measurement results of a few interesting samples are shown. Table 4 provides a list of the used samples. Sample A was one of the early samples where no ultrasonic cleaning step was performed, also the used HF was rather old and often used. For all other samples only fresh chemicals were used. Sample B and C are almost the same, but the HF dip in the cleaning sequence was changed from after the RCA clean to between SC1 and SC2. Sample D is made out of a silicon substrate for comparison.

The HF capacitance and conductance measurements were made with an Agilent 4294A high precision impedance analyzer and all LF-CV measurements were made using the self-made QS-CV measurement circuit. All measurements were performed inside a shielded needle prober stage under vacuum. The sample stage can be cooled and heated in the range of 35 to 650 K.

An atomic force microscope (AFM) from Bruker in tapping mode was used to inspect the oxide surface after the oxidation process. The surface topography of two different samples is depicted in figure 30. Sample A shows a very rough surface with an arithmetic average roughness of $R_a = 0.93$ nm. All the other samples which have been ultrasonically cleaned show a much smother surface with $R_a = 0.1$ nm. Presumably some organic residuals could not be removed without ultrasonic support and some carbon residuals got incorporated into the oxide during oxidation.

To measure the oxide thickness the surface was covered with photoresist and a circular test structure with 500 µm in diameter was patterned using standard photolithography. Afterwards the sample was etched in BOE for 2-3 min. After the resist was stripped the surface characteristics around the etched test structure was measured using an AFM. Figure 31 shows a typical mean surface profile at the edge of the prepared test structure. The step height equals the oxide thickness. As can be seen in table 4 the oxide thickness

Table 4: List of samples used in the following measurement results. Sample C is the main sample which has undergone all measurements. C_{ox} is measured in strong accumulation. (US = Ultrasonic Acetone cleaning)

Sample	**Substrate**	**Cleaning**	**Oxidation**	t_{ox}	C_{ox}
A	4H-SiC	SC1+SC2+HF	5 h O_2 1100 °C	63 nm	104 pF
B	4H-SiC	US+SC1+SC2+HF	5 h O_2 1100 °C	24 nm	285 pF
C	4H-SiC	US+SC1+HF+SC2	5 h O_2 1100 °C	24 nm	284 pF
D	Si	US+SC1+SC2+HF	40 min O_2 1000 °C	53 nm	131 pF

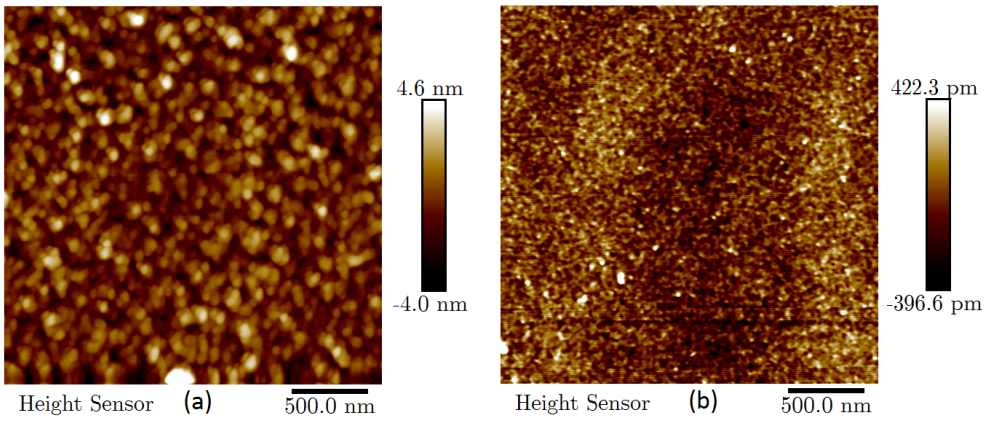

Figure 30: AFM images of the surface after oxidation (a): Sample A; (b): Sample C. Sample B, C and D have the same surface topology as the latter sample.

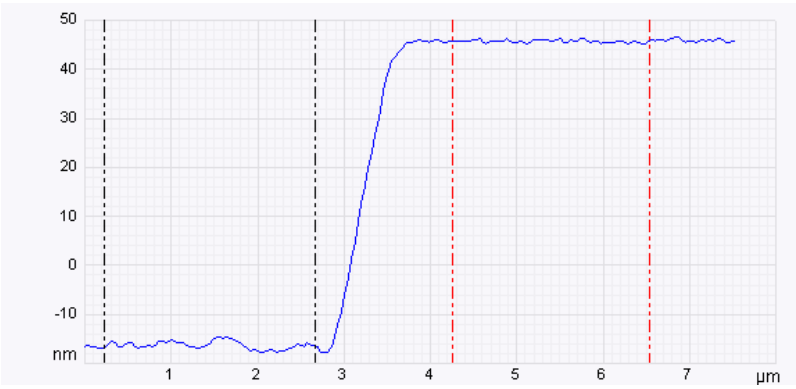

Figure 31: AFM measurement of the oxide thickness of sample A.

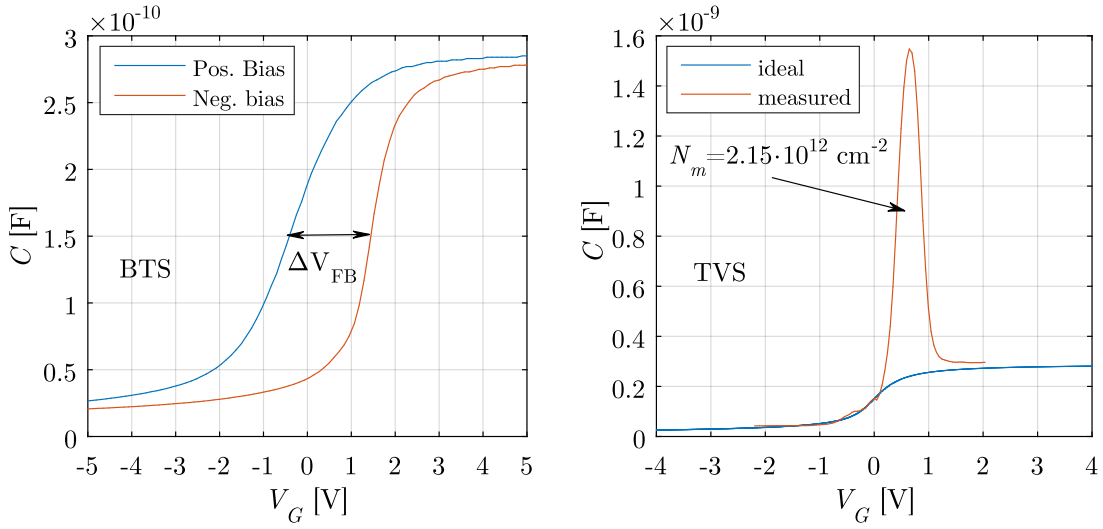

Figure 32: Measured CV curves of the BTS (left) and the TVS (right) method of sample C.

of sample A is much thicker compared to sample B and C, although all have been oxidized for the same amount of time in the same atmosphere. Presumably the oxide density of sample A is much lower due to incorporated carbon-oxide residuals. The permittivity ϵ_r of the four samples is calculated to be: A = 3.77; B = 3.93; C = 3.92; D = 3.99. The permittivity of sample A differs the most of the ideal value of $\epsilon_{r,SiO_2} = 3.9$.

5.1 Results of mobile charge measurements

Early HF-CV measurements at elevated temperatures showed a very steep increase of the CV curve, even steeper than the theoretical curve. This unusual shape indicated a massive amount of mobile ions in the oxide. During the voltage sweep the ions drift through the oxide, changing the flatband voltage and therefore lead to unusually steep CV curves. Therefore BTS measurements were performed on all samples to estimate the amount of mobile charges. An additional TVS measurement was performed on Sample C for comparison. In the BTS measurement the sample was heated to 550 K and a positive bias of 3-5 V was applied for 5 minutes. Then the sample was cooled down to 250 K under bias. When the temperature was reached a HF-CV curve from positive to negative voltage was measured. Afterwards the sample was heated up again and a negative bias was applied followed by a negative to positive CV measurement at 250 K. The measured CV curves of sample C are depicted in the left plot of figure 32. With this two CV curves the mobile charge density was calculated using equation 48 at several points around the estimated flatband capacitance point. Figure 33 shows the results. For the TVS measurement the self-made QS-CV measurement circuit was used. After the sample was heated to 600 K a QS-CV curve was measured with $\Delta V = 50$ mV and $t_m = 30$ s. At this high temperature

and with this long measurement time almost all mobile ion movements could be measured. The right plot of figure 32 shows the measured QS-CV curve in comparison with an ideal curve. The area between the two curves represents the amount of mobile charges according to equation 52. The results of all mobile charge measurements are depicted in figure 33. As can be seen in the figure, the sample A with the rough surface shows the highest amount of mobile charges of almost 10^{13} cm^{-2}. Using ultrasonic cleaning the mobile charge density could be reduced by almost a factor of five. Also the position of the HF dip in the RCA cleaning procedure seems to have an influence on the mobile charge density. The lowest mobile charge density of about 10^{12} cm^{-2} was measured in the Si sample. The fact that the mobile charge density in the silicon sample is still about two orders of magnitude above an acceptable value for MOSFETs, the main source of contamination is attributed to the manufacturing process, most likely to the oxidation furnace. The higher concentrations in the SiC samples might as well be due to intrinsic reasons such as CO_3-like defects as described in [44, 45]. A post oxidation annealing in Ar at even higher temperatures as the used 1000 °C might reduce the value closer to that of sample D. The TVS measurement of sample C is slightly higher but in the error range of the BTS measurement. The used QS measurement setup allowed to measure the slope of the output voltage transient and therefore the current at the point when the capacitance is measured. If the current after the 30 s measurement time is low it indicates that almost all mobile charges have been transferred. This was the case at 600 K. In the QS-CV curve at 500 K the capacitance bump appeared much smaller, which would falsely indicate a low amount of mobile charges, but the current was also high. Therefore 500 K was not enough to allow all mobile ions to drift through the oxide during the measurement time. All measured QS-CV curves at various temperatures are shown in the next chapter. With this information it can be assumed, that the TVS measurement at 600 K is rather accurate and the BTS measurement slightly underestimates the mobile charge density. Carrying out the BTS measurements at a slightly higher temperature should account for slower ions as well. Although the measured values seem rather high the mobile ion density of 4H and 6H-SiC MOSs and MOSFETs are reported to be in the $0.5 - 4 \cdot 10^{12}$ cm^{-2} range [71, 72, 73].

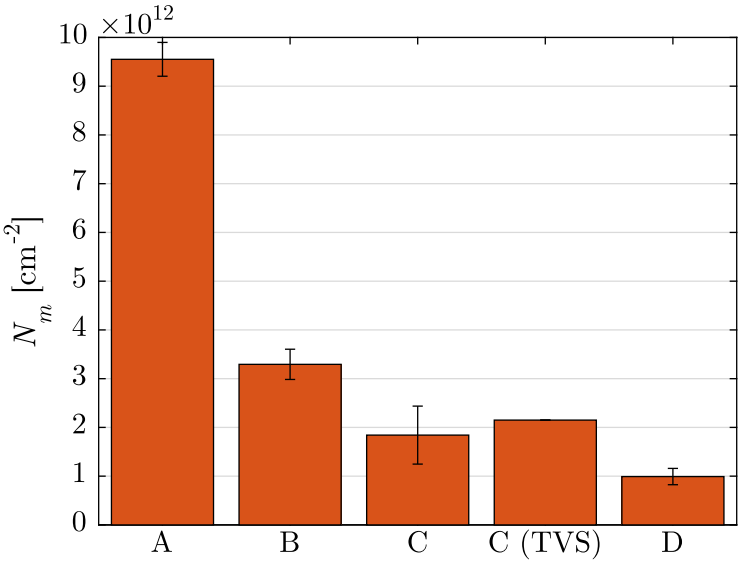

Figure 33: Mobile charge measurement results of all investigated samples.

5.2 Results of the interface trap density

For the interface trap characterization mainly Sample C was used because it showed the lowest amount of mobile charges. Four different techniques have been used to extract D_{it} out of the measured CV and Gω data. All measurements have been conducted at the temperatures: 150 K, 300 K, 400 K, 500 K and 600 K. The HF-CV curves were measured using a 30 mV Osc level and a sweep rate of 200 mV/s and the LF(QS)-CV curves were measured with $\Delta V = 50$ mV and a measurement time $t_m = 30$ s.

5.2.1 Terman method

The Terman method was used first because it is the simplest and fastest method. For the D_{it} evaluation HF-CV curves with negative to positive sweep direction and 1 MHz measurement frequency were used. At 150 K and 300 K hardly any hysteresis between the different sweep directions was observed. Figure 34 shows the measured HF-CV curves of the samples A and C, respectively. What stands out is the unnaturally steep rise of the CV curves at 400 K and above. It is assumed that this is due to the high amount of mobile charges. At this elevated temperatures they become mobile enough to influence the flatband voltage during the voltage sweep. Unfortunately, the Terman method is based on the strechout of the CV slope and therefore becomes unusable at these temperatures. The increase is steeper than the theoretical curve which would suggest negative interface traps. Nevertheless, D_{it} could be extracted at 150 K and 300 K. The results for sample A and C are depicted in figure 35. Close to the conduction band edge the 150 K curve should be

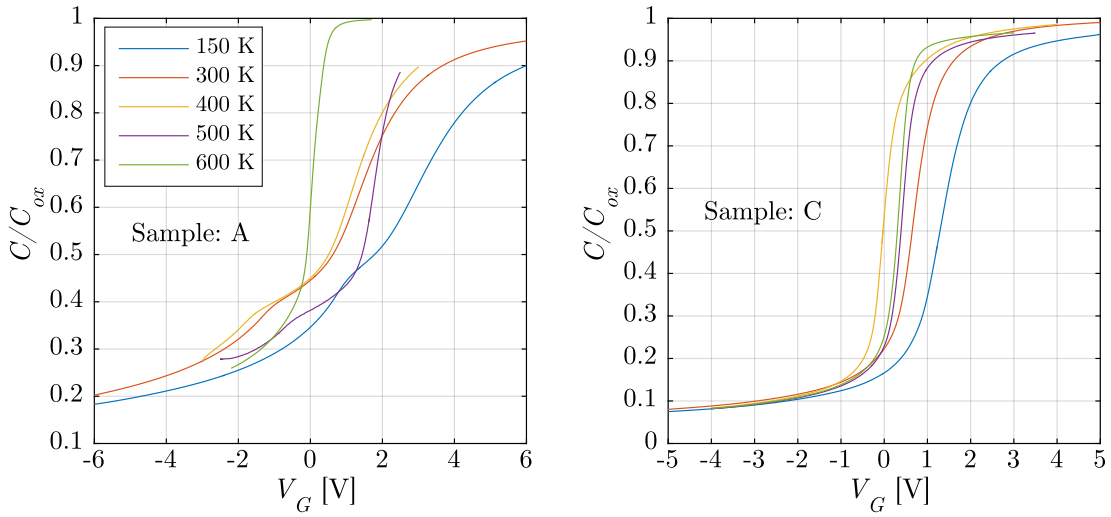

Figure 34: Measured HF CV curves (1 MHz) of sample C and sample A for various temperatures. Sweep direction from negative to positive voltages.

more accurate because the trap response time become slower at these low temperatures. On the other hand it starts to underestimate D_{it} further inside because slower traps are not taken into account. Therefore only a certain energy range can be considered as valid for each temperature (see section 2.4.3). The trap time constants evaluated with the conduction method (shown below) and the used measurement frequency and sweep rate suggests a validity range of roughly 0.02 to 0.15 eV at 150 K and 0.18 to 0.5 eV at 300 K. Not surprisingly, sample A showed much higher D_{it} values especially in the 0.5 eV region. There was a well pronounced hump in the HF-CV curve that accounts for this increase in D_{it}. The properly cleaned sample C did not show any hump in the HF CV curves. Humps like this have been observed in many studies with different semiconductors and insulators [74, 75, 76, 77]. Cohen *et al.* [78] suggest near interface oxide traps (NIOT) as source of the hump. At low enough frequencies electrons can tunnel from the semiconductor conduction band to the NIOTs, which are located inside the oxide, but very close to the interface. Sample A must have such a high amount of NIOTs that even at 1 MHz enough electrons are able to fill enough states to influence the CV curve.

5.2.2 Low frequency method

The next observed method was the low frequency capacitance method. Due to the longer measurement and evaluation times only the most promising sample C was measured. The QS-CV curves are depicted in figure 36. In contrast to the HF curves the previously discussed hump was now measured at sample C as well, supporting the theory of slow NIOTs as source of the hump. At the slow quasi static measurement speed traps inside the oxide have sufficient time to be filled by tunneling. Also the high steepness of the CV

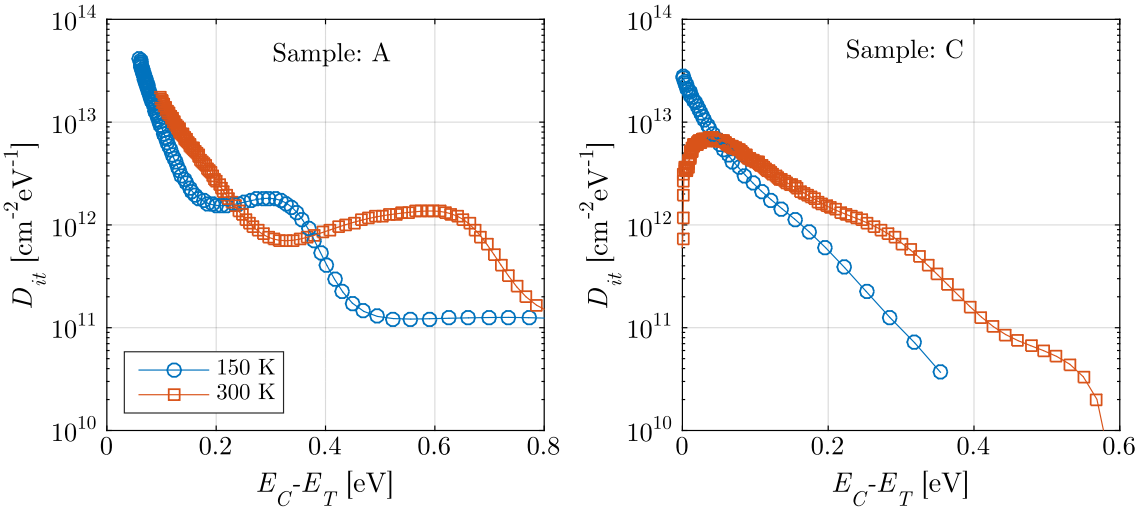

Figure 35: Extracted D_{it} values at 150 K and 300 K of Sample C and A using the Terman method.

curve at higher temperatures due to the mobile charges is visible again. Additionally, an extreme overshoot in capacitance in the 500 K and 600 K curves is observed. This bump is a result of the mobile ions drifting through the oxide and being measured as charge by the integrator of the QS measurement circuit. This property is used in the TVS method to extract the mobile charge density. It clearly reveals that at 500 K not all ions are transferred within the used measurement time. This would lead to an underestimation of N_m. Unfortunately, this mobile charge overshoot in the CV curve makes D_{it} extraction very faulty at elevated temperatures. Nevertheless, D_{it} was extracted using the Berglund integral and the flatband voltage was estimated via the flatband capacitance. The results are displayed in figure 37. Like before only a certain region of the D_{it} curve is valid at a certain temperature level.

5.2.3 High-Low method

The interface trap density was also extracted using the high-low (HiLo) frequency method. Here the HF and the QS-CV curves shown above are compared to obtain D_{it}. Figure 38 shows the QS and HF curves on the left and the resulting D_{it} values on the right. Again, only the 150 K and 300 K curves were used due to the distortions in the high temperature curves. The ψ_s - V_G relationship needed for the calculation of D_{it} was obtained using the Berglund integral and the $\psi_{s0}(0)$ value was obtained using the fit as in the $(C - \psi_s)$ method. Because the HF and the QS curves have been measured separately with different sweep rates they may be slightly shifted in voltage due to different mobile ion positions. The higher the temperature, the easier an offset arises between successive measurements. This will introduce a small error. This problem could be overcome by using an instru-

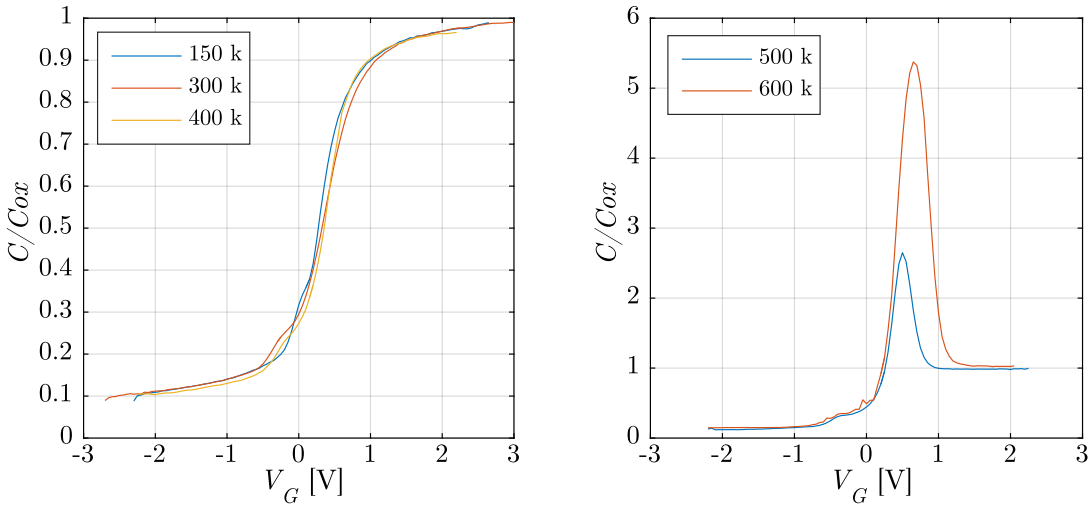

Figure 36: Measured QS-CV curves of sample C for various temperatures. Sweep direction from negative to positive voltages.

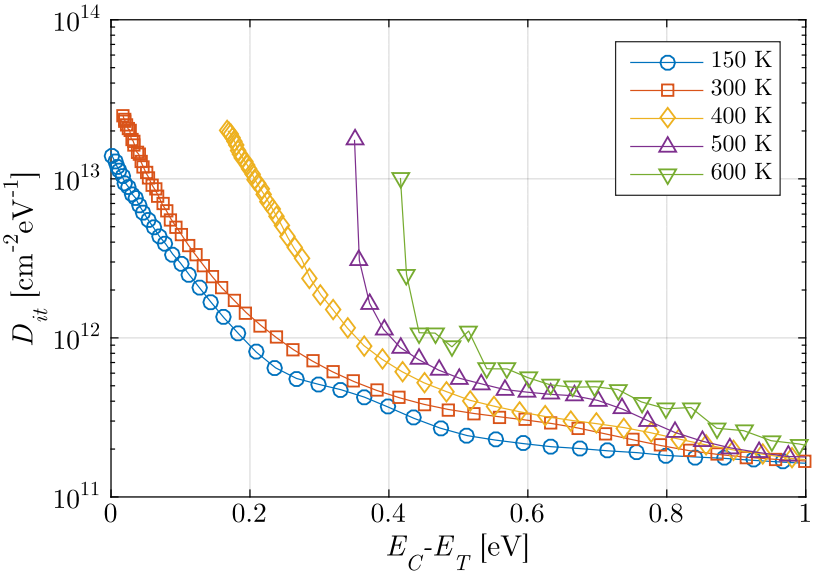

Figure 37: Extracted D_{it} values using the low frequency method for various temperatures of sample C.

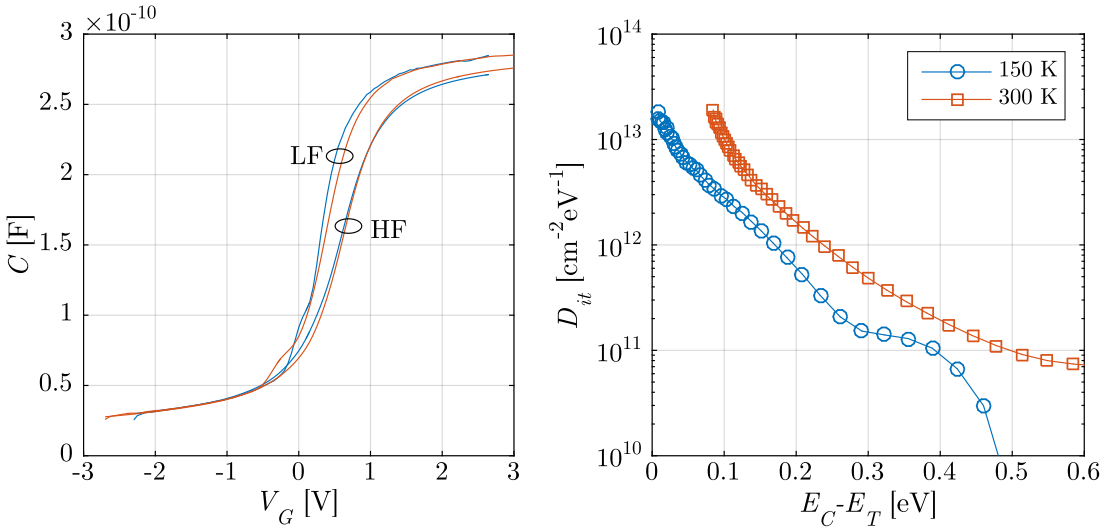

Figure 38: QS and HF-CV curves of sample C (left) and the extracted D_{it} profile using the high-low frequency method (right).

ment capable of performing simultaneous QS and HF-CV measurements like the Keithley Model 82.

5.2.4 Conductance method

For the conductance method the capacitance and conductance of sample C were measured in the frequency range of 1 kHz to 5 MHz. The accuracy of the measurement equipment did not allow lower frequencies and higher frequencies were limited due to the inductance of the setup. The measurements were done at several gate voltages in steps between 50 mV and 100 mV at temperatures from 150 K to 600 K. The series resistance and oxide capacitance for correction were measured in strong accumulation ($V_G \geq 4\ V$). Some of the measured and corrected conductance curves are depicted in figure 39. At 150 K a very interestingly shaped conductance curve was measured at some bias conditions. It is assumed that it consists of the main interface trap peak which is cut off on the left and an additional peak of very fast traps. A fit using two superimposed peaks was used giving the black line. With increasing gate voltage the main peak shifted further to the right while the fast peak did not move with gate voltage. Therefore the main peak 'absorbed' the fast peak with increasing gate voltage. At higher temperatures no such second peak could be observed, which is not surprising giving the fact that time constants get longer with temperature. The evaluation for all temperatures can be seen in figures 40 and 41. It stands out, that the D_{it} values obtained at various temperatures agree very well over a wide energy range. Only between 0.1 and 0.2 eV a few values are missing. A measurement at about 225 K would have closed this gap. The fast peak was evaluated separately and is depicted in the figures as well. The D_{it} values of the fast peak show a much lower trap con-

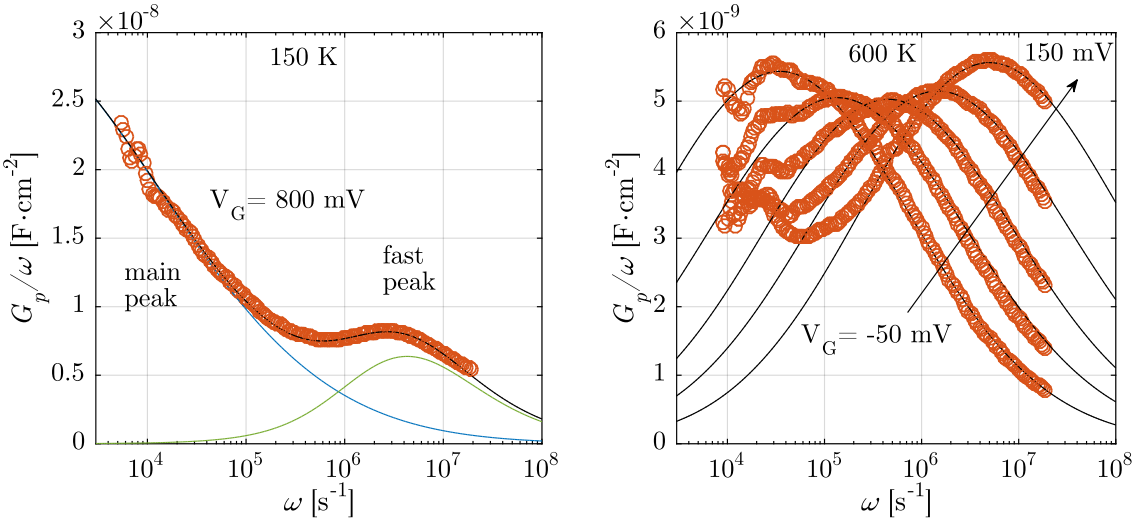

Figure 39: Measured and corrected G_p/ω curves. (left) Curve at one gate voltage at 150 K showing the fast peak and the beginning of the main peak. (right) All curves measured at 600 K. All at sample C. The black line is the best fit to the measured data-points.

centration and could be detected between 0.1 and 0.5 eV. Due to the used frequency range the trap time constants are all in the 10^{-6} to 10^{-4} s range and they are shifted towards midgap with increasing temperature. However, the fast traps showed a rather constant time constant of about $6 \cdot 10^{-6}$ s over the observed energy range. The capture cross-section σ_n was calculated using equation 25. For the main peak the cross-section started at about 10^{-20} cm^{-2} at the conduction band edge and increased to around 10^{-16} cm^{-2} where it remained from 0.4 eV towards the measurement limit of 0.85 eV. Due to the constant trap time constant of the fast peak the capture cross-section showed a strong dependency on the energy position. The surface fluctuation σ_s could also be extracted and is in the range of 4 k_BT/q at 300 K and decreased with increasing temperature to around 2.5 k_BT/q. Similar values have been measured for Si [32, 79] and SiC [80, 81] MOS capacitors. At 150 K much narrower peaks were observed with $\sigma_s \approx$ 2 k_BT/q for the main peak and 1.5 to 0.5 for the fast peak. The narrowness of the fast peak might be due to the fact that it only has a single or a very narrow time constant distribution. The main peak at 150 K might be smaller compared to the higher temperature ones because it does not include the fast traps. The fast traps might not be measurable at elevated temperatures but they may still contribute by broadening the G_p/ω peak. The energy position was determined using the ψ_s - V_G relationship obtained from the Terman method.

QS Hump and second conductance peak:

To further investigate the second peak observed at 150 K additional CV and GV curves at several frequencies were measured and are depicted in figure 42. In this figure the second

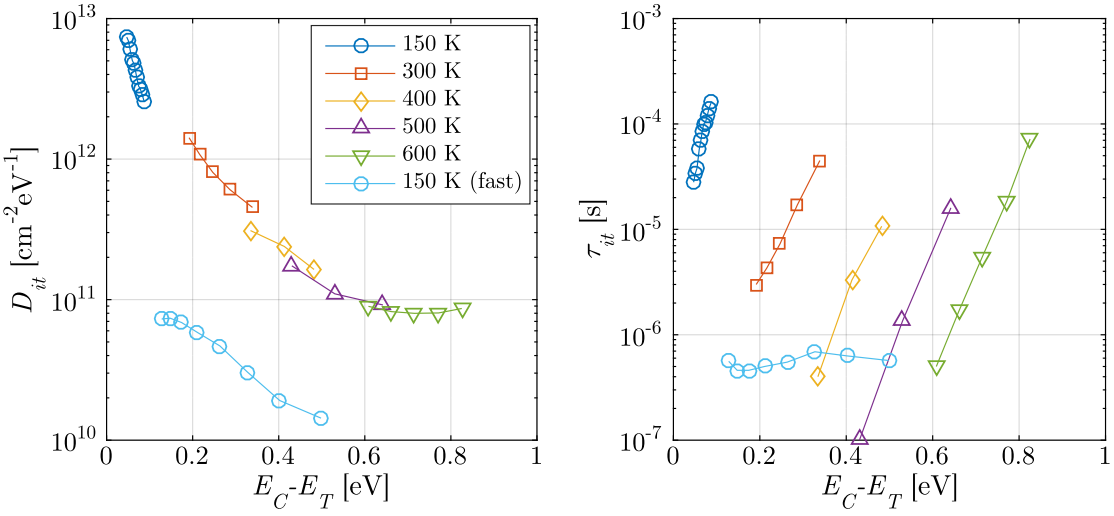

Figure 40: Extracted D_{it} values (left) and τ_{it} (right) for several temperatures of sample C using the conductance method.

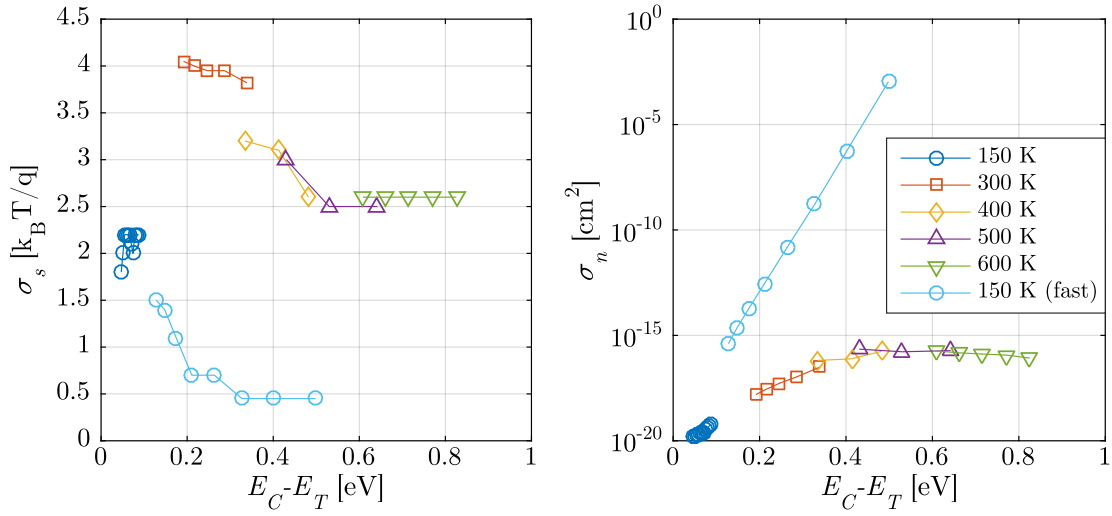

Figure 41: Extracted surface potential fluctuation σ_s and capture cross-section σ_n of sample C using the conductance method.

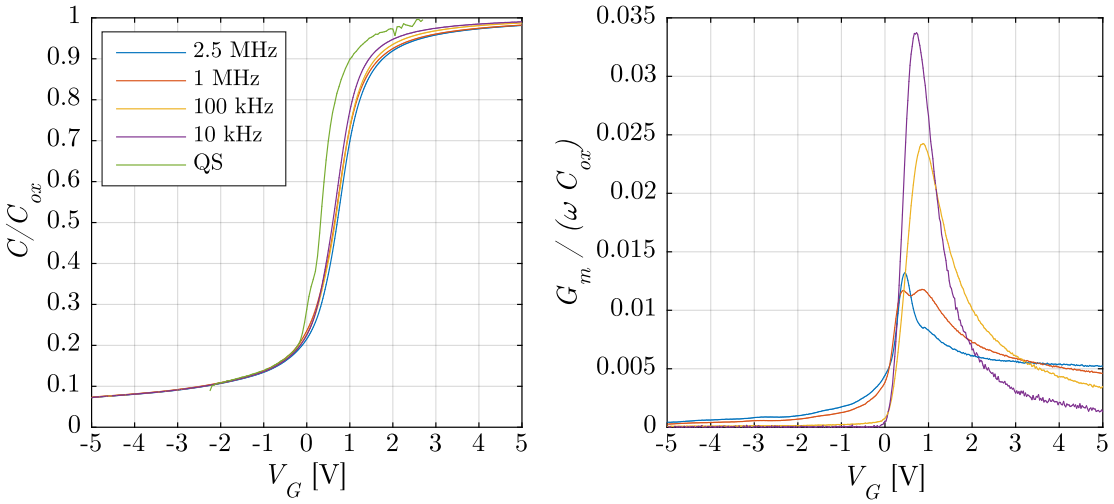

Figure 42: Normalized capacitance and conductance over gate voltage for different measurement frequencies of sample C at 150 K.

fast peak corresponds to the left one at around 400 mV which is very pronounced at 1 MHz and 2.5 MHz, but vanishes at 100 kHz and at 10 kHz, which makes sense due to its fast nature. A very similar double peak behavior has been measured and analyzed by Krieger *et al.* [82] in N implanted 3C-SiC MOS capacitors. In the case of 3C-SiC several publications describe this double peak behavior [83, 77]. In contrast to the results in figure 42 they observed an increase of the second pulse with lower measurement frequencies. Constant *et al.* suggested a correlation between the second conductance peak and the hump in QS-CV curves. But this would not make sense in our case, where the second peak is of very fast nature. Yoshioka et at. [84, 85] and others [86, 87] also observed a conductance peak at very high frequencies in 4H-SiC MOS capacitors. No real explanation for the origin of these traps could be found except nitrogen accumulated at or near the interface. Due to the independence of the fast traps on the gate voltage and hence, the surface potential they might as well be located in the bulk of the semiconductor. The fact that the response times of the slow NIOTs observed via the QS hump and the fast time constant of the second conductance peak differs by so many orders of magnitude leads to the conclusion that they are not due to the same type of trap. One suggestion is that a total of three trap types are present in the 4H-SiC MOS structure. The 'normal' interface traps, the slow NIOTs which are located in the first few Å inside the oxide and the very fast traps whose origin remains unclear.

Carbon clusters with incorporated nitrogen were suggested as the source of the NIOTs, this might as well be the case in this work because nitrogen donors could have been diffused in the oxide during growth. However, Halldor *et al.* [88] did not find any signs of carbon clusters and concluded that intrinsic defects formed in a transition layer between the SiC

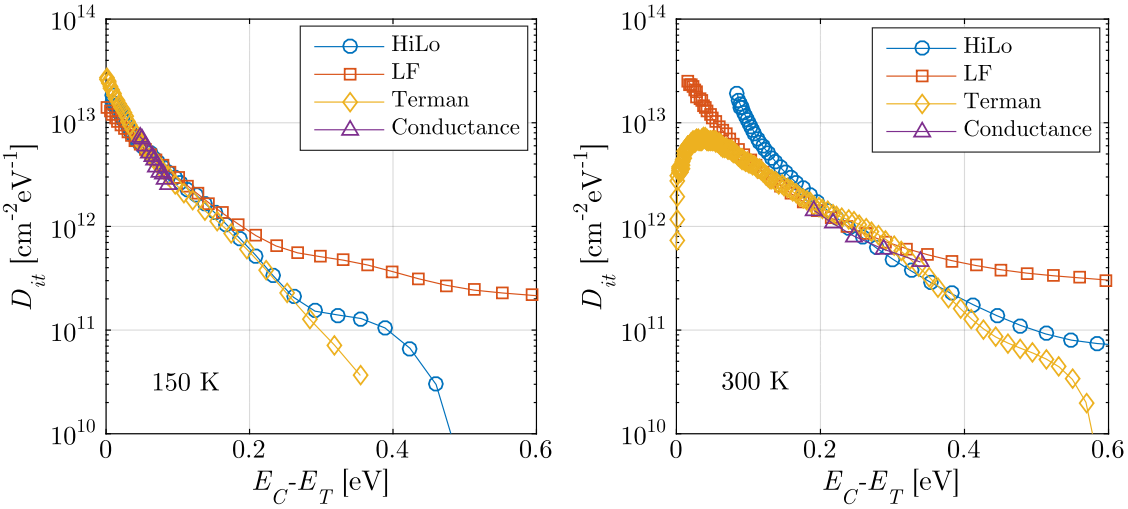

Figure 43: Overlay of the D_{it} profiles obtained with four different methods of sample C.

and SiO_2 to be the source of NIOTs in 4H-SiC. Out-diffusion of incorporated nitrogen during post oxidation annealing, leaving behind vacancies in the oxide seems to be the most promising explanation of NIOTs.

5.2.5 Comparison of methods

Finally, all four investigated interface trap characterization methods are compared. The resulting D_{it} profiles of sample C at 150 K and 300 K are depicted in figure 43. As mentioned earlier only a certain part of the energy band can be investigated at each temperature due to the strong temperature dependency of the trap time constant and the limitation to detect only traps with a certain time constant. Surprisingly, all four methods agree very well in a certain range of energy. At 150 K between 0.0 and 0.15 eV and at 300 K between 0.18 and 0.35 eV a very small deviation is observed. The fast traps observed at 150 K with the conductance method are not shown. Overall the measured D_{it} density is rather low considering that only Ar post annealing was used. Not much lower trap concentrations have been measured for 4H-SiC MOS capacitors produced with CVD grown oxides or by NO, N_2O oxidation and with NO, N_2O or N-plasma post oxidation annealing [73, 80, 74, 89], but a further reduction is still possible and required for high channel mobility values in MOSFET applications.

5.3 Breakdown measurement results

The last measurement series carried out was the determination of the breakdown voltage, because this is a destructive measurement. In this work the voltage ramp method was used on all four samples. This breakdown measurements should only give a rough value of

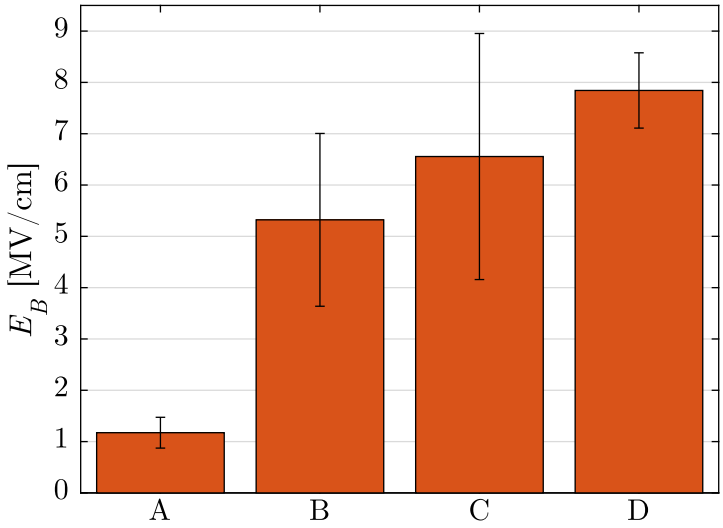

Figure 44: Measured dielectric strength using the voltage ramp method at room temperature.

the breakdown voltage to compare the different samples. Only a small number of about 5 different pads per sample have been measured to get an average value of the breakdown field strength. A current density of $J_l = 250$ µA/cm^2 was used as breakdown limit. The resulting averages and standard deviations are depicted in figure 44. For a Weibull statistic much more measurement points are needed. Again sample A showed the worst results, it could hardly resist field strengths above 1 MV/cm. Samples B and C showed much higher dielectric strengths, but the deviation between different pads was large, indicating many defect-related breakdowns. The silicon sample D showed the highest strength in the range of 8 MV/cm and a much lower deviation which suggests a dominating intrinsic breakdown mechanism. It is difficult to provide a general dielectric strength value for SiO_2 because the strength has been reported to increase with thinner oxides [90, 91]. But usually values between 7 and 11 MV/cm are found. Oxidized 4H and 6H-SiC with comparable thickness are measured to be around 10 MV/cm [92, 93]. The slightly lower values in this work may be explainable due to the higher amount of mobile charges and due to missing effort of post oxidation annealing which would have lowered the interface trap density.

6 Conclusions and Outlook

A detailed theoretical study of the 4H-SiC MOS structure with numerical and analytical approaches was done to obtain ideal CV curves. Also the temperature dependency of several SiC parameters such as Fermi level and intrinsic carrier concentration have been studied and was used to calculate CV curves in a wide range of temperatures which in turn were needed for the evaluation procedure. In the investigated temperature range from 150 to 600 K the shape of the CV curve changes only marginal, but the change in Fermi-level position and in bandgap are important for determining the correct energy position of interface traps.

Furthermore several important interface trap and mobile charge characterization methods were discussed theoretically.

In order to carry out QS-CV measurements, a QS-CV circuit after the improved feedback charge method was designed and realized. The setup showed very satisfying results like capacitance accuracy of about 1 pF and a very low offset current of only -28 fA.

A strong influence of the pre-oxidation cleaning procedure on the oxidation quality and oxidation rate was observed. A cleaning sequence consisting of an ultrasonic bath in acetone followed by RCA with an HF dip in between the SC1 and SC2 solutions showed the best oxide quality.

Mobile charge measurements using the BTS and TVS method showed rather high mobile ion concentrations in the $2 \cdot 10^{-12}$ cm^{-2} range. Besides an intrinsic source the oxidation furnace is suspected as main source of contamination.

For the interface trap characterization the Terman-, the low frequency-, the high-low frequency- and the conductance-method were used and compared. Due to the mobile charge densities all methods based on CV curves could only be used at 150 and 300 K. In contrast, the conductance method did work accurately up to 600 K. A very good agreement between the different methods was observed in certain energy ranges. Overall rather low D_{it} values around $2 \cdot 10^{13}$ cm^{-2}eV^{-1} close to the conduction band and 10^{11} cm^{-2}eV^{-1} towards mid-band were measured. It was shown that a wide energy range can be observed by performing the classic D_{it} characterization methods in a wide temperature range, but a low amount of mobile ions is required for all methods based on CV curves to work at higher temperatures. The QS-CV curves showed a small hump near 0 V which was attributed to NIOTs. At 150 K a second very fast peak in the conductance spectra was observed. This fast peak was measured in an energy range of 0.1 to 0.5 eV with a D_{it} in the upper 10^{10} cm^{-2}eV^{-1} range and a rather constant τ_{it} of about 0.6 µs. No satisfying explanation about the origin of this fast trap could be found.

Further investigations at lower temperatures and with other methods like Thermal

Admittance Spectroscopy (TAS) will be the scope for future works. Also the influence of different post oxidation annealing steps would be an interesting work for the future.

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