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DIPLOMARBEIT

Contactless chip cards simulation and measurements

Ausgeführt zum Zwecke der Erlangung des akademischen Grades eines Diplom-Ingenieurs
unter der Leitung von

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I hereby declare that this thesis is my original work and it has been written by me in its entirety.
I have acknowledged all the sources of information which have been used in the thesis.

Sandra Montoro Almendral
Vienna, June 2014

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Abstract

In this thesis I investigate the behavior of Proximity integrated circuit card (PICC) operating in the High Frequency (HF) band at 13.56MHz using Advanced Design System (ADS) simulator and also real measurements. Those PICC are passive tags powered by the reader antenna via inductive coupling and consist of a coil antenna and certain linear and non-linear components such as resistors, diodes or capacitors. One of the goals of this work was to understand how some of the elements affect the operation of the PICC in both simulation and measurement.

This work was organized in four chapters. In the first chapter I give a brief overview of the operation of the PICC according to the ISO/IEC 14443 standard and introduce the reference PICC circuit.

In the second chapter, reference PICC is analyzed both in ADS simulation and in measurement. For the measurements, a reference PICC is built on 2.2.1.

In the third chapter reference PICC is tested in a reader emulator called Test PCD assembly.

In the fourth and final chapter I give conclusions and outlook for a future work.

Contents

Chapter 1

Introduction

Radio frequency identification (RFID) has been used in several practical applications, such as improving supply chain management, tracking household pets, accessing office buildings, and speeding up toll collection on roadways.
Compared to its predecessor, the proximity card, a contactless card provides much greater security and contains 100 times the data storage of a traditional proximity card.
Contactless chip cards are used in variety of applications, e.g. for identification, in biometric passports, credit and bank cards etc. and they are developed to be read without a reader device using RFID.

In this first chapter the standards used and the reference PICC circuit are introduced. Furthermore, the operation principle of contactless cards is explained as well as the communication interface between card and reader.

The main part of the chapter includes the description of the reference PICC circuit defined in ISO 10373-6 which has been used as the base model for simulations and measurements.

1.1 Operating principle of contactless chip cards and requierements of ISO 14443

The components of an RFID field are a transponder or tag and a reader. The interaction between a transponder chip and a transponder antenna depends on several parameters such as the design of both coils or the operation frequency and it has been investigated in [1].
In this work we will focus on the non linear effects produce on the transponder chip produced when some parameters of its components are modified.

The operating principle of contactless chip cards 1.1 is based on magnetic coupling. It means that the transponder and the reader antenna are coupled by the magnetic flux through both coils. An AC voltage is induced in the card loop antenna and the PICC converts this AC voltage into DC in order to power the Integrated circuit (IC).

A tag typically consists of an electronic microchip and chip antenna designed to allow communications with a reader [2].
RFID tags fall into two categories, active tags, which may be totally or partially powered via its own battery supply, and passive tags, which obtain power from the signal of an external reader.
Because of their lower price and smaller size, passive tags are more commonly used than active tags for retail purposes. A passive tag consists of a microchip surrounded by a printed antenna and some form of encapsulation [3].
As we are working with passive tags, all the energy used in the tag is drawn from the primary

coil of the antenna therefore the power supply for the card is one of the main concerns in this work.

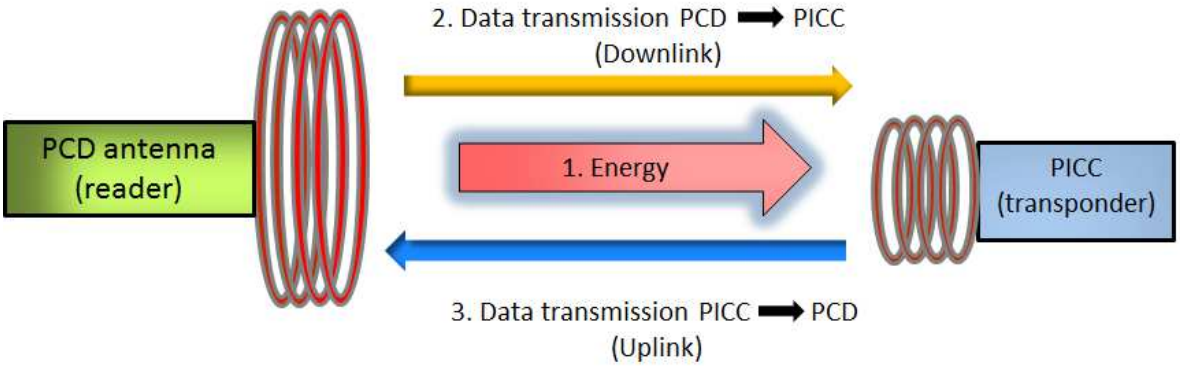

Figure 1.1: Operating principle contactless chip cards

ISO 14443 is an international standard for proximity or contactless smart card communication which describes how contactless cards and terminals should work to ensure industry-wide compatibility. For example it plays a key role in identity, security, payment, mass-transit and access control applications.
ISO 14443 is a four-part international standard for Contactless Smart Cards operating at 13.56MHz in close proximity with a reader antenna. PICC are intended to operate within approximately 10cm of the reader antenna [4].

- **Part 1:** defines size and physical characteristics of the card.

  The PICC antenna shall not exceed 86mm x 54mm x 3mm.
  The PICC should operate as intended after continuous exposure to a magnetic field of an average level of 10 A/m rms at 13,56 MHz. The averaging time is 30 seconds and the maximum level of the magnetic field is limited to 12 A/m rms.

- **Part 2:** defines the Radio Frequency (RF) power and signal interface. Type A and Type B cards are also defined in this part.

  The PICC shall operate as intended continuously between $H_{min} = 1.5A/m$ and $H_{max} = 7.5A/m$.
  Two communication signal interfaces, Type A and Type B are described in the standard.
  The Proximity coupling device (PCD) shall alternate between modulation methods when idling before detecting the presence of a PICC of Type A or Type B.
  The PICC shall be capable of communication to the PCD via an inductive coupling area where the carrier frequency is loaded to generate a subcarrier with frequency f_s. The subcarrier shall be generated by switching a load in the PICC.
  The frequency f_s of the subcarrier shall be $f_c/16$ (848 kHz). Consequently, during initialization and anticollision, one bit duration is equivalent to 8 periods of the subcarrier. After initialization and anticollision, the number of subcarrier periods is determined by the bit rate.
  The PICC shall generate a subcarrier only when data is to be transmited.

- **Part3:** defines the initialization and anticollision protocols for Type A and Type B.

  In order to detect PICCs which are in the operating field, a PCD shall send repeated Request commands. When a PICC is exposed to an unmodulated operating field (see ISO/IEC 14443-2) it shall be able to accept a request within 5 ms.

- **Part4:** defines the high-level data transmission protocols for Type A and Type B. The protocols described in this part are optional elements of the standard.

Two communication signal interfaces Type A and Type B have been mentioned before. In table 1.1 the differences between them are summarized.

Table 1.1: Type A and B communication interfaces

	Type A	Type B
Downlink Modulation (PCD to PICC)	100% ASK modified Miller code	10% ASK NRZ code
Signal/noise ratio	Very high (30% noise tol.)	Low (3% noise tolerance)
Uplink Modulation (PICC to PCD)	Load modulation, ASK Manchester code	Load modulation, BPSK NRZ code
Anti Collision	Binary Search method	Time slot method
Speed	no difference between Type A and Type B	
Security	no difference between Type A and Type B	
Power (energy eff.)	no difference between Type A and Type B	

As an example, the communication diagram between the reader and a Type B card is shown in 1.2 To initiate the communication the reader sends a Request command (REQ) command to the PICC.

For Type B signal interface, the PCD is continuously transmitting the unmodulated 13.56MHz RF carrier frequency when not transmitting data to the PICC.

The PCD modulates the amplitude of the alternating magnetic field strength with modulation pulses in order to transmit data from the PCD to the PICC.

The PICC loads the alternating magnetic field with a modulated subcarrier signal (load modulation) in order to transmit data from the PICC to the PCD.

When PCD deactivates the RF field, PICC should be deactivated after no longer than 5ms.

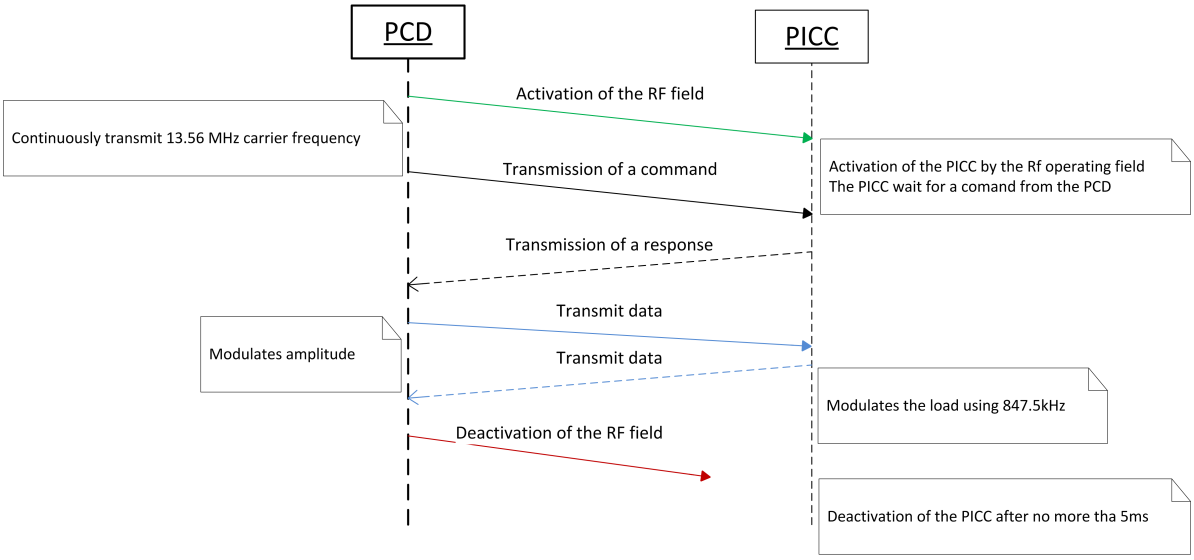

Figure 1.2: Communication interface diagram

1.2 Reference PICC circuit

Together with standard ISO 14443, Part 6 of the standard ISO 10373 [5] has been also considered. It defines test methods for identification cards and specifies the reference PICC components and construction.

In figure 1.3 the referece PICC circuit is shown and its parts are labeled and described below.

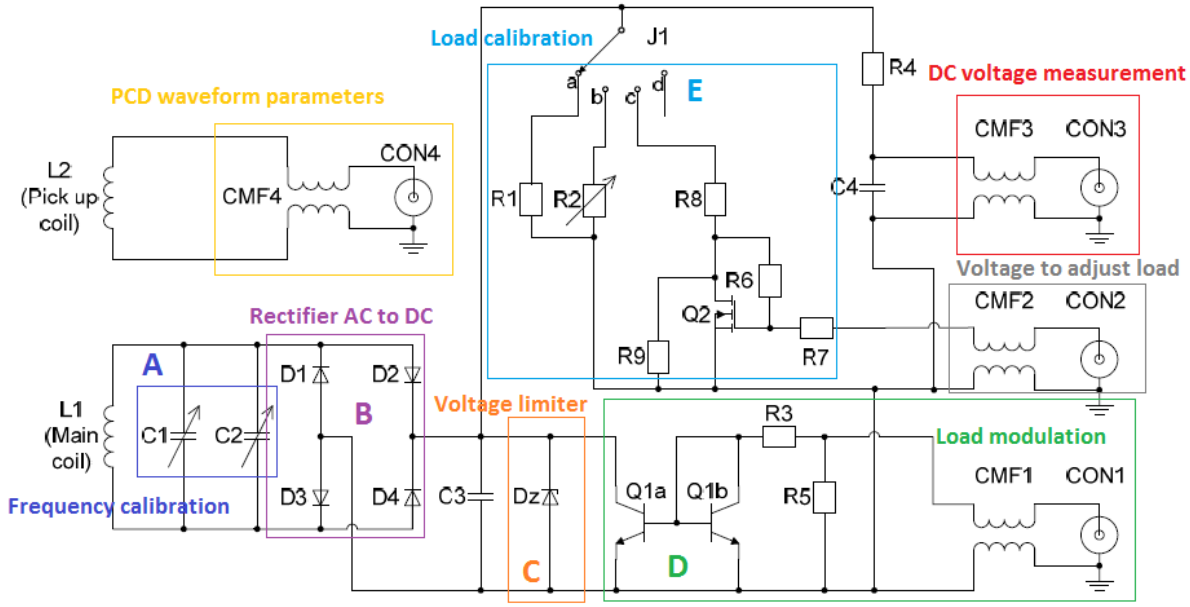

Figure 1.3: Reference PICC diagram

- **Block A** consists of two capacitors used for frequency tuning.
- **Block B** is made up of four Schottky diodes that constitute the rectifier where AC

voltage is sweep to DC in order to power the card.

- **Block C** consists of a Zener diode used for power regulation.
- **Block D** is a current mirror used for load modulation.
- **Block E** is for load calibration. Changing jumper J1 into a, b, c and d position the load value is modified.
- At **CON1** load modulation signal is applied.
- With the voltage at **CON2** the load can be adjusted until the required DC voltage is shown at CON3.
- In **CON3** we measured the PICC DC voltage with a high impedance voltmeter.
- **CON4** is used for picking up the PCD waveform parameters using a high impedance oscilloscope probe.

In this work the effects of load modulation are not analyzed therefore the circuit used for simulation and measurements is a simplified version of this one and will be shown in further sections.

In 1.2 the component values are shown.

Table 1.2: Reference PICC components list

Component	Value	Component	Value
L1	See Annex D	C1	7pF - 50pF (b)
L2	See Annex D	C2	3pF - 10pF (b)
R1	$1.8k\Omega$	C3	27pF
R2	$0k\Omega$ - $2k\Omega$ (a)	C4	1nF
R3	220Ω	D1, D2, D3, D4	BAR43S or equivalent (c)
R4	$51k\Omega$	Dz	BZX84, 15V or equivalent (c)
R5	51Ω	Q1a, Q1b	BCV61A or equivalent
R6	$500k\Omega$	Q2	BSS83 or equivalent
R7	110Ω	D1, D2, D3, D4	ACM3225-102-2P or equivalent
R8	51Ω	CON1, CON2, CON3, CON4	RF connector
R9	$1.5k\Omega$		
a: A multi-turn potentiometer (turns>10) should be used			
b: Q-factor shall be higher than 100 at 13.56 MHz			
c: Care should be taken on parameters Cj, Cp, Ls and Rs of equivalent diodes.			

Chapter 2

Simulation and measurements

In this section the circuit used for simulations will be introduced. It is simplified from the Reference PICC since it excludes the load modulation part. In addition, ADS simulations results are presented in time and frequency domain. In order to analyze how the components affect the circuit behavior, components with different values of basic parameters are used in the simulations. The behavior of the circuit is investigated for the wide range of input power. Although the simulations are performed using ADS, all the results are exported to the Matlab domain in order to make the comparison with measurements easier.
The method followed to build the circuit in a PCB is also reported. Afterward, the setup used is described and measurements results are showed.
To conclude chapter two a comparison between simulation and measurement results is done and differences are commented.

2.1 Chip card simulation

In this section one of the main goals of this work is covered: analyzing how some of the components affect the circuit response, especially the DC power measured in the load.
In figure 2.1 the simulated circuit is shown.

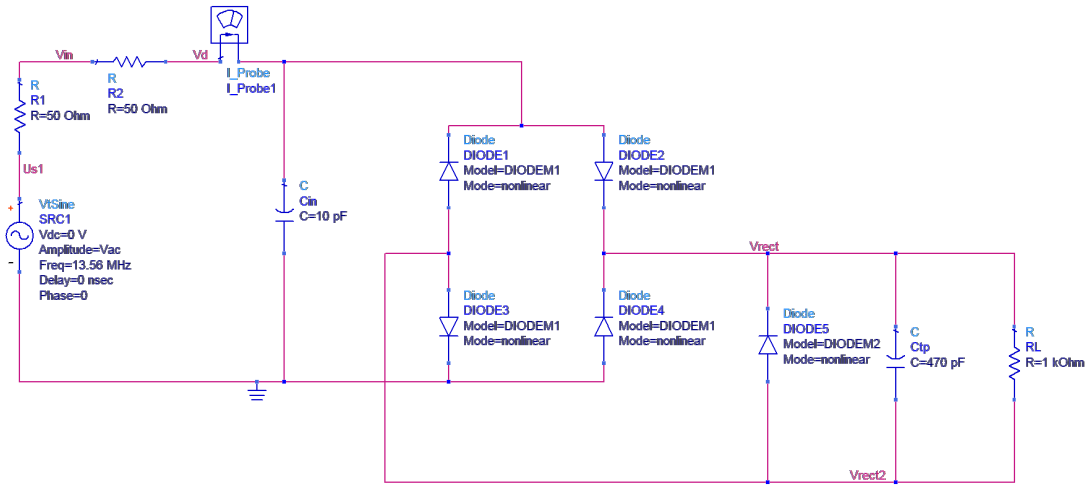

Figure 2.1: Simulated circuit

The variable components are C_{in}, C_{tp} and R_{L} and their ranges according to the list on standard 10373-6 are:

$$R_L = 50\Omega, 500\Omega, 1k\Omega, 1.5k\Omega, 2k\Omega \tag{2.1}$$

$$C_{in} = 10pF, 27pF, 47pF \tag{2.2}$$

$$C_{tp} = 470pF, 1nF \tag{2.3}$$

The values were chosen considering real values of components since later on this circuit was built and measurements were compared with simulation results. Special care have been taken when choosing the diode models since ADS allows you to set a wide range of parameters that cannot be easily found in a normal datasheet.

In the following graphs 2.2, 2.3, 2.4 the input power is swept from -2dBm to 20dBm. Three different values of C_{in}, C_{p} and R_{L} are chosen. The input voltage and input current of the chip card are plotted in frequency and time domain. The rectified voltage and the Lissajous curves are also plotted.

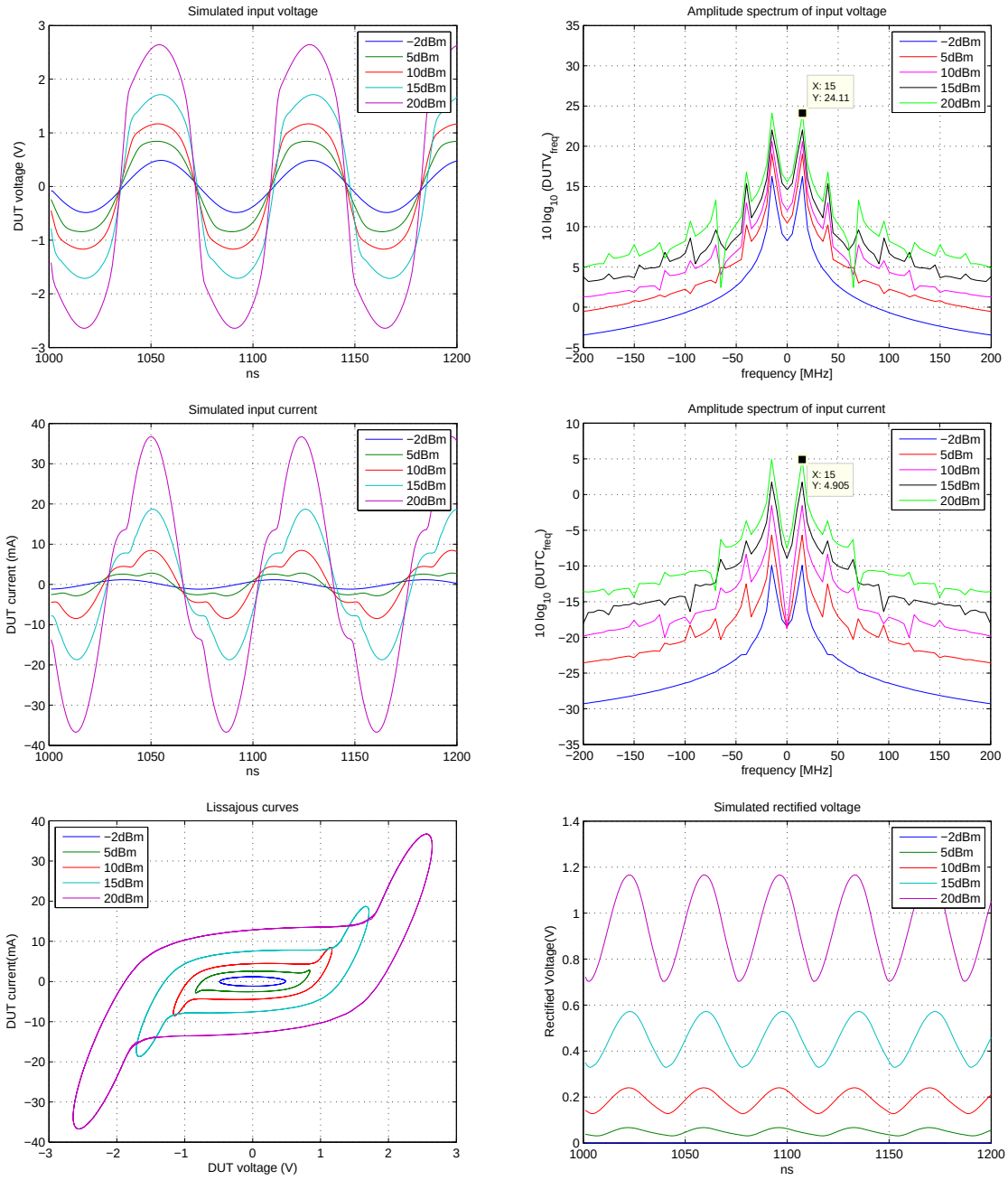

Figure 2.2: $R_{\mathrm{L}} = 50\Omega$, $C_{\mathrm{in}} = 27\mathrm{pF}$, $C_{\mathrm{p}} = 470\mathrm{pF}$

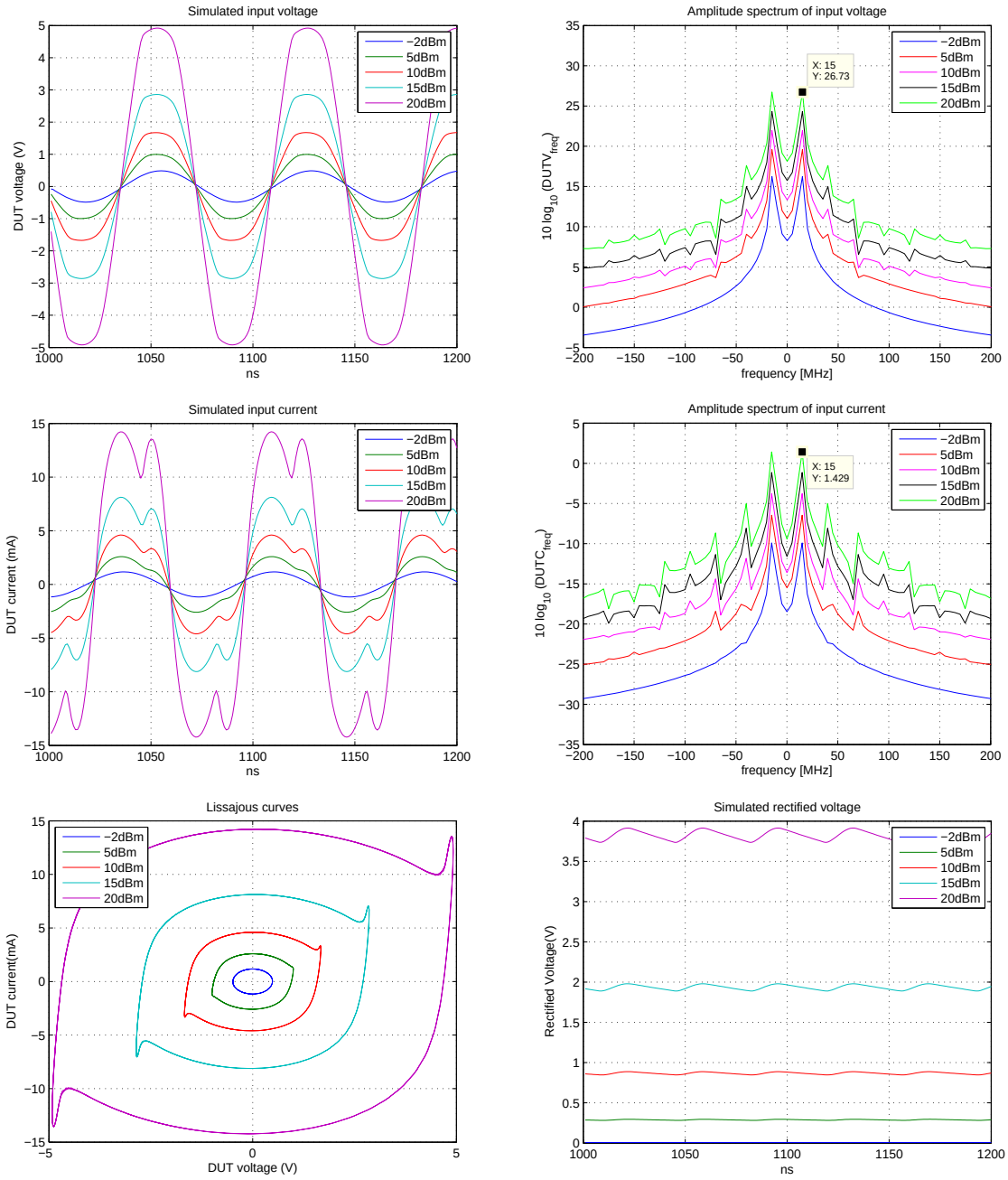

Figure 2.3: $R_{\mathrm{L}} = 1k\Omega$, $C_{\mathrm{in}} = 27\mathrm{pF}$, $C_{\mathrm{p}} = 470\mathrm{pF}$

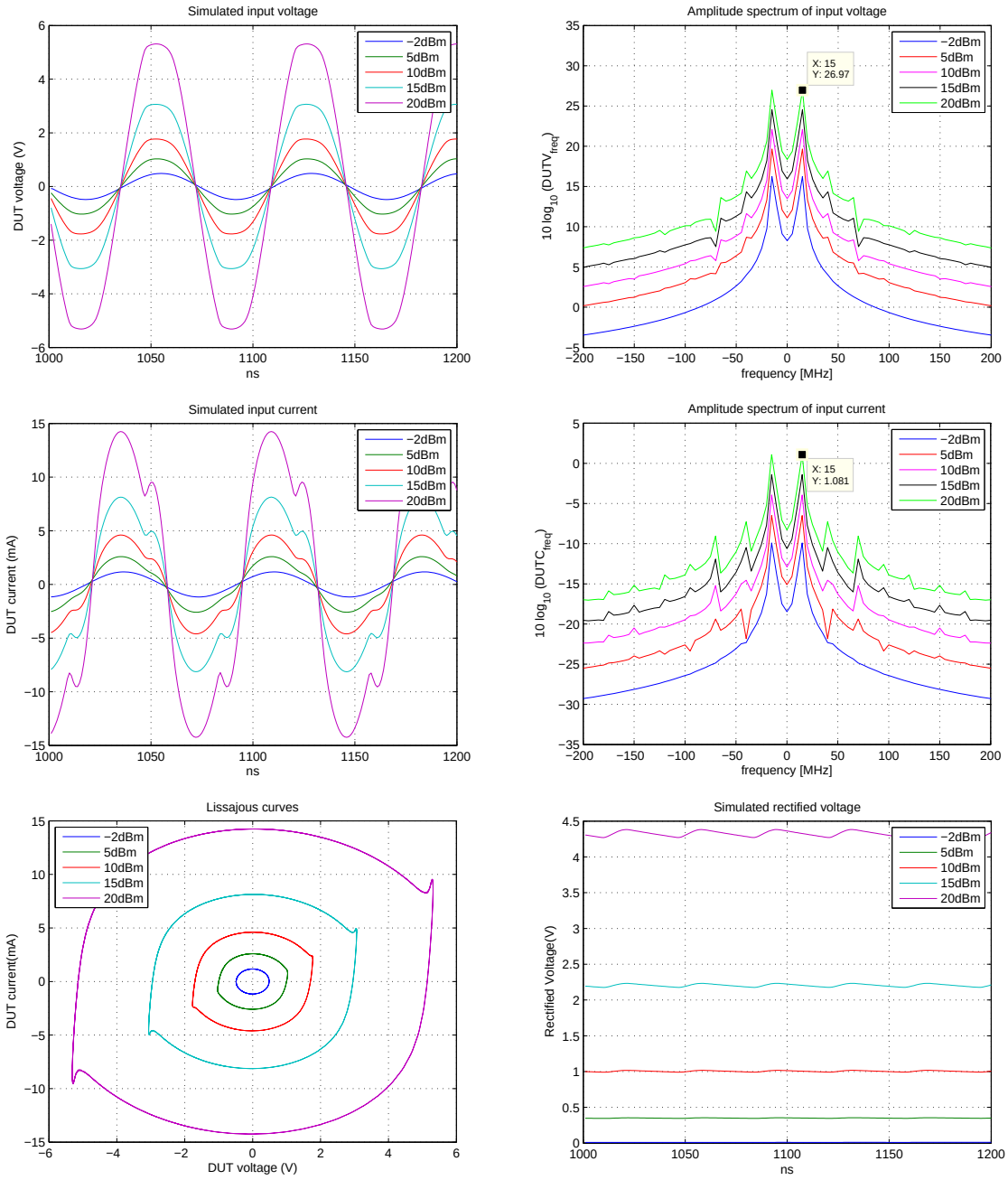

Figure 2.4: $R_{\mathrm{L}} = 2k\Omega$, $C_{\mathrm{in}} = 27\mathrm{pF}$, $C_{\mathrm{p}} = 470\mathrm{pF}$

At first sight, we notice that the rectified voltage increases when R_{L} and the input power increased. When the resistor R_{L} is too low as in 2.2 it is not possible to get a stable DC voltage. From the Lissajous curves we observe that for low input power the shape is a ellipse but when we increase the input power the ellipses start to change their shape because of nonlinear effects in the rectifier [6] [7].

At this point we will start analyzing how the different components mentioned before R_{L}, C_{in},

C_p influence the input voltage or the DC voltage[1] of the circuit.
In the following graphs an **input power of 20dBm** is applied. The value of R_L is swept and the values of the capacitors are modified in each graph to show how it affects the input voltage, input current and Lissajous curves plotted.

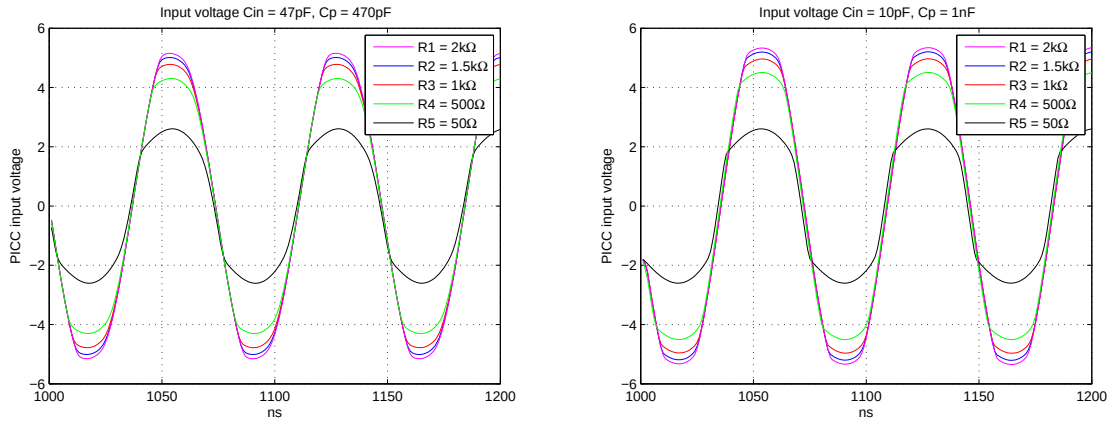

Figure 2.5: DUT input voltage

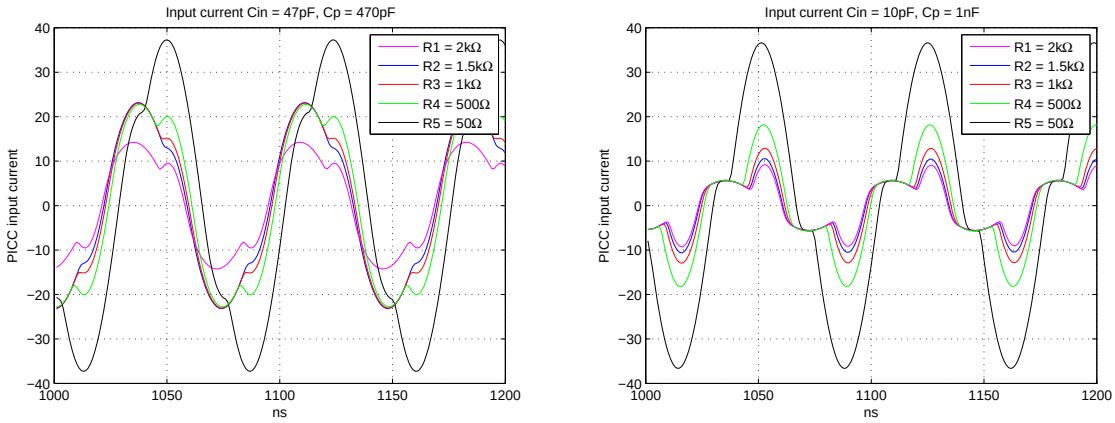

Figure 2.6: DUT Current

[1]Named in graphs as 'rectified voltage' from now

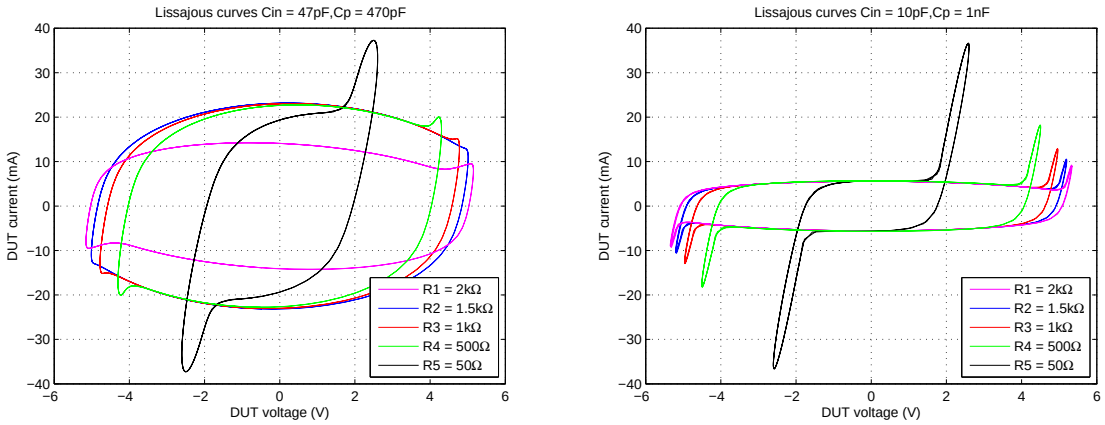

Figure 2.7: Lissajous curves

From the graphs we notice that there is almost no change on the input voltage when capacitances C_{p} and C_{in} are changed but when increasing R_{L} the input voltage of the chip also increases.

In the graphs below the value of R_{L} and C_{p} are fixed and again an **input power of 20dBm** is applied. We will evaluate the effects of $C_{\mathbf{in}}$ on the input voltage and current.

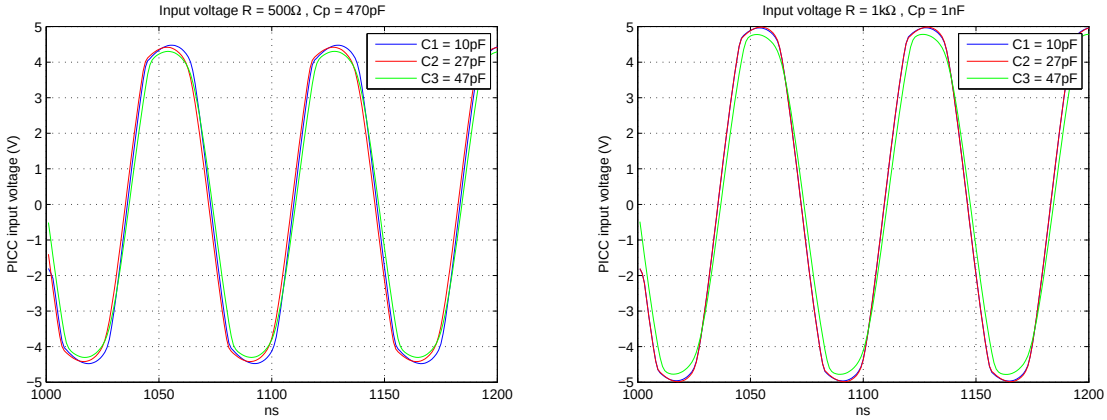

Figure 2.8: DUT input voltage

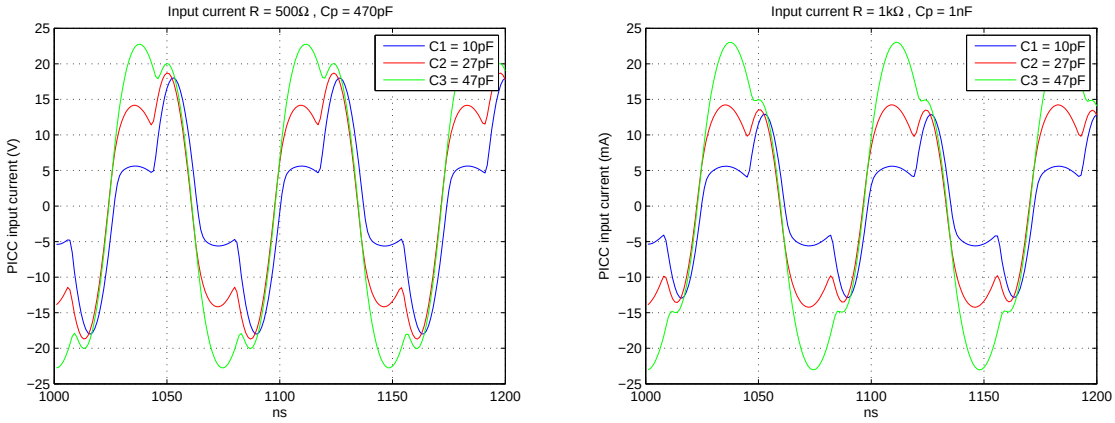

Figure 2.9: DUT Current

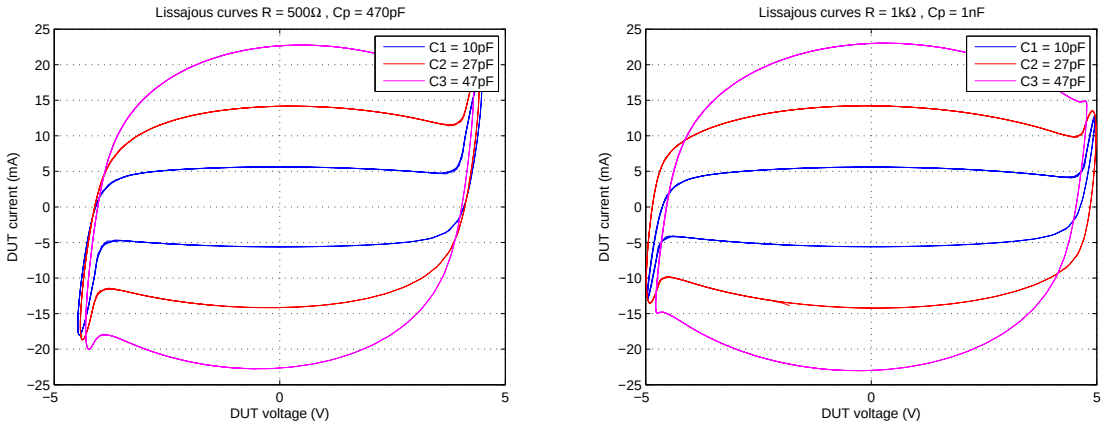

Figure 2.10: Lissajous curves

When the input capacitance C_{in} is smaller the input voltage slightly increases and the Lissajous curves become narrower on the y axis.

Now we will analyze the effect of the third element $C_{\mathbf{p}}$ on the input voltage and current. R_{L} and C_{in} are fixed and an **input power of 20dBm** is applied.

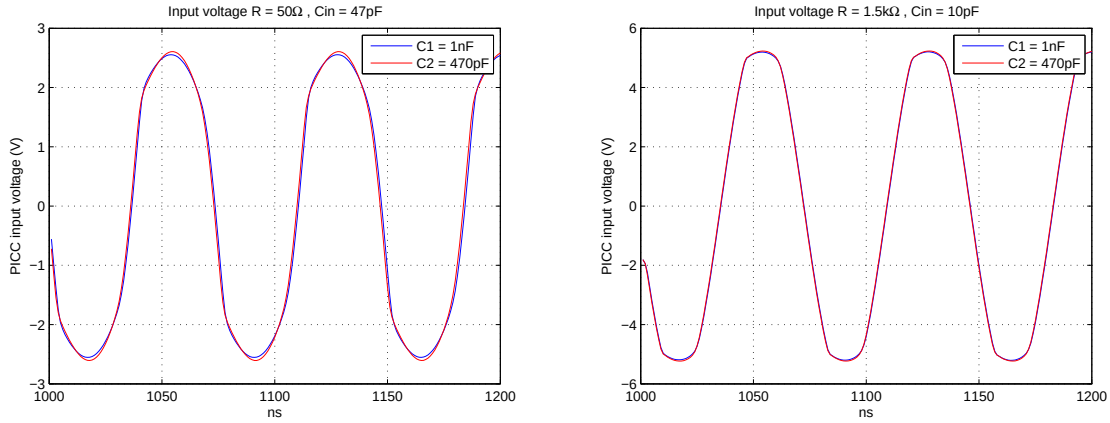

Figure 2.11: DUT input voltage

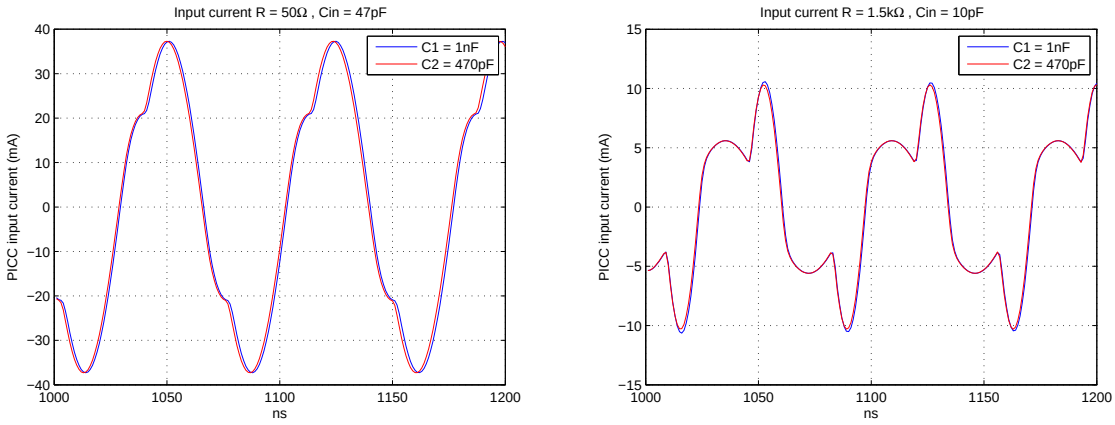

Figure 2.12: DUT Current

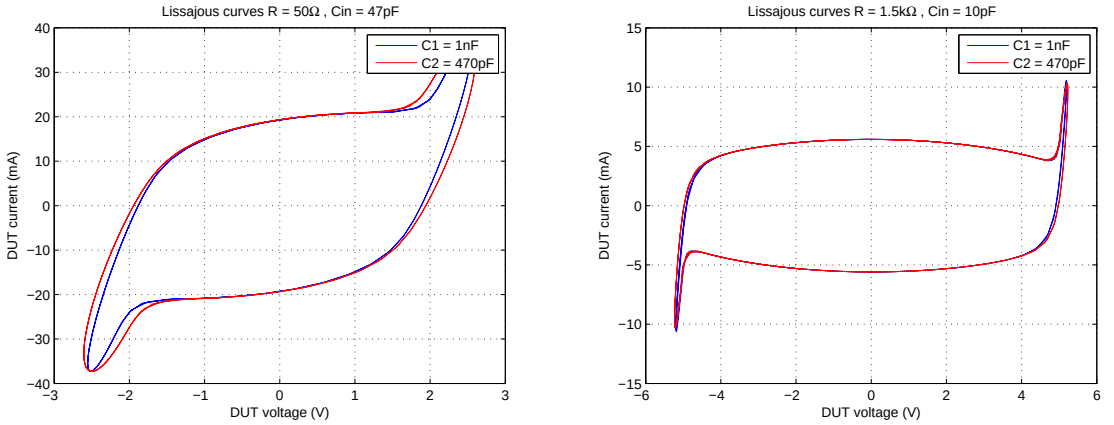

Figure 2.13: Lissajous curves

The input current as well as the input voltage are slightly modified by C_p when the value of the resistor increase.

The rectified voltage of the PICC is also plotted using an **input power of 20dBm**.

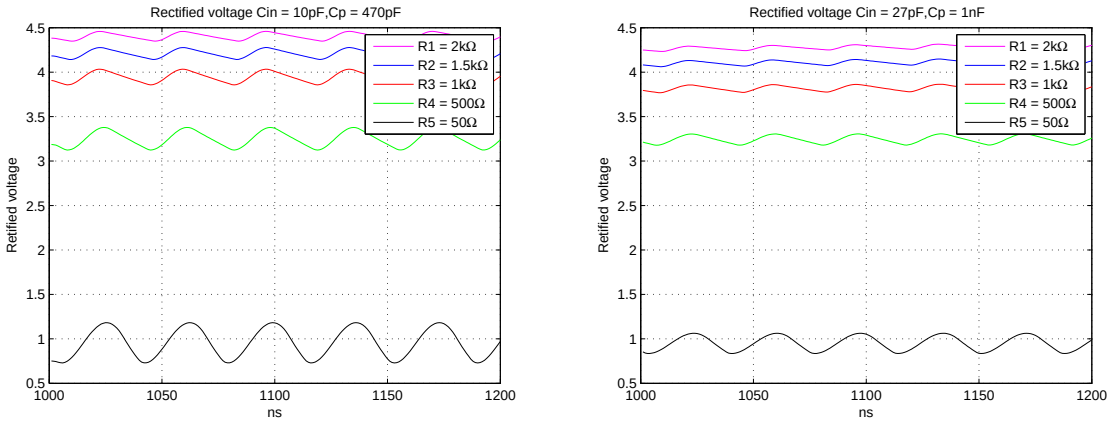

Figure 2.14: Rectified voltage

From the graphs we observe mutual dependence between C_p and R_L. If the capacitance is to high and resistance is to low, there is large variation in the rectified voltage. This is undesirable since for the chip's internal circuit we need DC voltage.

To conclude the simulation results section and with the aim of showing clearly how C_{in} and C_{p} affect the rectified voltage, two more graphs are plotted. In the first one C_{in} and the input power are swept while R_{L} and C_{p} are fixed and in the second one C_{p} and the input power are swept while R_{L} and C_{in} are modified.

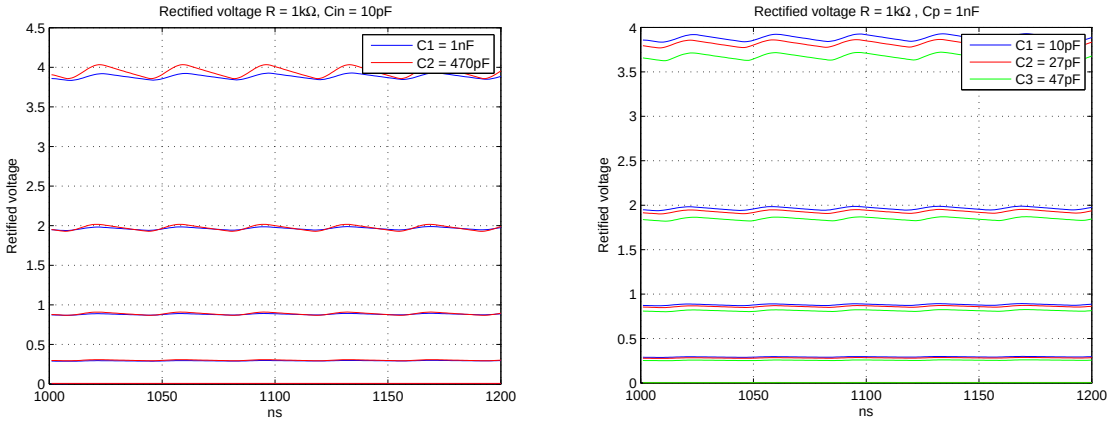

Figure 2.15: Rectified voltage modifying C_{in} (right) and C_{p} (left)

As it is visible in the graphs we have 5 groups of lines and going from top to bottom the upper group of lines correspond to a input power of 20dBm, the following to 15dBm and so on.
Analyzing those images if the input power is low there is no appreciable difference when C_{p} is modified. The change starts to be visible when the input power increases, for example 20dBm. At that point when the capacitance has a higher value the DC voltage is more stable.
Moreover on the right graph it is shown that the DC voltage obtained decreases when increasing the value of C_{in}. This effect is also more evident when the input power increases.

2.2 Chip card measurements

In this section the procedure followed to design and build the simulated circuit is described. Afterward, the setup used is introduced and the measurement results are shown as it was done for simulation.

2.2.1 PICC design and construction

The simulated PICC circuit was built in a Printed circuit board (PCB) board. First of all, the circuit was designed using Eagle PCB design software. Surface Mounted Devices (SMD) and normal size components were used. In the layout two layers of copper were used, one each side of the board. Figure 2.16 shows the layout.

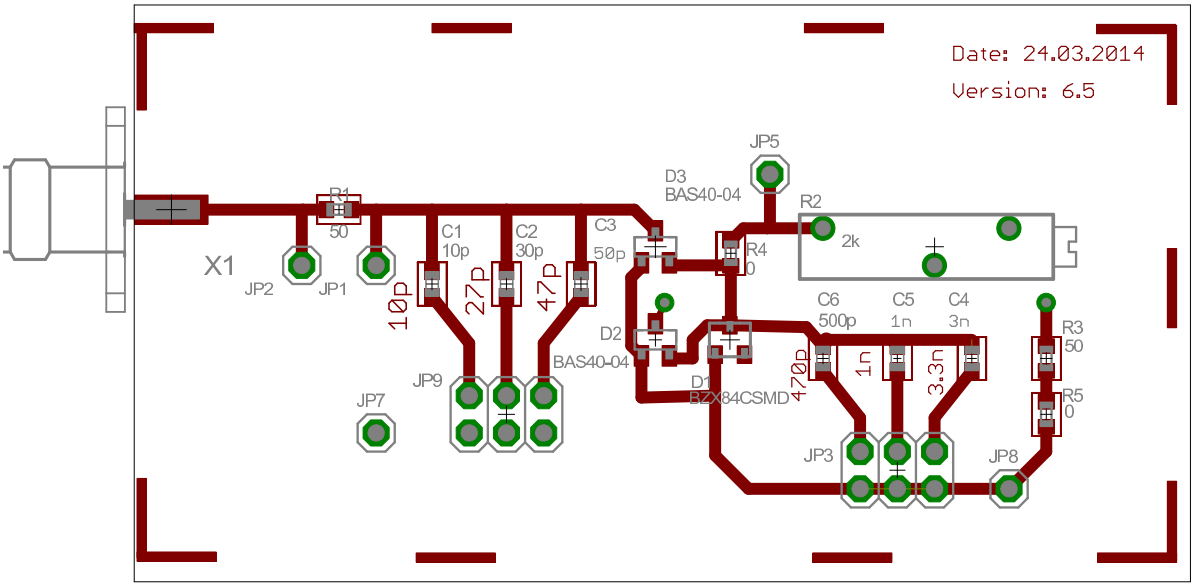

Figure 2.16: Circuit layout

Once the design was ready, it was printed using a laser printer on a photo positive film paper to get the mask. Figure 2.17 shows the top and bottom layer of the mask.

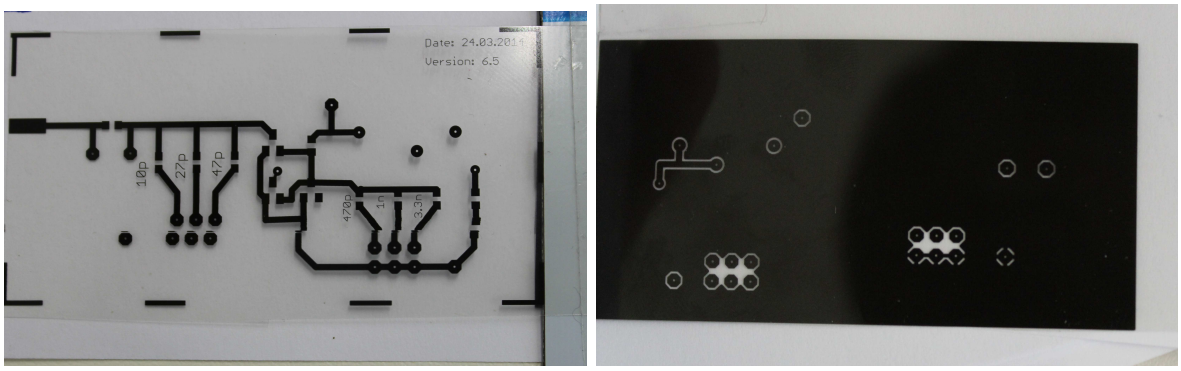

Figure 2.17: Mask front and back

A photographic method was used to engrave the pattern in the board. Using this process the entire surface of the substrate was first plated, and later on the areas that are not part of the desired pattern were subtracted.

After the mask was made, it was placed onto the photo-sensitive PCB board and was exposed to the UV for 30 sec. The next step was the developing process. Here the sensitized photoresist was taken away using a developer in order to unprotect the cooper to remove. Then the etching process was performed to remove the cooper left.

At that time the board was cleaned with alcohol and running water.
To end the building process of the PCB a manual driller was used to make the holes for the components and connections of the PCB. In the final step all the components where soldered. Figure 2.18 shows the PICC circuit built.

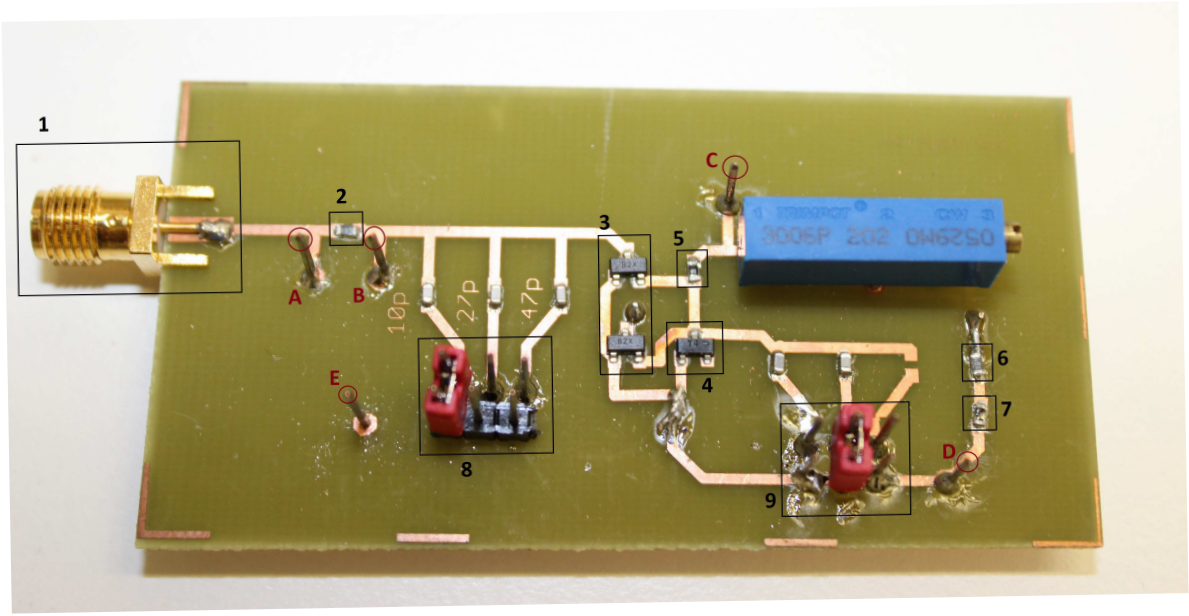

Figure 2.18: PICC built

The parts of the circuit have been labeled in the picture and they will be described in the next paragraphs. Numbers label the components and letters the pins used for measurements.

- **1:** A SMA connector was used to connect the signal generator to the PCB. The power values used were -2dBm, 5dBm, 10dBm, 15dBm and 20dBm..
- **2:** This resistor is a 50Ω resistor included in the setup for measuring the input current since there were not current probes available for that scope.
- **3:** Four Schottky diodes structure the rectifier. The diodes used are HSMS-2812 equivalent to the BAR43S defined in the standard.
- **4:** The Zener diode used is a BZX84C15LT1G; limit voltage of 15V. The main function of the diode is to limit the power supply.

- **5 and 6:** There are two 0Ω resistors in series with R_{L} and the 50Ω resistor able to be desoldered if needed.
- **7:** A 50Ω resistor was also included right after R_{L} to ensure that the load resistor is never 0.
- **8 and 9:** Two jumpers are used to change the value of the input and parallel capacitance. For the load resistor R_{L} a potentiometer $(0 - 2k\Omega)$ is used.
- **A and B:** Those pins are used to measure the input current of the chip using two channels of the scope. The input voltage of the PICC is directly measured in pin B, just right after the resistor.
- **C and D:** For measuring the rectified voltage we use again two channel of the scope and subtract them using those pins.
- **E:** Ground of the circuit.

In order to compare the simulations with the measurements the input voltage, input current and rectified voltage of the Device under test (DUT) shall be measured. The signal generator used was RohdeSchwarz SMF100A [8] [9] and the oscilloscope was a digital storage oscilloscope DSO-X 3024A from Agilent Technologies. The same devices where used for all the measurements.

2.2.2 Setup and results

Figure 2.19 shows the setup used. A filter was placed between the DUT and the signal generator in order to cancel out the harmonics of the generator. This filter is described in [6].

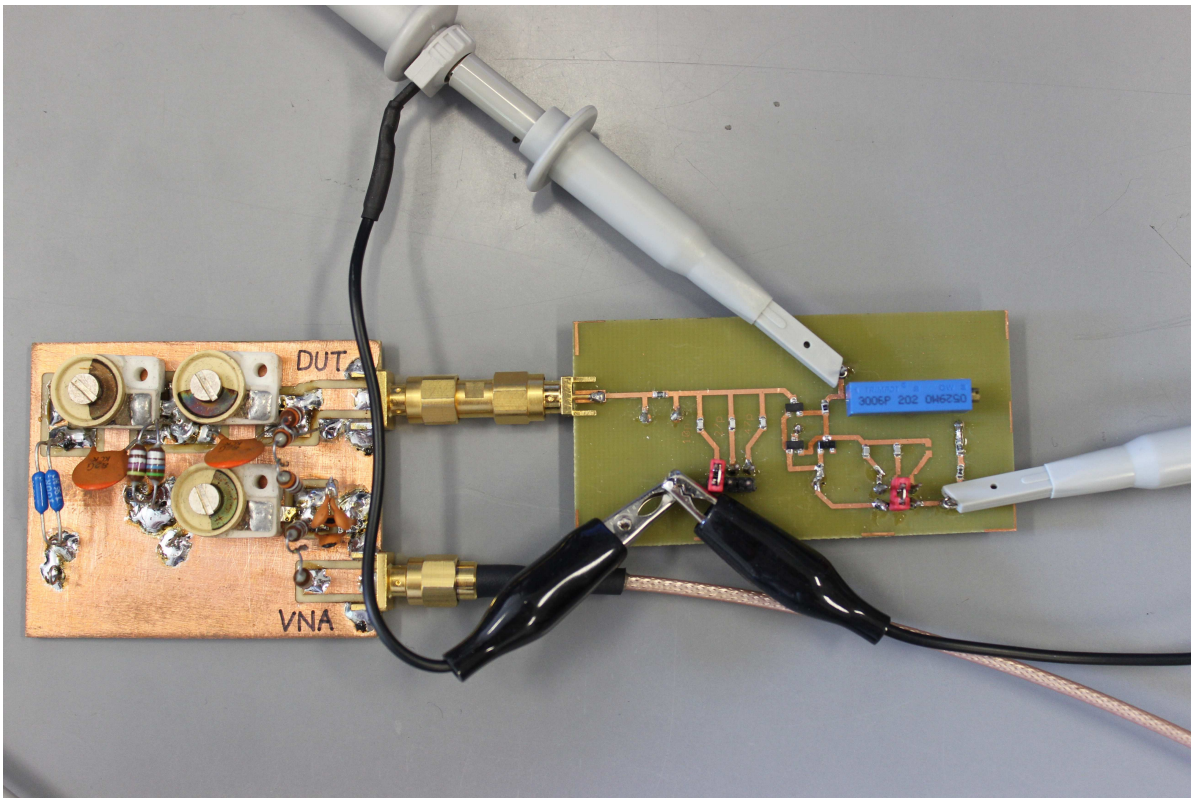

Figure 2.19: Measurement setup

As it was done for simulations, in the following graphs 2.20, 2.21, 2.22 some of the measurements are shown. The variable elements and the range was the same as in simulation 2.1, 2.2, 2.3.

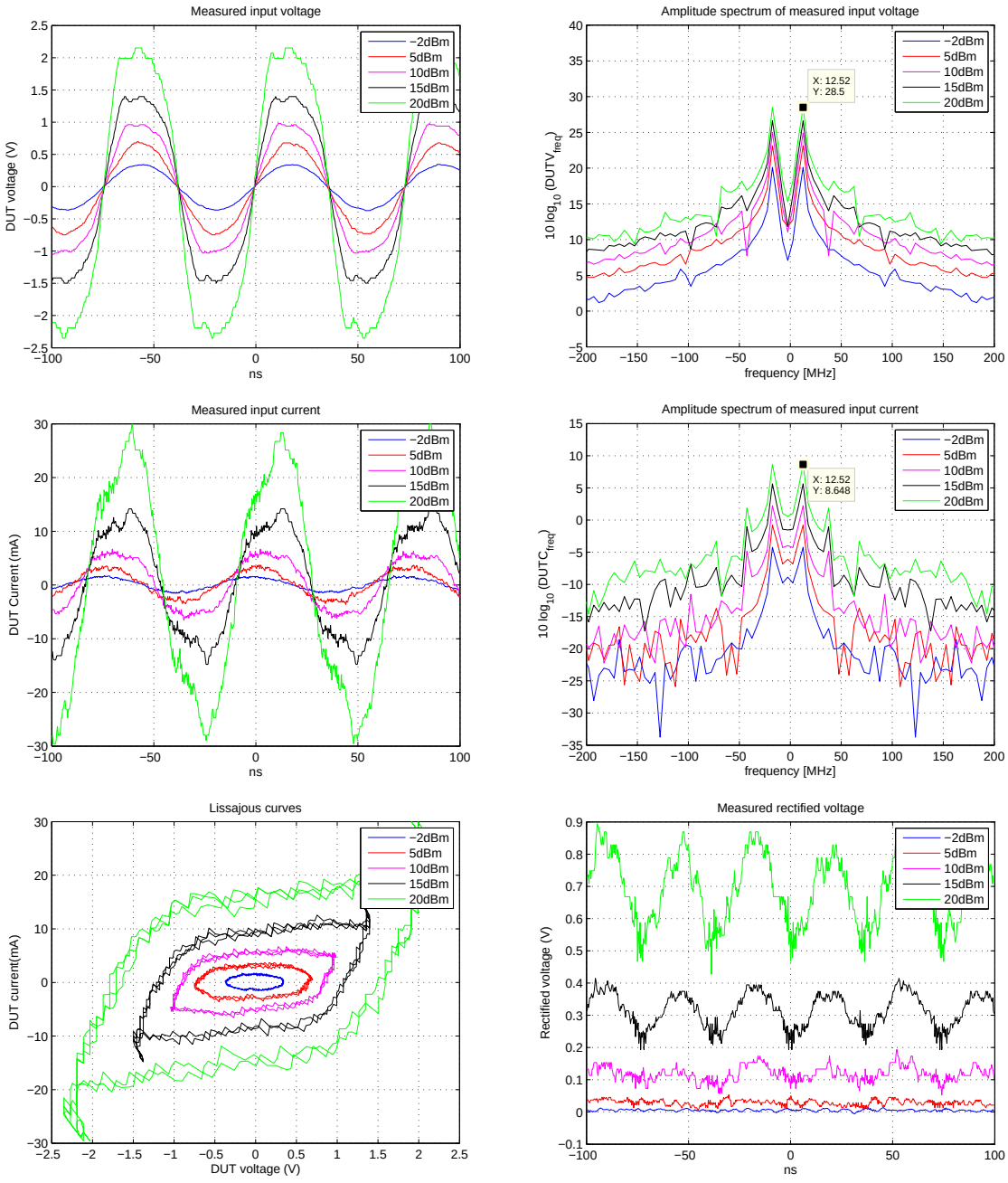

Figure 2.20: $R_{\mathrm{L}} = 50\Omega$, $C_{\mathrm{in}} = 27\mathrm{pF}$, $C_{\mathrm{p}} = 470\mathrm{pF}$

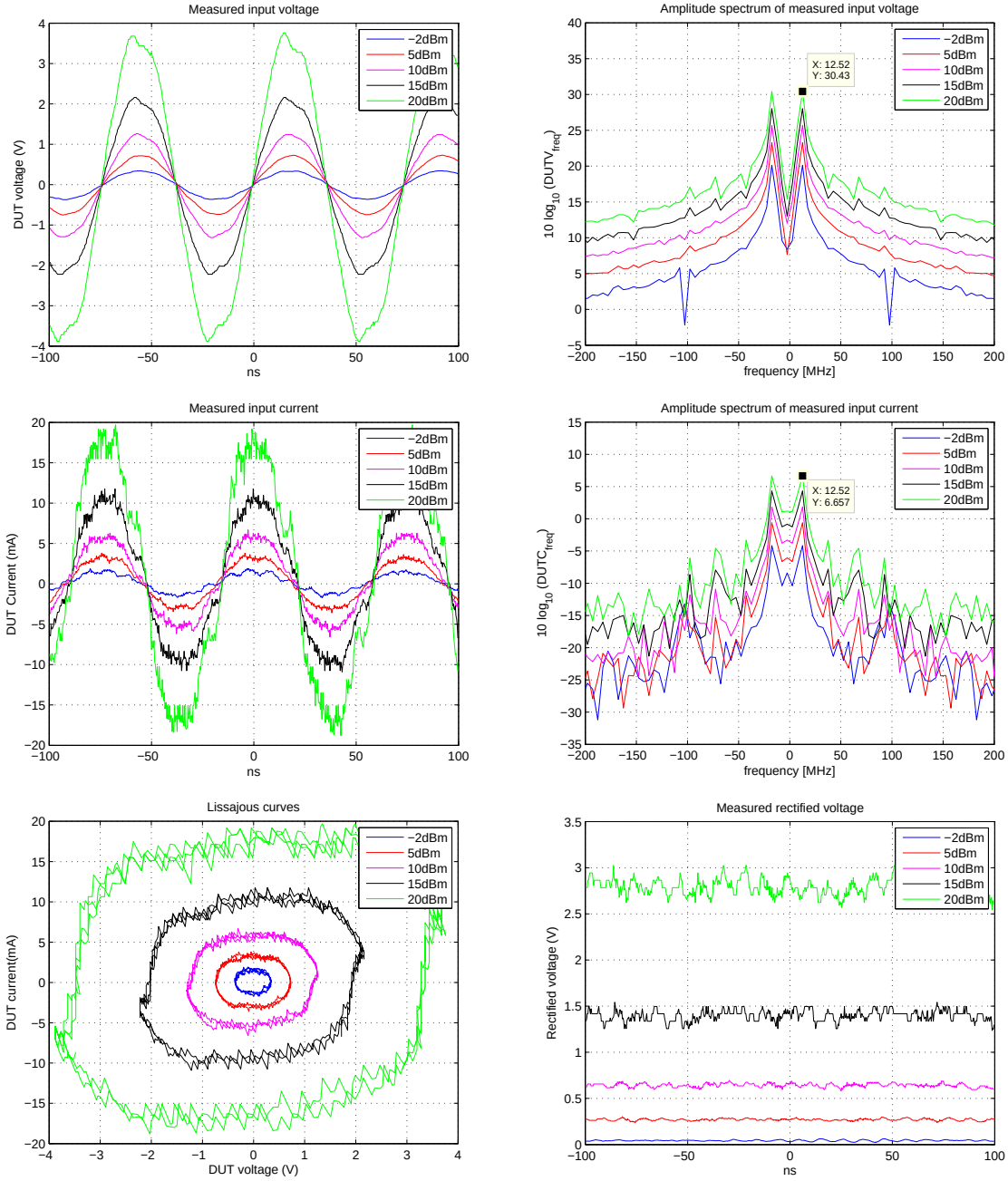

Figure 2.21: $R_{\mathrm{L}} = 1k\Omega$, $C_{\mathrm{in}} = 27\mathrm{pF}$, $C_{\mathrm{p}} = 470\mathrm{pF}$

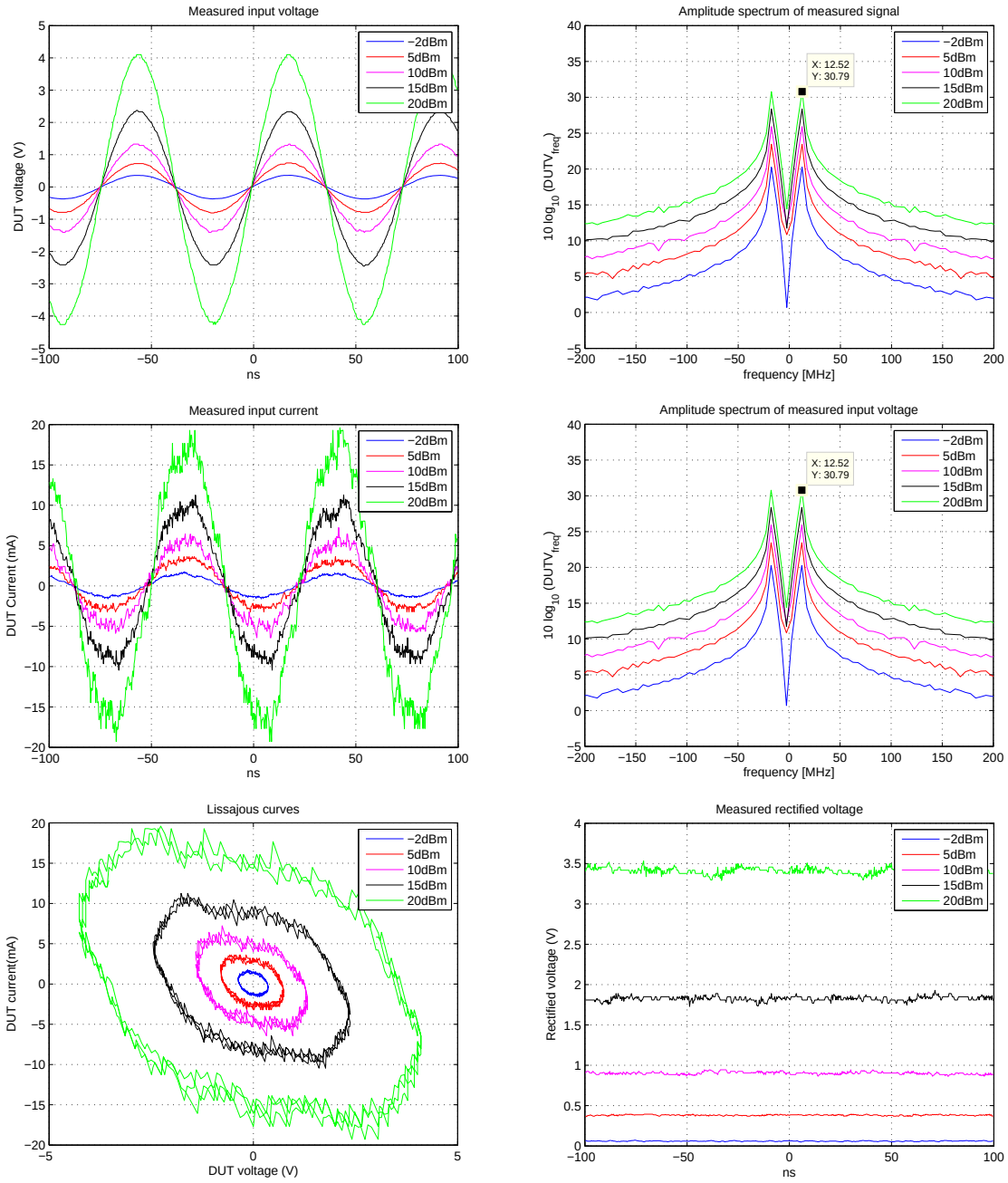

Figure 2.22: $R_{\mathrm{L}} = 2k\Omega$, $C_{\mathrm{in}} = 27\mathrm{pF}$, $C_{\mathrm{p}} = 470\mathrm{pF}$

A clear difference from the simulation graphs is noticeable: the graphs of the rectified voltage and the input current look a noisier now.
As it was said before, there were not differential probes available for the oscilloscope used and those measures came from subtracting two channels on the scope which results in an increment of the noise.

The variation of the rectified voltage when C_{p} and C_{in} change is shown in the upcoming graphs. A sweep in R_{L} and a fixed **input power of 20dBm** is applied.

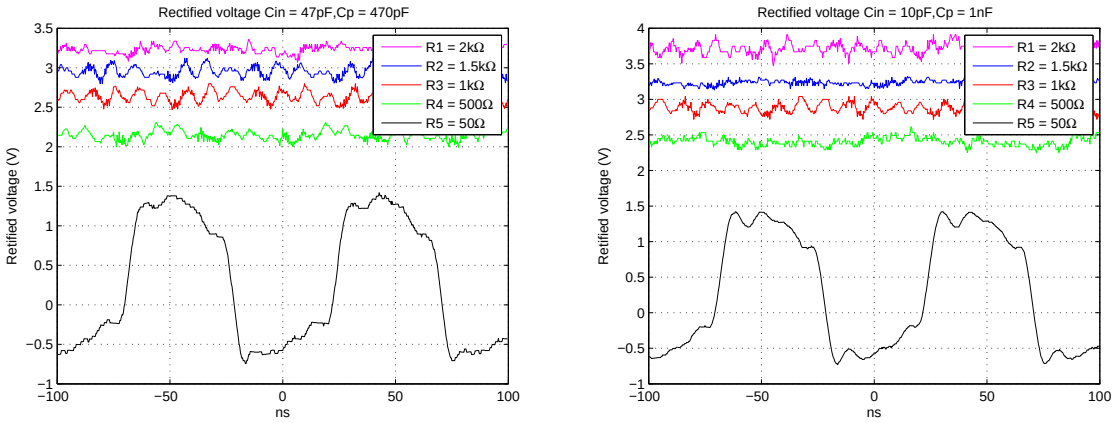

Figure 2.23: Rectified voltage

Similar effects to simulation are observed. There is a dependence between C_p and R_L and the DC voltage became more stable when increasing R_L.

To end this section the rectified voltage will be also plotted fixing the resistance R_{L} and one of the capacitors (C_{p} or C_{in}) and making a sweep on the input power.

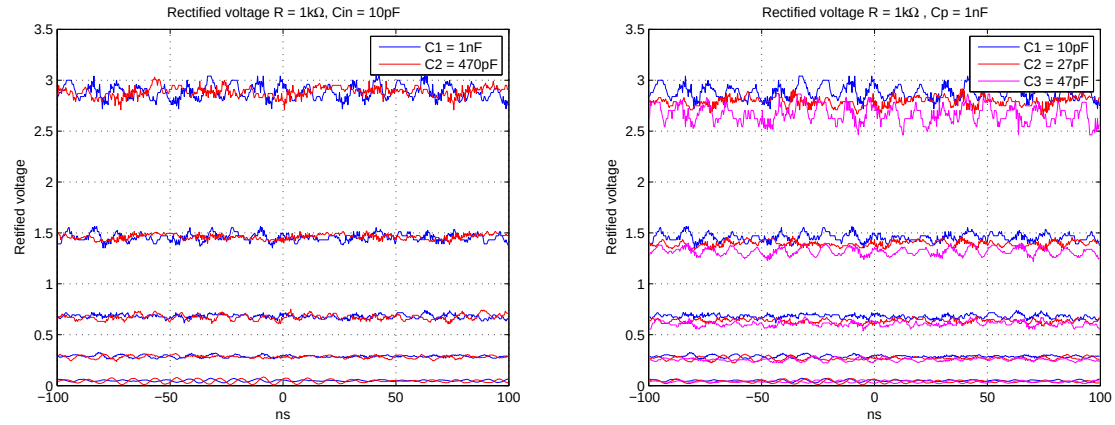

Figure 2.24: Rectified voltage modifying C_{in} (right) and C_{p} (left)

From top to bottom the input power is decreased, so the upper group of three lines correspond to the higher input power (20dBm).
Although here the effects cannot be clearly noticed in section 2.3 this problem will be solved.

2.3 Analyzing simulation and measurements results

In previous sections of this chapter simulation and measurement results are presented independently. Now I have tried to find a common tendency for the circuit behavior.

In the following graphs two values are fixed and one is swept. A power sweep was also performed. The graphs are presented as the input/rectified voltage versus input power and the results produced are commented.

Firstly, the effects on the input voltage will be analyzed and afterward the same will be done with the rectified voltage.
At that point simulation and measurement results for the input voltage are compared in the same graph. The values of the two invariable components are written as the title of the graphs. In the first pair of graphs R_{in} is swept, in the second C_{in} is swept and in the third on C_{p} is swept.
The power sweep is shown in the x-axis.
Simulation results are presented in dashed line and measurement results are shown in solid line.

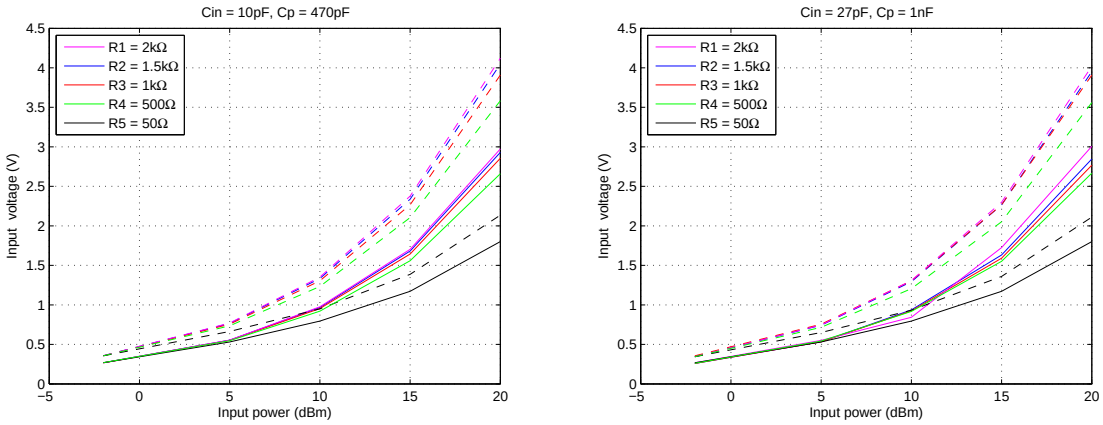

Figure 2.25: Input voltage simulated and measured, R_{L} sweep

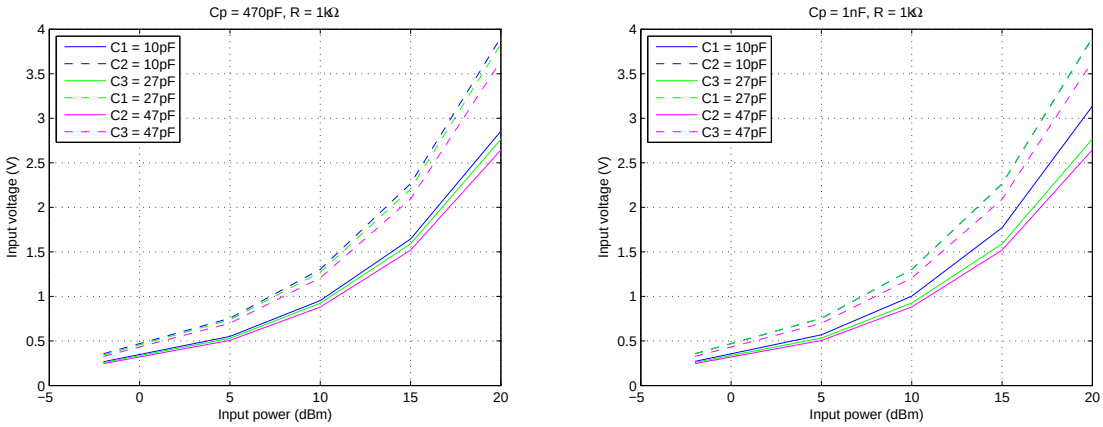

Figure 2.26: Input voltage simulated and measured, C_{in} sweep

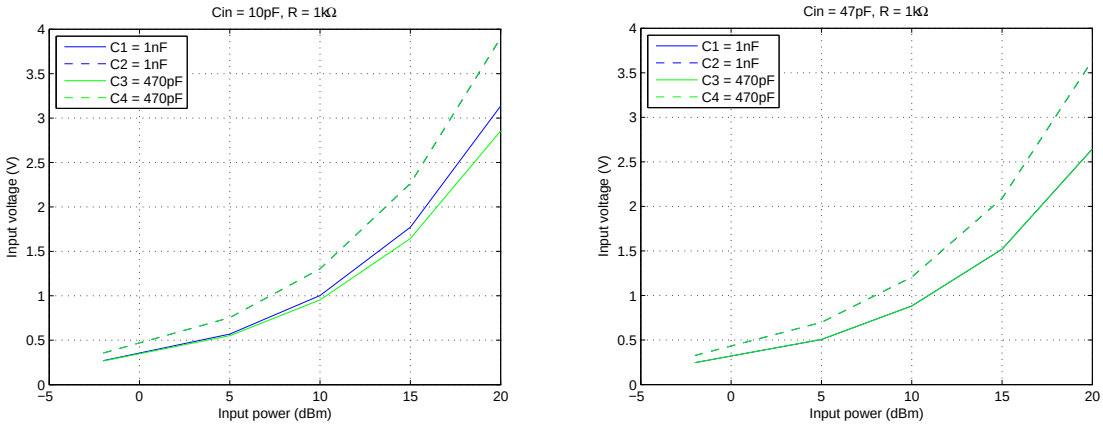

Figure 2.27: Input voltage simulated and measured, C_p sweep

A similar behavior between measured and simulated input voltage is illustrated on the graphs. Modifying C_p slightly affects the input voltage however increasing C_in reduces the input voltage.

A good measure to compare the simulation with the measurement results when the signal is closed to a sine wave is comparing the difference of the harmonics. As an example, for NXP a difference of 10dB is understood as a good alignment between the simulation and the measurement. Consequently an spectral analysis is performed for measured and simulated input voltage and input current in 2.28, 2.29, 2.30 and 2.31.

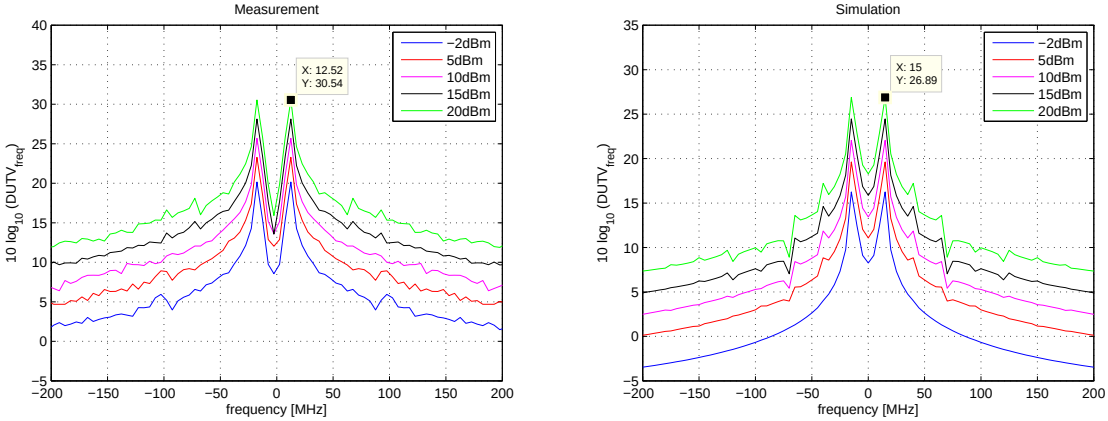

Figure 2.28: FFT input voltage, $R_{\mathrm{L}} = 1.5k\Omega$, $C_{\mathrm{in}} = 27pF$, $C_{\mathrm{p}} = 470pF$

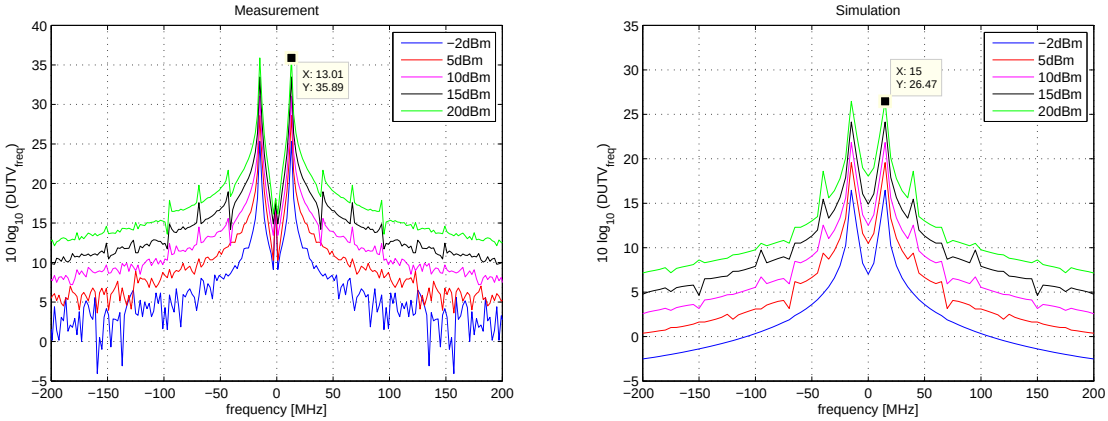

Figure 2.29: FFT input voltage, $R_{\mathrm{L}} = 500\Omega$, $C_{\mathrm{in}} = 10pF$, $C_{\mathrm{p}} = 1nF$

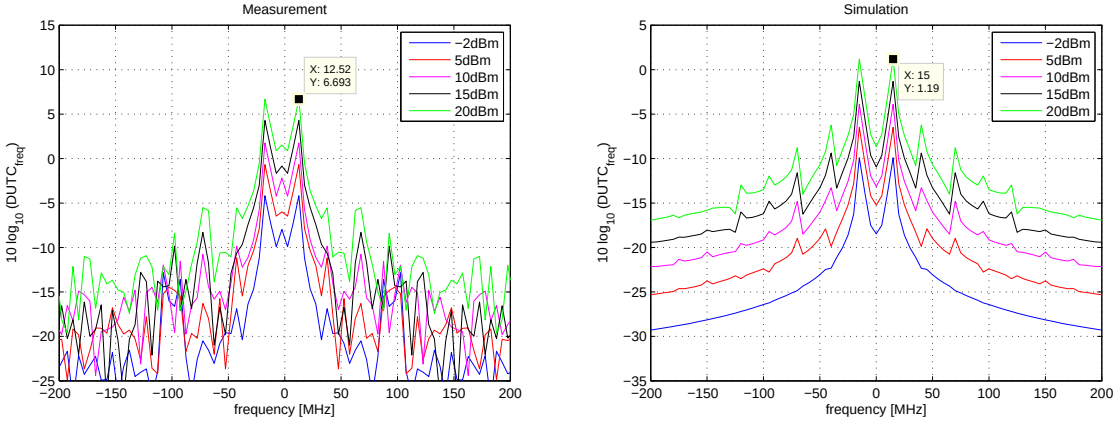

Figure 2.30: FFT input current, $R_{\mathrm{L}} = 1.5k\Omega$, $C_{\mathrm{in}} = 27pF$, $C_{\mathrm{p}} = 470pF$

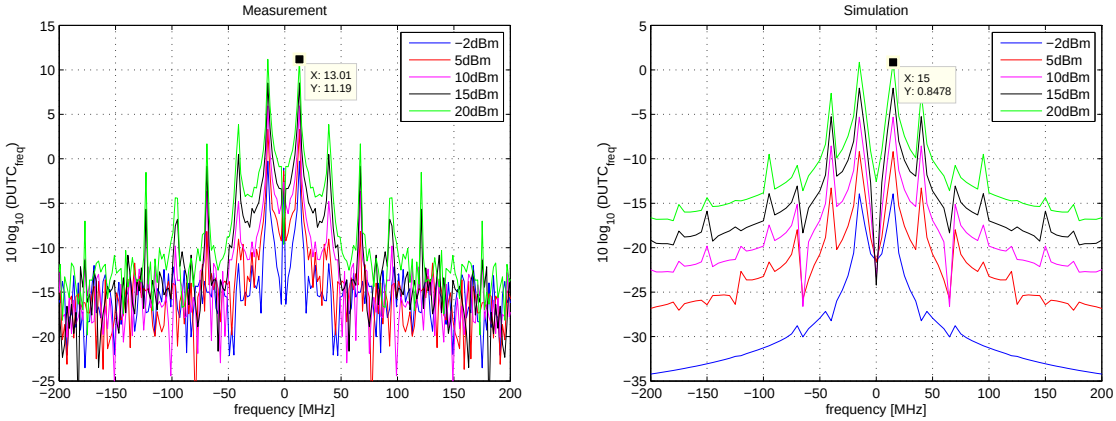

Figure 2.31: FFT input current, $R_{\mathrm{L}} = 500\Omega$, $C_{\mathrm{in}} = 10pF$, $C_{\mathrm{p}} = 1nF$

Two different set of values were chosen to perform the frequency analysis.
A cursor is placed on the plotted graphs so the maximum value is labeled and can be compared.
For both pairs of graphs the difference between the amplitude of the spectrum is less than 10dB so we can assume a good matching within simulation and measurement.
From the graphs it can also be observed that when the input power is increased the harmonics also increased.

At that point we will start analyzing the results for the rectified voltage.
As it was done previously, simulation and measurement results for rectified voltage are compared in the same graph.
Simulation results are presented in dashed line and measurement results are shown in solid line.

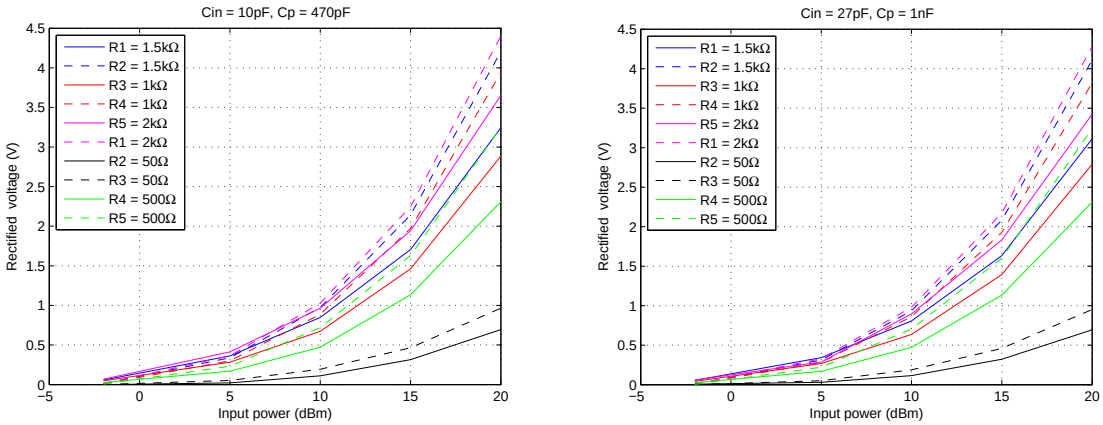

Figure 2.32: Rectified voltage simulated and measured, R_{L} sweep

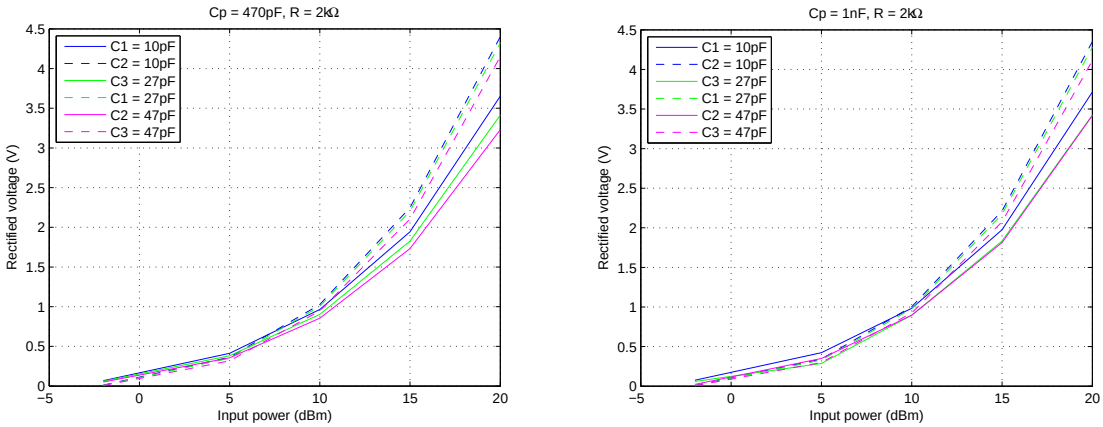

Figure 2.33: Rectified voltage simulated and measured, C_{in} sweep

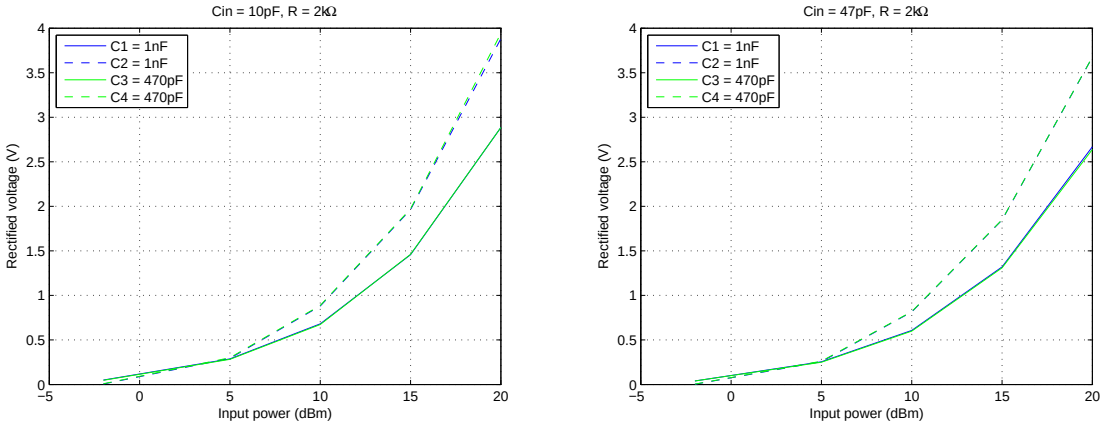

Figure 2.34: Rectified voltage simulated and measured, C_{p} sweep

As the figures show, the same behavior is present in simulation and measurement although higher values of the rectified and input voltage are achieved in simulation due to the acceptable losses in measurements produced for the measurement devices.

The noticeable effect is the incrementation of the rectified voltage when the input power and the resistor R_{L} value are increased. The more resistance you have, the slower the capacitor can discharge therefore a higher voltage is obtained.

If we look at each pair of graphs we can notice that when the parallel capacitance changes and the input capacitance does not there is a slightly difference on the rectified voltage, being somehow higher when the parallel capacitance is larger.
On the other hand if we vary the input capacitance C_{in} but leave C_{p} constant and the resistor R_{L} is up to 500Ω, we evidence that the rectified voltage decreases when C_{in} increases.

To end this section, the remarkable effects on the voltages produced because of the variation of the components will be summarized.
Consequences on input and rectified voltage are similar:

- Increasing R_{L} and the input power produces a higher input and rectified voltage.
- Increasing C_{in} decreases the input and rectified voltage.
- Apparently there are no significant changes on the input and rectified voltage when C_{p} is modified, except that the rectified voltage became more stable when C_{p} is increased.

Chapter 3

Test PCD assembly

3.1 Description

Chapter three includes the Test PCD assembly measurements.
The test apparatus is defined in detail in ISO/IEC 10373-6 [5] and ECMA-356 [10].
The primary purpose of this test assembly is to measure the load modulation coefficients of contactless cards, tags or devices dependent on the field strength. This test setup is also used as a standard reader antenna for other tests and measurements on cards (PICC), like testing the influence of the reader's signal waveform and the card's ability to detect them correctly.

Parts of test PCD assembly are explained and pictures show the setup used.

The PCD antenna is showed in figure 3.1. It is a one turn coil of 150 mm diameter. It contains an impedance matching network.

Figure 3.1: PDC antenna

In figure 3.2 the sense coil and the calibration coil are presented. Two sense coils are needed,

sense coil 'a' and sense coil 'b'. The sense coils are connected in a way that the signal from one coil is in opposite phase to the other. The goal of these coils it to measure the magnetic field strength at a certain distance from the reader.
The calibration coil is fixed to one of the sense coils. On the other coil, the PICC card is set. The calibration coil consists of a printed circuit board which has the height and width of an ID-1 type defined in ISO/7810 containing a single turn coil concentric with the card outline [11].
The calibration factor is given by the geometry of the coil and is 900mV (peak-to-peak) for a magnetic field strength of a 1.0 A/m (rms) at the operating frequency of 13.56 MHz.
The magnetic field strength can be calculated from the measured voltage on the calibration coil by the following formula:

$$H_{RMS} = 3.11 * V_{RMS} \tag{3.1}$$

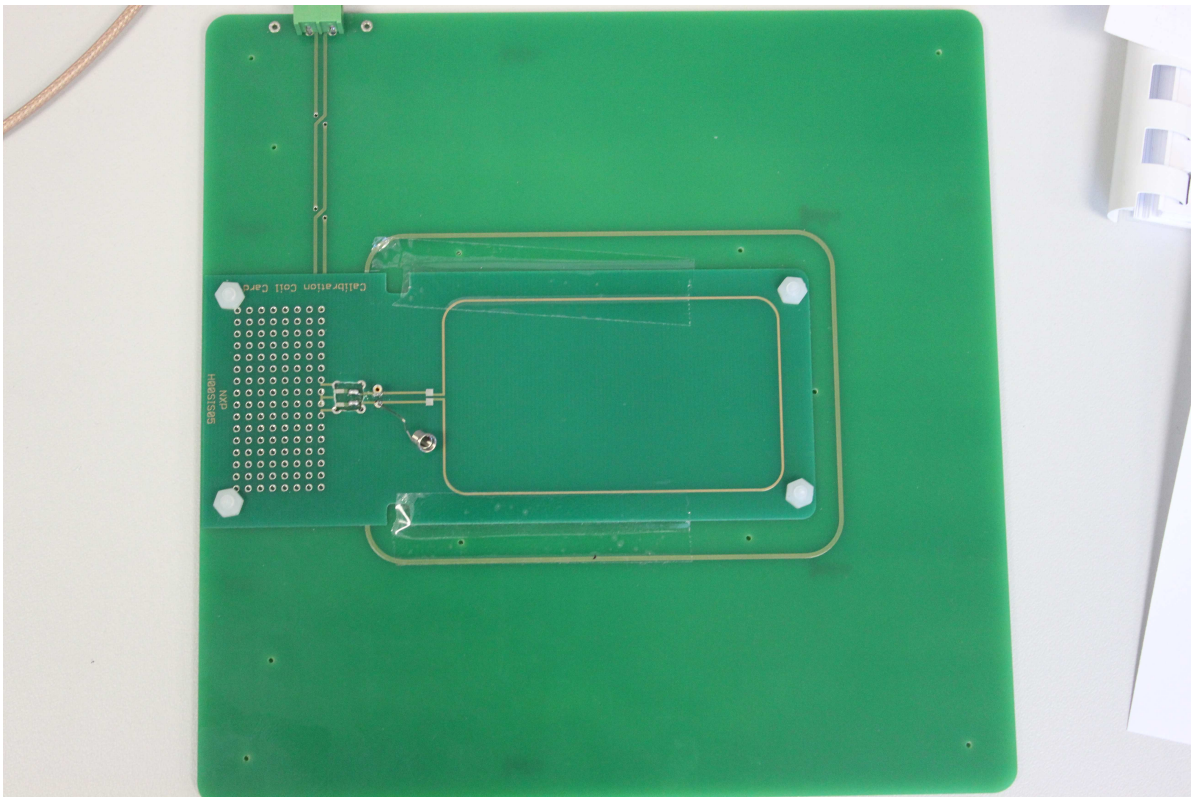

Figure 3.2: Sense coil and calibration coil

The PICC card is shown in figure 3.3. The parts and components of the reference PICC where described in 1.2. It is a class 1 card also provided by NXP.

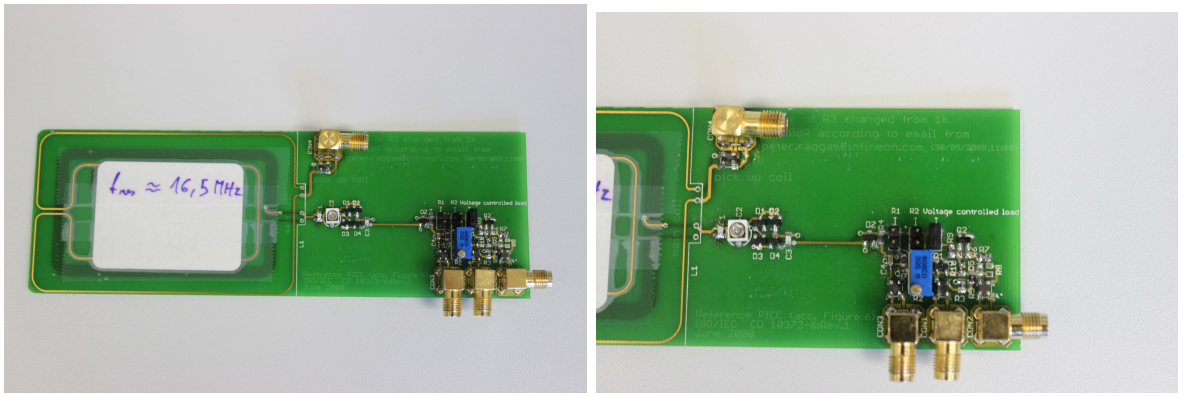

Figure 3.3: Class 1 PICC

There is also a balancing circuit consisting of a 10Ω potentiometer and two 240Ω resistors used to adjust the balance point when the sense coils are not loaded by a PICC.

Figure 3.4: Compensation circuit

Figure 3.5 gives an overview of the test PCD assembly.
The antenna is placed in the middle and the distance from the coils to the antenna is the same and equal to 37.5 mm. The calibration coil is fixed to the downer sense coil and the DUT will be place into the upper sense coil. The balancing circuit is on the right side of the figure.

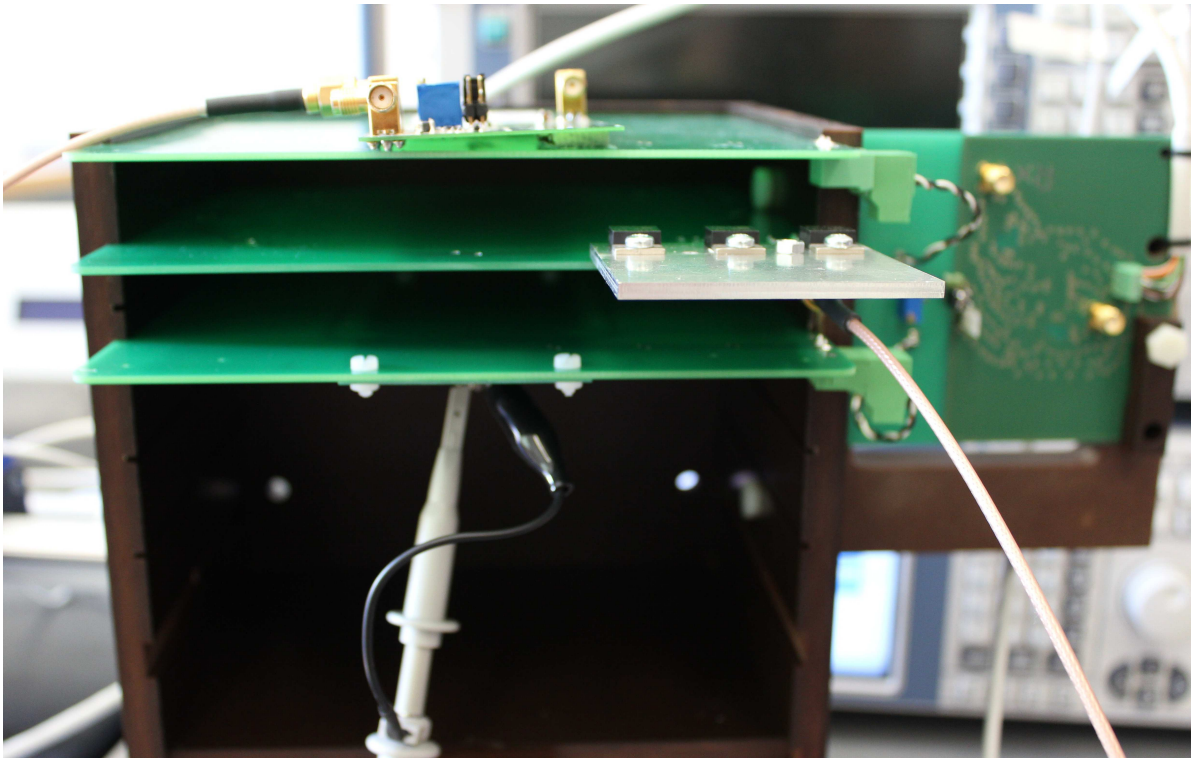

Figure 3.5: Test PCD Assembly

3.2 Reference PICC test using a reader emulator

Before any test of PCD was performed the resonance frequency of the card should be known and the balancing circuit of PCD test assembly should be tested.
With the calibration coil in place but without the DUT card in position the signal on the probe connected to the balancing circuit should be below 20mV (peak to peak) when the input power is increased until the probe on the calibration coil measures 2V (peak to peak). The 10Ω potenciometer P1 can be adjust for a minimum output voltage [11].

There are different methods of measuring the resonance frequency of the chip card [12][13][14]. In this work, a Vector network analyzer (VNA) was used and the S11 parameter was measured [15].
Firstly the calibration kit was used to calibrate one-port of VNA. The resonance frequency of a class 1 PICC and an ePasslet Suite was measured using the setup in 3.6 .

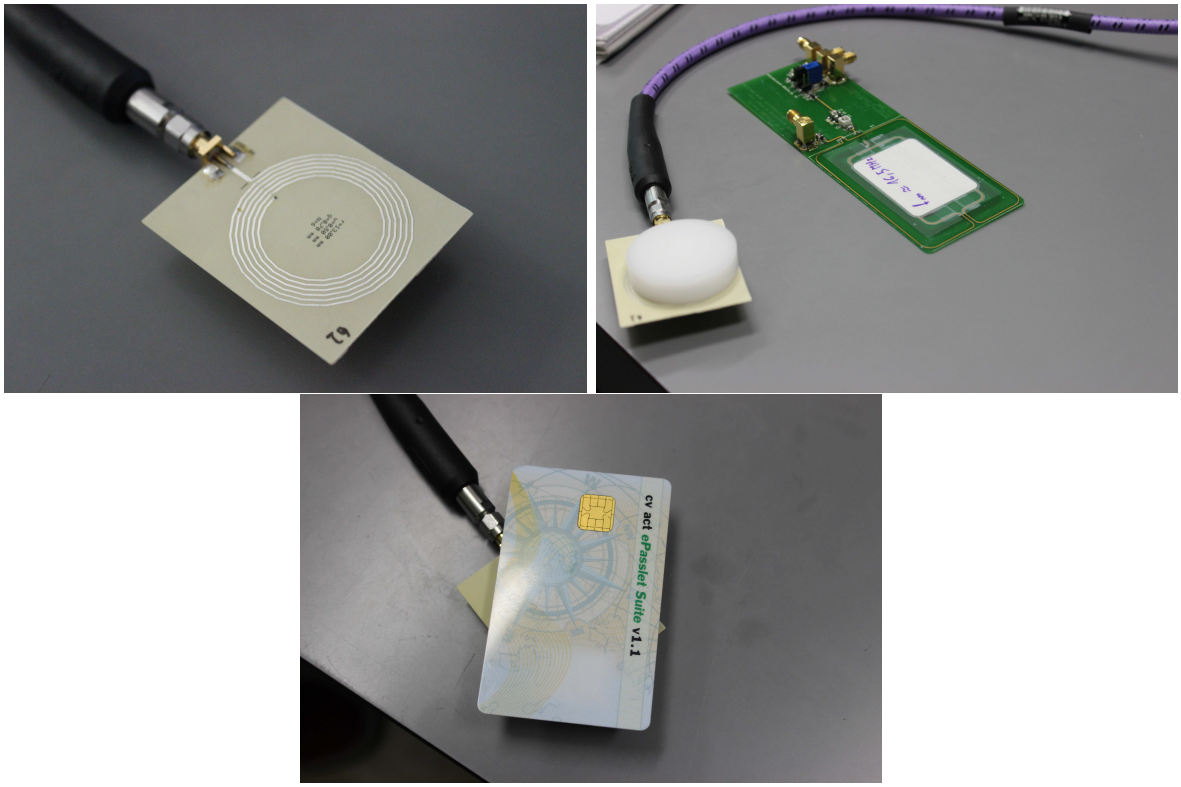

Figure 3.6: Resonance frequency measurement setup

Later on, the VNA was calibrated using the calibration coil in figure 3.6 as short instead of the short on the calibration kit.
The dimensions of the coil are r = 13mm, w = 0.5mm, g = 0.7mm and N = 6. With the same setup the resonance frequency was measured again.

Results of the resonance frequency measurement using the normal calibration or the custom calibration are shown in figures 3.7 and 3.8 for the class 1 PICC and the ePasslet Suite. The normal calibration is plotted on the left side and the custom calibration on the right side.

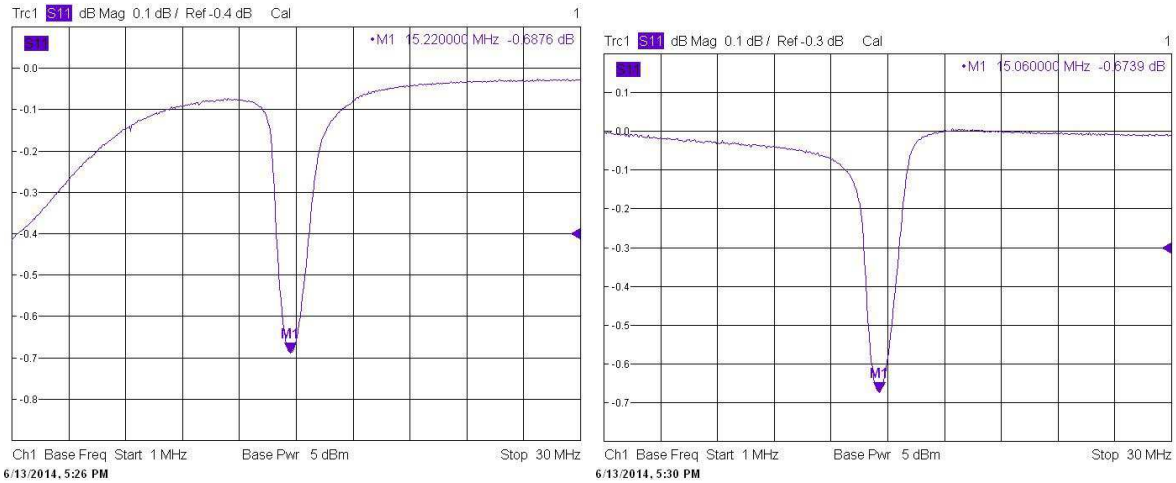

Figure 3.7: Resonance frequency ePasslet Suite

Figure 3.8: Resonance frequency class 1 PICC

In the figures where the normal calibration was used it is noticeable a mismatch in the right side of the graph but when using the custom calibration this mismatch disappears.

When the resonance frequency of the class 1 PICC was measured and checked that it was around 16.5MHz the following test procedure was done.

- 1: The PICC was placed into the DUT position on the Test PCD assembly.
- 2: A sine wave with a magnetic field strength of 1.5A/m, 3A/m, 4.5A/m and 7.5A/m was applied.
- 3: The voltage on the calibration coil was measured to verify the operating magnetic field strength.
- 4: The jumper J1 was switch to position 'b' and R2 was adjusted to obtain a DC voltage of 3V or 6V measured at CON3.
  The different values of R2 were noted.

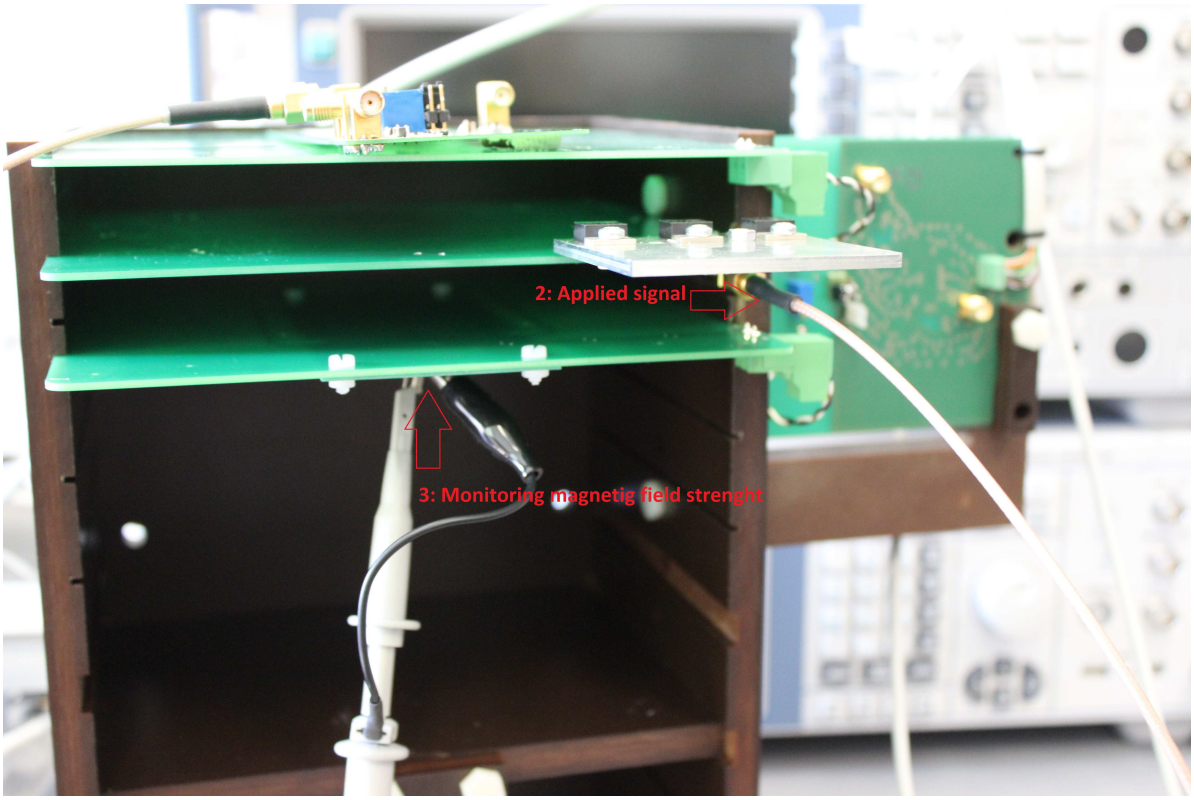

Figure 3.9: Test setup

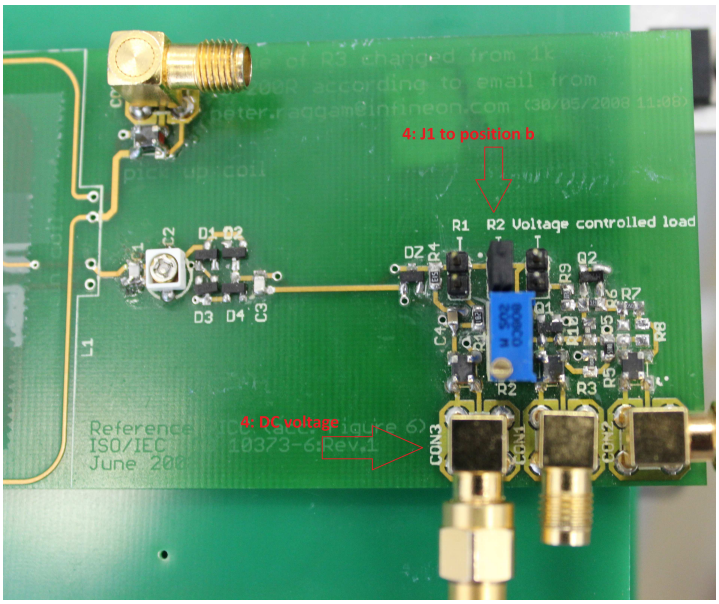

Figure 3.10: Test setup

Using 3.1 the voltage that should be measured on the calibration coil for different values of the magnetic field strength is calculated and shown in 3.1.

H_{RMS}	1.5A/m	3 A/m	4.5A/m	7.5A/m
V_{RMS}	0.4812 V	0.9642 V	1.4464 V	2.4106 V

Table 3.1: V_{RMS} for different magnetic field strength

The values of the variable resistor R2 measured for the different magnetic field strength are shown in the following graph.
As an example, figure 3.12 shows a screenshot from the scope where the blue signal is the signal measured in the balancing circuit, the green signal is the signal measured on the calibration coil (in this case, corresponding to a magnetic field strength of 7.5A/m) and the yellow signal in the DC voltage measured in CON3, in this case around 3V.

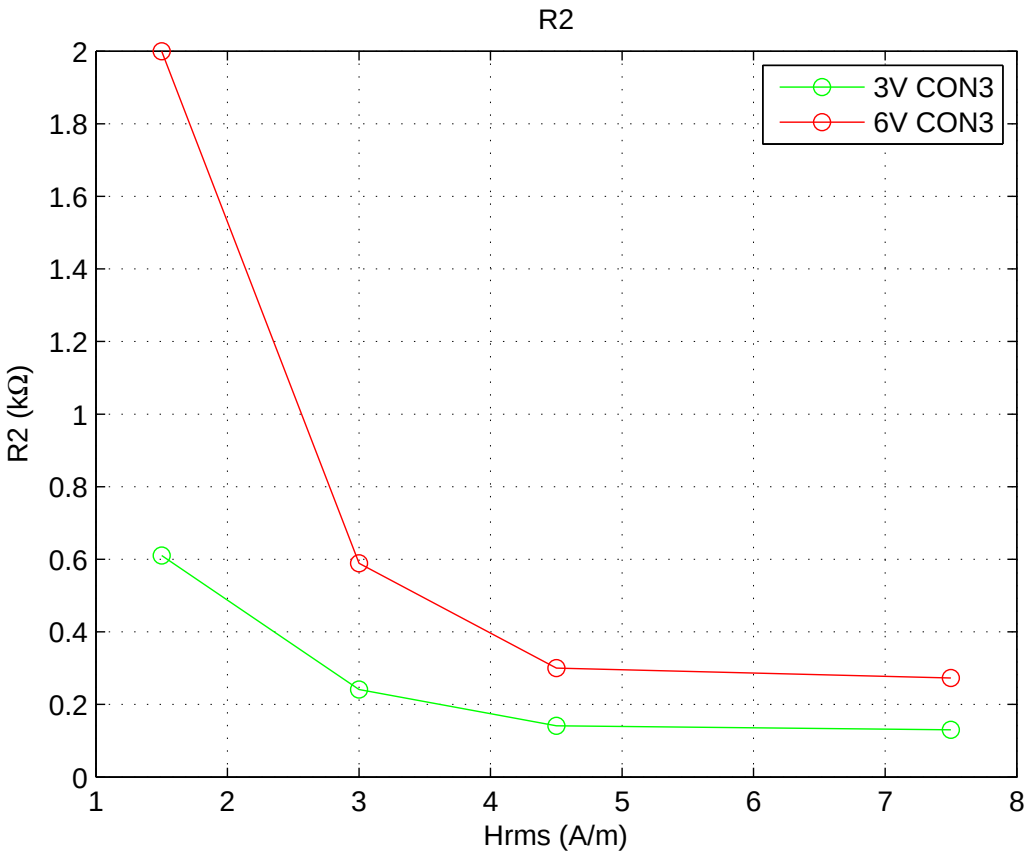

Figure 3.11: R2 values for different magnetic field strength

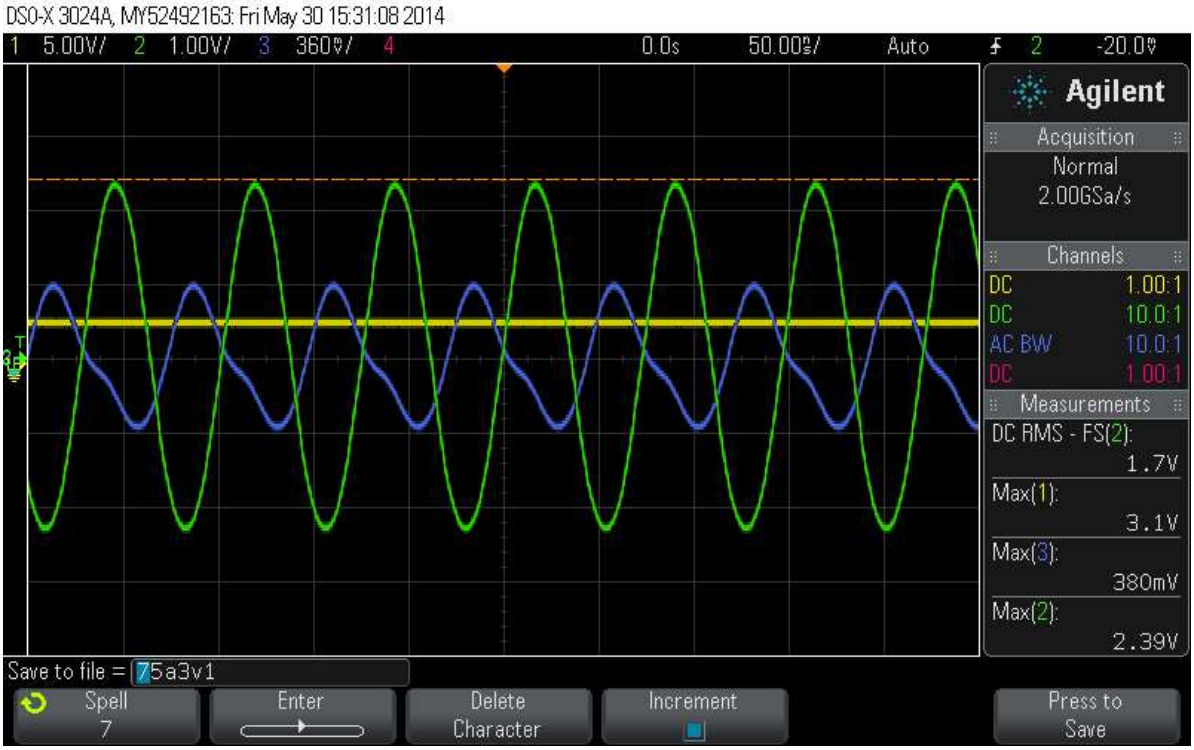

Figure 3.12: Screenshot

If the magnetic field strength is increased a smaller value of R2 is needed to obtain the same DC voltage measured in CON3.

Later on, the jumper J1 was switched to position 'c' and an external source of voltage was connected in CON2 as shown in 3.13. Now the load of the PICC is modified using CON2 and the DC voltage is measured at CON3.
The voltage in CON2 is modified until the desired voltage of 3V or 6V is reached in CON3. The different values of the adding voltage and noted.

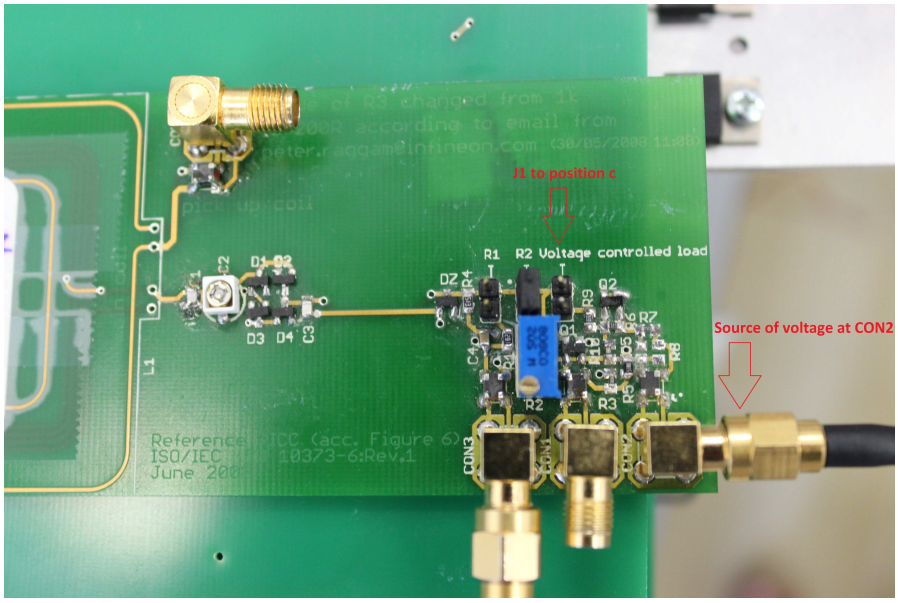

Figure 3.13: Test setup

The next figure shows the measurements done.

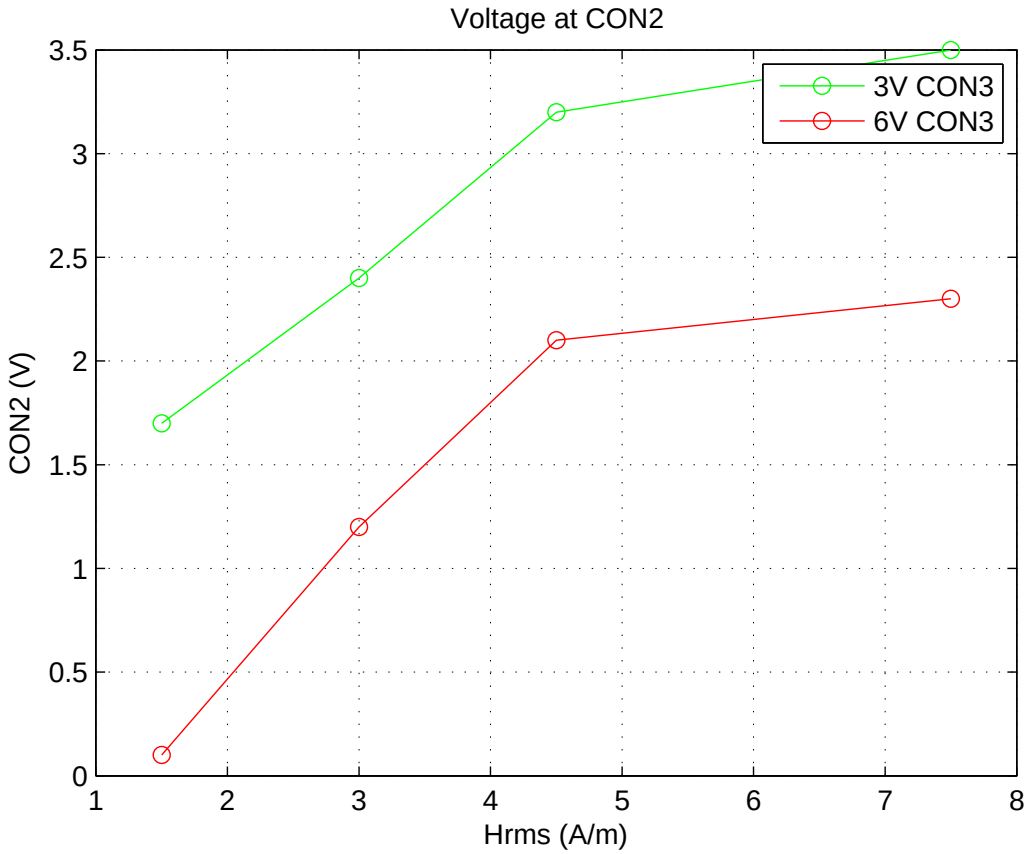

Figure 3.14: CON2 values for different magnetic field strength

When the magnetic field strength is increased the voltage at CON2 should also be increased in order to get the same voltage (3V or 6V) at CON3.

Chapter 4

Conclusion and Outlook

This thesis covers the analysis of non linear behavior of class 1 PICCs according to standard ISO 14443. It has been shown how the variation of some components affects the input voltage, input current and DC voltage of the card.
In the reference circuit used for measurements DC-output voltages of the rectifier do not have a reference to ground. They are pulsating in common mode with 13.56MHz. In order to improve the measurements, active differential probes could be used in further times to measure the DC voltage and the input current of the DUT. With these probes results should have best noise performance and the least parasitic capacitance. It was also noticeable from the Fast Fourier Transform (FFT) analysis that the harmonics grow when the input power is increased.

It was mention in the beginning that the load modulation wouldn't be included in this work. After having analyzed the power supply of the PICC the next logical step would be to introduce in simulation as well as in measurements the components corresponding to the load modulation and analyze how the card communicates with the reader.

On the other side, a test using the PCD assembly was performed in 3.2. To make sure what could we expect from this emulator and also continue the track of this work comparing simulation and measurement, it would be a good idea to simulated the PCD assembly in ADS and compare it with the measurement results. For this purpose, the coupling factor between the PICC coil and the PCD coil should be known and the losses due to the measurement devices, such as amplifiers and attenuators, should be considered.
As the load modulation was not included only PICC tests defined in ISO 10373-6 have been accomplished although the effects of load modulation should be also included in future works.

List of Figures

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