Diplomarbeit

Atomically thin transistors

ausgeführt durch

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Abstract

WSe_2 and MoS_2 belong to the family of transition metal dichalcogenides (TMDCs). These materials can be reduced to one single layer by the so-called Scotch tape technique. This mechanical exfoliation procedure is possible because TMDC crystals consist of a stack of layers. While the interlayer bonds are strong, the van der Waals forces that hold together the layers forming the bulk crystal are weak. WSe_2 and MoS_2 have band gaps in the 2.0 eV and 1.9 eV range, which makes them a suitable complement to graphene, the most common 2-D material, which lacks this band gap. As the band gap is a crucial property for switching in semiconductor circuitry, scientists find these TMDCs very attractive for building such electronic devices as transistors.

A very limiting factor in the performance of nano-structured devices is their contact resistance. A comprehensive understanding of metal 2-D crystal interfaces, which primarily determine the contact resistance, is essential for improving 2-D crystal-based electronics and using them as next-generation semiconductor technology.

For this reason, WSe_2 as well as MoS_2-based transistors were fabricated and electrically measured within the framework of this master thesis. Raman and photoluminescence spectroscopy were used to determine the thickness of the TMDC flakes that served as transistor channel. The results of these measurements suggest that transistor P1 has a bulk piece of WSe_2 as channel, while the channel of transistor P2 is a monolayer of the same material. In addition, Schottky barrier heights were extracted from temperature-dependent measurements. They were 0.12 eV and 0.0445 eV, respectively, for transistors P1 and P2, which is fully in line with results reported in the pertinent literature. The MoS_2-based transistors were contacted with MoO_x, a novel contact material. The transistors showed n-type transistor behaviour. The characteristic output curve of such transistors suggests ohmic contacts resulting in maximum currents of 258 nA.

Kurzfassung

WSe_2 und MoS_2 gehören zur Gruppe der Übergangsmetal-Dichalcogenide. Diese in der Natur in kristalliner Form vorkommenden Verbindungen bestehen aus übereinander gestapelten Einzellagen. Sie können mit der Scotch Tape Methode mechanisch exfoliert werden, weil zwischen den Lagen nur schwache Kräfte wirken, jedoch innerhalb einer Atomlage kovalente Bindungen, sogenannte van der Waals Kräfte, für eine starke Bindung sorgen. WSe_2 und MoS_2 haben Bandlücken im Bereich von 2.0 eV und 1.9 eV, was sie zu einer guten Ergänzung für Graphen, das meist verbreitete 2-D Material, macht, dem diese Bandlücke fehlt. Weil die Bandlücke ein entscheidendes Element für das Schalten von elektronischen Bauteilen in der Halbleiterschaltungstechnik ist, begannen Wissenschaftler, elektronische Bauteile wie Transistoren aus diesen Übergangsmetal-Dichalcogeniden zu bauen.

Ein sehr limitierender Faktor in der Nanoelektronik ist der Kontaktwiderstand der verwendeten Bauelemente. Ein umfassendes Verständnis des Kontaktes zwischen einem Metall und einem 2-D Kristall ist deshalb entscheidend, um die auf diesem Material basierende Elektronik zu verbessern und sie als zukünftige Halbleitertechnologie zu verwenden.

Folglich wurden im Rahmen dieser Masterarbeit WSe_2 sowie MoS_2 Transistoren hergestellt und elektrisch vermessen. Die Dicke der Dünnschichten, welche als Transistorkanal verwendet wurden, wurde mittels Raman und Photolumineszenz bestimmt. Die Resultate dieser Messungen lassen darauf schließen, dass es sich bei dem Kanal in Transistor P1 um ein dickes Stück WSe_2 handelt, während der Kanal in Transistor P2 aus einer Einzellage dieses Materials besteht. Außerdem wurden temperaturabhängige Messungen vorgenommen, mit deren Hilfe die Schottky Barrieren Höhen abgeleitet wurden. Diese ergaben sich zu 0.12 eV und 0.0445 eV im Falle von Transistor P1 und P2, was mit den in der Fachliteratur angeführten Ergebnissen übereinstimmt. Die auf MoS_2 aufgebauten Transistoren wurden mit MoO_x, einem neuartigen Material, kontaktiert. Die Transistoren

zeigten n-Typ Transistorverhalten. Die Ausgangskennlinie lässt auf ohmsche Kontakte schließen, mit maximalen Strömen von 258 nA.

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1 Introduction and Motivation

The first theoretical studies on graphene were carried out more than 60 years ago. At that time, this crystalline allotrope was not considered to be stable in free state [1]. However, in 2004, Novoslev and Geim from the University of Manchester, UK, incidentally found graphene on the adhesive side of scotch tape [2]. This opened up a new field of research around the topic of two-dimensional crystals and constituted a milestone in scientific history, which the Nobel Committee honoured by awarding the Nobel Prize in Physics to Novoslev and Geim in 2010.

Graphene is the first two-dimensional crystal to be produced mechanically. It has extraordinary mechanical, electric [3, 4] and magnetic [5] properties, which make it a very promising material for novel applications in electronics, signal processing, energy storage, solar energy conversion and optoelectronics. Per definition, most of the semiconductors currently used in these research fields have a band gap. As single-layer graphene lacks this band gap, it is considered a semimetal. This means that it has no band gap between the valence and conduction bands, a property that is crucial for switching in semiconductor circuitry. In view of this shortcoming, scientists have searched for new two-dimensional compounds which are stable under ambient conditions but do not lack the band gap.

For example, the monolayered form of Tungsten diselenide (WSe_2) has a semiconductor-like band structure and a band gap of 1.35 eV [6]. This also holds true for molybdenum disulfide (MoS_2), which has a band gap of 1.2 eV [7]. Both of these materials are transition metal dichalcogenides (TMDCs). In particular the monolayered forms of these compounds have been intensively studied as their large carrier mobility [11], high current-carrying capacity [12], electrostatic coupling [7] and strong absorption in the visible frequency range [13], along with their chemical and mechanical stability, make them promising candidates for

use in electric applications [9, 10]. Single layers of bulk TMDC crystals can be obtained by mechanical exfoliation, because TMDCs typically have many single layers of their specific compound stacked on top of each other and held together by weak Van der Waals forces [8]. Using the so-called "scotch tape method", a bulk crystal can be put between two stripes of adhesive tape and cleaved numerous times until the thickness of the crystal has reached the nanometre regime. The atomically thin layers of single crystal can then be transferred to a substrate, which makes it easy to locate them, measure their physical properties or process them into different electrical components.

Since MoS_2 can be grown by chemical vapour deposition (CVD) [14, 15, 16, 17], it became a promising candidate for such practical applications as light-emitting devices that need high-quality, continuous, large-area thin films. The hole injection required in addition to the conventional electron injection in MoS_2 currently constitutes a challenge in this field of research. In order to be able to establish the necessary relation between the band structure of the 2-D material and the work function of the metal contact, we need high work function materials for contacting the 2-D material.

Another very limiting factor in the performance of nano-structured devices is their contact resistance [18]. Hence, a comprehensive understanding of metal 2-D crystal interfaces is essential for improving 2-D crystal-based electronics and using them as next-generation semiconductor technology. When such an interface is formed, a Schottky barrier describes the electric potential at this very interface. The so-called Schottky barrier height determines the electric behaviour of the contact. A temperature-dependent electric measurement can be used to investigate this physical property [19] and can deepen our understanding of the physical mechanisms governing the behaviour of 2-D crystal-based devices.

The aim of this master thesis was to build WSe_2 back-gated transistors and investigate the Schottky barrier height between the two-dimensional semiconducting material and the metal contact by using a temperature-dependent measurement. Moreover, I used high work function metal contacts to fabricate MoS_2 transistors in order to examine if hole injection can be achieved in the way described by other groups [20].

2 Theoretical Background

2.1 Introduction to transition metal dichalcogenides

In the late 1960s, there was a growing interest in the structural, optical, electrical, magnetic and superconducting properties of layered transition metal dichalcogenide compounds [24]. In 1969, Yoffe et al. [23, 22] studied their electrical, structural and optical properties. First theoretical semi-empirical models [23] for the band structure of TMDCs were based on the idea that their physical properties are governed by their two-dimensional structure [25, 26, 27]. Hence it does not come as a surprise that scientists fabricated the first TMDC-based field effect transistor [28] soon after the scotch tape method had been discovered.

TMDCs can be described by the chemical formula MX_2, where M is a transition element and X is a chalcogen [23]. Various combinations of these elements yield 40 different compounds, but not all of them are layered solids [29]. Weak van der Waals forces exist between the MX_2 layers, which can move effortlessly relative to each other. Hence, some TMDCs already have a long history as dry lubricant for both domestic and industrial purposes, e.g., for fixing squeaky door hinges. Due to such physical effects as quantum confinement or changes in symmetry [30, 31], the electrical properties of semiconducting TMDCs vary strongly with the number of their layers.

2.1.1 Crystal Structure

The transition metal elements from group IV (Ti, Zr, Hf, etc.), group V (e.g., V, Nb or Ta) and group VI (Mo, W, etc.) as well as certain elements from the group of chalcogens (S, Se or Te) are among the materials that form layered compounds of the X-M-X type, in which the chalcogen atoms in two hexagonal planes are separated by a plane of metal atoms (see Figure 2.1).

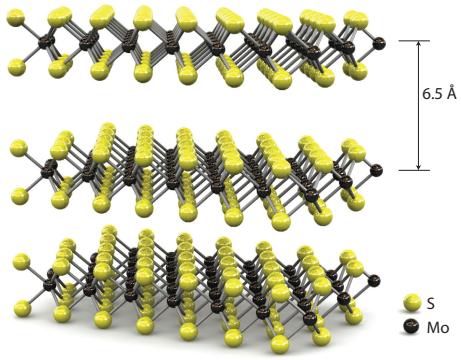

Figure 2.1: Typical crystal structure of a transition metal dichalcogenide compound. Source:[7].

The stacking order and the coordination of the bordering layers determine which polytype the crystal forms in its bulk structure. The metal atoms within the crystal structure have trigonal prismatic or octahedral coordination. As shown in Figure 2.2, the TMDCs' crystal structure symmetry usually is either rhombohedral or hexagonal. The lattice constants for the two TMDCs WSe_2 and MoS_2 are 3.28Å and 3.16Å, respectively [46].

2.1.2 Band Structure

Tight-binding and first principal approximations [33] as well as spectroscopic measurements [30, 32] show that the electronic band structures of the different TMDCs do not differ much in their general features. Unlike transition metal dichalcogenide compounds that include the transition metals niobium (Nb) and tantalum (Ta) (i.e., NbX_2 and TaX_2), molybdenum and tungsten-based

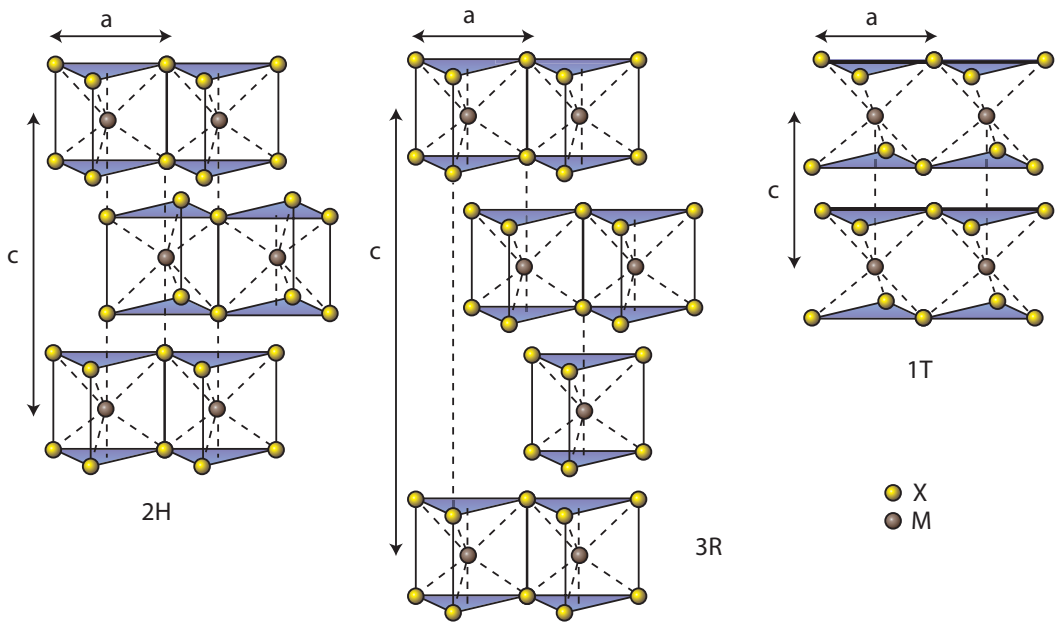

Figure 2.2: Rhombohedral and hexagonal crystal structures of TMDCs. Source:[9].

compounds (i.e., MoX_2 and WX_2) clearly show semiconducting behaviour. Figure 2.3 and Figure 2.4 depict the band structures calculated from first principles for two different TMDCs in their bulk- and monolayered forms. They clearly demonstrate that the band gap transition at the τ-point changes from an indirect transition in bulk material to a direct transition in monolayer material, while the direct excitonic transition at the K-point hardly changes with the number of layers. The electronic distributions are spatially correlated to the atomic structure [32]. TMDC compounds of the MoX_2 and WX_2 type are assumed to share a comparable indirect to direct band gap transformation with descending layer numbers, with band gap energies ranging from 1.1 to 1.9eV [33, 34]. The fact that silicon (nowadays mainly used for digital transistors) has a band gap of 1.1 eV and most semiconducting TMDCs have similar band gap energies in their bulk- and monolayered forms, highlights the great potential of TMDCs as digital transistors [35].

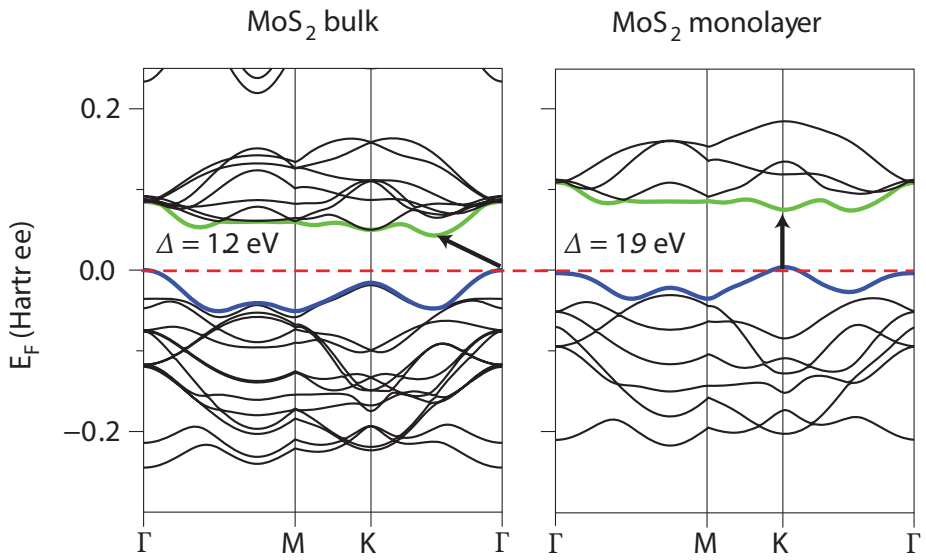

Figure 2.3: Band structure of MoS_2 created by first principle calculations. Source:[9].

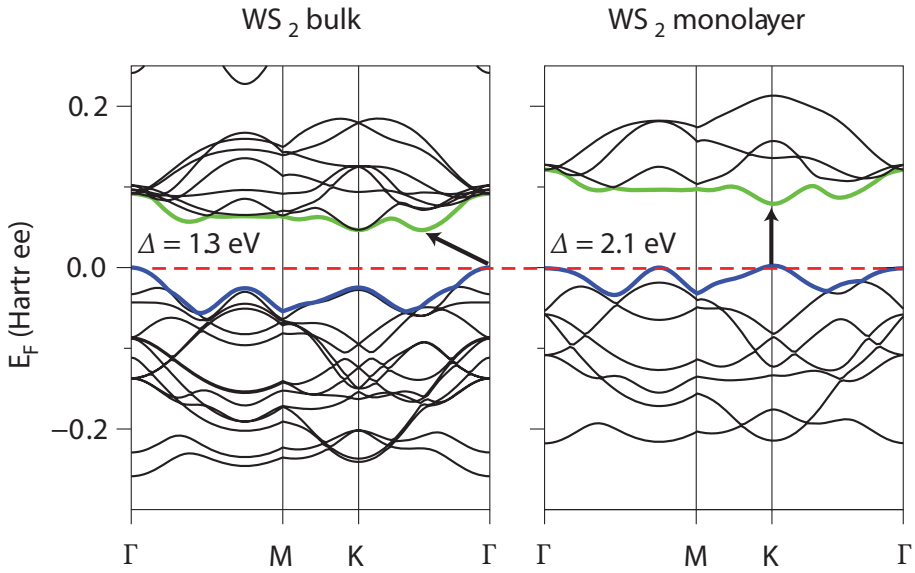

Figure 2.4: Band structure of WS_2 created by first principle calculations. Source:[9].

2.1.3 Effective Mass

Effective mass is a quantity that has the same dimensions as mass in the classical sense. It is helpful when describing the properties of quasiparticles. An electron in the conduction band of a crystal structure that is subjected to an external force f, for example by an applied electrical field E, can be described as the motion of a free electron experiencing the same force but possessing a different mass, i.e., the effective mass m^*. The interaction of the electron with the surrounding crystal lattice is taken into account by the difference between m and m^*.

Let an external force f be applied to a band electron. The force will do work

$$\delta E = f v \delta t \tag{2.1}$$

in time δt with $v = \frac{\mathrm{d}\omega}{\mathrm{d}k}$. Additionally,

$$\delta E = \frac{\mathrm{d}E}{\mathrm{d}k}\delta k = \hbar v \delta k \tag{2.2}$$

When these two formulas are equated and divided by δt and the limit $\delta t \to 0$ is taken into account, we get the expression

$$\hbar \frac{\mathrm{d}k}{\mathrm{d}t} = f \tag{2.3}$$

We can write the equivalent more dimensional as

$$\hbar \frac{\mathrm{d}\vec{k}}{\mathrm{d}t} = \vec{f} \tag{2.4}$$

where $\vec{k}$ and $\vec{f}$ now denote vectors. Equation 2.4 clearly shows that in a crystal $\hbar\frac{d\vec{k}}{dt}$ is equal to the external force on an electron. The change in velocity over time can be expressed as follows:

$$\frac{\mathrm{d}v}{\mathrm{d}t} = \frac{1}{\hbar}\frac{\mathrm{d}^2E}{\mathrm{d}k\mathrm{d}t} = \frac{1}{\hbar}\frac{\mathrm{d}^2E}{\mathrm{d}k^2}\frac{\mathrm{d}k}{\mathrm{d}t} \tag{2.5}$$

Substituting $\frac{\mathrm{d}k}{\mathrm{d}t}$ from equation 2.4 and rearrangement yields

$$\frac{\hbar^2}{\frac{\mathrm{d}^2E}{\mathrm{d}k^2}}\frac{\mathrm{d}v}{\mathrm{d}t} = m^*\frac{\mathrm{d}v}{\mathrm{d}t} = f \tag{2.6}$$

where the effective mass m^* is defined by

$$m^* = \hbar\frac{\hbar^2}{\frac{\mathrm{d}^2E}{\mathrm{d}k^2}} \tag{2.7}$$

Equation 2.6 shows that the concept of the effective mass is a convenient way for describing band electrons that experience an external force, because we can use the identity $F = ma$ by simply substituting the inertial mass with m^*. In general, the direction of acceleration of an electron in a crystal lattice is not parallel to the external force f. In fact, acceleration may even be antiparallel to f, i.e., a negative effective mass. Because the properties of electrons with negative effective mass greatly differ from those of ordinary particles, holes are usually described as quasiparticles which have a positive charge and a positive effective mass.

A paper published in 2013 reported that the effective mass of electrons and holes for different TMDC alloys was calculated with the help of first-principles calculations by applying the supercell method and effective band approximation [41]. Figure 2.5 shows that for MoS_2 and WS_2 the effective mass of holes is larger than that of the electron.

2.1.4 Photoluminescence

Photoluminescence (PL) is the spontaneous emission of light by an optically excited material. PL is measured to investigate discrete states of electrons,

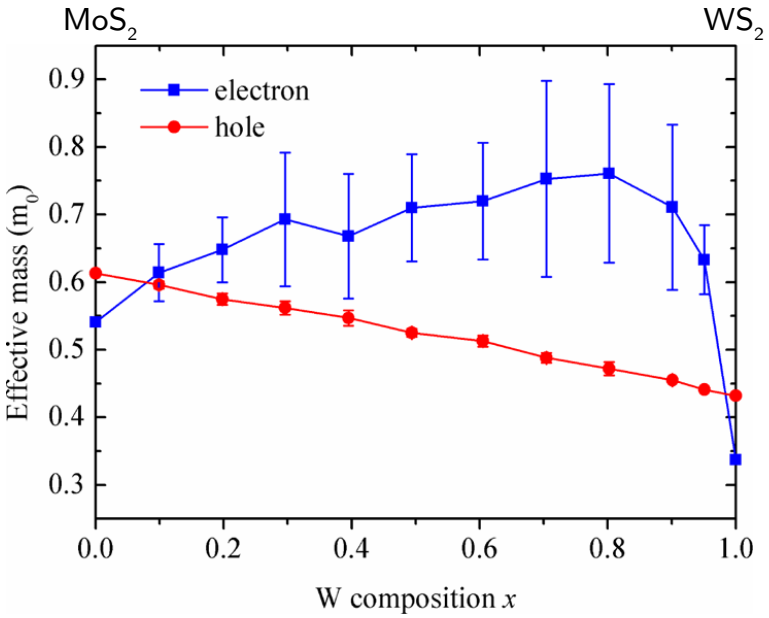

Figure 2.5: Calculated composition-dependent effective masses of electrons and holes for $W_xMo_{1-x}S_2$ monolayer alloys. Red circles represent the effective mass of electrons, while the blue squares represent that of electrons. m_0 is the bare electron mass which constitutes m_e with the deviation described in chapter 2.1.3. Source:[41].

for example in a semiconductor, in a non-invasive, selective and extremely sensitive way. Materials have characteristic emission spectra. Their analyses can be helpful not only for identifying surface, interface and impurity levels but also in estimations about alloy disorders or interface roughnesses. The fundamental limitation of the significance of PL measurement is its dependence on the investigated material's radiative efficiency. In case of low-quality indirect band gap semiconductors, which have a poor radiative efficiency, characterisation with ordinary PL is difficult. A good way to increase the radiative response of a material is to illuminate the sample at its resonant frequency. Hence a photoluminescence excitation measurement (PLE) can be used to investigate the frequency that produces the highest yield of reemitted photons. Compared to an ordinary PL spectrum, this yields a superior signal-to-noise ratio.

Figure 2.6 shows a schematic sketch of a typical setup for PL measurements. A laser is used as monochromatic light source, which is focused on the sample. An optical lense assembly directs the emitted light beam to a spectrometer. Inside the spectrometer, a grating reflects the incoming light in frequency-dependent angles. This yields an intensity pattern that can be read out by a charge-coupled device (CCD) sensor.

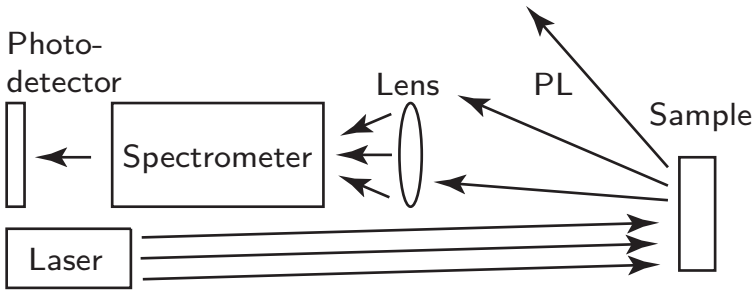

Figure 2.6: Schematic sketch of a typical PL setup.

Figure 2.7 illustrates the mechanisms underlying PL in a semiconductor. In picture (a), an electron is excited by an incoming photon, which has the energy $E = h\nu$. In picture (b), the valence electron is lifted up into the conduction band. This corresponds to the creation of an electron hole, i.e., an unoccupied state in the valence band. In picture (c), the excited electron in the conduction band

relaxes to the lower edge of the conduction band by emitting a phonon of the energy $E = \hbar kc$. Picture (d) shows the formation of an excitation, i.e., a bound state of an electron and a hole held together by the electrostatic Couloumb force. The exciton-binding energy constitutes the excessive energy the electron needs to emit in form of another phonon of the energy $E = \hbar k'c$ in order to occupy the energetically lower state within the exciton. This state lies within the band gap of the semiconductor, as shown in Figure 2.7d. In picture (e), the electron recombines with the hole it formed the exciton with and emits a photon with a characteristic wavelength corresponding to the energy $E = h\nu'$.

2.1.5 Raman Spectroscopy

Arthur Holly Compton's discovery of the effect named after him, for which he also received the Nobel Prize in 1927, led Sir Chandrasekhara Venkata Raman to investigate if the novel effect found for X-rays also applied to visible light. He therefore conducted an experiment, in which he used a mercury arc lamp as a monochromatic light source that shone on transparent material and set up a spectrograph behind the penetrated material to record the allegedly scattered light. In addition to the well-known lines of the monochromatic light source he detected slightly shifted lines, which he called Raman lines. He presented his findings at a scientific meeting held in Bangalore, India, in 1928 [45]. Two years later, he was awarded the Nobel Prize in physics for his work on the scattering of light and the discovery of the Raman effect.

Nowadays, the monochromatic light source usually is a laser. When interacting with the sample, the light is inelastically scattered, which results in a frequency change of the absorbed and then reemitted photons. The frequency shift of the reemitted photon contains information about vibrational, rotational and other low-frequency transitions in molecules. This Raman effect can be used to study gaseous, liquid and solid samples and is based on molecular deformations in an electric field E determined by molecular polarisability α, where the laser beam can be regarded as an oscillating electromagnetic wave with an electric vector E. By interacting with the sample, it induces an electric dipole moment P = α E, which causes the deformation of the molecules. This deformation happens

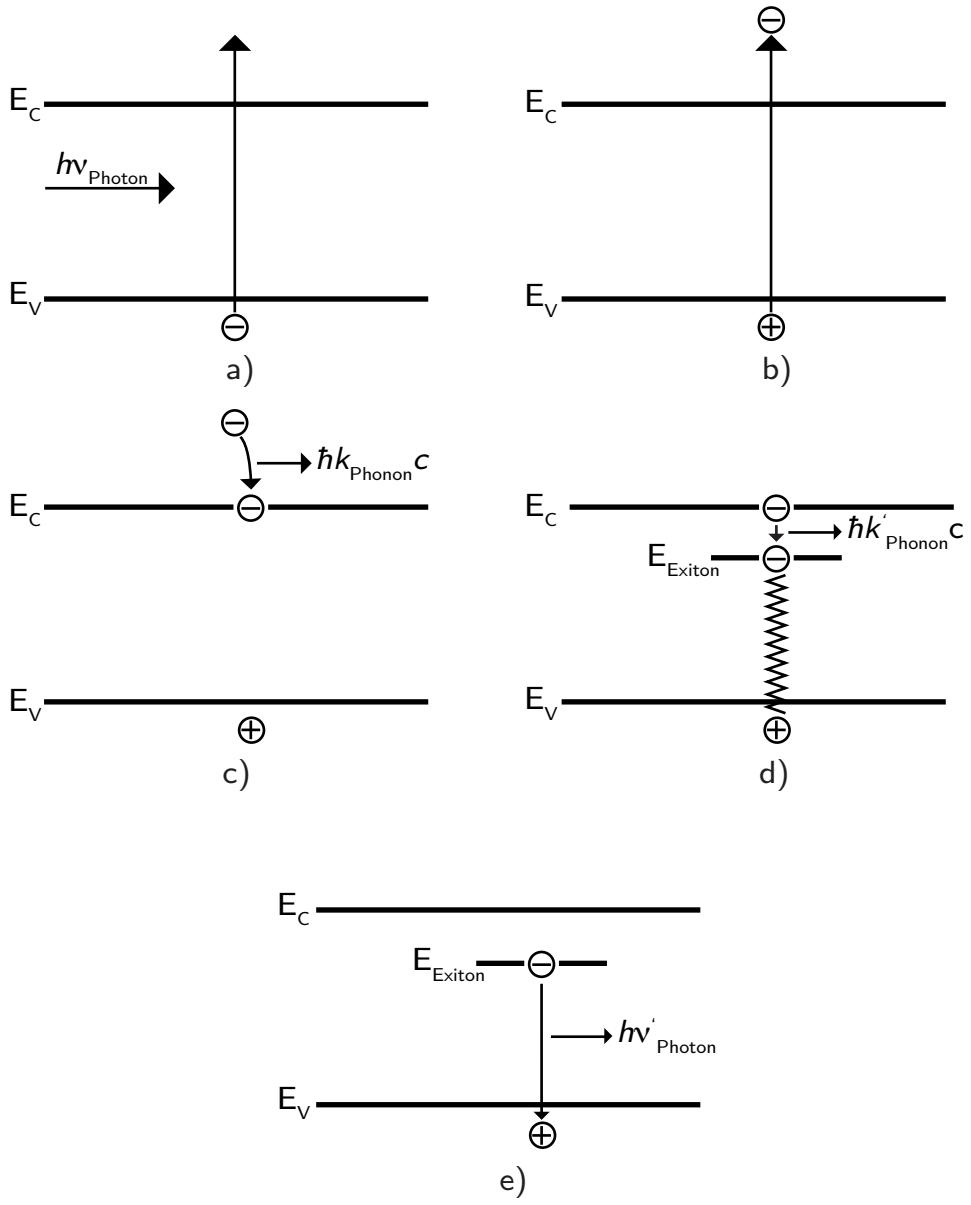

Figure 2.7: Schematic sketch of the mechanism underlying the creation of a PL signal originating from the radiative recombination of an exciton. (a) Incoming photon penetrates semiconductor. (b) Valence electron is excited into the conduction band and leaves a hole in the valence band. (c) Electron relaxes to the lower edge of the conduction band by emitting a phonon. (d) Electron forms an exciton with a hole by emitting another phonon of the exciton-binding energy. (e) Electron recombines with the hole it formed the exciton with by emitting a photon.

periodically and the molecules start to vibrate with a characteristic frequency ω_0. In other words, the monochromatic laser source with a frequency ω_0 excites a molecule and transforms it into an oscillating dipole. The amplitude of this oscillation is called nuclear displacement. Such an oscillating dipole can emit light at three different frequencies.

In the first case, a photon with the energy $\hbar\omega_0$ gets absorbed by a molecule with no Raman-active modes . Hence the light is once more emitted at the frequency ω_0. The molecule is excited to a so-called virtual state E_{virt} by the photon and relaxes back to the basic vibrational state E_0 it started from. This mechanism is called elastic Rayleigh scattering.

In the second case, the light quantum gets absorbed by a molecule with Raman-active modes at the very moment of the interaction when the molecule is in its basic vibrational state E_0. A certain part of the photon's energy is transferred to the Raman-active mode which has the frequency ω_r. This changes the so-called Stokes (frequency) of the scattered light $\omega_0 - \omega_r$.

In the third case, monochromatic light gets absorbed by a molecule with Raman-active modes at the very moment of the interaction when the molecule is in an excited vibrational state . The molecule is excited by the energy of the photon $\hbar\omega_0$ but relaxes back to its basic vibrational state ω_0. As a result, the frequency of the scattered light increases to $\omega_0 + \omega_r$. This frequency is called anti-Stokes frequency.

Approximately 99.999% of all incident photons in spontaneous Raman undergo elastic Rayleigh scattering. Because this scattering mechanism does not contain any information about the object of investigation, it is useless for molecular characterisation. Only around 0.001% of the incident light produces an inelastic Raman signal with frequencies $\omega_0 \pm \omega_r$. Because Rayleigh scattering is so dominant, instruments like notch filters, tuneable filters and laser stop apertures are used to achieve high-quality Raman spectra.

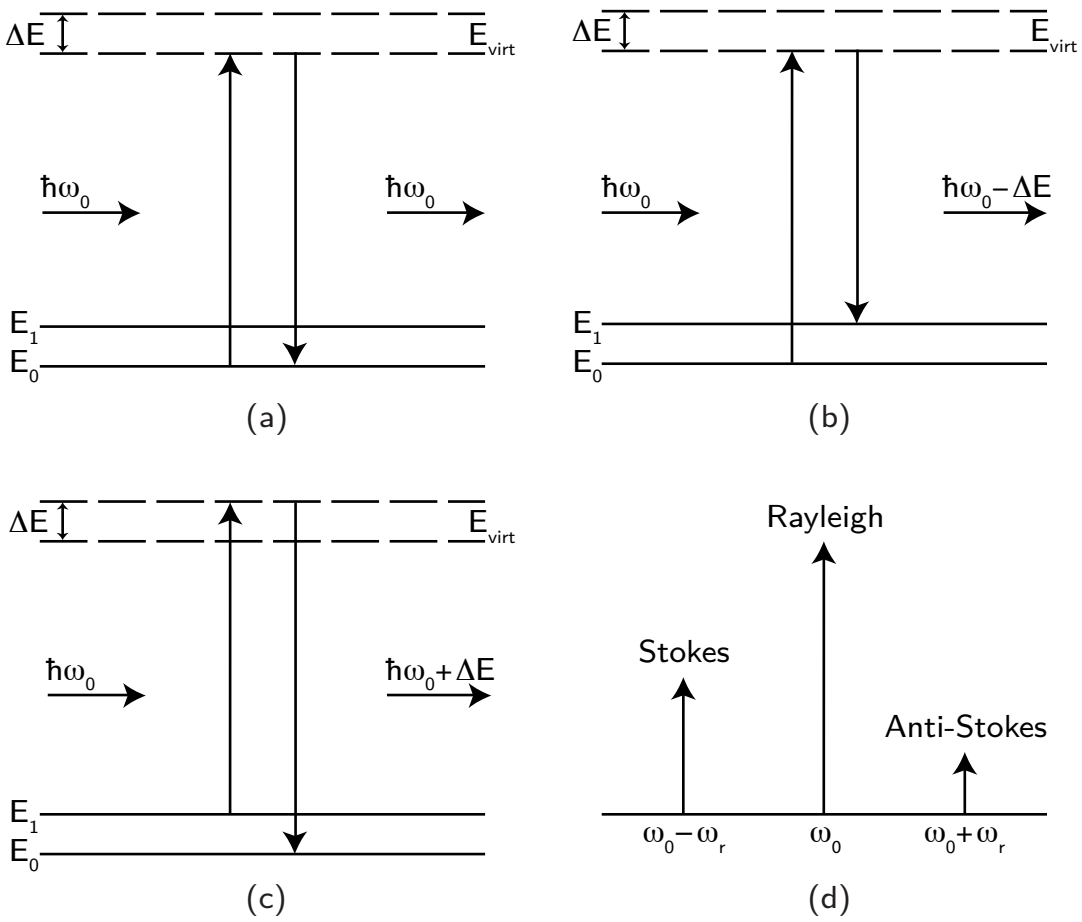

Figure 2.8: (a) Principle of Rayleigh scattering. (b) Principle of Stokes shift. (c) Principle of anti-Stokes shift. (d) Illustration of the frequency shift of Stokes and anti-Stokes relative to the Rayleigh line and their intensity distribution.

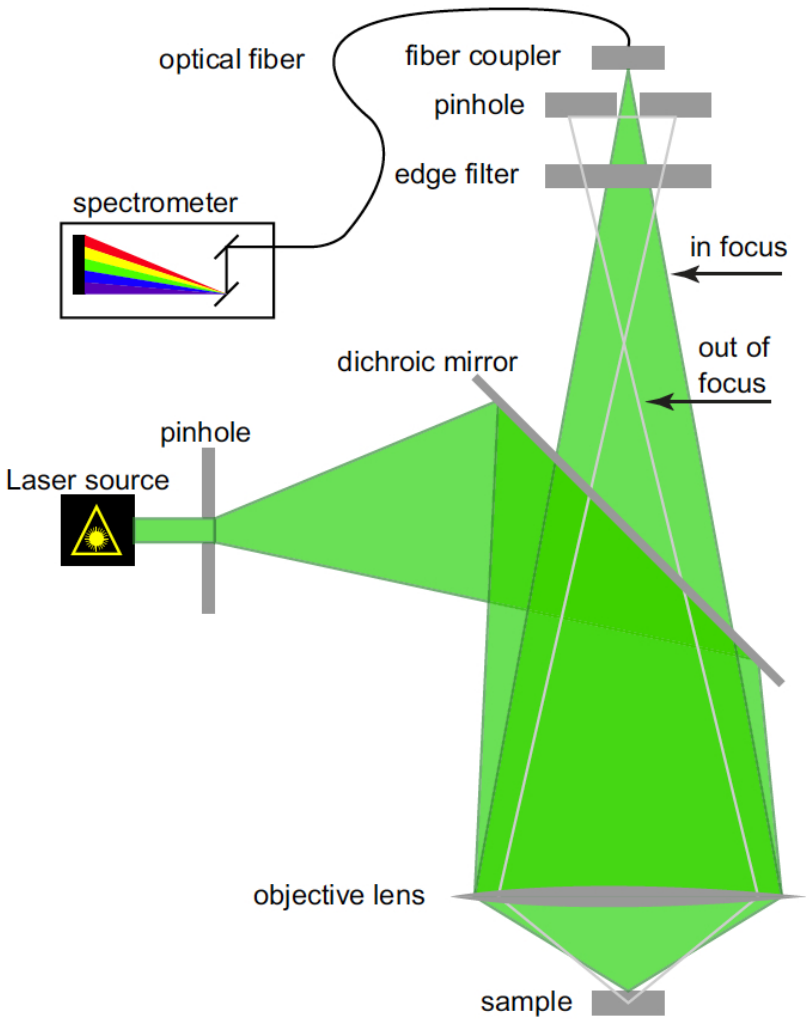

Figure 2.9: Illustration of a confocal Raman setup. Source:[57].

2.2 Field effect transistors

The metal-oxide-semiconductor field-effect transistor (MOSFET) has been used in electronic circuitry since the 1970s. Its huge advantage over former types of transistors is the fact that MOSFETs can be made very small and thus occupy much less space on an integrated circuit chip. Around the same time, Moore's law was established. It claims that in the history of computing hardware the number of transistors on an integrated circuit doubles every two years. Because all digital circuits such as microprocessors and memories can be designed without using any resistors or diodes by solely employing MOSFETs, they play a key role in all modern digital applications. In a MOSFET, the current is controlled by an electric field applied perpendicular to the surface of the semiconductor as well as by the direction of the current. By exploiting the field effect (i.e., the modulation of the electrical conductivity of a material by the application of an external electric field) the current flow over the MOSFET can be controlled.

Figure 2.10 shows a simplified cross-section of a typical n-type MOSFET. It comprises a source and a drain area and two strongly n-doped semiconductor regions. The current in a MOSFET is the result of the charge flow in the p-type area bordering the gate oxide that separates the gate from the semiconductor. This area next to the oxide-semiconductor interface is called channel region. The length of the channel in standard integrated circuit MOSFETs is less than 1 μm and the oxide thickness of the gate oxide layer is typically in the order of 400 Å or less.

If no bias voltage is applied to the gate, the source and drain terminals are separated by the p-region, which is equivalent to two back-to-back diodes, and no current can flow over the transistor. If the applied gate voltage exceeds a certain threshold voltage, an electron inversion layer (channel) is formed at the oxide-semiconductor interface. It connects the n-source and n-drain areas (see Figure 2.10). If a voltage is applied between source and drain, electrons can flow through the channel. Because these charge carriers are electrons, this type of transistor is called n-channel MOSFET. The magnitude of the flowing current depends on the amount of charge carriers in the inversion layer, which is a function of the applied gate voltage. When a positive gate voltage is applied, a

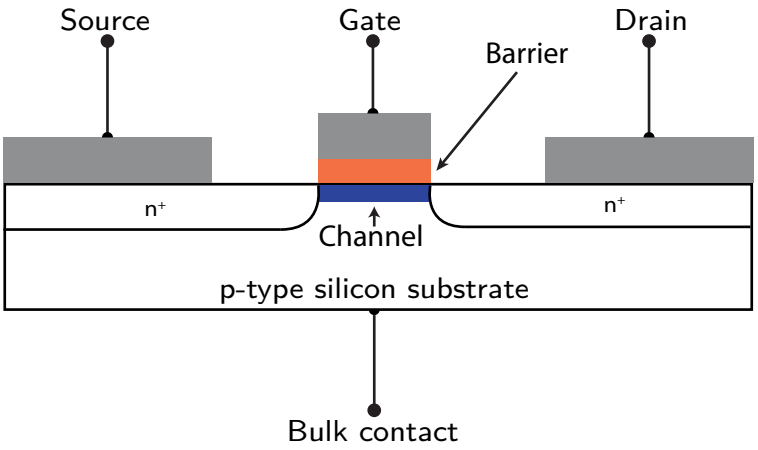

Figure 2.10: Cross-section of a MOSFET device.

reverse-biased drain-to-substrate pn junction is formed, which causes a current flow through the channel and not through a pn junction. The isolating gate oxide prevents any leakage current through the gate terminal.

Figure 2.11a shows the basic characteristic output curve of a MOSFET for small values of V_{ds}. When the applied gate voltage V_{gs} is smaller than the threshold voltage V_{th}, no drain current can be observed. When V_{gs} exceeds V_{th}, the channel inversion charge is formed and the drain current is directly dependent on V_{ds}. Area A in Figure 2.11b shows an example for small values of V_{ds}. In this case, the drain current is basically constant along the entire channel length. Area B shows the behaviour of the characteristic output curve for increased V_{ds}, which causes a decreased voltage drop across the oxide near the drain terminal. This is equivalent to a diminution of the induced inversion charge density near the drain. This, in turn, decreases the incremental conductance of the channel at the drain. As a result, the slope of the characteristic output curve declines. Area C, called saturation region, shows how the transistor behaves if V_{ds} increases even more. Then the potential difference across the oxide at the drain terminal reaches the value of V_{th}. This sets the induced inversion charge density at the drain terminal as well as the incremental channel conductance to zero, hence the slope of the characteristic output curve also becomes zero.

This leads to the following relation:

$$V_{gs} - V_{ds}(sat) = V_{th} \tag{2.8}$$

Figure 2.11 shows a set of characteristic output curves for an n-channel MOSFET. It demonstrates that the increase of gate voltage V_{gs} leads to an increase in maximum device current.

The ideal current-voltage characteristics in the region on the left side of the dashed line are described by the equation

$$I_{ds} = K_n(2(V_{gs} - V_{th})V_{ds} - V_{ds}^2) \tag{2.9}$$

In the saturation region on the right side of the dashed line, the ideal current-voltage characteristics are described by the equation

$$I_{ds} = K_n(V_{gs} - V_{th})^2 \tag{2.10}$$

Since the ideal drain current is independent of V_{ds} in the saturation region, the incremental resistance is infinite, which can be described by the expression

$$r_0 = \left.\frac{\Delta V_{ds}}{\Delta I_d}\right|_{V_{gs}=\text{const.}} = \infty \tag{2.11}$$

The conduction parameter K_n for the n-channel device is given by the equation

$$K_n = \frac{W\mu_n C_{ox}}{2L} \tag{2.12}$$

where μ_n is the mobility of the electrons in the inversion layer and W and L are the width and the length of the channel. The variable C_{ox} is the oxide capacitance per unit area, which is calculated as follows:

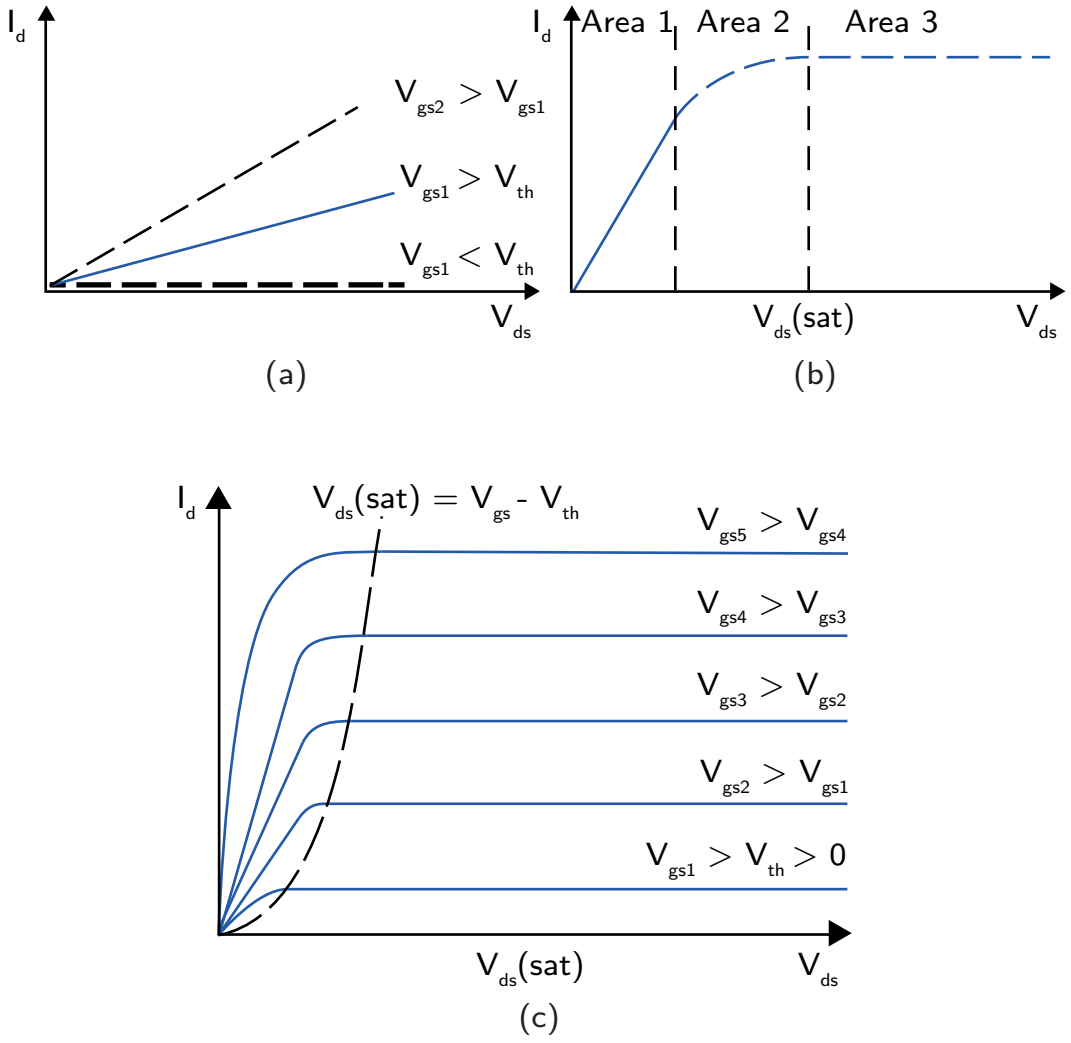

Figure 2.11: (a) Characteristic output curve of a MOSFET for small values of V_{ds}. (b) Area A and B illustrate the behaviour of a typical MOSFET for small and increased V_{ds} voltages, respectively. Area C shows the saturation region, when V_{ds} is increased even more. (c) Illustration of the behaviour of a typical MOSFET for different gate voltage V_{gs}.

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \tag{2.13}$$

where t_{ox} stands for the oxide thickness and ϵ_{ox} for the oxide permittivity. Equation 2.12 indicates that the conduction parameter is dependent on both the electrical and geometrical parameters. The wish to obey Moore's law in the future led scientists to search for new semiconducting materials for building transistors. Silicon-based transistors are about to reach their limits in terms of physical dimensions as it is impossible to further reduce their size. In addition to small dimensions, other desirable characteristics of next generation transistors would be high charge carrier mobilities for fast operation, high ON/OFF ratios ($10^4 - 10^7$), high conductivities, low off-state conductances for low power consumption during the operation as well as low fabrication costs. With a tuneable direct bandgap in the range of $1 - 2eV$ in their monolayered form, TMDCs have a property that is crucial for high ON/OFF ratios. Moreover, they are expected to have high mobility values of $200cm^2V^{-1}s^{-1}$ at room temperature. In combination with the high mechanical stability and transparency of monolayered TMDCs, these properties make them a promising candidate for next generation transistor technology.

2.2.1 Atomically thin transistors

In many respects, TMDC-based transistors behave in a similar way to MOSFETs [7]. These atomically thin film transistors can be made of various TMDCs, for example MoS_2, WSe_2, $MoSe_2$ or WS_2. By mechanically exfoliating their bulk crystals or growing them on a metal using chemical vapour deposition (CVD) and subsequent transfer, these atomically thin layers can be placed on a substrate. CVD grown TMDC nanolayers directly on a substrate have been reported as well [54]. By different lithography methods (see chapter 3.3) metal contact pads can be formed on both sides. This makes the atomically thin layer act like a conduction channel. If a TMDC is transferred on a SiO_2 layer that is grown on a silicon substrate, the transistor can be back-gated by using the SiO_2 layer as a dielectricum. A second fabrication model is to deposit a dielectric layer, for example HfO_2, on top of the semiconduction layer. As this dielectric

layer is topped by a third metal contact pad, a gate voltage can be applied. Both configurations are shown in Figures 2.12a and b, respectively. Two great advantages of the top-gated transistor configuration are that transistors on one substrate can be controlled individually and that top-gated transistors have shown higher mobilities [7] than back-gated transistors. This makes them more suitable for practical devices.

In both device configurations, the device current is directly dependent on the applied gate voltage. For example, when a positive gate voltage is applied, the Fermi level in the semiconductor together with its conduction band lower edge and valence band upper edge is shifted more downwards leading into more electrons, which can contribute to the device current. For example, the band gap of intrinsic MoS_2 has a value of $1.8eV$, which is very large and makes it a promising candidate for devices that benefit from high on/off ratios, e.g., complementary metal-oxide semiconductors (CMOS) in logic devices.

In 2011, Radisavljevic et al. [7] published the first measurements of a single-layer MoS_2 transistor. They observed large mobilities of at least $200cm^2V^{-1}s^{-1}$ in the range of graphene nanoribbons and achieved room-temperature on/off ratios of $1x10^8$, which means much lower power consumption as compared to classical transistors. Their configuration is shown in Figure 2.12b. They used $50nm$ thick gold contacts for the contactation of the drain and source, and $30nm$ of HfO_2 for the top-gate dielectricum.

They observed MOSFET-like transfer characteristics (see Figure 2.13a). In the characteristic output curve of their device, they also noted linear current voltage dependence, which indicates that gold contacts are ohmic for small V_{ds} (see Figure 2.13b).

2.2.2 Field effect mobility

If an electric carrier is brought into an electric field E, it is subject to a force, which can be defined as $F = qE$. The field effect mobility μ connects the electric field E and the drift velocity v_d, which is reached by the carrier due to force F. The field effect mobility plays a crucial role in terms of the operation speed

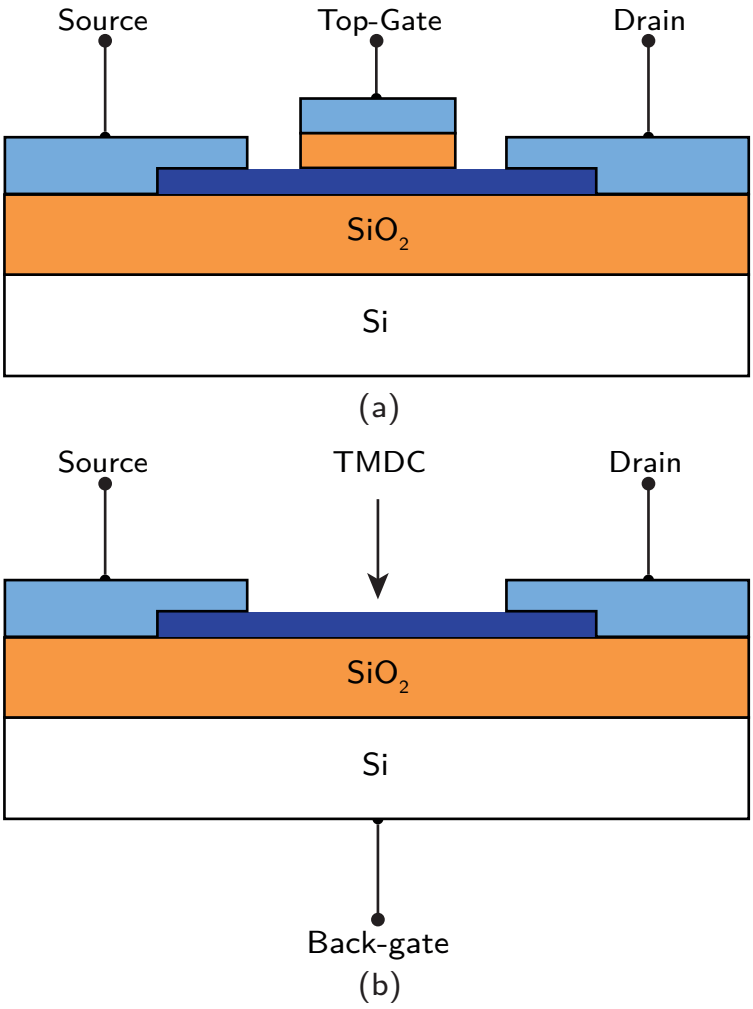

Figure 2.12: (a) TMDC-based transistor in top-gate configuration. (b) TMDC-based transistor in back-gate configuration.

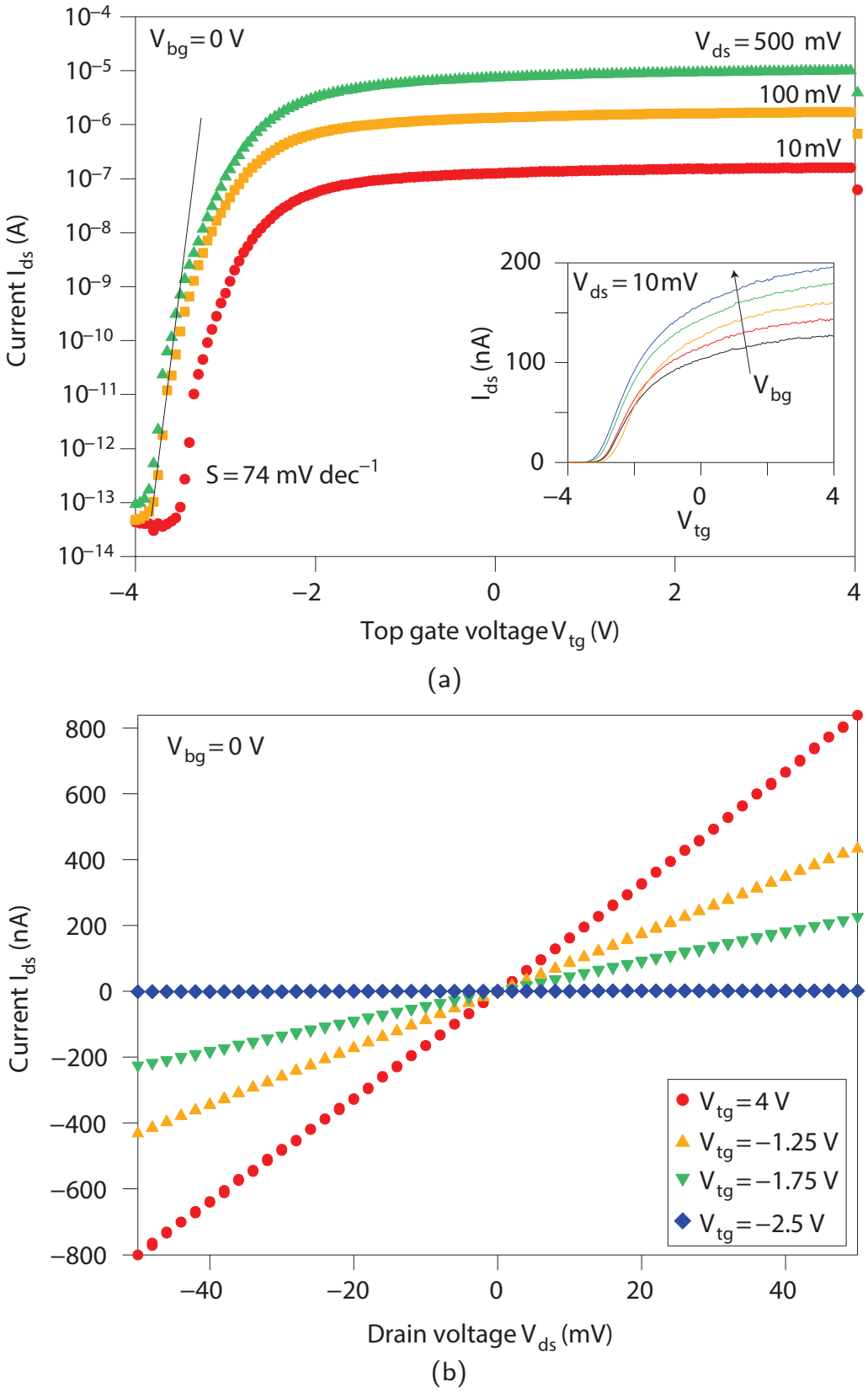

Figure 2.13: (a) Transfer characteristics of a top-gated single-layer MoS_2 transistor. (b) Characteristics output curve of a top-gated single-layer MoS_2 transistor. Source:[7].

of a transistor that is used as a switch. The most accurate measurement for investigating the field effect mobility of field effect transistors (FET) based on two-dimensional materials can either be achieved by cyclic voltammetry [38] or Hall-effect measurements [37]. For an initial estimation, it is often useful to derive the field effect mobility from the FET's transfer characteristics. It has, however to be noted that, unlike a Hall-effect measurement, this estimation is strongly dependent on the contact resistance of the FET and can therefore greatly vary for different devices with similar dimensions and specifications. To illustrate how the field effect mobility is derived, Figure 2.14 shows a 2-D-material-based transistor.

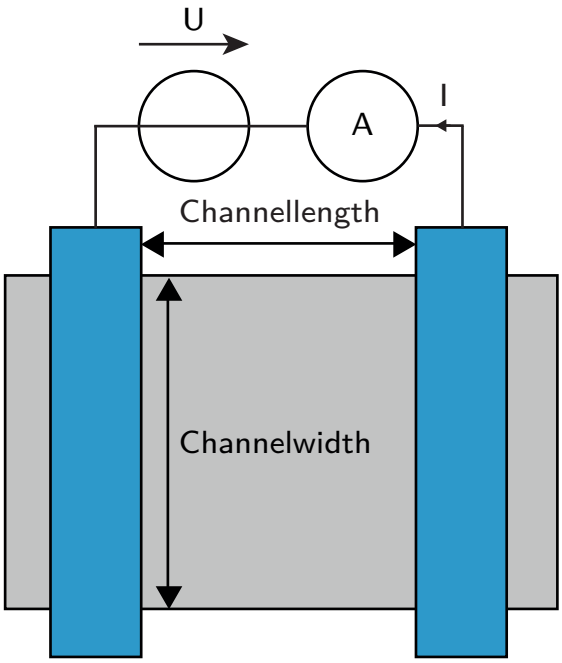

Figure 2.14: Sketch of geometry used for the derivation of the mobility.

Current density can be written as

$$K = \frac{I}{W} = nev_d \tag{2.14}$$

where K describes the current I along a width W, n stands for the number of electrons, e is the electron charge and v_d is the drift velocity an electron

experiences due to an applied electrical field E. Drift velocity can be calculated as follows:

$$v_d = \mu E = \mu \frac{U_{ds}}{L} \tag{2.15}$$

When rearranging equation 2.14 and using the expression from 2.15 we get:

$$I_{ds} = neW\mu \frac{U_{ds}}{L} = \frac{W}{L}\mu neU_{ds} \tag{2.16}$$

The charge accumulated in the atomically thin layer caused by the applied gate voltage U_{gs} can be calculated as follows:

$$Q = CU = C_{ox}U_{gs} = \frac{\varepsilon_0 \varepsilon_r A}{d} U_{gs} \tag{2.17}$$

This equation can be rearranged to

$$\frac{Q}{A} = \frac{\varepsilon_0 \varepsilon_r}{d} U_{gs} = ne \tag{2.18}$$

When substituting ne of equation 2.16 with the expression for the surface charge density of equation 2.16, we get a new formula for the drain source current I_{ds}:

$$I_{ds} = \frac{W}{L}\mu \frac{\varepsilon_0 \varepsilon_r}{d} U_{gs} U_{ds} \tag{2.19}$$

By rearranging this equation, we can calculate the field effect mobility μ:

$$\mu = \frac{L}{W} \frac{d}{\varepsilon_0 \varepsilon_r} \frac{1}{U_{ds}} \frac{dI_{ds}}{dU_{gs}} \tag{2.20}$$

2.2.3 Electrical contacts for two-dimensional materials

A metal and a semiconductor can form two different kinds of contacts, namely an ohmic and a Schottky contact. In an ohmic contact, the contact resistance of the semiconductor-metal interface is very small as compared to the resistance of the semiconducting material as such. In a characteristic output curve diagram (i.e., a diagram that displays the current over the device versus drain-source voltage) the measured curve shows linear behaviour. This means that non-linear components do not play a role in the relation between current density and contact resistance and the contact strictly follows Ohm's law. Such a behaviour can be achieved if the work function of the metal is lower than the Fermi level of the semiconductor involved. For details see Figures 2.15a and b. The I-V curve of a Schottky contact shows non-linear behaviour, which originates from a large electron barrier at the metal-semiconductor interface. This case can occur if the work function of the metal is higher than the Fermi level of the semiconductor. For details see Figures 2.15c and d.

The electron barrier is formed because thermal equilibrium has to be established whenever two materials are contacted. As a result, electrons move from the material with the occupied, energetically higher states to unoccupied, energetically lower states in the other material. In case the semiconductor's Fermi level is higher than the work function (which represents the equivalent to the semiconductor's Fermi level) of the metal, electrons diffuse from the semiconductor to the metal. In turn, this produces an electron-depleted area in the semiconductor, which causes the valence and the conduction band of the semiconductor to bend. The occurred charge transfer creates a voltage that antagonizes the charge stream until thermal equilibrium has been reached. The diffused electrons form a Schottky barrier at the semiconductor-metal interface.

In case of an ohmic contact, electrons move from the occupied, energetically higher states in the metal to the non-occupied, energetically lower states in the semiconductor. The result is a small electron-doped area in the semiconductor, which entails only a small barrier. As a consequence, electrons can move in both directions. Because of the high charge carrier density in metals, no depletion region is formed in the metal.

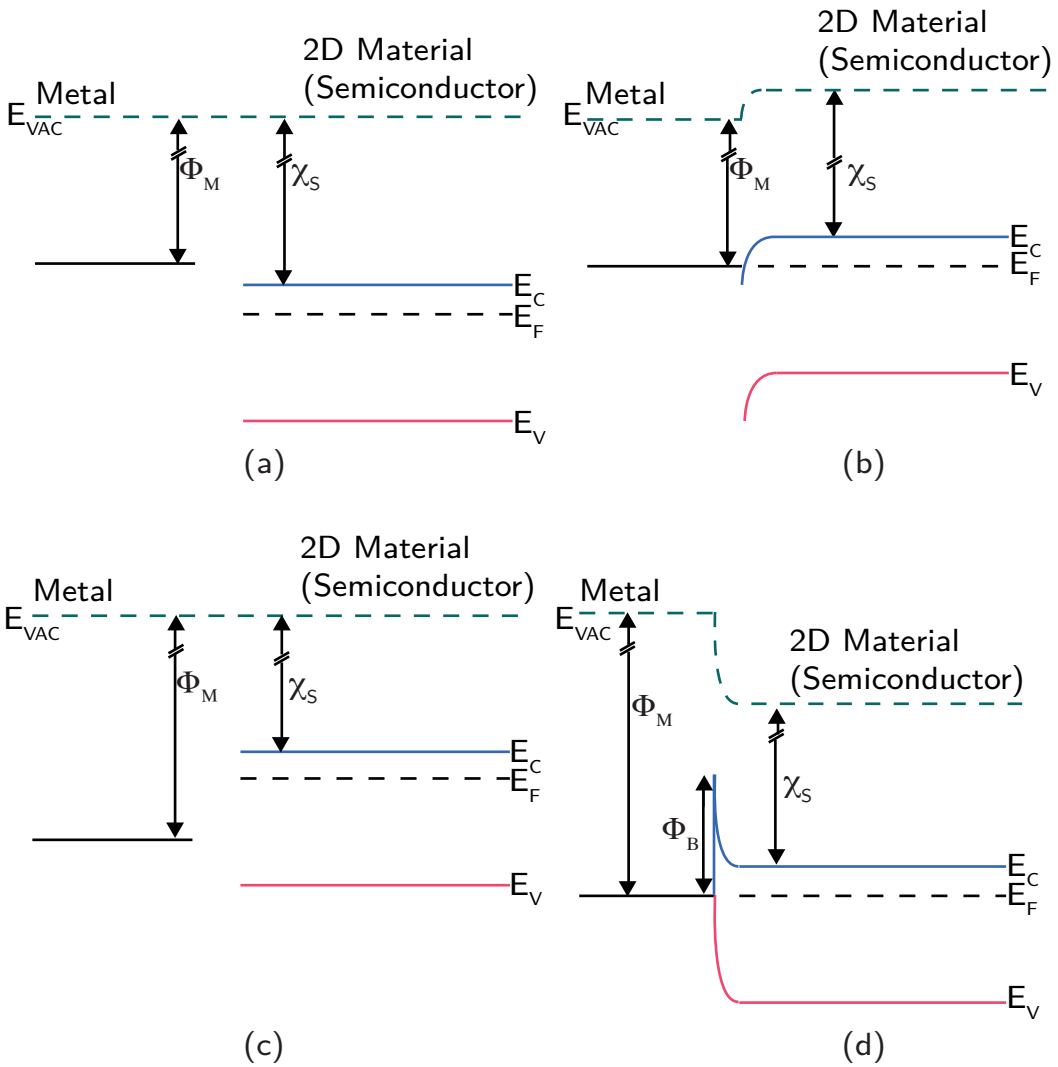

Figure 2.15: (a) Band diagram of a metal and an n-doped semiconductor before they are brought in contact. The Fermi level of the metal is higher than that of the semiconductor leading to an ohmic contact. (b) Band diagram of the same configuration as case (a) after the metal and the semiconductor were brought in contact. Due to the low barrier at the interface, current can flow in both directions. (c) Band diagram of a metal with a higher work function than in case (a) and (b) and an n-doped semiconductor before they are brought into contact. (d) Band diagram of the same configuration as case (c) after these materials were brought into contact. A barrier forms at the interface, allowing the current to only flow in one direction, which constitutes a rectifiying behaviour.

In electrostatics, the Schottky barrier height problem is a key issue at metal semiconductor junctions. The electron exchange at the interface is strongly influenced by the barrier height, which controls everything in semiconductor technology from laser diodes to field effect transistors in high-speed logic.

2.2.3.1 Fermi-level Pinning

Why Schottky barriers form at a metal-semiconductor interface has been an issue for researchers for decades [36].

Originally, the Schottky-Mott model assumed that there is no interaction between the semiconductor and the metal, which led to the assumption that the charge distribution can simply be regarded as the superposition of the charge distribution of the free surfaces of the semiconductor and the metal. Because the experimental results were not in line with this simple model, other models were developed, which take surface states [47, 48], metal-induced gap states [49, 50, 51], defect states [52] or disorder-induced gap states [53] into account. With two-dimensional materials that have a very large surface as compared to their mass and volume, surface states derived from photoresist residues or dirt particles can play a big role in the formation of these additional electronic states. Normally, when a metal and a semiconductor are contacted, they exchange charges until they reach thermal equilibrium and their Fermi level is equalised. The charge transport is necessary, because the work function of the metal and the Fermi level of the semiconductor usually differ before the two materials are contacted. The transport of the charge causes the band of the semiconductor to bend at the interface and the formation of a barrier. When additional states (e.g., surface states) within the band gap start to play a major role, the charge needed to equalize the Fermi between semiconductor and metal can be provided by these additional states. The occupation of these states is determined by their position above or below the semiconductor's Fermi level. Throughout this process, the Fermi level is pinned to the energy level of the surface state. Hence, the resulting electron barrier at the interface is rather determined by the additional states and their occupation than by the original electron configuration of the semiconducting material that was used.

3 Processing

3.1 Mechanical Exfoliation

The famous scotch tape technique was used to place two-dimensional TMDC crystals on a silicon/silicon dioxide wafer. The wafers used in this master thesis had silicon dioxide thicknesses of 285 nm. The thickness of the transparent oxide layer not only determines the applied electrical field when a gate voltage is applied at the back-gated transistor. When searching for the 2-D material by optical microscopy, it also plays a crucial role with respect to the contrast between the silicon substrate and the atomically thin layer. The fact that 2-D materials can be spotted on such a wafer with the help of an optical microscope is one of the main reasons why research in the field of 2-D materials underwent a significant upturn once the scotch tape method had been invented in 2004.

In this master thesis, ordinary wafer dicing tape was used. The samples were exfoliated and transferred onto the wafer in the cleanroom. The bulk MoS_2 and WSe_2 crystals were bought from SPI Inc. and Nanosurf Inc., respectively. Figure 3.1 shows a typical picture of an atomically thin flake of MoS_2. The same flake was used to fabricate a MoS_2-based transistor with MoO_x/Pd contacts. The measurements conducted on this transistor are documented in chapter 4.5.

3.2 Microscope Search

After mechanical exfoliation, the silicon/silicon dioxide wafer chips containing the TMDC in thin layers were scoured for promising flakes of the 2-D material, which

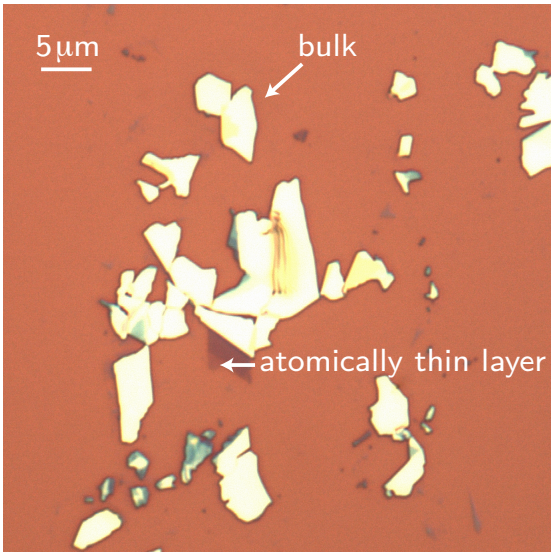

Figure 3.1: Picture of a typical atomically thin flake on a silicon/silicon-dioxide substrate.

are suitable for building transistors. Auspicious TMDC flakes were photographed with different magnifications. The picture with the biggest magnification always constituted the basis for a dxf-file produced with the Autocad programme, while the other pictures were used to spot flakes on the substrate when utilising the laserwriter to write contacts in photoresist. This process will be described in more detail in chapter 3.3.1.

Why atomically thin films can be spotted in an optical microscope is explained in chapter 3.2.1.

3.2.1 Visibility

One key reason for the huge rise of research on two-dimensional material after graphene had been discovered on the adhesive side of scotch tape in 2004 was the fact that graphene and many other 2-D materials can be located on a silicon/silicon-dioxide wafer by optical imaging. Atomic force microscopy (AFM), which constitutes one alternative for locating two-dimensional films, however is very time-consuming and has a very small throughput compared to optical microscopy. Other alternatives would be scanning electron microscopy (SEM),

as well as transmission electron microscopy (TEM), but both of these sample characterisation methods have huge disadvantages as compared to optical imaging. In the case of SEM the contamination, originating from electron-beam-induced deposition, and in the case of TEM from knock-on damage due to the electron-beam radiation-induced displacement of atoms are serious drawbacks of these methods, while optical imaging is fast, cheap and non-invasive.

As early as 2004, Novoselov [2] documented that atomically thin carbon films are sufficiently transparent to add an optical path, which will show an interference colour that differs from that of an empty wafer under an optical microscope. With some practice, researchers can spot these films and even distinguish various thicknesses. This holds true in particular for certain thicknesses of the SiO_2 layer of a Si/SiO_2 wafer, which led Benameur et al. [39] to calculate the most favourable thickness of the SiO_2 layer, for spotting atomically thin flakes.

Benameur et al. therefore analysed a stacking that comprised a thin film of a TMDC on top of a SiO_2 layer, which, in turn, rested on silicon. As the thickness of the silicon is several orders of magnitude higher than that of the other two layers, it is considered a semi-infinite film. Formula 3.1 describes the reflected light intensity for normal light that shines on the sample [40]. In this formula 3.2, 3.3 and 3.4 are the relative indices of refraction and 3.5 describes the phase shifts, which are induced by changes in the optical path. In order to derive the intensity of the reflected light in the absence of an atomically thin film n_1 (see Figure 3.2), its relative index of refraction has to be set as $n_1=1$. Equation 3.6 shows the resultant formula for the reflected light intensity, with the relative index of refraction at the interface between air and the dielectric thin film shown in equation 3.7.

$$R(n_1) = \left| \frac{r_1 e^{i(\phi_1+\phi_2)} + r_2 e^{-i(\phi_1-\phi_2)} + r_3 e^{-i(\phi_1+\phi_2)} + r_1 r_2 r_3 e^{i(\phi_1-\phi_2)}}{e^{i(\phi_1+\phi_2)} + r_1 r_2 e^{-i(\phi_1-\phi_2)} + r_1 r_3 e^{-i(\phi_1+\phi_2)} + r_2 r_3 e^{i(\phi_1-\phi_2)}} \right|^2 \tag{3.1}$$

$$r_1 = \frac{n_0 - n_1}{n_0 + n_1} \tag{3.2}$$

$$r_2 = \frac{n_1 - n_2}{n_1 + n_2} \tag{3.3}$$

$$r_3 = \frac{n_2 - n_3}{n_2 + n_3} \tag{3.4}$$

$$\Phi_i = \frac{2\pi d_i n_i}{\lambda} \tag{3.5}$$

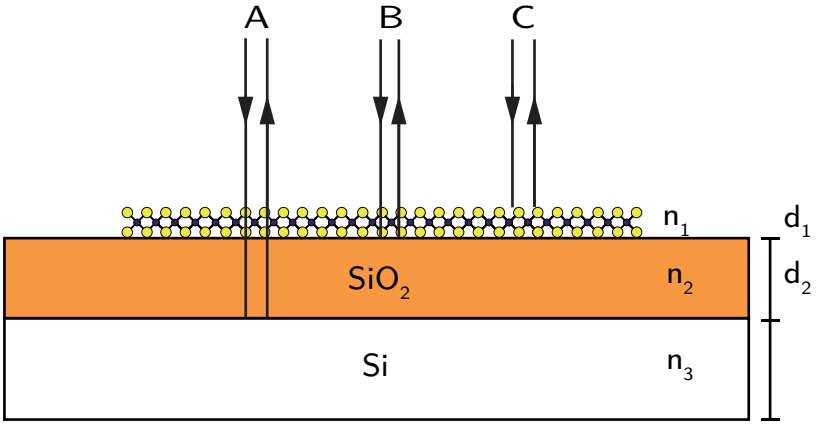

Figure 3.2: Schematic sketch of the three different cases of reflection and transmission mechanisms for an atomically thin layer with a thickness d_1 and its complex index of refraction n_1, which rests on a SiO_2 layer with a thickness d_2 and its index of refraction n_2 and is based on a silicon layer of semi-infinite thickness.

The contrast between a monolayer and the underlying surface is defined as the relative intensity of the light in the absence and presence of an atomically thin film, which is indicated in equation 3.8. Figure 3.3 shows the calculated contrast of MoS_2.

$$R(n_1 = 1) = \left| \frac{r_2' e^{i(\Phi_2)} + r_3 e^{-i(-\Phi_2)}}{e^{i(\Phi_2)} + r_2' r_3 e^{-i(-\Phi_2)}} \right|^2 \tag{3.6}$$

$$r_2' = \frac{n_0 - n_2}{n_0 + n_2} \tag{3.7}$$

$$\text{Contrast} = \frac{R(n_1 = 1) - R(n_1)}{R(n_1 = 1)} \tag{3.8}$$

3.3 Lithography

Two different methods were used to form contacts for the back-gated transistor. The MoS_2 transistors were fabricated by using a laserwriter (Heidelberg DWL fs) and the WSe_2 transistors were constructed by using electron beam lithography. These two processes are described in chapter 3.3.1.

3.3.1 Laser and electron beam lithography

In order to write contacts with laser lithography, undiluted photoresist (AZ5214) was spun onto the sample with 9000rpm for 35 seconds by using a spin coater. The sample was subsequently baked on a hot plate at 100°C for one minute and cooled down to room temperature by placing it on a metal surface for a few seconds. It was transported in a light-tight sample box to avoid that the light-sensitive photoresist is exposed to light before it has been put into the laserwriter.

Once the sample was in the laserwriter and the flake had once more been identified with the help of the additional picture of its environment (see chapter 3.2), the dxf file was used to write the metal contacts pattern, which had been drawn in Autocad beforehand. After the laser beam had exposed certain areas of the photoresist that contained the contact pattern, the sample was removed from the laserwriter and developed for three seconds in developer (AZ351B), which was diluted with water at a ratio of 1:2. Subsequently, it was pivoted in distilled water for 12 seconds to remove the developer and to achieve an accurate lithography pattern. Then the sample was blown dry with nitrogen.

For the electron beam lithography PMMA EBL resist (Allresist AR-P 679.04)

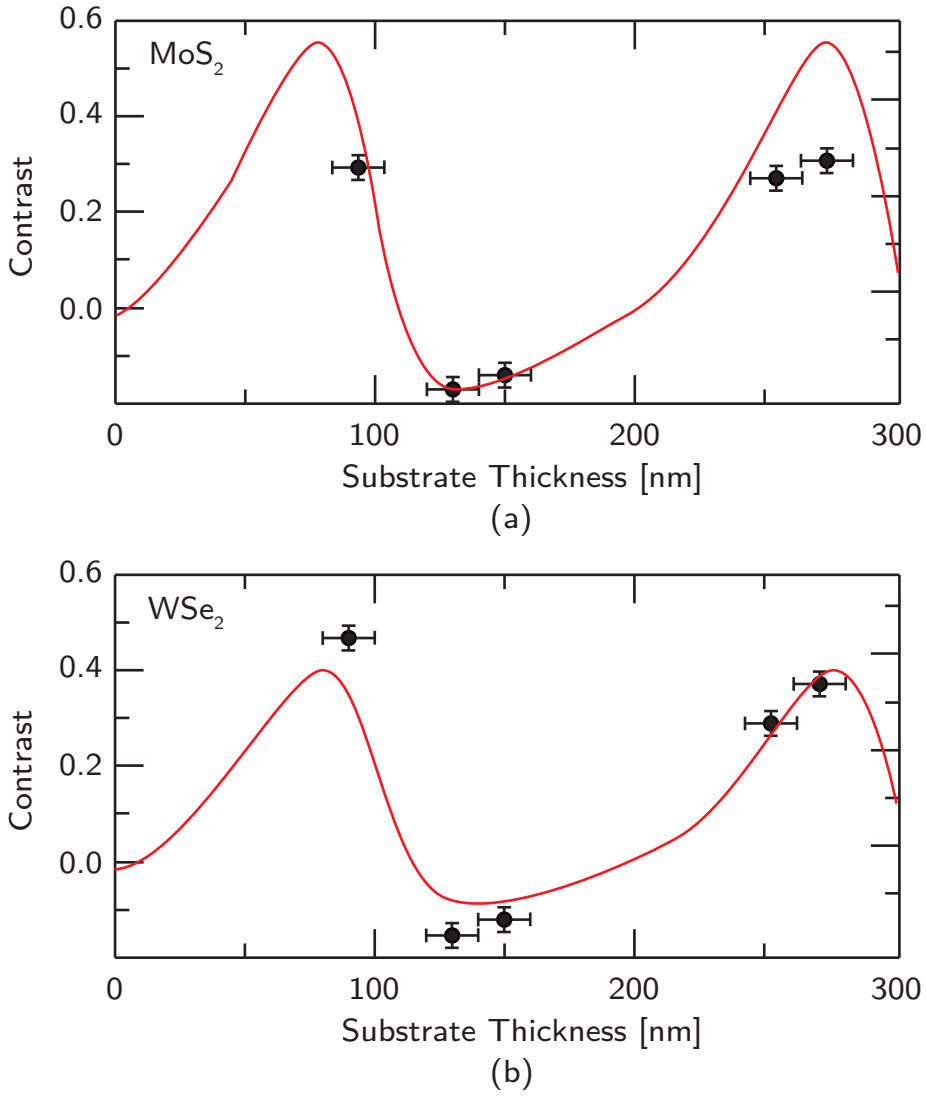

Figure 3.3: The Figure shows contrast versus SiO_2 layer thickness for broadband illumination. The reflected light was detected by using the green channel (495-530 nm) of a colour camera. The black marks show experimental data points. The Figure shows that the SiO_2 thickness has a strong influence on the reflected light intensity. The frequency of the light used for illumination also plays an albeit much less important role.

was spun onto the sample at 4000 rpm for 35 seconds. This was followed by a pre-exposure bake of 5 minutes at 170°C. Afterwards the photoresist was exposed to a radiation dose of 100 $\mu C/cm^2$. Then the sample was unmounted and developed by using developer AR 600-56 for 30 seconds. A stopper was subsequently applied for 30 seconds to halt the development and to achieve a decent contact pattern. In the end, the sample was blown dry with nitrogen.

3.3.2 Vapour deposition

The metal contacts were created by using a metal evaporation device (Leybold). The contacts were evaporated at a base pressure of around $5*10^{-6}$ bar.

3.3.2.1 Titanium gold contacts

In order to contact the WSe_2 transistors, a 10 nm thick layer of titanium was first evaporated at an evaporation rate of 0.5 Å/s. After 5 minutes, the target was changed to gold and a 60 nm thick layer of gold was evaporated at an evaporation rate of 0.5 Å/s. After another 5 minutes, the chamber was vented and the sample removed. To separate the excess metal from the sample, it was put into acetone for 6 hours. To prevent the acetone from vaporising, the laboratory glass was covered with aluminium foil.

3.3.2.2 MoO_x Contacts

The MoS_2 transistors were contacted with a 30 nm thick molybdenum oxide layer MoO_x that was topped with a 30 nm thick palladium layer. The MoO_x contact layers were thermally evaporated by using a molybdenum boat. The MoO_3 powder (99.9995% purity, Alfa Aesar) was thermally evaporated at a base pressure of $8*10^{-7}$ bar and an evaporation rate of 0.5 Å/s. It should be noted that adjusting the desired evaporation rate was very challenging, because it takes around 5 minutes before the powder starts to evaporate at detectable rates. If too much voltage is applied at the beginning of the evaporation procedure,

the parts of the powder right on the surface of the molybdenum boat seem to sublimate and entrain the rest of the powder. Once the molybdenum boat is empty, one has to vent the chamber and put new powder into the boat. As it takes around 6 hours to pump the evaporation chamber down to base pressure, incidents like the one just outlined above should be avoided by all means. It is therefore very important to check which voltage is required to achieve the desired evaporation rate and to wait patiently at a certain voltage until the powder starts to evaporate.

4 Measurements

4.1 Photoluminescence

In its bulk form, WSe_2 exhibits an indirect band gap at $1.2eV$, which is equivalent to $1.03\mu m$ of the light's wavelength. According to [12], the direct transitions of A and B excitons are in the range of $1.4 - 1.8eV$ (886 - 690 nm) and 2.3 eV (540 nm), respectively [23]. The two different excitonic transitions arise from valence band splitting. Figure 4.2 shows the PL spectrum of device P2. The black curve has its maximum at 1.67 eV, which is in line with the spectrum measured by Tonndorf et al. [21]. Figure 4.1 shows the spectrum for WSe_2 as described in their publication. The black curve relates to monolayer WSe_2 and has its maximum at 1.65 eV (752 nm). The difference in luminescence quantum efficiency between a monolayered TMDC and its bulk form is in the order of 10^3 [30]. For this reason, PL measurements are unsuitable for a decent characterisation of bulk TMDC crystals and no PL spectrum was measured for the bulk part of device P1.

4.2 Raman Spectroscopy

Raman spectroscopy is a powerful tool in TMDC-based research. It allows us to determine exactly how many layers an atomically thin layer consists of, because the energy, width and amplitude of vibrational modes (see chapter 2.1.5) strongly depend on the thickness of the investigated flake [21]. For the measurement described in this chapter, a Horiba iHR320 imaging spectrometer and a laser emitting light at 532 nm were used in a confocal optical setup to conduct the measurement. The grating in the spectrometer was 150 l/mm and the selected

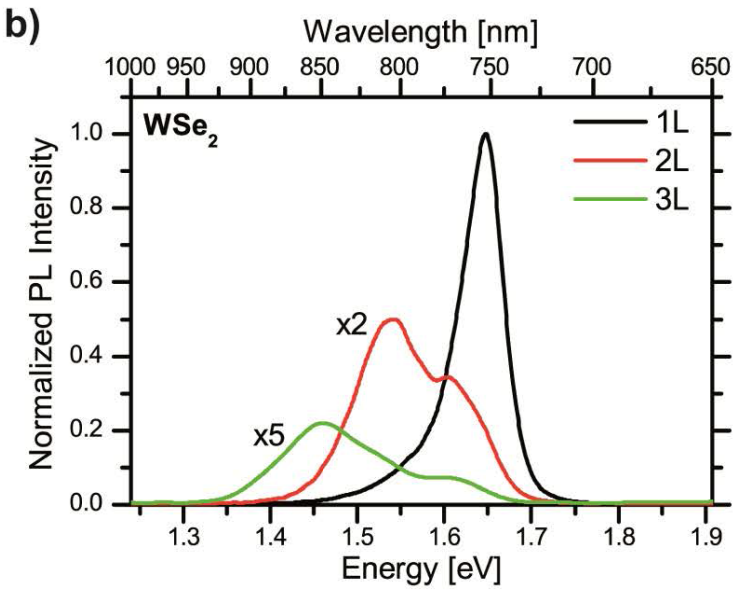

Figure 4.1: PL spectra for several WSe_2 flake thicknesses. Source:[21].

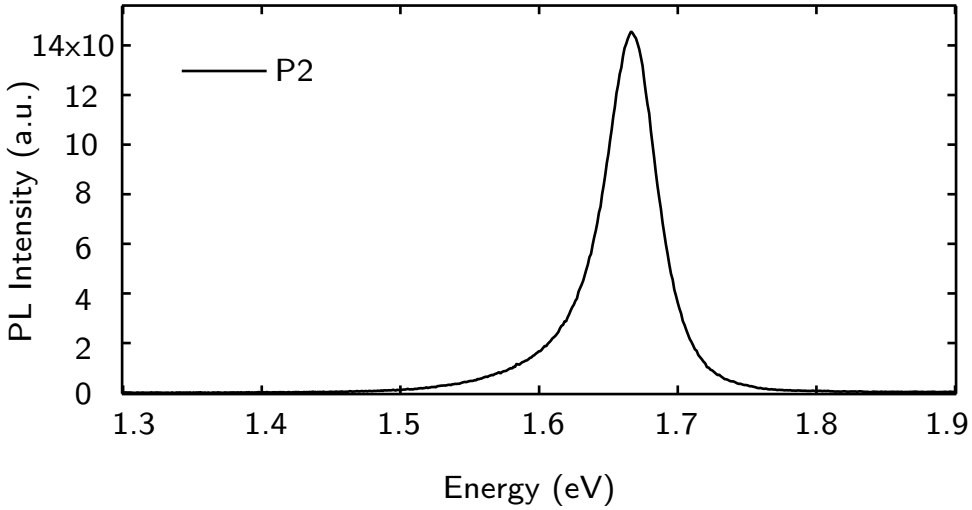

Figure 4.2: PL spectrum of TMDC flake built in device P2.

laser power used was 45 μW. Figure 4.6 shows the Raman spectra of devices P1 and P2, respectively. The red curve shows the measured Raman spectrum of device P1. It has its highest peak at 250.5 cm^{-1} and can be referred to as A_{1g} vibrational mode. This is in line with data collected by other groups [21]. The black curve shows the Raman spectrum of device P2. It has its maximum at 248.2 cm^{-1}, which is also in line with data quoted in the literature. Figure 4.3 shows the Raman spectrum for WSe_2 measured by Tonndorf et al. [21]. When comparing Figure 4.6 and Figure 4.3, we can see that the width and shape of the maxima are rather similar in both Figures. Moreover, the ratio between the red and the black curve is the same as that between the dashed line and the red line in Figure 4.3. This implies that the red curve in Figure 4.6 corresponds to bulk material and the black line corresponds to bi-layer WSe_2. It should be noted that Raman spectra in Figure 4.3 were vertically displaced for clarity. In addition, the red curve has a small peak at 259 cm^{-1}, which is another indication for the fact that the WSe_2 layer of device P1 is bulk.

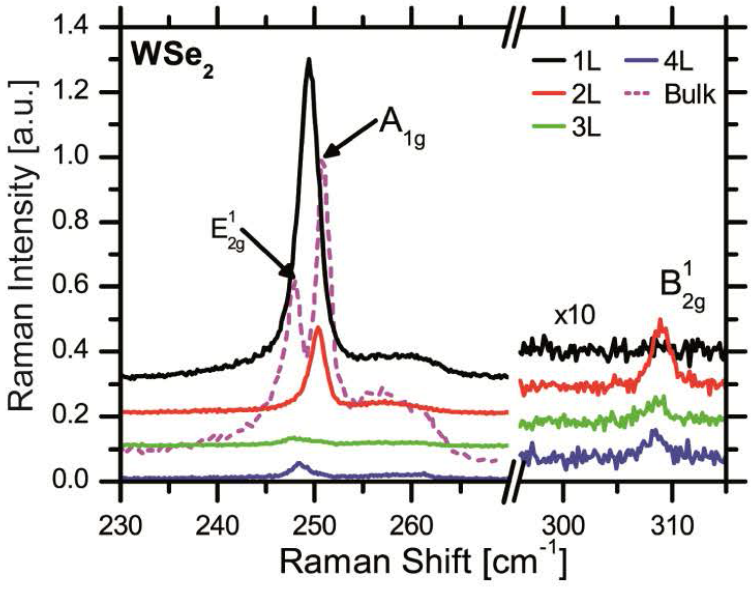

Figure 4.3: Raman spectra for several WSe_2 flake thicknesses. Source:[21].

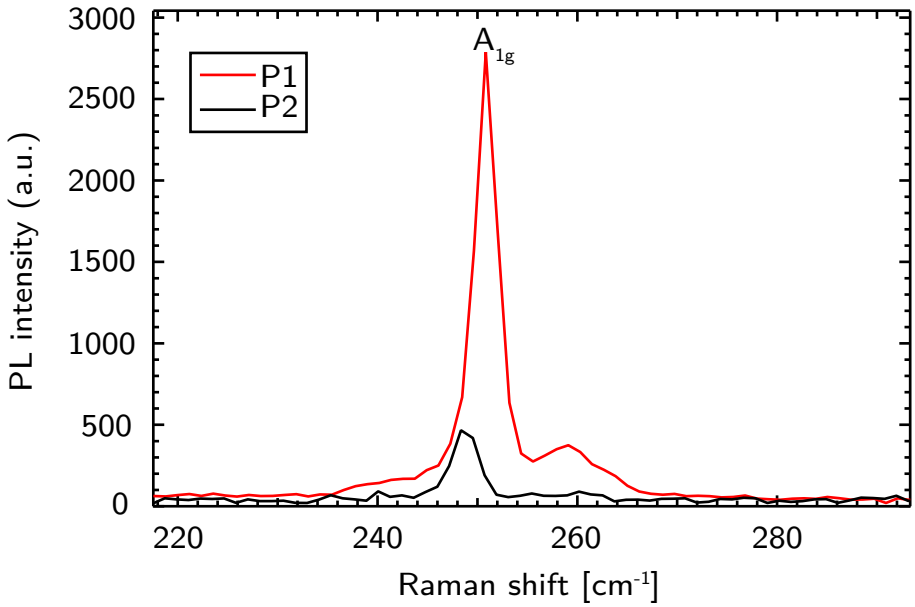

Figure 4.4: Raman spectra of the flakes built in device P1 and P2, respectively.

4.3 Electrical Characteristics of WSe_2 transistors

For the first electrical characterisation, I-V measurements were performed in wafer probe station Lake Shore TTPX. The characteristic output curve as well as the transfer characteristics of devices P1 and P2 are shown in Figure 4.6. The measurements were performed at room temperature after pumping down the pressure to around $10^{-4} mbar$ while the sample was illuminated with light. Both devices show typical n-type field-effect transistor behaviour as described in detail in chapter 2.2. In the positive gate voltage range, the drain source current I_{ds} is directly dependent on the applied gate voltage V_g. For highly negative gate voltages, weak p-type field-effect transistor behaviour can be observed, which is also documented by other groups [42]. This can be explained by the low electron affinity of WSe_2 as compared to other TMDCs such as MoS_2, which only has electron conductance.

Figure 4.7 shows the effect of the applied gate voltage on the energy levels of the conduction and valence bands. In case (a), a positive gate voltage is applied

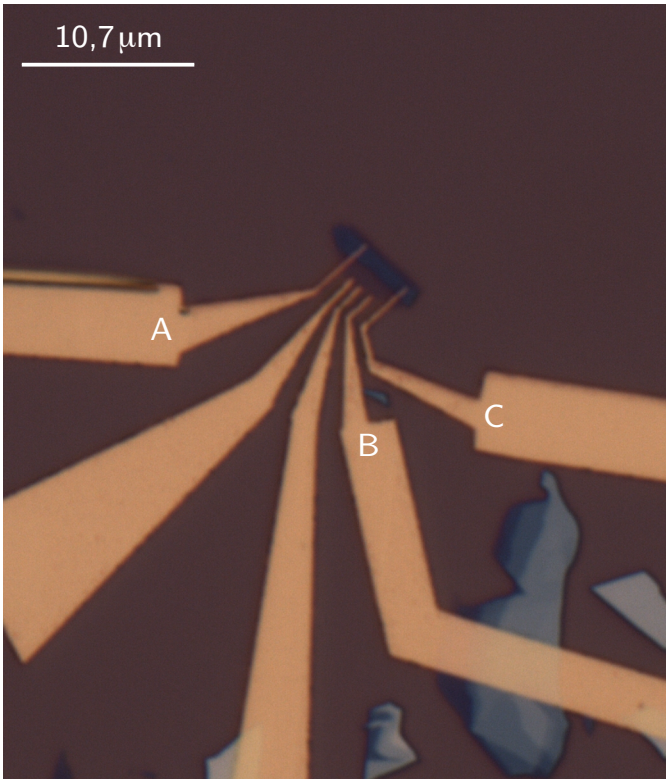

Figure 4.5: Picture of transistors P1 and P2. The electric measurements drain-source voltage was applied for device P1 between the contact pads A and C, wheareas for device P2 it was applied between the contact pads B and C, respectively.

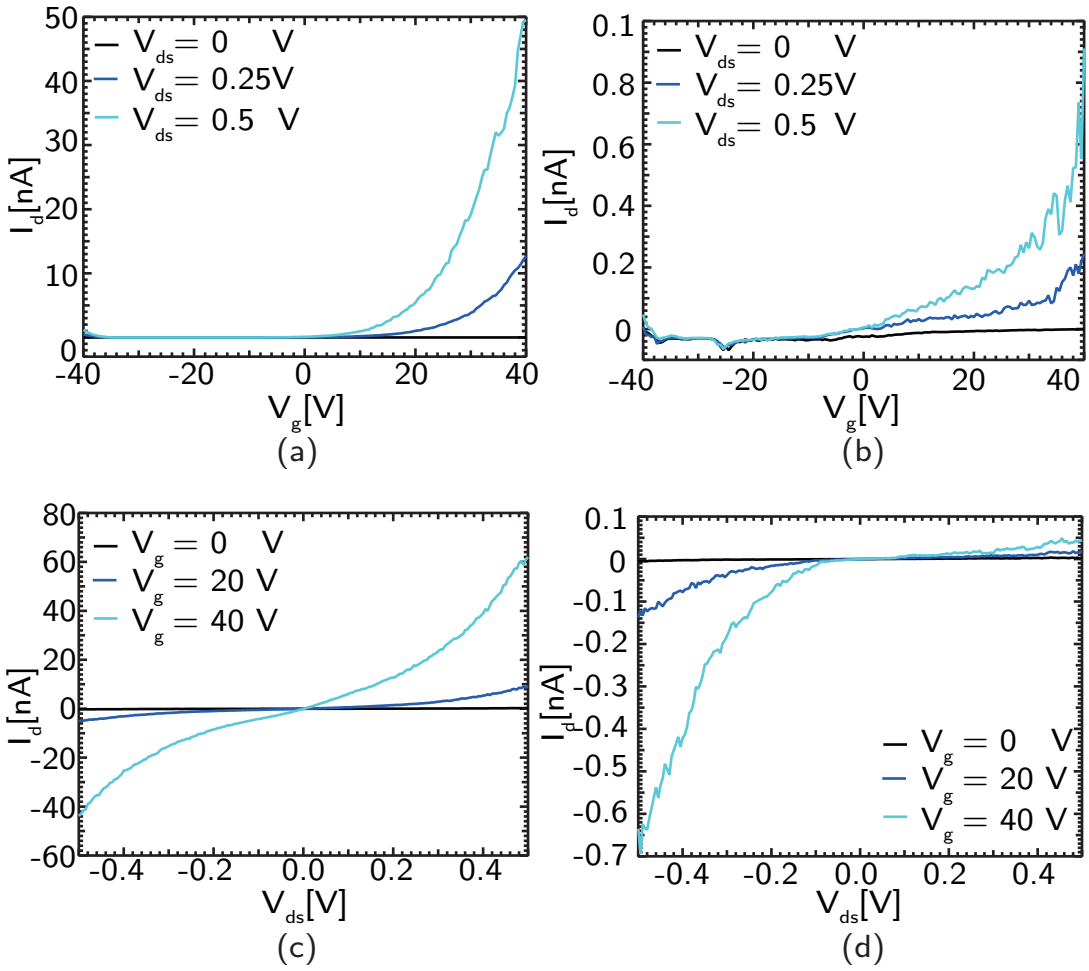

Figure 4.6: (a) and (b) show transfer characteristics of devices P1 and P2, respectively. (c) and (d) show characteristic output curves of devices P1 and P2, respectively.

and the conduction as well as the valence bands shift downwards. This may cause n-type electron conduction if the applied gate voltage is large enough and the lower edge of the conduction band reaches the Fermi level thus permitting electrons to tunnel through the small barriers at the interface, which is equivalent to a current flow. In case (b), a negative gate voltage is applied. This leads to an up-shift in the conduction and valence bands, which can entail p-type conductance (hole conductance) in case the valence band of the semiconductor reaches the Fermi level and holes can tunnel through the barrier at the interface.

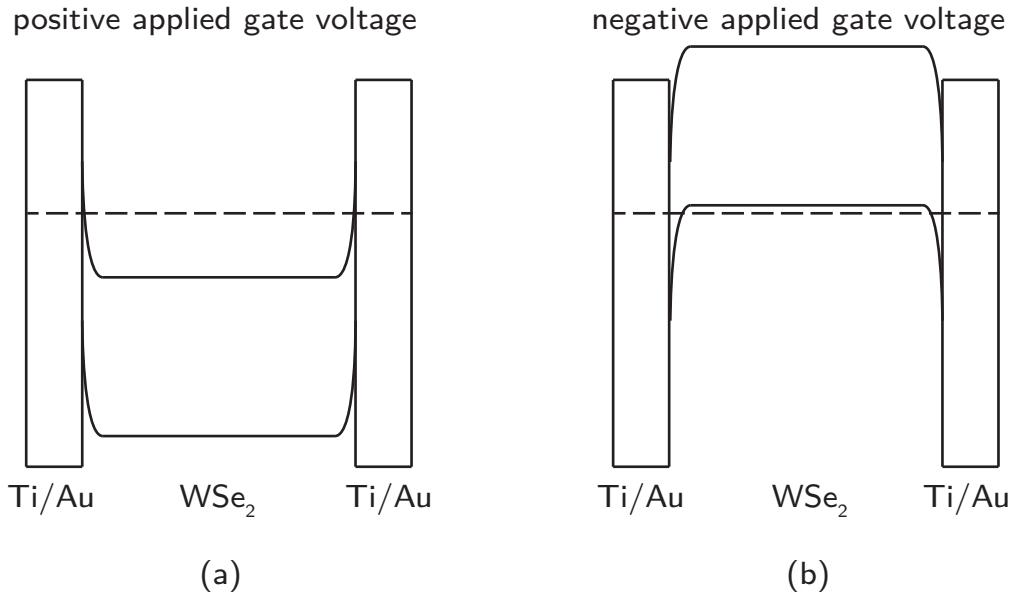

Figure 4.7: (a) Bent band diagram of WSe_2 when a positive voltage is applied at the back-gate of the transistor. (b) Bent band diagram of WSe_2 when a negative voltage is applied at the back-gate of the transistor.

Subsequently, temperature-dependent measurements were performed. The transfer characteristics of devices P1 and P2 for temperatures in the 300-380 K range are shown in Figures 4.8a and b, respectively. The characteristic output curves of devices P1 and P2 for the same temperatures are shown in Figures 4.8c and d, respectively. As temperatures rise, mobility and maximum current both increase and the on-state threshold voltage of the transistor shifts to small or even negative gate voltages. The shifted threshold voltage can be explained by the higher kinetic energy of the electrons along with a higher probability

that they overcome the barrier at the metal-semiconductor interface. Another explanation is the annealing effect caused by the temperature increase up to 380 K. By heating up the sample in a pumped chamber, water molecules, photoresist residues as well as water molecules attached to the surface of the two-dimensional material come off the TMDC and get pumped out of the chamber. These additional surface impurities can cause trap states in the electronic structure of the semiconductor. When a charge carrier passes such a localised impurity, it gets trapped for a certain time and can no longer participate in the charge transport, which decreases the current flow. During the annealing procedure, the number of these trap states is reduced and the performance of the device improves.

After this measurement, a temperature-dependent measurement at low temperatures (range: 100-250K) was performed in order to determine the Schottky barrier height of these transistors. Without breaking the vacuum after the measurements taken in the range of 300-380 K, the samples were therefore annealed at 380 K for around 6 hours to improve the performance of the device.

The transfer characteristics of devices P1 and P2 for temperatures in the range 100-250 K are shown in Figures 4.9a and b, respectively. The characteristic output curves of devices P1 and P2 for the same temperatures are shown in Figures 4.9c and d, respectively. In this temperature range, the devices show the same typical transistor behaviour as in the 300-380 K temperature range. As the temperature increases, the threshold voltage once more shifts to smaller or even negative gate voltages and the mobility also increases as the temperature rises. The highest mobilities of 0.53 and 0.009 $cm^2V^{-1}s^{-1}$ for devices P1 and P2 were observed at temperatures of 360 and 380, respectively.

For devices P1 and P2 the mobility was calculated using formula 2.20. Figure 4.10 shows the temperature-dependent mobility. It is important to note that the quality of the contacts influences the mobilities calculated in this study. In order to obtain mobility values that are independent of the contact's quality, a Hall-effect measurement is needed [37]. The outlier at 300 K can be explained by the fact that the samples were not annealed when the measurement was taken at 300 K. The subsequent measurements at 320-380 K apparently followed a short annealing procedure, which explains why the mobility values for these temperatures are not compatible with the mobility value of 300 K.

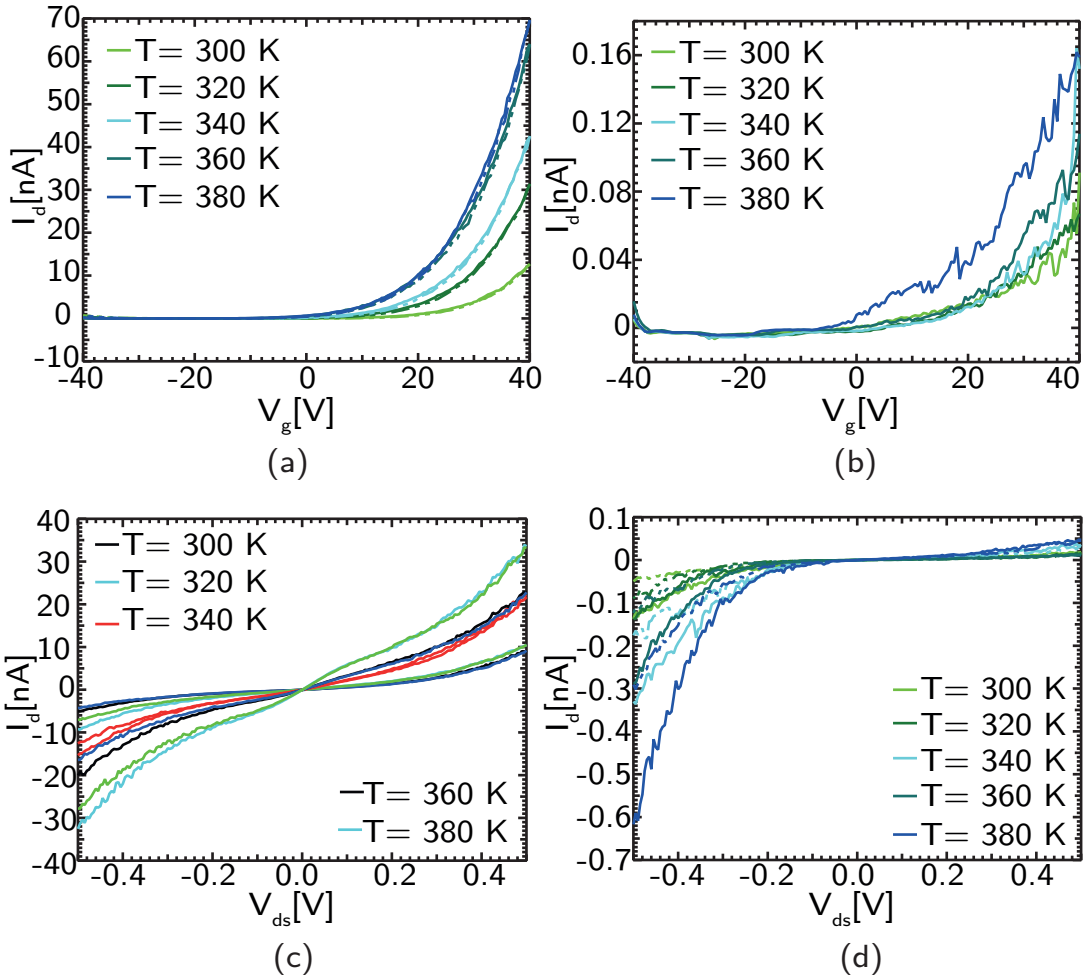

Figure 4.8: (a) Transfer characteristics of device P1 for temperatures from 300-380 K. (b) Transfer characteristics of device P2 for temperatures from 300-380 K. (c) Characteristic output curve of device P1 for temperatures from 300-380 K. (d) Characteristic output curve of device P2 for temperatures from 300-380 K.

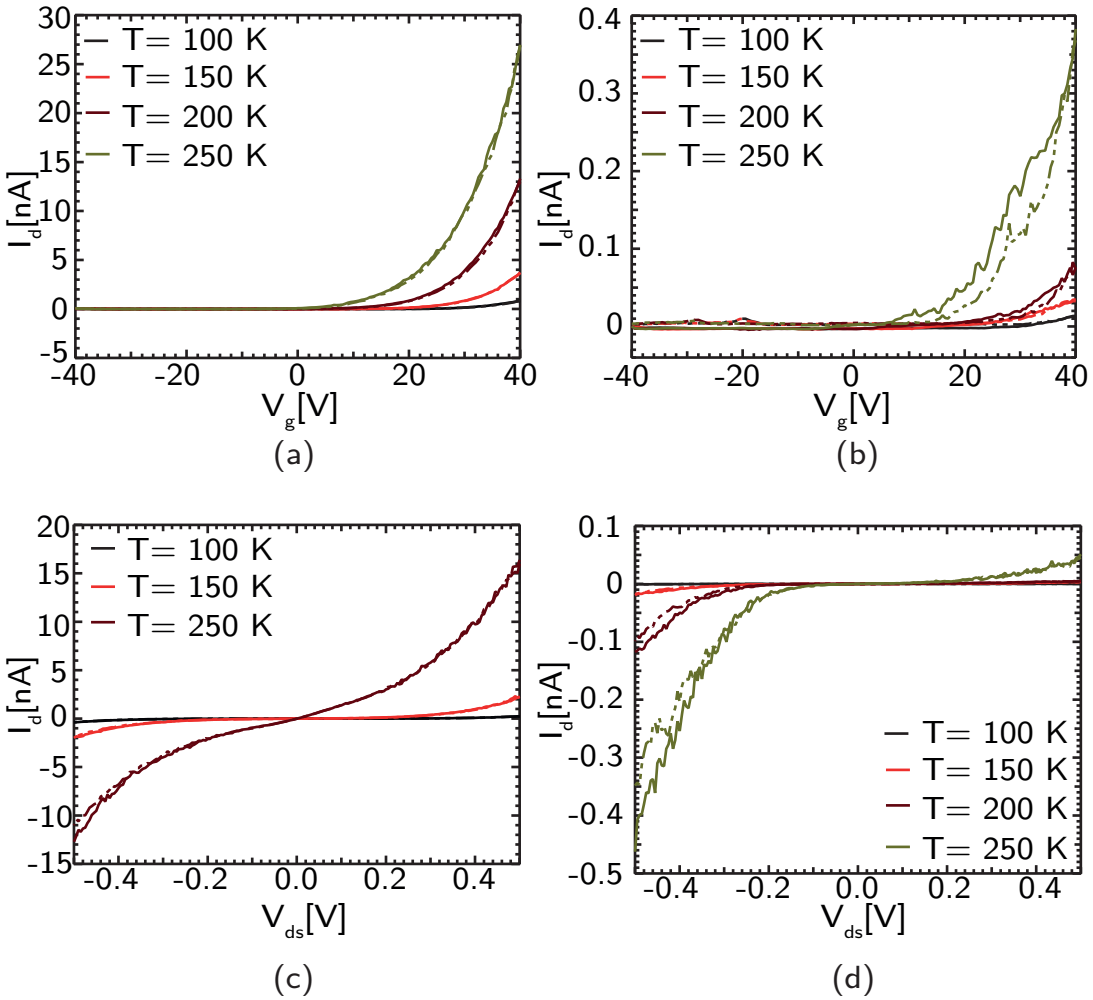

Figure 4.9: (a) Transfer characteristics of device P1 for temperatures from 100-250 K. (b) Transfer characteristics of device P2 for temperatures from 100-250 K. (c) Characteristic output curve of device P1 for temperatures from 100-250 K. (d) Characteristic output curve of device P2 for temperatures from 100-250 K.

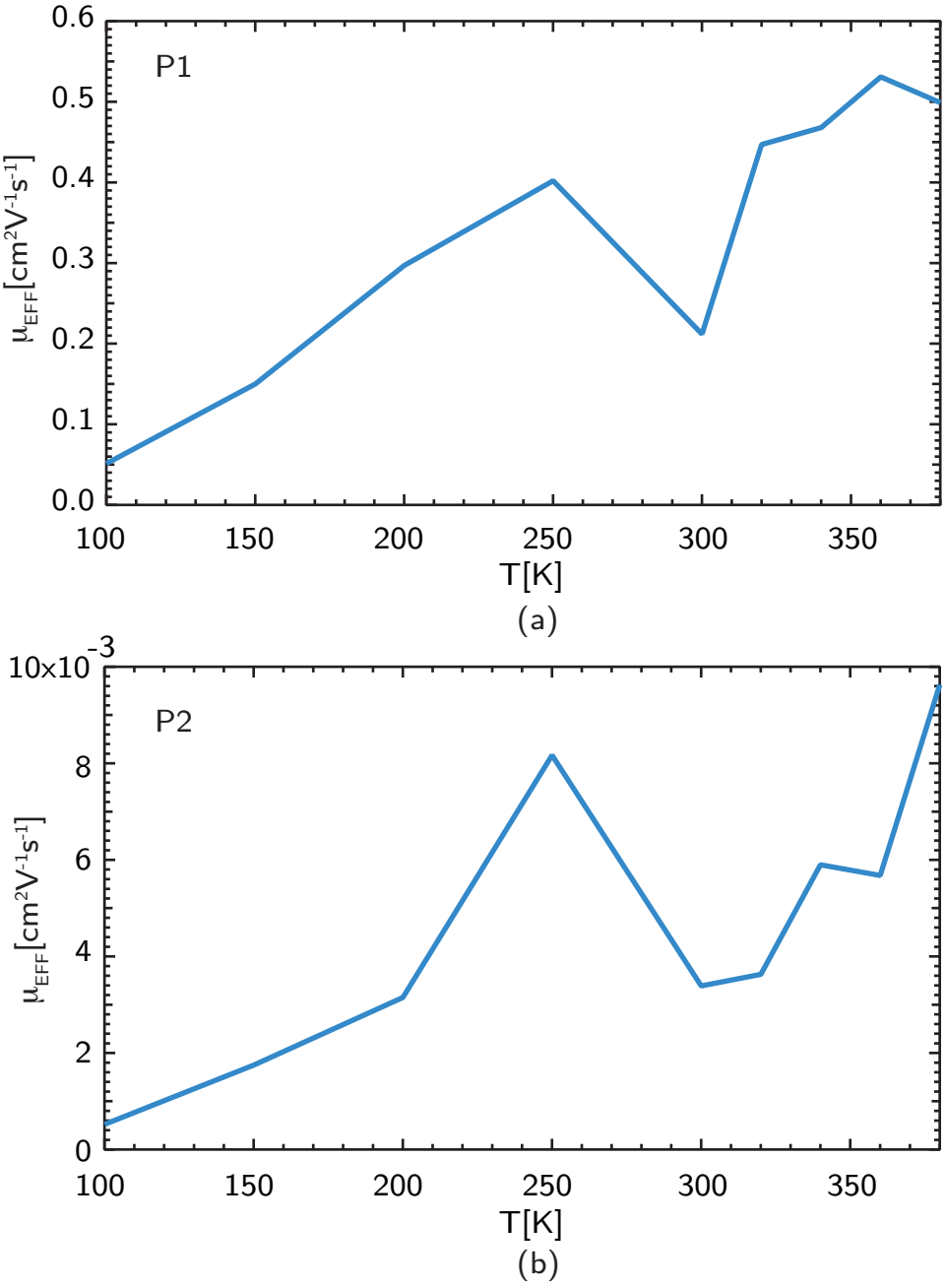

Figure 4.10: Temperature-dependent mobility for devices P1 and P2. The lower mobility at 300 K can be explained by the fact that the device was not annealed when the measurement data were collected at this temperature.

4.4 Determination of Schottky barrier height

The interface is the major performance-limiting factor for any such low-dimensional matter as 2-D materials. Initially researchers focused on improving interface problems between the gate dielectric and the 2-D material to obtain ultimate gate control [43, 44]. In 2012, Das et al. [19] published a comprehensive experimental study on contacts to a TMDC. To investigate the different Schottky barrier heights for high and low work function contact metals, they did a temperature-dependent study that considers both thermionic emission over and thermally assisted tunnelling through the Schottky barrier. If the applied gate voltage V_g is below the so-called flat band voltage V_{FB}, the current consists exclusively of the thermionic emission current component $I_{thermionic}$. If the applied gate voltage V_g is above V_{FB}, the energy bands of the semiconductor bend down and electrons can tunnel through the barrier at the metal semiconductor interface. In this gate voltage regime, the thermally assisted tunnelling current component $I_{tunneling}$ dominates I_d. In the framework of this master thesis, a similar analysis to the one of Das. et al. was performed on two WSe_2-based back-gate transistors with different WSe_2 layer thicknesses.

In order to determine the Schottky barrier height for a certain metal semiconductor interface, experimental transfer characteristics have to be collected at different operating temperatures. Figures 4.11 and 4.13, respectively, show the transfer characteristics of the temperature range (100-250 K) that was used to determine the Schottky barrier height for devices P1 and P2.

The next step in the extraction of the Schottky barrier height was to take the I_d currents for several gate voltages from the transfer characteristics of all four temperatures that had been considered. It is important to choose the right values of the gate voltages in order to get reasonable results. For device P1 the I_d values at gate voltages V_g ranged from -10 to 30 and for device P2 the I_d values at gate voltages ranged from 5 to 35 volts. Subsequently, the I_d values were plotted on a $1000/T$ x-axis, which is called an Arrhenius plot. L. Yu et al. used the following formula [55] for extracting the Schottky barrier height:

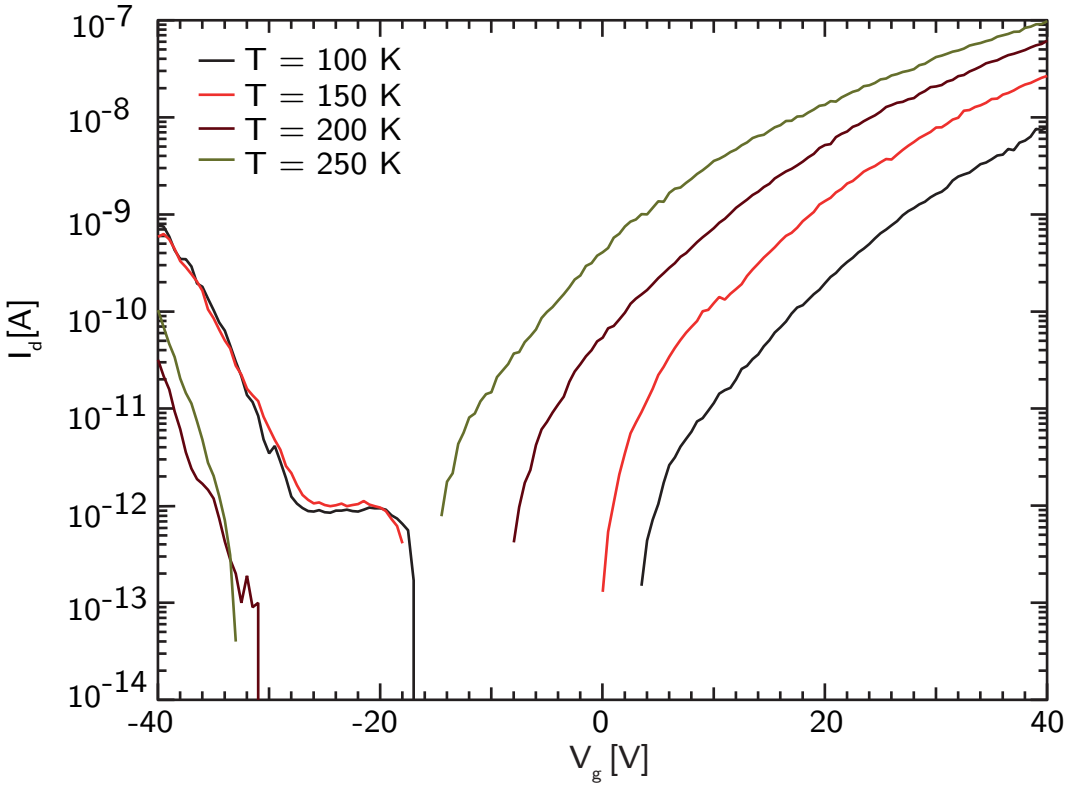

Figure 4.11: Transfer characteristics of device P1 for the temperature range between 100-250 K. Below the flatband voltage V_{FB} only termionic emission $I_{thermionic}$ determines the current flow through the device.

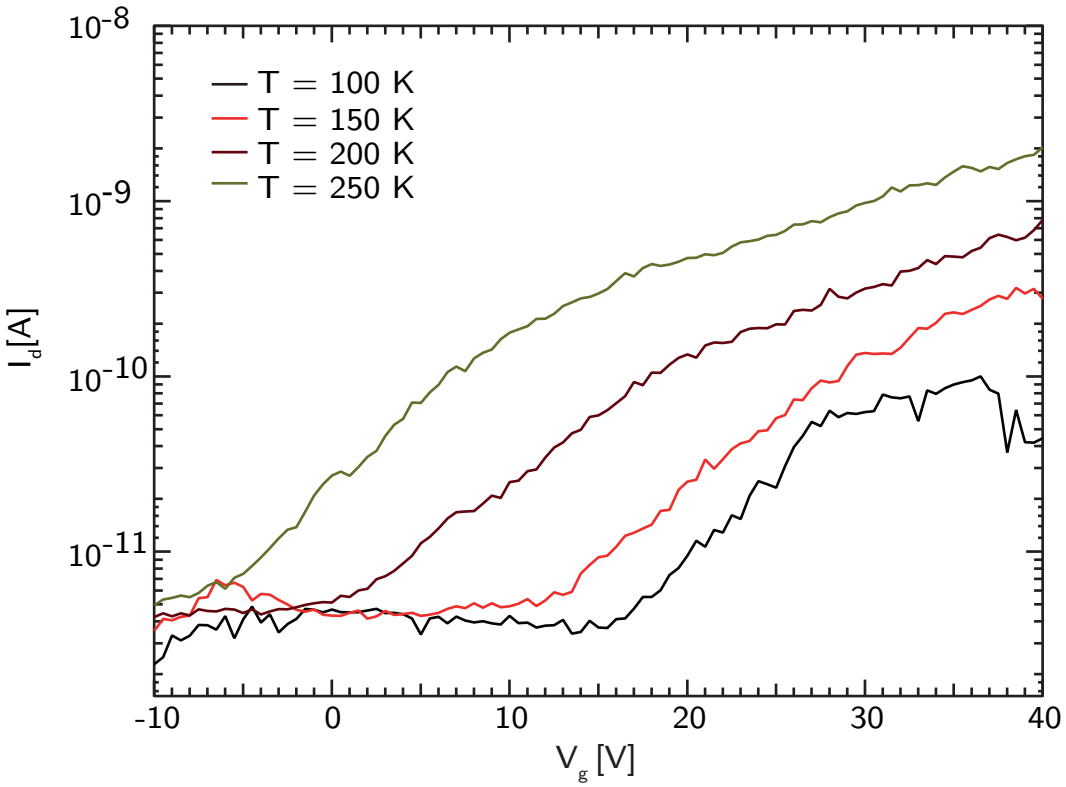

Figure 4.12: Transfer characteristics of device P2 for the temperature range between 100-250 K. Below the flatband voltage V_{FB} only termionic emission $I_{thermionic}$ determines the current flow through the device.

$$I_d = AT^{3/2} e^{\frac{-q\Phi_B}{k_B T}} (e^{\frac{qV_{ds}}{nk_B T}} - 1) \tag{4.1}$$

In equation 4.1 I_d is the current through the device, A is Richardson's constant, k_B is the Boltzmann constant, q is the electronic charge, T is the temperature and V_{ds} is the source to drain bias. However, in order to obtain an appropriate result, a simplified formula had to be used. The different curves, each referring to the same gate voltage, were fitted with the following equation in order to extract the effective Schottky barrier height:

$$I_d = T^{3/2} e^{\frac{-q\Phi_B}{k_B T}} K \tag{4.2}$$

In equation 4.2 the second bracket as well as the Richardson's constant A of equation 4.1 contribute to constant K. This can be seen as a reasonable simplification, because all variables within K are independent of the applied gate voltage and can therefore be assumed to be constant. In addition, the nonideal factor n as well as the series resistance of the transistor are unknown. The I_d versus $1000/T$ plot with the corresponding fitting functions are displayed in Figures 4.13 and 4.15, respectively. To get the flat band voltage V_{FB}, the variables Φ_B of the fitting functions have to be plotted against the inherent gate voltages V_g. This plot (see Figure 4.13) has to be analysed in order to extract the Schottky barrier height for a device. For small negative gate voltages, the effective barrier height linearly responds to the gate voltage V_g, which is apparent in the fact that only $I_{thermionic}$ determines the current flow through the device. When Φ_B starts to aberrate from the linear behaviour, $I_{tunneling}$ starts to come into play and V_{FB} is reached. Figures 4.14 and 4.16 show the Φ_B versus V_g plot for devices P1 and P2. The flat band voltage V_{FB} for device P1 and P2 was extracted as being 0 and 20 volts, which results in effective Schottky barrier heights of $0.12eV$ and $0.0445eV$, respectively. The calculated Schottky barrier height of device P2 matches very well with results from S. Das et al. [19] for transistors with Ti/Au contacts that have only a few layers.

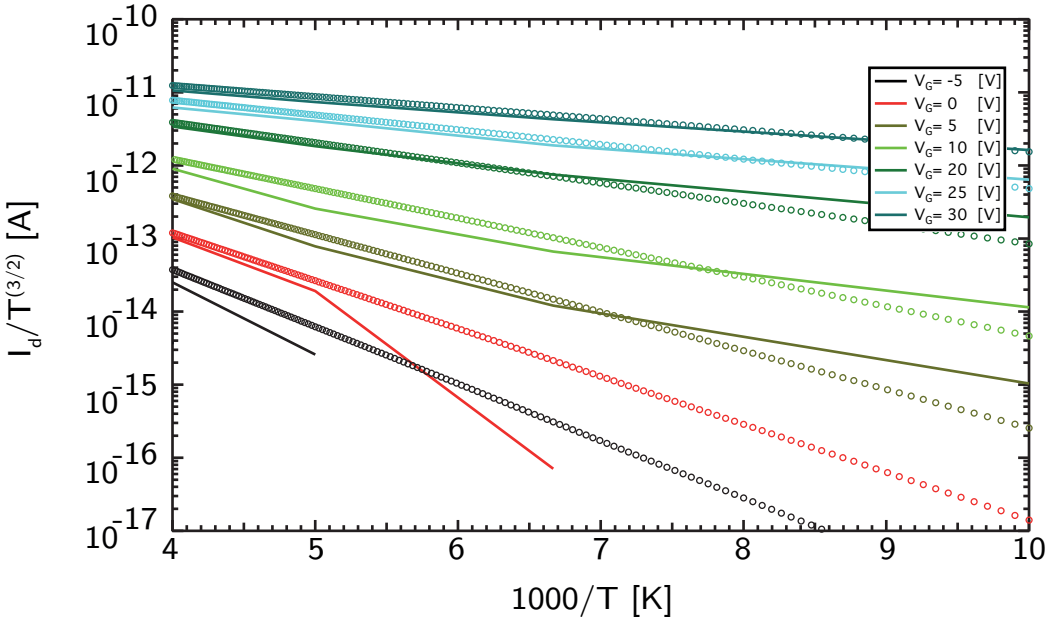

Figure 4.13: I_d versus $1000/T$ for device P1. The solid lines show the measured data and the circles show the fitting function.

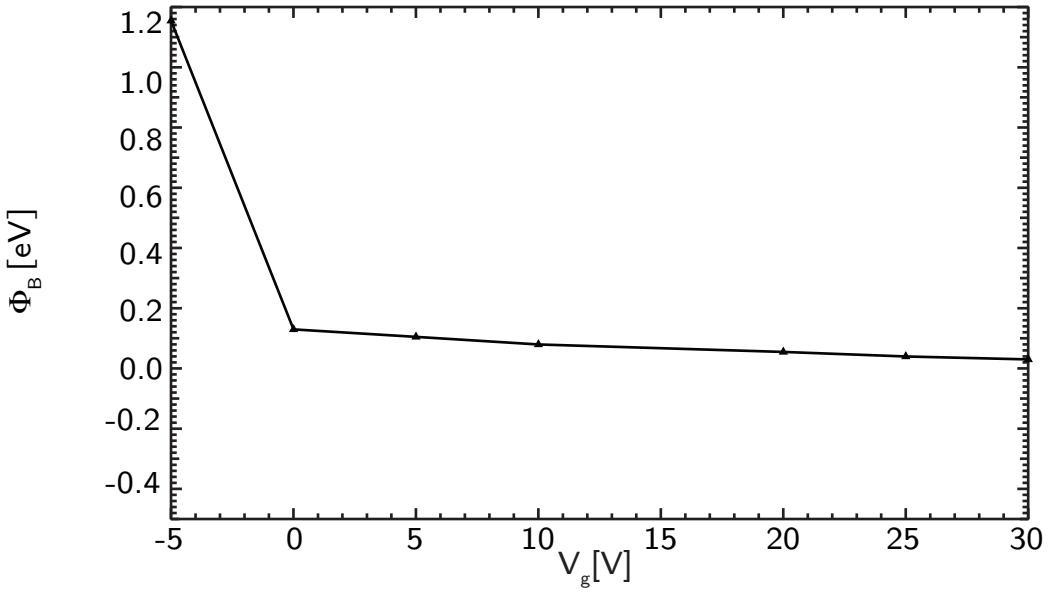

Figure 4.14: Φ_B versus V_g for device P1 for gate voltages ranging from -5 to 30 volts. The flatband voltage V_{FB} was assumed to be $0.12eV$.

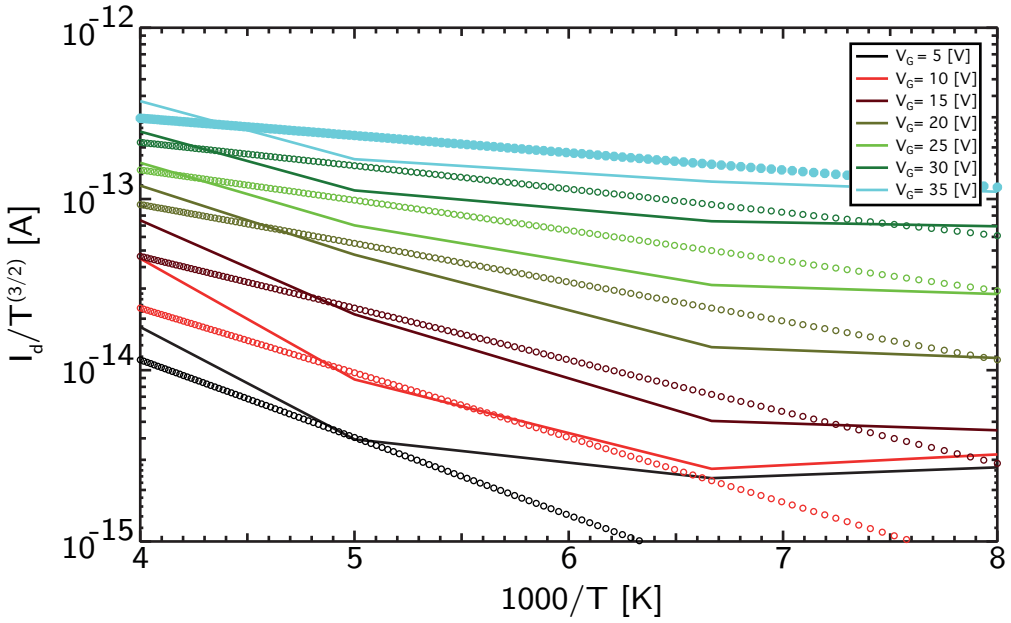

Figure 4.15: I_d versus $1000/T$ for device P2. The solid lines show the measured data and the circles show the fitting function.

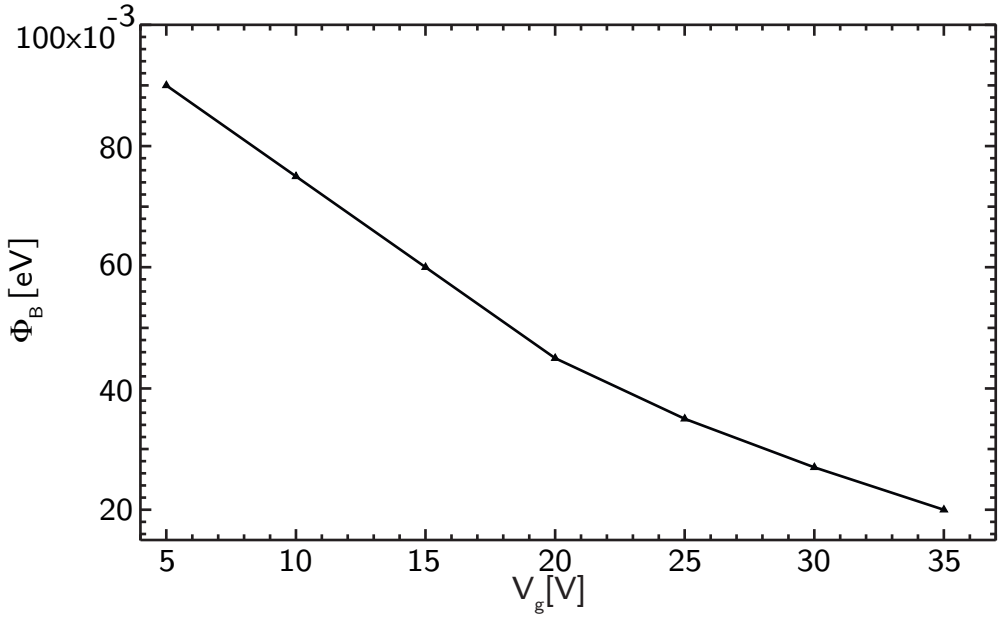

Figure 4.16: Φ_B versus V_g for device P2 for gate voltages ranging from 5 to 35 volts. The flatband voltage V_{FB} was assumed to be $0.0445eV$.

4.5 Electrical characteristics of MoS_2 with MoO_x contacts

A novel contact material, MoO_x was used to investigate the performance of transistors which are contacted with this material. For this purpose, MoS_2 transistors with a 30 nm thick MoO_x layer that was topped with a 30 nm thick palladium layer were built. The procedure is described in chapter 3.3.2.2. Figure 4.17a and b shows the MoO_3 powder and the final transistor M1, respectively.

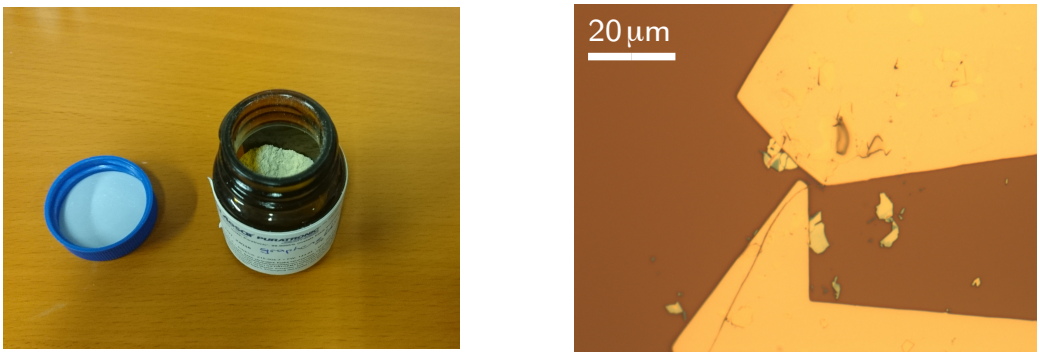

Figure 4.17: (a) MoO_3 powder (b) Picture of the transistor M1.

The transfer characteristics as well as the characteristic output curve are displayed in Figures 4.18a and b, respectively. The transfer characteristics show that the annealing procedure improved the performance of the device. After annealing, the mobility was calculated to be $0.6 cm^2 V^{-1} s^{-1}$. The characteristic output curve shows ohmic behaviour, which is an indicator for low Schottky barriers, as described in more detail in chapter 2.2.3. Chuang et al. [20] documented that a device with a MoS_2 channel and MoO_x contacts shows p-type transistor behaviour. Such a hole conductance is a crucial criteria for the fabrication of light emitters for example, which is why MoO_x with its high work function of $6.6 eV$ [56] can be seen as a promising material to enable p-type transistor behaviour in a MoS_2 transistor. However, the transfer characteristics (Figure 4.18a) clearly reveal that the device measured within the framework of this masterthesis does not show hole conductance.

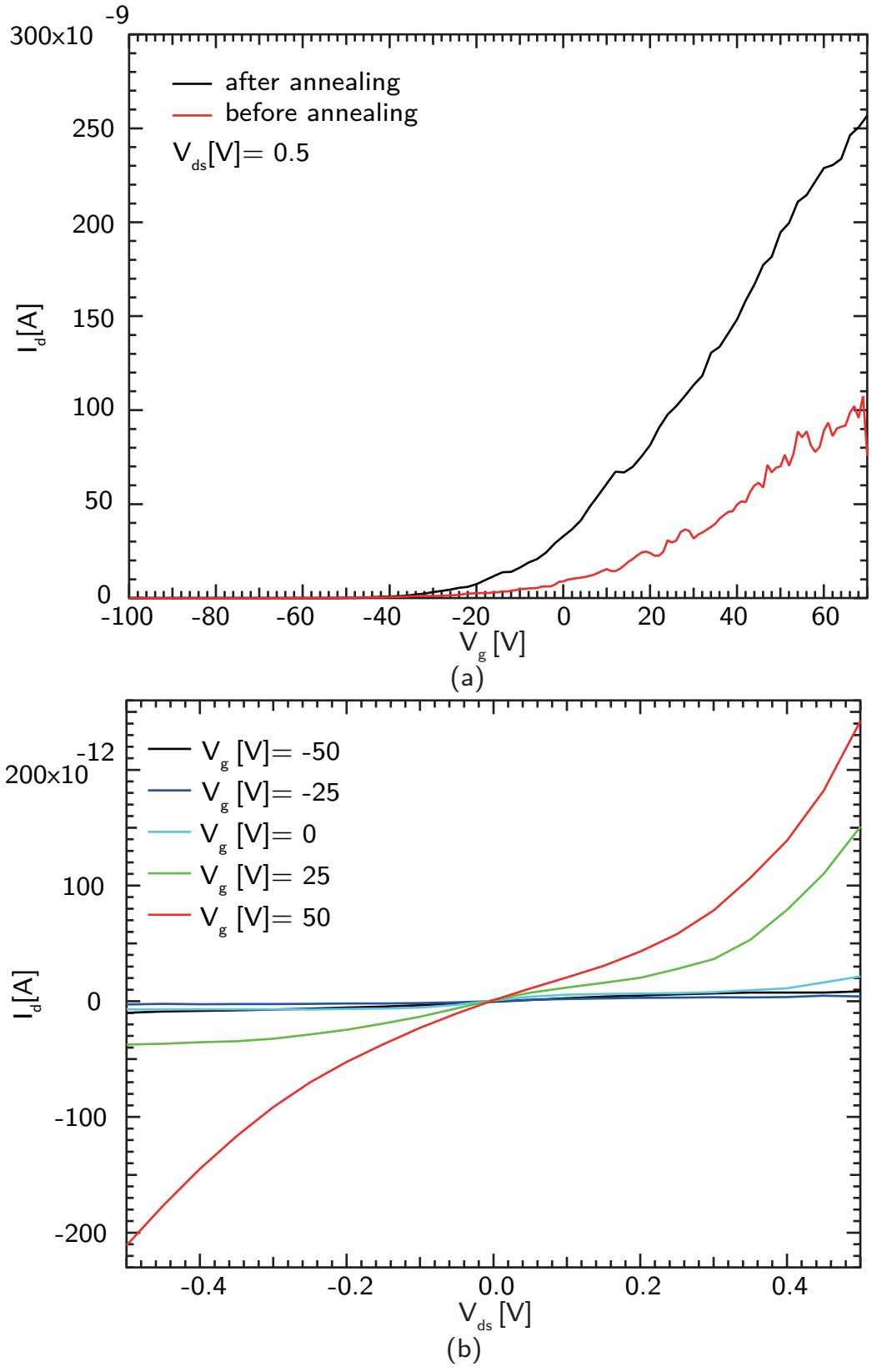

Figure 4.18: (a) Transfer characteristics of device M1. (b) Characteristic output curve of device M1.

5 Conclusion

Within the framework of this master thesis, WSe_2 and MoS_2 transistors were fabricated and characterised. Mechanical exfoliation was used for both of these TMDCs to separate atomically thin layers from their bulk crystals. In case of WSe_2, the flakes were transferred on a Si/SiO_2 wafer and subsequently measured by using photoluminescence and Raman measurements in order to obtain information about their thickness. The interpretation of these two measurements suggests that in device P1 the channel is a bulk piece of WSe_2, whereas in device P2 the channel is a monolayer of WSe_2. Electrical contacts were fabricated with the help of electron beam lithography. This was followed by electron-beam evaporation of Ti/Au contacts. After the transistors had been processed, their electric properties were measured in a needle prober station connected to a semiconductor parameter analyser. Device P1 showed p-type as well as n-type transistor behaviour, whereas device P2 only showed n-type transistor behaviour. This is demonstrated by the fact that the monolayer WSe_2 has a much bigger band gap as compared to the bulk WSe_2. It means that a higher Schottky barrier is formed at the interface and a higher gate voltage has to be applied in order to enable the electrons to overcome the barrier. The mobilities calculated from the transfer characteristics for devices P1 and P2 are 0.53 and 0.009 $cm^2V^{-1}s^{-1}$, respectively. Both of them are rather low.

After the measurements conducted at 300 K, temperature-dependent measurements were made for temperatures ranging from 100-380 K. All the transistors showed higher currents as well as mobilities with increasing temperatures. The highest mobility and device currents were obtained for devices P1 and P2 at 380 and 370 K, respectively. With increased temperature, the transistors' threshold voltage shifted to lower values of the gate voltage V_g. This is logical in view of the fact that charge carriers have higher kinetic energy at higher temperatures

and thus are more likely to overcome a barrier at the semiconductor metal interface. In addition, the Schottky barrier height was extracted by using a so-called Arrhenius plot, whereby Schottky barrier heights of devices P1 and P2 were calculated as 0.12 eV and 0.0445 eV, respectively. This is in agreement with the theoretical knowledge that the band gap of monolayered WSe_2 is bigger than that of bulk WSe_2 and hence the Schottky barrier that forms is also higher.

Moreover, a MoO_3 powder was used as evaporation source for the contactation of a MoS_2 flake. By using a molybdenum boat, the powder was thermally evaporated onto the sample, producing 60nm thick MoO_x/Pd contacts. Typical n-type transistor behaviour could be achieved, resulting in maximum currents of $258nA$ and a mobility of $0.6cm^2V^{-1}s^{-1}$.

In conclusion, it can be said that their physical properties make thin films of WSe_2 and MoS_2 promising candidates for various applications in future electronics and photonics. Research in this area has just begun, however, by exploiting these materials' extraordinary combination of properties such as high thermal stability, direct band gap, chemical inertness, transparency and mechanical flexibility, great progress lies ahead in this field.

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