TECHNISCHE UNIVERSITÄT WIEN
Vienna University of Technology

DISSERTATION

Strain Engineering in Intrinsic Silicon Nanowires using MEMS Devices

ausgeführt zum Zwecke der Erlangung des
akademischen Grades eines Doktors der technischen Wissenschaften

an der Technischen Universität Wien
Institut für Festkörperelektronik

unter der Leitung von

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Wien, Juni 2015 .....

Abstract

Strain engineering in silicon has a long tradition for more than sixty years. Soon it turned out that the piezoresistivity of silicon, i.e. the change of resistance under strain, is ten to twenty times higher than in e.g. metals. This finding made silicon a promising alternative for strain gauges with high sensitivity. Strained silicon became also an established expedient to increase the mobility and thus the performance of silicon transistors. With the steady miniaturization of silicon structures, in the last ten to fifteen years, research activities were expanded on silicon nanowires. Atypical effects found in nanowires like anomalous- and giant piezoresistivity have the capability to improve strain sensitive sensors dramatically. While doped nanowires have been intensely investigated in the last years, the piezoresistive behavior of intrinsic silicon nanowires was mostly neglected.

In this thesis the piezoresistivity of VLS grown intrinsic silicon nanowires is investigated under several measurement conditions to gain insight into the origin of the anomalous piezoresistive effect in such nanowires. Strain related electrical measurements on nanowires require an accurate and reliable mechanical characterization, which in turn requires the development of novel experimental strain engineering platforms. Such a platform was found in utilizing MEMS technology. In this work the design and manufacturing of an electrostatic actuated straining device (EASD) is presented which allows piezoresistive measurements in-situ in the scanning electron microscope, under cryogenic conditions and in the micro-Raman spectroscopy setup. Furthermore two different methods of nanowire integration into the EASD, i.e. monolithic- and "pick and place"-integration, are demonstrated. Spatial resolved noninvasive probing of the tensile strain applied to the nanowire was employed with micro-Raman spectroscopy. Due to the sophisticated design of the EASD, high strain levels can be achieved, enabling measurements of the nanowire piezoresistivity up to the fracture strain of the nanowire.

Measurements under ambient conditions exhibited an anomalous piezoresistive behavior of intrinsic silicon nanowires, i.e. although the nanowire appears to be p-type, the nanowire exhibits n-type piezoresistive behavior with increasing strain. Cryogenic measurements in vacuum verified the strong dependency of the piezoresistivity on surface traps in <111> oriented silicon nanowires. This behavior is a result of a strain induced modulation of the surface potential, leading to an electron depopulation of the surface traps. The resulting change of the charge carrier majority type leads to the altered piezoresistive behavior of the nanowire.

For piezoresistive measurements of the <111> oriented nanowire under 532 nm laser excitation, a piezoresistive behavior dominated by a combination of the n- and p-type piezoresistive effects, was observed. Surface related effects played only a minor role. The occurring photo current exhibited a laser power and strain dependency, i.e. increasing laser power as well as strain increased the photo current in the nanowire.

A Raman spectroscopy investigation of a <112> oriented nanowire revealed the existence of polytype structure domains inside the nanowire caused by periodic crystalline stacking faults. The resistivity of this nanowire was about ten times smaller compared to the resistivity of <111> oriented nanowires. The piezoresistive measurement exhibited only a weak dependency on surface related effects.

Due to its versatility the EASD proved to be an excellent strain engineering platform for high strain experiments.

Kurzfassung

"Strain engineering" in Silizium hat eine mehr als sechzig jährige Tradition. Schnell stellte sich heraus, dass die Piezoresistivität von Silizium, i.e. die Widerstandsänderung unter Verspannung, zehn bis zwanzigfach höher ist als in zum Beispiel Metallen. Diese Erkenntnis machte Silizium zu einer viel versprechenden Alternative als Dehnungsmesser mit hoher Sensitivität. Verspanntes Silizium wurde des Weiteren ein etabliertes Hilfsmittel um die Mobilität und dadurch die Leistungsfähigkeit von Silizium Transistoren zu verbessern. Mit der stetigen Miniaturisierung von Siliziumstrukturen erweiterten sich in den letzten zehn bis fünfzehn Jahren die wissenschaftlichen Untersuchungen auf Silizium Nanodrähte. Die in den Nanodrähten gefundenen atypischen Effekte wie die anormale Piezoresistivität und die Riesen-Piezoresistivität haben das Potential verdehnungssensitive Sensoren dramatisch zu verbessern. Während dotierte Nanodrähte in den letzten Jahren intensiv untersucht wurden, ist das piezoresistive Verhalten von intrinsischen Nanodrähten weitgehend vernachlässigt worden.

In dieser Dissertation wird die Piezoresistivität von VLS gewachsenen intrinsischen Siliziumnanodrähten unter verschiedenen äußerlichen Einflüssen untersucht um Einblick in den Ursprung der anormalen Piezoresistivität in diesen Nanodrähten zu gewinnen. Elektrische Messungen an Nanodrähten unter Verspannung benötigen eine genaue und zuverlässige mechanische Charakterisierung, welche wiederum die Entwicklung von neuartigen Experimental-Verdehnungseinrichtungen benötigen. Eine solche Einrichtung wurde durch die Anwendung der MEMS Technologie gefunden. In dieser Arbeit wird der Entwurf und die Fertigung einer elektrostatisch aktuierten Verdehnungseinrichtung (EASD) gezeigt, welche Piezoresistivitätsmessungen in-situ im Rasterelektronenmikroskop, unter kryogenen Bedingungen und im Raman Spektroskopie Aufbau ermöglicht. Des Weiteren werden zwei Arten zur Nanodraht-Integration in die EASD demonstriert, die monolithische Integration und die Integration durch ablegen und fixieren des Nanodrahtes. Räumlich aufgelöste nicht-invasive Messungen der am Nanodraht anliegenden tensilen Verspannung wurden mit Hilfe der Ramanspektroskopie durchgeführt. Aufgrund des ausgereiften Designs der EASD konnten hohe Verspannungen erzielt werden, welche die Messung der Nanodraht-Piezoresistivität bis zur Bruchspannung des Nanodrahtes ermöglichten.

Messungen an Atmosphäre zeigten ein anomales piezoresistives Verhalten der intrinsischen Siliziumnanodrähte, i.e. intrinsische Nanodrähte mit urpsprunglichem p-Typ Verhalten zeigten mit steigender Verspannung n-Typ piezoresistives Verhalten. Kryogene Messungen im Vakuum verifizierten eine starke Abhängigkeit der Piezoresistivität von den Oberflächenzuständen der <111> orientierten Nanodrähte. Dieses

Verhalten ist das Resultat einer durch Verdehnung verursachten Modifizierung des Oberflächenpotentials welche zu einer Ausschüttung der Elektronen aus den Oberflächenzuständen führt. Die daraus erfolgende Änderung der Ladungsträgermajorität führt zu einem geänderten piezoresistiven Verhalten des Nanodrahtes.

Für piezoresistive Messungen an einem <111> orientierten Nanodraht unter 532 nm Laseranregung wurde ein, von einer Kombination aus p- und n-Typ piezoresistiven Effekt dominiertes piezoresistives Verhalten beobachtet. Oberflächen bezogene Effekte spielten nur eine untergeordnete Rolle. Der auftretende Photostrom zeigte eine Laserlichtstärken- und Verdehnungsabhängigkeit, i.e. ein steigender Photostrom mit steigender Laserlichtstärke und Verdehnung.

Eine Ramanspektroskopieuntersuchung an einem <112> orientierten Nanodraht deckte die Existenz von Domänen polytyper Strukturen im Nanodraht auf, verursacht durch periodische kristalline Versetzungsfehler. Die Resistivität dieses Nanodrahtes war ca. zehnmal kleiner als die Resistivität von <111> orientierten Nanodrähten. Die Piezoresistivitätsmessung zeigten nur eine schwache Abhängigkeit von oberflächenbezogenen Effekten.

Durch seine Einsatzflexibilität erwies sich die EASD als exzellente "strain engineering" Plattform für Experimente unter hoher Verspannung.

Danksagung

Ich möchte hiermit jedem danken der mich auf meinem Weg durch diese Dissertation begleitet hat. Allen voran meinem Betreuer Alois, meinen Kollegen, meiner Familie Karl, Hilde, Johanna und Martin und ein besonderer Dank gebührt dir liebe Sandra.

Contents

Chapter 1

Introduction

With the capability to produce crystalline semiconductors like silicon and germanium with different doping types and concentrations and the subsequently realization of the transistor, a new age in electrical engineering started and was changing the world dramatically. Mechanical components and vacuum tubes were exchanged with solid state electronic devices, leading to a high reliability and a steady miniaturization of electronics. Silicon became by far the used material for integrated circuits in the semiconductor industry.

Long time before strained silicon was introduced into mature silicon processing technology the influence of mechanical strain on the electrical and optical properties of materials was part of material research since the steady increasing research on semiconducting materials in the early 1950s. The formulation of the theory of deformation potentials and mobilities in nonpolar crystals [1] as well as the first experimental description of the piezoresistive effect in germanium and silicon [2] exhibited the potential for new applications with these materials. As novel field of research, strain engineering in semiconductors was born. In the last decades extensive research on the interrelationship of strain and its effects on the material properties led to a better understanding how this effects are related to quantum physical properties of the strained material.

Strain alters the crystal symmetry and thus modifies the bandstructure, bandgap, effective mass and charge carrier concentration. Knowing the physical principles enabled the development of new electrical devices. Piezoresistivity - changing electrical

resistivity of a material due to applied mechanical stress - was quickly adopted to realize micro-electro-mechanical transducer sensors systems [3]. This strain effect, closely related to the silicon carrier mobility enhancement opened a new way to improve the transduction physics of silicon based transistors and ended in strained Si-CMOS [4–6]. Strained channel field effect transistors are a good example how strain engineering has succeeded the step from research into mass production in semiconductor industry [7, 8].

Applied elastic strain in materials and thereof resulting effects are limited by the maximum fracture stress of the material itself. Bulk silicon for example can only withstand yield stress lower than 3 GPa [9] without damaging the crystal structure. However, a down-scaling of the semiconductor dimensions increases the fracture stress limits at nearly the same Young's modulus [10]. The steady miniaturization and the ability to fabricate single-crystal quasi defect free nanowires, enabled new preconditions for piezoresistivity in silicon. E.g. vapor-liquid-solid (VLS) grown silicon nanowires with diameters below 200 nm exhibit fracture stress values of 12±3 GPa on average [11]. For germanium nanowires, even elastic uniaxial tensile strain values of 10 % and more have been demonstrated [12]. Thus, the application of crystalline nanowires in strain engineering is advantageous for the investigation at high strain levels implementing higher strain related effects.

With the reduction of the material dimensions to nanometric scale also the surface to volume ratio changes to a region where surface related transport effects play a significant or even dominating role. While the basic piezoresistive effect of bulk silicon for both n- as well as for p-doped silicon and its crystallographic anisotropy is well understood since the early 80s of the last century [13], piezoresistivity measurements at extremely high strain values on semiconductor nanowires reveled unexpected results. Especially after the discovery of a giant piezoresistive effect by He and Yang [14] in 2006, piezoresistivity in silicon nanostructures became a hot topic. The strong influence of doping as well as dimension of the silicon nanostructures on their piezoresistivity let presume surface related effects. Since then the origin of the giant piezoresistive effect is under debate [15–17]. Doped silicon nanowires exhibits the same piezoresistive behavior as for bulk silicon with respective doping type and crystallographic orientation. However the piezoresistive coefficient values are partly higher compared to bulk values [18, 19]. An exception was reported in 2010 by Lugstein et al. [20] demonstrating the anomalous piezoresistive effect in intrinsic silicon nanowires. Here an unexpected change in sign of the piezoresistive coefficient of <111> oriented silicon nanowires, was found for strain levels beyond 1%.

The characterization of nanowires in terms of strain engineering requires accurate and reproducible mechanical manipulation of the nanowire. First attempts with atomic force microscopy (AFM) setups or nano-manipulation stages [21–23] to apply mechanical stress on nanowires had the drawback of complex handling and positioning of nanometer-sized objects and the limited portability and thus incompatibility with other in situ characterization techniques e.g. cryostatic measurements. Another concept to induce strain into nanowires is the three- or four-point bending method [14, 24]. They appear to be more flexible with respect to portability, however with the drawback that shear forces on the nanowire have to be considered for such straining techniques.

A convenient technique to carry out strain engineering on nanowires are micro-electro-mechanical-systems (MEMS) [25–27]. The ability to apply pure uniaxial strain on individual nanowires combined with the compactness and portability of such devices make MEMS to versatile material characterization tools.

Hence, in this thesis a MEMS device was explored to investigate the anomalous piezoresistivity of intrinsic silicon nanowires in detail. An electrostatic actuated straining device (EASD) was fabricated which satisfies the requirements to perform different kinds of measurements under several environment conditions. Two different nanowire orientations, <111> and <112> were investigated. Measurements at ambient air and in vacuum at temperatures of 300 K down to 200 K as well as measurements under laser light excitation were carried out to reveal the nature and origin of the anomalous piezoresistivity in silicon nanowires.

Chapter 2

Theory

This chapter gives attention to the theoretical aspects for the work on strained silicon nanowires. The first section presents the basic physical-chemical properties of silicon followed by a section about nanowire synthesis. Further a short overview of the electronic properties of silicon is given with attention to surface induced carrier transport which is of particular interest for nanostructures. After discussing the theory of strain and stress, a mathematically description of the piezoresistance effect as well as its physical origins are given. Further the basic theory of Raman spectroscopy and particularly utilization for strain measurements is described. Finally the mathematically description of an electrostatic comb drive actuator for the EASD is presented.

2.1 The semiconductor silicon

Named after the Latin word *silex*, for flint, silicon was first mentioned by Antoine Lavoisier in 1787. In 1808 Sir Humphry Davy added the ending "-ium" to silicium in the belief the element is a metal. Between the first synthesis of pure amorphous silicon by Gay-Lussac and Thénard in 1811 and Berzelius in 1823, the chemist Thomas Thomson renamed the element in 1817 by changing the ending to "-on" similar to the nonmetal carbon. The first crystalline silicon was prepared in 1854

by Henri Étienne Sainte-Claire Deville [28].

Silicon as a group IV semiconductor with the atomic number 14 has four valence electrons and crystallizes in a diamond cubic crystal structure, with a lattice constant of 5.430710 Å. The diamond cubic crystal structure is defined by a face-centered-cubic (fcc) lattice with the basis {(0,0,0), (1/4,1/4,1/4)} as illustrated in figure 2.1. For better imagination, the diamond cubic crystal structure can also be constructed by shifting an fcc lattice against another one for a quarter of the space diagonal.

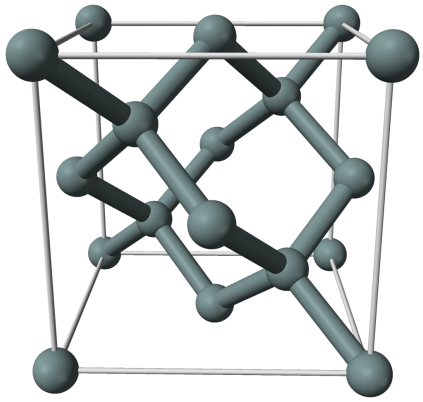

Figure 2.1: *Schematic illustration of the diamond cubic crystal structure of silicon.*

The band structure in figure 2.2 a) indicates that silicon is an indirect semiconductor with a bandgap with 1.107 eV at room temperature. Therefore a radiative recombination of electron and hole requires a phonon assisted transition which lowers the probability of such recombination drastically. The band diagram exhibits six equivalent valleys in the conduction band (2.2 b). The surfaces of constant energy in k-space are ellipsoids due to the different effective masses along longitudinal and transversal directions [29].

Intrinsic silicon is poorly conducting with a resistivity of $3 \cdot 10^5\ \Omega cm$ [30] at 300 K. By the insertion of impurities i.e. doping, the resistivity can be tuned over six orders of magnitude. A more detailed description of doping and its influence of the electrical properties is given in section 2.3.2.

Actually at ambient conditions silicon is reacting with oxygen to silicon dioxide (SiO_2), an isolator with a resistivity of about $10^{15}\ \Omega cm$ at 300 K. After the formation of a native SiO_2 layer on the silicon surface further oxidation is stopped since the oxygen atoms are not able to diffuse through the oxide layer at ambient condition. A self-passivating about 1nm thick oxide layer is formed on the silicon surface after an hour [31]. By increasing the temperature beyond 700 K, oxygen

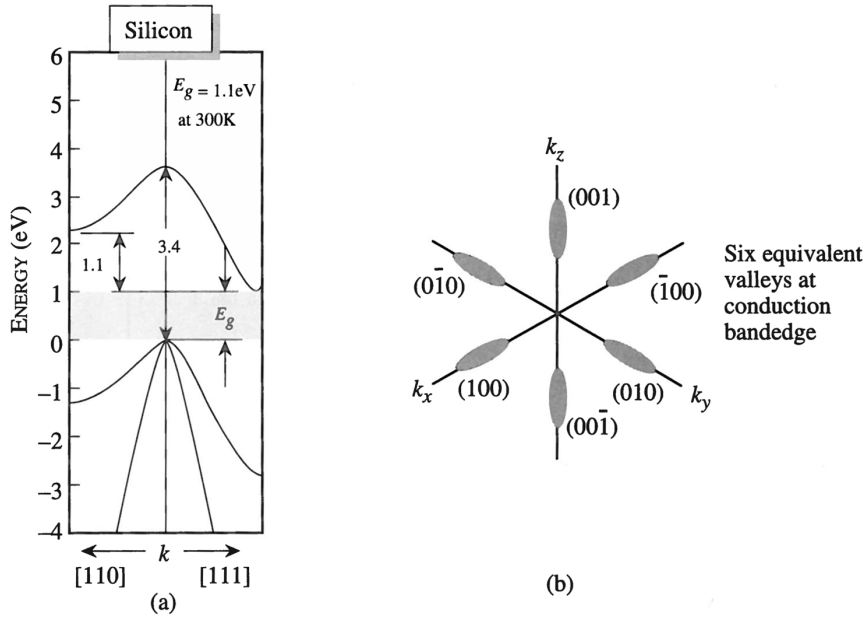

Figure 2.2: *a) Schematic of band structure of crystalline silicon and b) the six equivalent valleys with constant energy ellipsoids of silicon conduction band in the three dimensional k-space. [29]*

atoms are able to diffuse through the native oxide layer and thicker SiO_2 layers can be formed via thermal oxidation.

The possibility of tuning the resistivity of silicon by doping and the good isolating properties of its stable oxide, made silicon to the most important semiconductor material. Even the expression "Silicon Age" was created for the second half of the 20th century according to former material embossed ages like "Stone Age" or "Bronze Age".

2.2 Nanowire growth

Next to methods which etches nanowires out of bulk silicon [32] and the solid-liquid-solid mechanism [33], the VLS mechanism, introduced by Wagner and Ellis [34] in 1964, is one of the most common ways to synthesize single-crystalline silicon nanowires. While the first grown wires had micrometer scale, Westwater et al. [35] showed 1997 the synthesis of VLS grown silicon nanowires at nanometer scale. In figure 2.3 the synthesis of such silicon nanowires is illustrated.

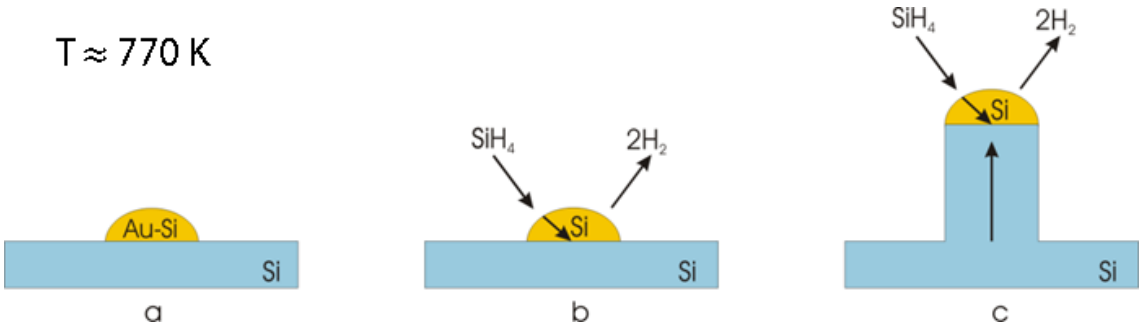

Figure 2.3: *Schematic illustration of the silicon nanowire synthesis using the VLS mechanism. a) The gold catalyst is deposited on the silicon substrate, b) the silane precursor gas is decomposed on the gold droplet surface and c) due to a supersaturation of silicon inside the droplet, a precipitation of crystalline silicon at the droplet/substrate interface leads to a directional growth of the silicon nanowire.*

The three terms in VLS represent the three aggregation states which silicon will pass through the nanowire synthesis. Necessary for the VLS mechanism are nanosized metal particles catalyzing the quasi 1D growth of silicon nanostructures. The most common catalyst material used for silicon nanowire synthesis with the VLS mechanism is gold. The catalyst is deposited on the silicon substrate surface in form of a thin gold layer, which will dewet at growing temperature and forms nanosized droplets to minimize their surface energy. Alternatively, nanosized collide particles can be directly deposited on the substrate surface (figure 2.3 a). The metal particles are melted and become liquid at the enhanced growing temperatures.
After heating up the substrate inside a low pressure chemical vapor deposition (LPCVD) reactor a semiconductor material containing precursor gas e.g. silane (SiH_4) will be inserted. The precursor gas represents the vapor phase of the semiconductor in VLS mechanism. The silane get decomposed at the catalytic gold droplet surface. Silicon atoms get absorbed and the remaining hydrogen volatilizes and will be pumped out of the LPCVD chamber (figure 2.3 b). The semiconductor material get incorporated in the catalytic particle, forming a liquid-alloy. This phase represents the liquid term of the VLS mechanism. Thus the silicon content inside

the liquid gold droplet increases until it supersaturates. Due to the supersaturation crystalline silicon will precipitate at the droplet/substrate interface lifting the droplet and forming a silicon nanowire (figure 2.3 c). The nanowire represents the solid term of VLS.

2.2.1 VLS growth engineering

By varying the growth parameters, the geometry as well as crystallographic orientation of the nanowire can be controlled. The metal particle size determines the nanowire diameter [36] while growth duration, temperature and partial precursor gas pressure determines the nanowire length [37]. The growth temperature depends on the precursor gas, the catalyzing metal and its eutectic temperature with the semiconductor. Growth rate increases with temperature and partial precursor gas pressure.

High growth temperatures lead to a preferred radial growth due to uncatalytic side wall deposition, leading to cone shaped, i.e. tapered nanowires. Also the occurrence of defects increases with temperature. At lower temperatures the axial growth is preferred and the nanowires exhibit rod-like shape with uniform diameter [35].

At low partial precursor pressure nanowires tend to growth in <111> crystallographic orientation while with increasing pressure the <112> crystallographic orientation is the energetic favored growing direction of the nanowires [38]. Normally at <111> growth direction, the largest decrease in Gibbs free energy occurs since (111) planes of silicon have the largest density of surface atoms when acting as interface. At very small diameters however the free energy of the side faces have to considered, leading to a change of the growth direction. When the diameter is below 20 nm also <110> oriented nanowires can occur [39].

By mixing the precursor gas with dopant containing precursor gases, i.e. diborane (B_2H_6) for p-type doping and phosphine (PH_3) for n-type doping, doped semiconductor nanowires can be achieved [40]. The doping gas will be decomposed on the catalyst surface in the same way as the silane, the dopant atoms become absorbed while the hydrogen volatilizes. These dopant atoms will be inserted into the crystal structure of the precipitated crystalline silicon by replacing silicon atoms.

2.3 Electronic properties of silicon

In this section basic semiconductor physics is reviewed with special attention to silicon. Further details on this topic can be found in textbooks like "Semiconductor devices: basic principles" from J. Singh [29].

As described in section 2.1, silicon is an indirect semiconductor with a band gap separating the conduction band and the valence band. Inside the band gap exist no energy states which can be occupied by electrons. Thus the electrons are situated in the conduction band and in the valence band. The amount of possible electron states per energy level in the bands is given by the density of states $N_e(E)$. Next to a free energy states, a probability that this states are occupied have to be given for the existence of electrons at a certain energy level. The occupancy is dependent on temperature and energy and is represented by the Fermi-Dirac distribution function $f(E)$. The energy at which the probability for an electron occupancy of 50% is given, is called Fermi level E_F. Density of states, occupation probability as well as carrier concentration in intrinsic silicon is illustrated in figure 2.4.

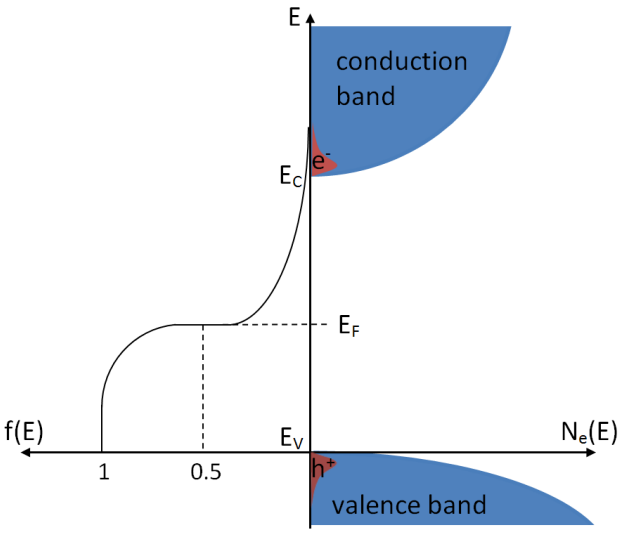

Figure 2.4: *Illustration of the blue colored density of states and the occupation probability for an intrinsic semiconductor. For energy levels in the conduction band where the density of states as well as the occupation probability are not zero, this red marked energy states are occupied with free electrons. In intrinsic semiconductors, the number of holes in the valence band has to be the same as free electrons in the conduction band.*

2.3.1 Intrinsic carrier concentration in semiconductors

The intrinsic carrier concentration is given by the electrons and holes in the conduction and valence band, respectively. The number of the conduction band electrons n is given by the integral over the electron density of states $N_e(E)$ multiplied with the Fermi-Dirac distribution function $f(E)$.

$$n = \int_{E_c}^{\infty} N_e(E) f(E) dE \tag{2.1}$$

Using the Boltzmann approximation, valid for small carrier concentrations like in intrinsic silicon, it is

$$n = N_c \, exp\left(\frac{E_F - E_c}{k_B T}\right) \tag{2.2}$$

with

$$N_c = 2\left(\frac{m_e^* k_B T}{2\pi\hbar^2}\right)^{3/2} \tag{2.3}$$

where N_c is the effective density of states at the conduction band edge, E_F and E_c are the Fermi level and the conduction band edge level, m_e^* the density of states effective electron mass, k_B the Boltzmann's constant, T the temperature and $\hbar$ the reduced Planck constant.

Similar as for electrons, the number of holes in the valence band p is given, under utilization of the hole distribution function, by

$$p = N_v \, exp\left(\frac{E_v - E_F}{k_B T}\right) \tag{2.4}$$

with

$$N_v = 2\left(\frac{m_h^* k_B T}{2\pi\hbar^2}\right)^{3/2} \tag{2.5}$$

where N_v is the effective density of states at the valence band edge E_v.

In intrinsic semiconductors the electron concentration has to be equal to the hole concentration since holes are available only when electrons are lifted from the valence to the conduction band. The intrinsic carrier concentration is given by the square root of the product of the electron and hole concentration ($n_i = \sqrt{np}$) and is dependent only on temperature and the bandstructure (bandgap and effective masses).

In thermal equilibrium it is

$$n_i = p_i = 2 \left(\frac{k_B T}{2\pi\hbar^2} \right)^{3/2} (m_e^* m_h^*)^{3/4} \, exp \left(\frac{-E_g}{2k_B T} \right) \tag{2.6}$$

with $E_g = E_c - E_v$ the energy bandgap. Semiconductors with large band gap have a lower intrinsic carrier concentration. Increasing the temperature rises the number of electrons excited into the conduction band and thus increases the carrier concentration. At 300 K silicon has an intrinsic carrier concentration of $n_i = 1.5 \cdot 10^{10} \, cm^{-3}$. The intrinsic Fermi level can be calculated with

$$E_{Fi} = \frac{E_c + E_v}{2} + \frac{3}{4} k_B T \, ln \left(\frac{m_h^*}{m_e^*} \right) \tag{2.7}$$

The Fermi level of an intrinsic semiconductor is located close to the center of the bandgap.

2.3.2 Extrinsic carrier concentration in semiconductors

As mentioned before the carrier concentration in intrinsic semiconductors is dependent on the temperature and the bandgap. To increase the number of free charge carriers at room temperature, doping of the semiconductor is necessary. Therefore foreign atoms will be inserted into the crystal structure of the semiconductor as shown in figure 2.5.

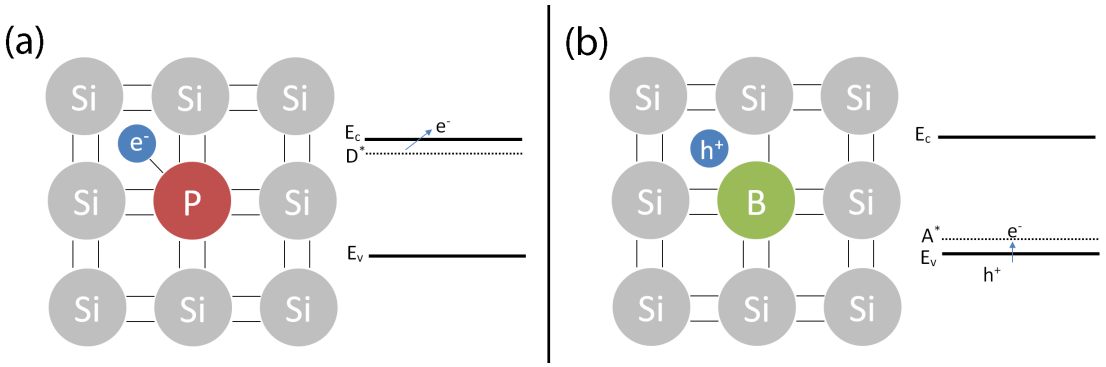

Figure 2.5: *Schematic of a silicon crystal structures with different dopant atom inserted and the respective band diagrams. (a) The phosphorus atom has an energy level close to the conduction band of the silicon. Hence it will be thermally ionized and the surplus electron can act as free charge carrier in the conduction band. (b) The boron atom has an energy level close to the valence band. Due to thermal energy an electron is lifted from the valence band to the boron energy level remaining a free hole.*

When silicon is doped with group V elements like phosphorus or arsenic, these dopant atoms are called donors. The energy states for such atoms are slightly below the energy level of the conduction band. The donor atoms are fully ionized by thermal energy even at low temperatures (>100 K) so that they donate their surplus electron to the conduction band 2.5(a). Electrons became the majority charge carriers and the semiconductor is called n-type doped.

By doping silicon with group III elements like boron, now the energy states of the so called acceptors are situated slightly above the valence band. Valence band electrons from the silicon atoms can now occupy the free bonds of the acceptor atoms leaving holes in the valence band of the silicon 2.5(b). When holes are the majority charge carriers the semiconductor is called p-type doped.

For doped semiconductors the free carrier concentrations n and p are no longer equal. Due to the law of mass action a relation between the carrier concentrations is given by

$$np = n_i^2 = constant \tag{2.8}$$

Now, again using the Boltzmann approximation, doping type dependent Fermi levels are calculated for n-type semiconductors according to

$$E_F = E_c + k_B T \; ln\left(\frac{N_D}{N_c}\right) \tag{2.9}$$

and for p-type semiconductors

$$E_F = E_v - k_B T \; ln\left(\frac{N_A}{N_c}\right) \tag{2.10}$$

N_D and N_A are the donor and acceptor concentration, respectively. The Boltzmann approximation does not hold for very high doping levels ($> 10^{20}\ cm^{-3}$). In this case, the semiconductor is called degenerated, the Fermi level is situated slightly below or in the conduction band and thus the semiconductor acts more like a metal but with still lower free carrier concentration.

2.3.2.1 Temperature dependency of the carrier concentration

While for intrinsic semiconductors the carrier concentration is directly dependent on the temperature and the bandgap, in extrinsic semiconductors the ionization of the dopants plays a major role. Figure 2.6 shows the electron density of n-type silicon with $N_D = 10^{15}\ cm^{-3}$ as a function of temperature revealing three distinct regimes. At low temperatures only parts oft the donor atoms are ionized. Some electrons are still bonded to their donor atoms and not available as free charge carriers. With increasing temperature the number of ionized donor atoms and hence the electron concentration increases. This regime where some donor atoms are still not ionized is called freezeout range. In the saturation regime all donor atoms are ionized and the electron density is equal to the donor concentration N_D. At even higher temperatures thermal energy is high enough that electrons from the the valence band are excited the conduction band. In this so called intrinsic regime, the electron density of extrinsic silicon is similar to that of intrinsic silicon.

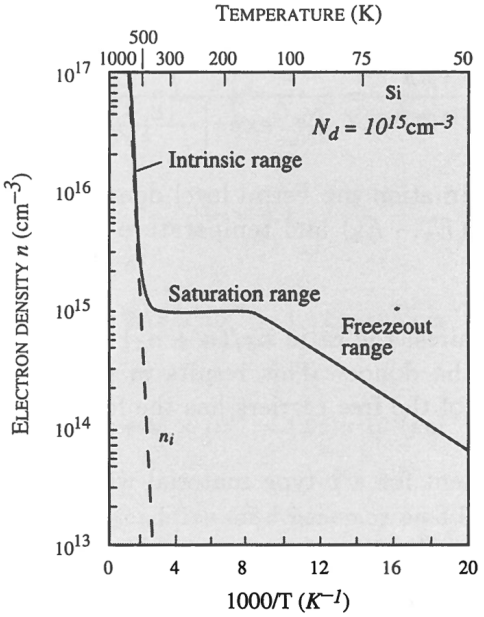

Figure 2.6: *Electron density as function of temperature for n-type silicon with* $N_D = 10^{15}\ cm^{-3}$. *For temperatures below 100 K, the donor atoms "freezes out" and are only partial ionized. The carrier concentration is proportional to the number of ionized donors. At room temperature all donor atoms are ionized. The carrier concentration "saturates" to the donor density. For temperatures above 500 K, electrons are thermally activated and can pass the band gap. The carrier concentration is similar to that of intrinsic silicon at respective temperatures.[29]*

2.3.3 Electric transport in semiconductors

Charge carrier currents in a semiconductor are a combination of carrier drift along an electric field and diffusion due to a concentration gradient. In this section the mathematical description for the current density in semiconductors is given.

In a perfect intrinsic semiconductor charge carriers will move without any scattering through the periodic potential of the crystal. However, in real semiconductors, carriers undergo different scattering events caused by e.g. ionized impurities (dopants), lattice vibrations (phonons) or due to surface roughness. Due to the scattering process the charge carries will gradually loss energy, momentum and finally coherence to its initial state values. The average time it takes to lose coherence is called relaxation time or scattering time τ_{sc}.

Under influence of an electric field $\mathcal{E}$ the electrons are moving opposite to the field direction and gain velocity until they scatter, losing their momentum. The average velocity of an electron is called the drift velocity v. From the Drude model the equation of motion is given by

$$m^* \frac{dv}{dt} + \frac{m^*}{\tau_{sc}} v = -e\mathcal{E} \tag{2.11}$$

with e the elementary charge and m^* the conductive effective mass.

In the steady state ($\frac{dv}{dt} = 0$) the drift velocity is given by

$$v = -\frac{e\tau_{sc}}{m^*}\mathcal{E} = -\mu\mathcal{E} \tag{2.12}$$

with the carrier mobility

$$\mu = \frac{e\tau_{sc}}{m^*} \tag{2.13}$$

Together with equation 2.12 the current density is given by

$$J = -nev = \frac{ne^2\tau_{sc}}{m^*}\mathcal{E} \tag{2.14}$$

with n the carrier concentration. In accordance with Ohm's law the conductivity σ and the resistivity ρ is given by

$$\sigma = \frac{ne^2\tau_{sc}}{m^*} = \frac{1}{\rho} \tag{2.15}$$

In case that both, electrons and holes are involved in carrier transport, the conductivity is given by

$$\sigma = ne\mu_n + pe\mu_p \tag{2.16}$$

where μ_n and μ_p are the mobilities for electrons and holes and n and p the respective carrier concentrations.

Hence the conductivity is directly proportional to the carrier mobility and concentration. The carrier concentration is dependent on the temperature, especially for intrinsic semiconductors. The carrier mobility is determined by temperature dependent scattering time and effective carrier mass. The effective mass m^* is derived from the bandstructure by

$$\frac{1}{m^*} = \frac{1}{\hbar^2}\frac{d^2E}{dk^2} \tag{2.17}$$

with E the energy and k the wave vector.

Therefore, mainly temperature and bandstructure define the conductivity (resistivity) of semiconductors.

Next to the drift current, another important transport mechanism is the diffusion of charge carriers. Carriers diffuse from regions of high concentration to regions with low concentration. The carrier flux is thus determined by carrier concentration gradient multiplied with the diffusion coefficient D.

$$\phi(x) = -D\frac{dn(x)}{dx} \tag{2.18}$$

According to the Einstein's relation D is given by

$$D = \mu \frac{k_B T}{e} \tag{2.19}$$

Now the overall current densities for electrons and holes in semiconductors under a certain field are given by

$$J_n = e\mu_n n\mathcal{E} + eD_n \frac{dn}{dx} \tag{2.20}$$

and

$$J_p = e\mu_p p\mathcal{E} - eD_p \frac{dp}{dx} \tag{2.21}$$

The equations above hold for homogeneous bandstructures, the bandgap is constant over whole semiconductor. In the chase of an inhomogeneous bandstructure, the bandgap of the semiconductor alters over the length due to e.g. a strain gradient or inhomogeneous material composition like in alloys, the current density equations have to be modified as described in [41] to

$$J_n = \mu_n n \left(\frac{dE_c}{dx} - k_B T \frac{dlnN_c}{dx} \right) + k_B T \mu_n \frac{dn}{dx} \tag{2.22}$$

and

$$J_p = \mu_p p \left(\frac{dE_v}{dx} + k_B T \frac{dlnN_v}{dx} \right) - k_B T \mu_p \frac{dp}{dx} \tag{2.23}$$

2.3.4 Generation and recombination of carriers in silicon

For semiconductors at finite temperature, thermal energy will excite electrons from the valence band to the conduction band leaving behind a hole in the valence band. This process is called thermal generation. In the same way electrons from the conduction band can recombine with the holes in the valence band. Under equilibrium the generation rate R_G equals the recombination rate R_R.

Generation of carriers also occurs when electrons leave the donor atoms or occupy acceptors generating holes in the valence band. In the reverse process again recombination of carriers can occur.

Next to the induction of thermal energy several other processes play an important role for electron hole generation and recombination. One mechanism is the carrier generation and recombination due to absorption and emission of light. When a photon, with energy $\hbar\omega$ larger than the band gap energy E_g, is absorbed by the semiconductor, an electron will be excited to the conduction band. Thereby also the crystal momentum k for electron and photon system has to be conserved. Since k-values of photons are essentially zero compared to k-values for electrons, the electrons k-value in conduction and valence band have to be the same. Thus only vertical k transitions are allowed in bandstructure diagrams as illustrated in figure 2.7 with a green arrow.

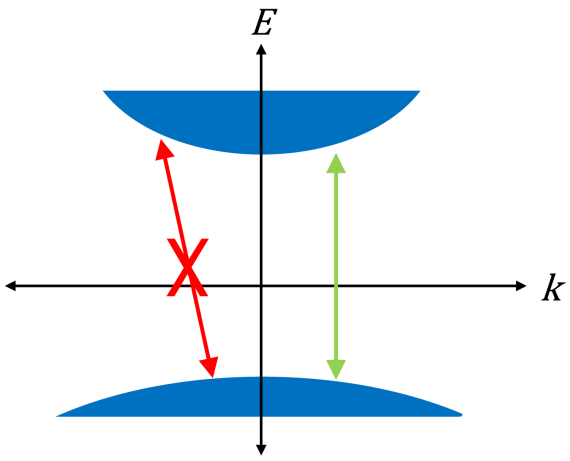

Figure 2.7: *Schematic illustration of allowed (green arrow) and forbidden electron transitions (red arrow) between conduction and valence band.*

In indirect semiconductors like silicon, where the minimum of the conduction band and the maximum of the valance band are situated at different crystal mo-

menta in k-space, electrons can be excited into the conduction band when the photon energy is higher than the direct band gap energy. But for radiative recombination (light emission) a lattice vibration (phonon) with k-value in the size of the difference between direct and indirect bandgap positions in k-space, is necessary. Radiative lifetime of carriers τ_r (time until the carrier recombines; $R_R \propto \frac{1}{\tau_r}$) in indirect transition is thus much higher than in direct transition. Therefore in silicon non-radiative recombinations with lifetime $\tau_{nr} < \tau_r$ have a higher probability.

2.3.5 Electron trapping and de-trapping in silicon

Real semiconductors have always unintentional impurities or native defects like vacancies that may produce electronic levels in the bandgap. These bandgap levels (trap levels) act as free states which electrons can occupy temporary. Transitions between valence and conduction band can take place by using the trap levels as an intermediate step. Non-radiative recombination of electrons from the conduction band to the valence band over trap levels is called Shockley-Read-Hall recombination and is the main recombination mechanism in silicon. The probability for a trap level to act as recombination center enhances the closer the trap level is situated to mid gap. Such traps with levels situated close to mid gap are called deep level traps.

Figure 2.8 shows the electron trapping and recombination in a semiconductor with a deep level trap. The four possible trapping/de-trapping processes as shown in figure 2.8(a) are explained in the following listing.

1. Electron trapping: A conduction band electron becomes trapped by occupying a free trap state. While it is trapped it does not participate to the carrier transport.

2. Electron de-trapping: An electron from an occupied trap state moves to the conduction band and is attended to the carrier transport.

3. Hole trapping: An electron from a trap state recombines with a hole from the valence band. The hole no longer participates to the carrier transport.

4. Hole de-trapping: An electron moves from the valence band to a trap state leaving behind a hole for carrier transport.

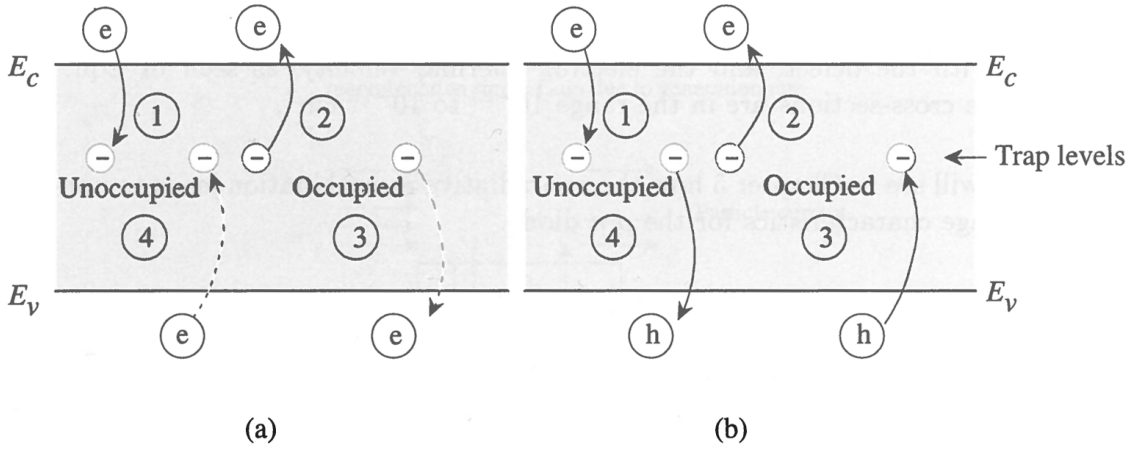

Figure 2.8: *Schematic of trapping and recombination of charge carriers in a semiconductor with a deep level trap. Processes 1 and 2 represent electron trapping and de-trapping and 3 and 4 hole trapping and de-trapping, respectively. (a) Trapping and de-trapping of carriers. (b) Recombination of carriers via trap level. [29]*

In a trap assisted non-radiative recombination the electron moves from the conduction band over a trap level (1) to the valence band (4) as shown in figure 2.8(b).

At the surface region of silicon, trap levels are also caused by dangling bonds, interface states and oxide states. In gold catalyzed VLS grown silicon nanowires the high surface to volume ratio causes a dominant surface related recombination while gold impurities caused deep level recombination can be neglected [42]. The surface recombination lifetime is direct related with the nanowire diameter d and the surface recombination velocity S [43] by

$$\frac{1}{\tau_{surf}} = \frac{4S}{d} \tag{2.24}$$

2.3.5.1 Surface related influence on the electrical transport behavior of silicon nanowires

Nanowires have due to their rquasi 1D geometry and nanoscale dimensions a large surface to volume ratio. Consequently the electrical properties are strongly influenced by the nanowire surface. Especially trapped charges of the Si/SiO_2 interface influences the charge carrier density of silicon nanowires. Derivation of the effective

carrier concentration in silicon nanowires as a function of the nanowire radius, doping concentration and interface charge density is given by [44] and is summarized on the following pages.

Charges at or close to the Si/SiO_2 interface can be subdivided into two categories, fixed oxide charges with a density Q_f and interface trap charges with a respective density Q_{it}. Only the interface trap charges interact via a charge transfer with the nanowire. Source of the interface trap charges are the interface trap levels with the level density D_{it}.The Interface trap level density typically vary between $D_{it} \approx 10^{10}\ to\ 10^{13} cm^{-2} eV^{-1}$. As origin of these interface traps, the so-called P_b resonance centers could be identified as trivalent silicon atoms bonded to three underlying silicon atoms [45].

The P_b centers are amphoteric. In the lower half of the bandgap they act as donors. When the Fermi level is located in the lower half of the bandgap (p-type silicon) P_b centers below the Fermi level (filled traps) are neutral while centers between Fermi level and mid gap (empty traps) are positively charged. In the same way the P_b centers act as acceptors in the upper bandgap half. If the Fermi level is located in the upper half of the bandgap (n-type silicon), the centers are negatively charged between Fermi level and midgap (filled traps) and neutral above the Fermi level (empty traps). The density of interface trap states is U-shaped with a region of nearly constant density $\pm 0.25\ eV$ around the midgap and increasing density beyond $\pm 0.25\ eV$.

As model for the effective charge carrier concentration determination an infinitely long homogeneously doped cylindrical nanowire is considered. Figure 2.9(a) shows schematically the radial band diagram of a circular slice of n-type silicon with interface traps of density D_{it}. The Fermi level E_F at the surface is located above midgap, corresponding with a positive surface potential φ_s. The trap levels between Fermi level and midgap will be occupied by electrons and become negatively charged. Since electrons provided by the conduction band (donors) will be consumed to charge the interface traps, the nanowire becomes depleted to an inner depletion radius $r = r_d$. Due to the missing charge carriers in the depleted region, the electrically relevant nanowire diameter r_{elec} becomes smaller than the real physical diameter r_{phys}. Figure 2.9(b) shows a schematic cross-section of a nanowire with depleted surface region.

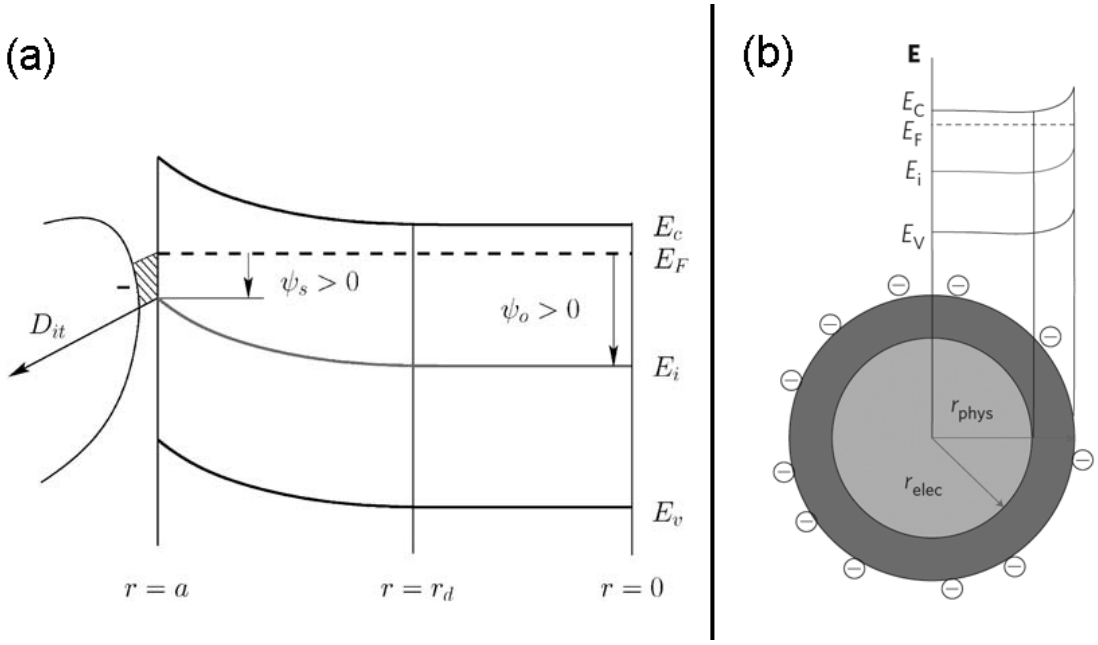

Figure 2.9: *(a) Schematic of the Si/SiO_2 interface bandstructure of an n-doped nanowire. The shaded area indicates the filled interface trap levels and negative surface charges. The nanowire is depleted in the region $r_d < r < a$. [44] (b) Schematic cross-section of a nanowire with depleted surface region (dark gray ring) due to the negative surface charges. [46]*

The corresponding surface potential φ_s is calculated by

$$\varphi_s = \varphi_0 - \frac{\varrho}{4\epsilon_s}\left(a^2 - r_d^2\right) \tag{2.25}$$

with φ_0 the potential in the non-depleted nanowire region, ϵ_s the dielectric constant of the nanowire, and $\varrho = q(N_D - N_A)$ the charge density in the depletion layer. The interface trap density, doping concentration and fixed surface charges determine the depletion grade of a silicon nanowire with a certain radius. For high trap level densities D_{it} and low doping, the Fermi level is pinned to the trap level center and Q_{it} can be expressed as

$$Q_{it} = -e^2 D_{it}\varphi_s \tag{2.26}$$

In this case the nanowire can be fully depleted over the whole diameter. For that purpose the nanowire radius a has to be smaller than a critical radius a_{crit} which can be approximated with

$$a_{crit} \approx \frac{2}{\varrho}\left(e^2 D_{it}\varphi_0 - Q_f\right) \tag{2.27}$$

For a silicon nanowire with a doping concentration of $N_D = 9 \cdot 10^{18}\ cm^{-3}$ and a trap density of $D_{it} = 2 \cdot 10^{13}\ cm^{-2}eV$ the critical radius is 20 nm.

Finally the effective electron carrier density is given by

$$n_{eff} = n_0\ exp\left(\frac{e\varphi_0}{k_B T}\right)\left\{\frac{r_d^2}{a^2} + \frac{4\epsilon_s k_B T}{e\varrho a^2}\left[1 - exp\ \left(\frac{e\varrho}{4\epsilon_s k_B T}\ (r_d^2 - a^2)\right)\right]\right\} \tag{2.28}$$

for a partial depleted nanowire and

$$n_{eff} = n_0\ exp\left(\frac{e\varphi_0}{k_B T}\right)\frac{4\epsilon_s k_B T}{e\varrho a^2}\left[exp\ \left(\frac{e\varrho a^2}{4\epsilon_s k_B T} - 1\right)\right] \tag{2.29}$$

for a fully depleted nanowire.

Aside of interface traps, chemical adsorbents have a huge influence on the electric transport in silicon nanowires. Especially for intrinsic nanowires, where the pinned Fermi level is close to midgap the Si/SiO_2 interface trap centers are symmetric around the Fermi level and the surface charges are neutralized. Then additional charges from chemical adsorbents are dominating the electrical transport.

Under ambient condition, water molecules will be adsorbed on the nanowire surface via dangling bonds. These water molecules may trap electrons from the silicon nanowire, resulting in OH^- ions. The negative charges on the surfaces of the silicon nanowire cause a band bending and therefore an accumulation of holes in the valence band as shown in figure 2.10. For p-type silicon nanowires the conductivity will thus be enhanced [47, 48] and for n-type silicon nanowires the conductivity will be reduced due to surface depletion [46]. For slightly n-doped nanowires even a change in transfer characteristic from n-channel field effect transistor (FET) to p-channel FET behavior is reported [47].

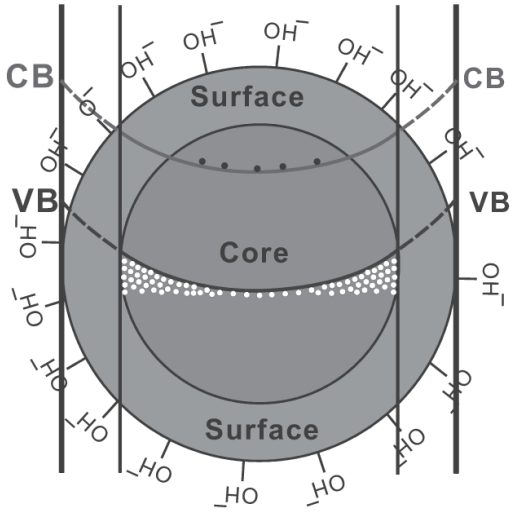

Figure 2.10: *Schematic band model of a silicon nanowire in ambient air. The adsorbed OH^- molecules cause band bending in the surface region leading to an accumulation of holes (white dots) in the valence band and a depletion of electrons (black dots) in the conduction band. [47]*

Due to this surface charge induced hole accumulation, intended intrinsic silicon nanowires show p-type semiconductor behavior [20, 40, 49].

2.4 The effect of strain on material properties

In this section the mathematical description of strain in crystalline materials is given and the influence of strain on material properties is discussed. For further information about strain effects in semiconductors, the textbook "Strain Effect in Semiconductors: Theory and Device Applications" by Sun et al. [50] is recommended.

2.4.1 Formal description of strain and stress

2.4.1.1 Strain

Strain in crystalline materials is defined as the relative lattice displacement due to deformation. Figure 2.11 illustrates the deformation of a simple 2D square lattice. The two unit vectors $\vec{x}$ and $\vec{y}$ fully describe the unstrained lattice. $\vec{x}\,'$ and $\vec{x}\,'$ are the modified vectors which arise under an th uniform deformation of the lattice both in orientation and length under consideration of the out of plane vector $\vec{z}$.

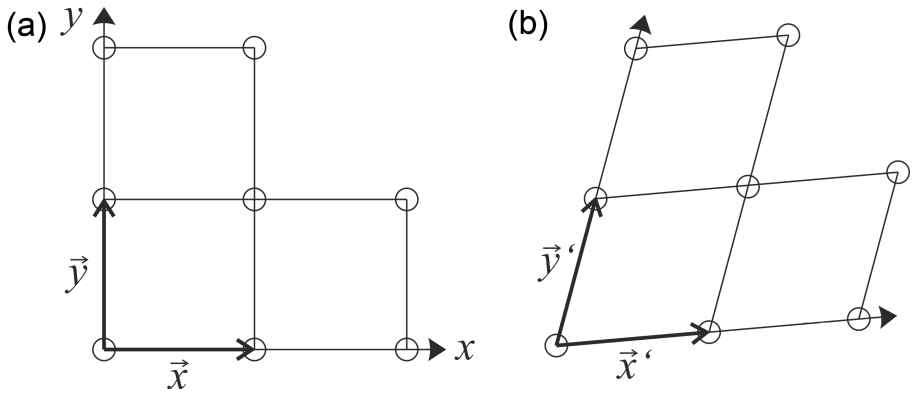

Figure 2.11: *Schematic of an (a) unstrained and (b) strained square lattice with corresponding unit vectors.*

The new vectors can be written as

$$\vec{x}\,' = (1 + \varepsilon_{xx})\vec{x} + \varepsilon_{xy}\vec{y} + \varepsilon_{xz}\vec{z} \tag{2.30}$$

$$\vec{y}' = \varepsilon_{yx}\vec{x} + (1 + \varepsilon_{yy})\vec{y} + \varepsilon_{yz}\vec{z} \tag{2.31}$$

In the case of a 3D lattice also the deformed vector $\vec{z}'$ has to be considered.

$$\vec{z}' = \varepsilon_{zx}\vec{x} + \varepsilon_{zy}\vec{y} + (1 + \varepsilon_{zz})\vec{z} \tag{2.32}$$

The dimensionless strain coefficients ε_{ij} can be arranged to a 3 x 3 matrix

$$\varepsilon = \begin{pmatrix} \varepsilon_{xx} & \varepsilon_{xy} & \varepsilon_{xz} \\ \varepsilon_{yx} & \varepsilon_{yy} & \varepsilon_{yz} \\ \varepsilon_{zx} & \varepsilon_{zy} & \varepsilon_{zz} \end{pmatrix} \tag{2.33}$$

which is called the strain tensor. A lattice point $\vec{r}$ will thus be transferred to $\vec{r}' = \vec{r} + \Delta\vec{r}$ with $\Delta\vec{r} = \varepsilon \cdot \vec{r}$. The strain tensor is symmetric, i.e. $\varepsilon_{ij} = \varepsilon_{ji}$. The antisymmetric elements ($i \neq j$) of the tensor represents a rotation of the lattice body.

In literature also engineering strain can be found often, which is another, slightly different mathematically description of strain. While length changes are defined in the same way as changes in volume

$$e_{ij} = \varepsilon_{ij};\ \forall\ i = j \tag{2.34}$$

the antisymmetric components are now defined as changes of the angle between the basic vectors. Second order terms are much smaller than 1 and will be neglected. Therefore the antisymmetric components are given by:

$$e_{ij} = \vec{i}' \cdot \vec{j}' = \varepsilon_{ij} + \varepsilon_{ji} = 2\varepsilon_{ij};\ \forall\ i \neq j \tag{2.35}$$

Strain is completely defined by six strain components which can be summarized to the array

$$\mathbf{e} = \{e_{xx}, e_{yy}, e_{zz}, e_{yz}, e_{zx}, e_{xy}\} = \{\varepsilon_{xx}, \varepsilon_{yy}, \varepsilon_{zz}, 2\varepsilon_{yz}, 2\varepsilon_{zx}, 2\varepsilon_{xy}\} \tag{2.36}$$

2.4.1.2 Stress

Stress is defined as the force (which deforms the crystal) in response to strain in an unit area. Figure 2.12 illustrates the nine components of the stress tensor σ on the basis of an infinitesimal volume cube. σ_{xi} for example represents a force per unit area applied in the direction x on a plane normal to $i = x, y, z$.

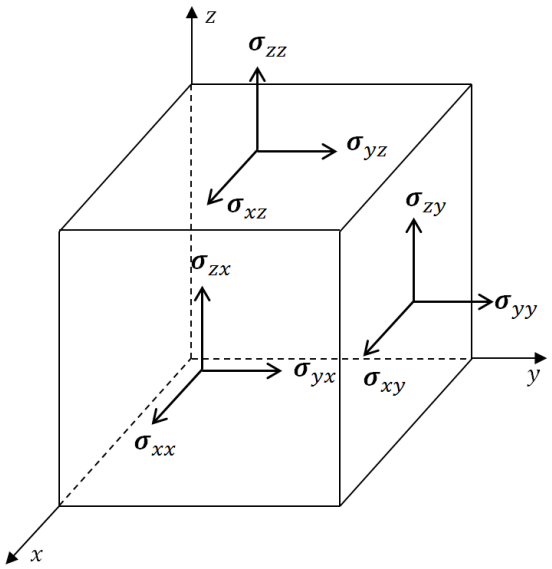

Figure 2.12: *Illustration of the nine stress components applied on the surface of an infinitesimal volume cube.*

The stress tensor can be arranged as a 3 x 3 matrix

$$\sigma = \begin{pmatrix} \sigma_{xx} & \sigma_{xy} & \sigma_{xz} \\ \sigma_{yx} & \sigma_{yy} & \sigma_{yz} \\ \sigma_{zx} & \sigma_{zy} & \sigma_{zz} \end{pmatrix} \tag{2.37}$$

or, due to its symmetry in the same way like the strain tensor, as a six component array.

$$\sigma = \{\sigma_{xx}, \sigma_{yy}, \sigma_{zz}, \sigma_{yz}, \sigma_{zx}, \sigma_{xy}\} \tag{2.38}$$

According to Hooke's law for elastic material, stress is proportional to strain by an elastic stiffness constant $C_{ij\alpha\beta}$.

$$\sigma_{ij} = \sum_{\alpha\beta} C_{ij\alpha\beta}\, e_{\alpha\beta}\,;\ i,j,\alpha,\beta = x,y,z \tag{2.39}$$

Due to the high symmetry in cubic crystals Hooke's law reduces to

$$\begin{pmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{zx} \\ \sigma_{xy} \end{pmatrix} = \begin{pmatrix} C_{11} & C_{12} & C_{12} & 0 & 0 & 0 \\ C_{12} & C_{11} & C_{12} & 0 & 0 & 0 \\ C_{12} & C_{12} & C_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & C_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & C_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & C_{44} \end{pmatrix} \cdot \begin{pmatrix} e_{xx} \\ e_{yy} \\ e_{zz} \\ e_{yz} \\ e_{zx} \\ e_{xy} \end{pmatrix} \tag{2.40}$$

and with the elastic compliance constant $S_{ij\alpha\beta}$ to

$$\begin{pmatrix} e_{xx} \\ e_{yy} \\ e_{zz} \\ e_{yz} \\ e_{zx} \\ e_{xy} \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{11} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{12} & S_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & S_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & S_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & S_{44} \end{pmatrix} \cdot \begin{pmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{zx} \\ \sigma_{xy} \end{pmatrix} \tag{2.41}$$

where the relations between S and C are

$$\begin{aligned} S_{11} &= \frac{C_{11} + C_{12}}{(C_{11} - C_{12})(C_{11} + 2C_{12})} \\ S_{12} &= \frac{-C_{12}}{(C_{11} - C_{12})(C_{11} + 2C_{12})} \\ S_{44} &= \frac{1}{C_{44}} \end{aligned} \tag{2.42}$$

The elastic stiffness constants for silicon are $C_{11} = 165.7$ GPa, $C_{12} = 63.9$ GPa and $C_{44} = 79.6$ GPa [51]. For an applied stress of magnitude P in [111] crystallographic direction, the stress tensor in the crystallographic coordinate system reads

$$\sigma_{[111]} = \begin{pmatrix} P/3 & P/3 & P/3 \\ P/3 & P/3 & P/3 \\ P/3 & P/3 & P/3 \end{pmatrix} \tag{2.43}$$

After inserting 2.43 in 2.41 the corresponding strain tensor becomes

$$\varepsilon_{[111]} = \frac{P}{3} \begin{pmatrix} S_{11} + 2S_{12} & \frac{S_{44}}{2} & \frac{S_{44}}{2} \\ \frac{S_{44}}{2} & S_{11} + 2S_{12} & \frac{S_{44}}{2} \\ \frac{S_{44}}{2} & \frac{S_{44}}{2} & S_{11} + 2S_{12} \end{pmatrix} \tag{2.44}$$

where the elements on the main diagonal are representing the hydrostatic strain and the other elements the shear strain. For a distinct crystallographic direction of stress and strain, they are linked by a scalar called Young's modulus Y_{ijk}.

$$Y_{[ijk]} = \frac{\sigma_{[ijk]}}{\varepsilon_{[ijk]}} \tag{2.45}$$

For silicon $Y_{[111]}$ is about 187 GPa [10].

2.4.2 Piezoresistivity in silicon

Piezoresistivity is defined as change of resistivity due to applied stress. The piezoresistance constant π is defined as

$$\pi = \frac{\Delta R/R}{\sigma} \tag{2.46}$$

where R is the initial resistance of the unstrained material, ΔR the stress induced change in resistance and σ the applied mechanical stress. The resistance of a material is given by

$$R = \varrho \frac{l}{wh} \tag{2.47}$$

with ϱ the specific resistivity of the material and l, w, and h denote the geometric dimension parameters length, width and height, respectively. The ratio $\Delta R/R$ can also be expressed as the addition and subtraction of the participating relative change terms.

$$\frac{\Delta R}{R} = \frac{\Delta l}{l} - \frac{\Delta w}{w} - \frac{\Delta h}{h} + \frac{\Delta \varrho}{\varrho} = (1 - 2\upsilon)\varepsilon_{||} + \frac{\Delta \varrho}{\varrho} \tag{2.48}$$

The geometrical terms of relative changes caused by the axial strain $\varepsilon_{||}$ can be summarized by the Poisson's ratio υ. In most common semiconductors, the resistance change due to geometric parameters can be neglected in comparison to the resistance change due to piezoresistive effects ($\upsilon_{Si[111]} = 0.262$ [52]). Hence the relative resistance change is equal the relative resistivity change ($\frac{\Delta R}{R} \cong \frac{\Delta \varrho}{\varrho}$). As for strain and stress, the symmetry in the cubic crystal system simplifies the relative resistivity change to a vector with six elements which is related to the stress vector by the piezoresistance tensor.

$$\frac{\Delta \varrho_i}{\varrho} = \sum_{k=1}^{6} \pi_{ik}\sigma_k \tag{2.49}$$

with

$$\pi_{ik} = \begin{pmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{pmatrix} \tag{2.50}$$

Due to the cubic crystal symmetry in silicon, the piezoresistance matrix consists of only three independent π coefficients. π_{11} depicts the piezoresistive effect along a principal crystal axis with stress applied along the same axis (longitudinal piezoresistive effect), π_{12} depicts the piezoresistive effect when stress is perpendicular to the principal crystal axis (transversal piezoresistive effect) and π_{44} represents the piezoresistive effect for shear stress. Kanda [13] calculated the π coefficients for moderately p-doped and n-doped silicon under tensile stress, which as shown in table 2.1.

doping type	n-type	p-type
ϱ $[\Omega cm]$	11.7	7.8
π_{11}	-102.2	+6.6
π_{12}	+53.4	-1.1
π_{44}	-13.6	+138.1

Table 2.1: *Piezoresistive coefficients* $[10^{-11}\ Pa^{-1}]$ *for n- and p-doped silicon at room temperature. [13]*

The Piezoresistivity is dependent on the doping concentration N and the temperature T of the silicon. High doping concentrations and increased temperatures led to a decrease of the piezoresistive coefficient. Figure 2.13 shows the piezoresistivity dependency on the basis of the multiplication factor P(N,T) which is defined as the π coefficient value at a certain temperature T divided by the value at $25^{\cdot}C$ for a certain doping concentration N.

In [111] crystal orientation of silicon the uniaxial piezoresistive coefficient $\pi_{[111]}$ is given by

$$\pi_{[111]} = \frac{(\pi_{11} + 2\pi_{12} + 2\pi_{44})}{3} \tag{2.51}$$

Hence, with the values from table 2.1 and at room temperature the uniaxial piezoresistive coefficients are $\pi_{[111]} = 93.5\ 10^{-11}\ Pa^{-1}$ and $\pi_{[111]} = -7.53\ 10^{-11}\ Pa^{-1}$ for moderate p- and n-doped silicon, respectively. Therefore resistance of n-doped silicon is decreasing (increasing) with tensile (compressive) strain while for p-doped silicon the resistance is increasing (decreasing).

Another common parameter which can be found in literature to characterize piezoresistivity is the gauge factor GF. The gauge factor is defined (with same assumption that dimension related resistance change can be neglected for silicon) by the following equation:

$$GF = \frac{\Delta R}{R\,\varepsilon} = \frac{\Delta \varrho}{\varrho\,\varepsilon} = \frac{\Delta \varrho\, Y}{\varrho\,\sigma} \tag{2.52}$$

Depending on crystal orientation, temperature, doping type and doping concentration the gauge factor of crystalline silicon can vary from -125 to +200.

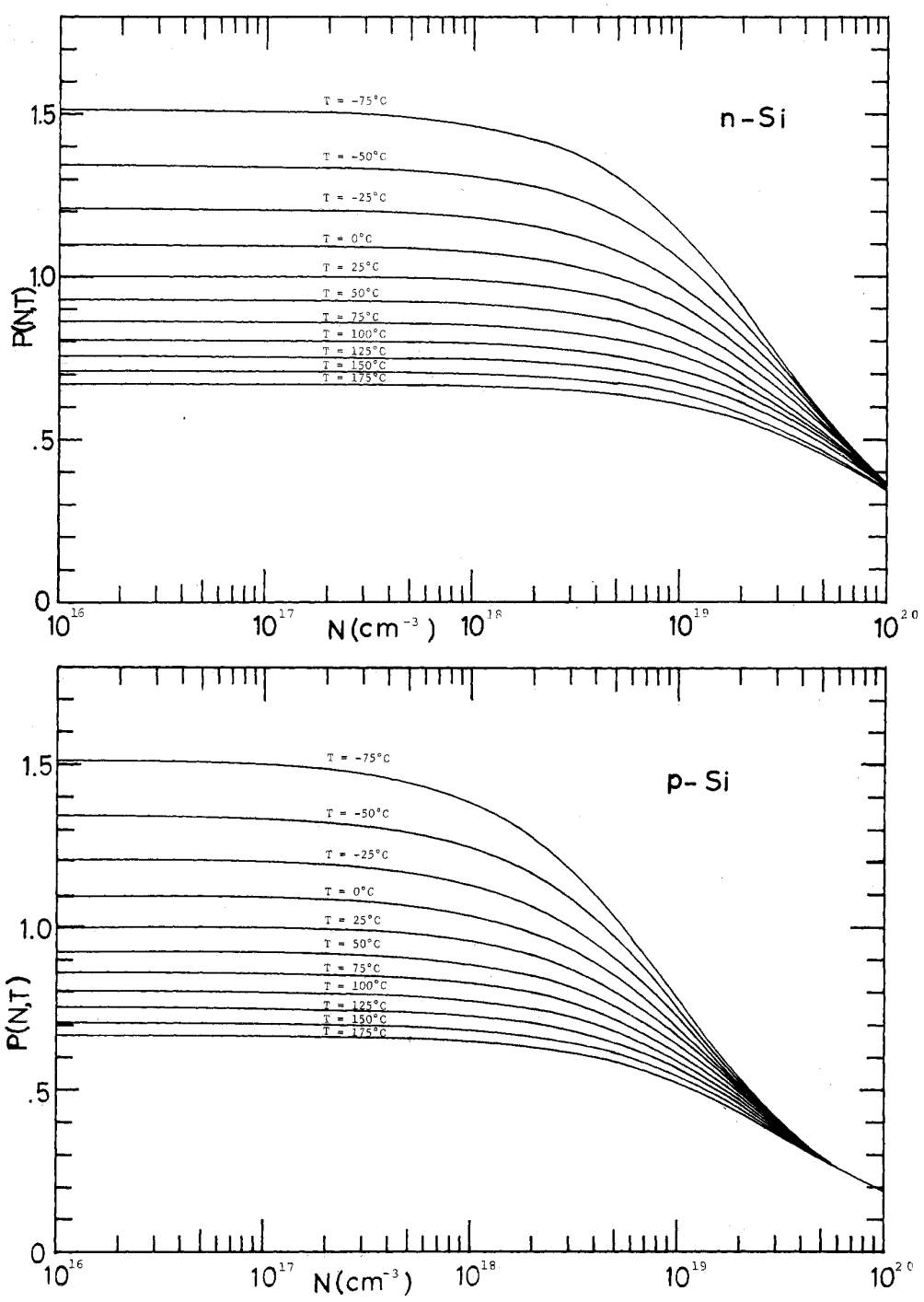

Figure 2.13: *Piezoresistance multiplication factor P(N, T) as a function of doping concentration and temperature for n- and p-type silicon. [13]*

2.4.3 Origin of the piezoresistive effect in silicon

Band degeneracies are defined by semiconductor crystal symmetry. When strain reduces the original symmetry some degeneracies are lifted and thus band splitting occurs. Under hydrostatic strain, the crystal symmetry will not be changed and has therefore no effect on lifting the band degeneracy. However the interatomic interaction increases or decreases when the atoms in the crystal lattice are approach each other or move further apart. Hence the hydrostatic strain changes the distance between conductive band and valence band, the semiconductor bandgap shifts. Compressive hydrostatic strain leads to a widening of the semiconductor bandgap while under tensile hydrostatic strain the bandgap diminishes.

For biaxial or uniaxial strain the cubic symmetry will be altered. Hence, both strains cause the valence band degeneracy lifting which provokes a split of the degenerate heavy hole (HH) and light hole (LH) valence bands in two separate bands. For the conduction band the effect of biaxial and uniaxial strain differs for the six conduction band valleys of silicon (figure 2.2b)). The four valleys along x and y (Δ_4 valleys) affects a different lifting as the two valleys along z direction ((Δ_2 valleys). As exception, in conduction bands with edges located not in the Γ point i.e. indirect semiconductors, uniaxial stress along [111] does not split the Δ valleys since again symmetry will not be altered.

With the introduction of the deformation potential theory by Bardeen and Shockley [1] and later, with the generalization including different scattering modes by Herring and Vogt [53], the strain induced band edge energy shift can be quantitative predicted by a linear relation of strain ε and energy shift ΔE with the deformation potential Ξ.

$$\Delta E = \sum_{ij} \Xi_{ij}\, \varepsilon_{ij} \tag{2.53}$$

Band energy shift can thus be described with three deformation potentials. For uniaxial strain along the [111] direction the hydrostatic strain components of the bands shifts can be calculated with [54]

$$
\begin{aligned}
\Delta E_{v,av} &= a_v(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) \\
\Delta E_c^{\Gamma} &= a_c^{\Gamma}(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) \\
\Delta E_c^{\Delta} &= a_c^{\Delta}(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) \\
a &= \left(\Xi_d + \frac{1}{3}\Xi_u\right)
\end{aligned}
\tag{2.54}
$$

The shear stress components are given by

$$
\begin{aligned}
\Delta E_{v,HH} &= \frac{1}{3}\Delta_0 - \frac{1}{2}\delta E_{111} \\
\Delta E_{v,LH} &= -\frac{1}{6}\Delta_0 + \frac{1}{4}\delta E_{111} + \frac{1}{2}\left[\Delta_0^2 + \Delta_0\delta E_{111} + \frac{9}{4}(\delta E_{111})^2\right]^{1/2} \\
\Delta E_{v,SO} &= -\frac{1}{6}\Delta_0 + \frac{1}{4}\delta E_{111} - \frac{1}{2}\left[\Delta_0^2 + \Delta_0\delta E_{111} + \frac{9}{4}(\delta E_{111})^2\right]^{1/2} \\
\delta E_{111} &= 2\sqrt{3}d\varepsilon_{xy}
\end{aligned}
\tag{2.55}
$$

In table 2.2 the values of the corresponding deformation potentials for silicon are given. Ξ_d is the hydrostatic deformation potential and Ξ_u is the shear deformation potential. The subscripts c , v , HH, LH and SO denote conduction-, valence-, heavy hole-, light hole and split-off band, respectively. The superscripts Γ and Δ denote the corresponding conduction band valley positions in the k-space.

a_v	a_c^{Γ}	a_c^{Δ}	Δ_0	d
2.46	1.98	4.18	0.04	-5.32

Table 2.2: *Deformation potentials of silicon. The subscripts v and c are indicating the valence and the conduction band and Δ_0 the spin-orbit splitting. The index av denotes the average of the respective band. The superscripts Γ and Δ denote the corresponding conduction band valley positions in the k-space. All values are in eV. [54]*

2.4.3.1 Piezoresistivity in n-type silicon

The piezoresistive effect is strongly dependent on the majority carrier type. In n-type silicon the Δ valley splitting for uniaxial stress in <100> and <110> direction is the

main cause of the piezoresistive effect. In figure 2.14 the population of the different Δ valleys is shown for uniaxial compressive stressed silicon (1+2), unstressed silicon (3) and uniaxial tensile stressed silicon (4+5).

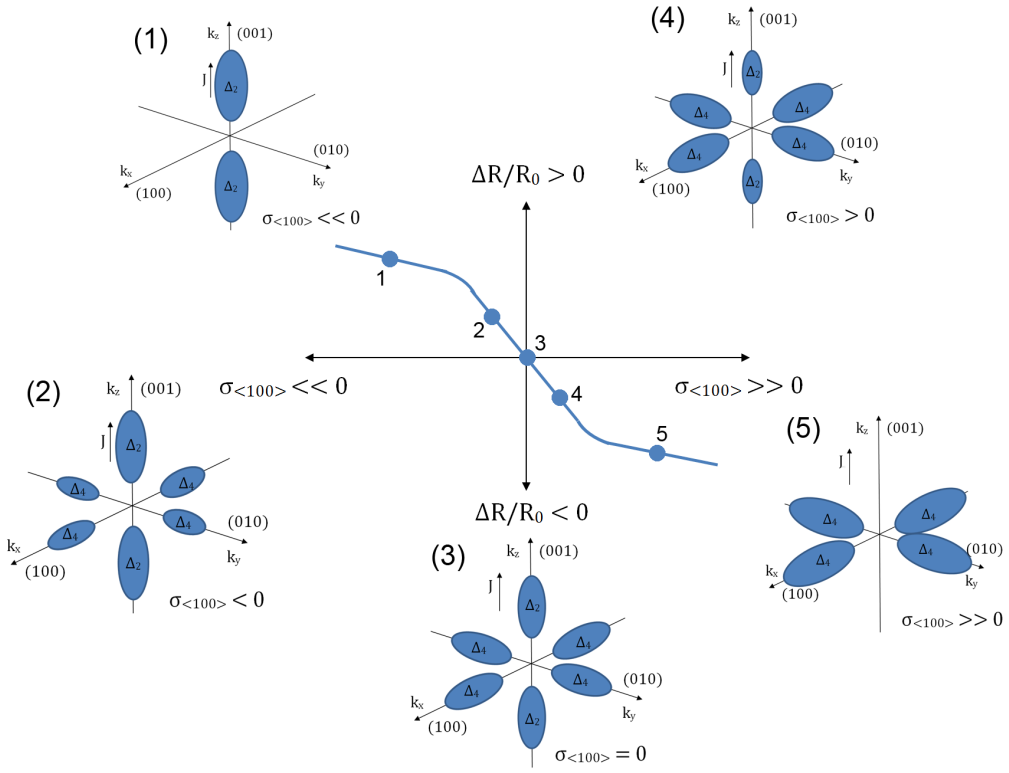

Figure 2.14: *Schematic of the six conduction band valleys and their population under <100> compressive (1, 2), without stress (3) and <100> tensile stress (4, 5). Under compressive stress, carriers are transferred from the Δ_4 valleys to the Δ_2 due to a degeneracy lifting of the energy valleys, and in consequence an increase in resistance occurs. Under tensile stress, carriers are transferred from the Δ_2 valleys to the Δ_4 leading to decrease in resistance. For both high tensile and compressive stress the piezoresistive effect saturates. In the center of the figure, the trend for the resistivity change as function of applied stress is illustrated. The numbers mark the cases described above.*

Without applied stress the six equivalent valleys along the <100> directions are degenerated and equally populated. Under compressive stress the longitudinal Δ_2 valleys shift downwards in energy relative to the four transverse Δ_4 valleys. Therefore the Δ_2 valleys become higher populated and the density of states effective mass changes. Since the parallel mass is bigger than the transverse mass, the resistance increases. When all carriers are transferred from the transverse Δ_4 valleys to the Δ_2 valleys the strong piezoresistive effect saturates.

At tensile stress the longitudinal Δ_2 valleys shift upwards in energy relative to the four transverse Δ_4 valleys. Here the carriers are transferred to the transverse Δ_4 valleys leading to a reduction of the parallel density of states effective mass and therefore a reduction of the resistance. After the transfer of all carriers into the transverse Δ_4 valleys the effect again saturates, the piezoresistive effect becomes the same as for uniaxial stress in the <111> direction.

At uniaxial strain in <111> direction only the bandgap energy will be altered but not the effective density of states at the conduction band edge N_c. According to equation 2.6 a tensile (compressive) strain induces a reduction (widening) of the bandgap and will thus increase (decrease) the carrier density and therefore decrease (increase) the resistance.

2.4.3.2 Piezoresistivity in p-type silicon

In p-type silicon, the piezoresistive effect is primarily caused by stress induced decoupling of the degenerated valence bands. The valence band structure of silicon comprehend three bands, the heavy hole, the light hole and the spin-orbit split-off band, where the first two are degenerated at Γ point ($k = 0$) (see figure 2.15(a)). The spin-orbit split-off band is shifted downwards by 4.4 meV and thus predominantly depopulated in comparison to the heavy and light hole band. Since charge carrier transport in p-type silicon takes place by a hole current, the conductivity σ_h is given by

$$\sigma_h = e^2\tau \left(\frac{p_{HH}}{m^*_{HH}} + \frac{p_{LH}}{m^*_{LH}} \right) \tag{2.56}$$

with e the elementary charge, p the hole concentration, τ the relaxation time and m^* the effective mass of the degenerated heavy holes HH and light holes HL. The stress induced resistivity change can be explained with hole transfer and mass change phenomena [55].

- **Hole transfer phenomenon:**
  In case of uniaxial tensile stress along the [111] crystallographic directions of silicon the heavy hole band moves up while the light hole band goes down in energy as illustrated in figure 2.15. Since holes in the valence band are filled beginning from the valence band edge, a hole transfer from the light hole band

to the heavy hole band take place. And since the effective mass of the heavy holes is higher than the conductive mass of the light holes ($m^*_{HH} > m^*_{LH}$), the hole conductivity according equation 2.56 will decrease resulting in an increase of the resistance.

- **Mass change phenomenon:**
  The mass change phenomenon has two origins. The first one is originated in the mixing of the approaching light hole band and spin-orbit split-off band leading to a stress dependent mass shift for light holes. The effective mass m^*_{LH} shift is inverse proportional to the applied tensile stress by a negative constant and thus the conductivity decreases with stress. The second mass change phenomenon is originated in the decrease of the interaction between heavy and light hole bands due the degeneracy lifting. At highly stressed silicon the coupling between the heavy and the light hole band is completely removed leading to the modification of the energy surfaces as shown in figure 2.15(b) and therefore a change in both heavy hole and light hole effective masses.

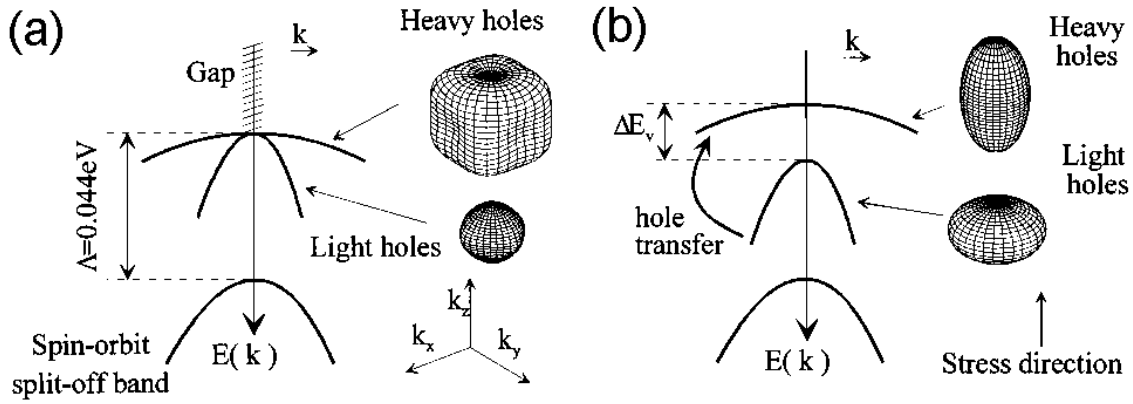

Figure 2.15: *Schematic of the valence band structure at the* Γ *point for (a) unstressed and (b) highly tensile stressed silicon and the corresponding energy surfaces. [55]*

The second mass change phenomenon affects only the transversal effective masses. In the case of uniaxial (longitudinal) stress, only hole transfer and the band mixing mass change phenomenon are influencing the effective masses and therefore the conductivity of silicon. Hence, the resistance of p-type silicon increases with increasing uniaxial tensile stress along the [111] crystallographic direction.

2.4.4 Piezoresistivity in silicon nanowires

Due to the large surface to volume ratio, surface related effects have a huge impact on the electrical behavior of silicon nanowires. The carrier concentration and therefore the resistivity in silicon nanowires is strongly affected by the trap states of the Si/SiO_2 interface and adsorbed molecules (see chapter 2.3.5.1). These effects exhibit a strain dependency and can be therefore seen as pseudo piezoresistive effects which determine, together with the classical piezoresistive effects described in the chapter above, the nanowire resistivity under strain.

He and Yang [14] reported a giant piezoresistive effect in VLS grown [111] oriented silicon nanowires with π_{111} values up to $3500 \cdot 10^{-11}\ Pa^{-1}$ for compressive stress. As shown in figure 2.16, for nanowires with high doping concentration and diameters above 200 nm the piezoresistive coefficient is approximately equal to bulk silicon with similar doping concentration. With decreasing nanowire diameter and decreasing doping concentration of the nanowire the piezoresistive coefficient increases rapidly.

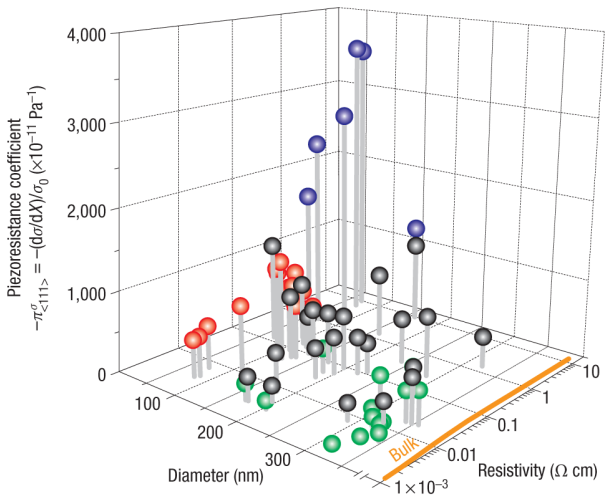

Figure 2.16: *Longitudinal piezoresistance coefficients of p-type silicon nanowires as function of nanowire diameter and resistivity. [14]*

Although He et al. suggest the origin of the giant piezoresistive effect in an enhancement of the carrier mobility, they also found hints for a surface dependency of the giant piezoresistive effect. Different chemical surface treatments exhibit conductivity changes of the nanowires showing the surface dependency. The doping concentration as well as the diameter dependency also indicates a surface related

effect on the transport carrier concentration.

In 2008 Rowe [16] discussed a possible origin for the giant piezoresistive effect in silicon nanowires measured by He et al.. The surface trap states of the Si/SiO_2 interface lead to a surface depletion region with a width dependent on the doping concentration. When the nanowire radius is below the critical value (see equation 2.27) this surface depletion region width can span the whole diameter leading to a fully depleted nanowire. Mechanical stress will alter the trap state levels [56] and the surface potential and therefore the surface depletion region width. Hence the conductive channel through the nanowire is controlled by the applied mechanical stress. Compressive stress narrows the depletion region width (widens the conductive channel) and increases the conductivity. On the contrary, tensile stress depletes the p-type nanowire more (narrows the conductive channel) and decreases the conductivity.

Yang and Li [57] measured a change in sign of the piezoresistive coefficient in [110] oriented p-type silicon nanobeams for thicknesses below 20 nm. They argued the origin of these effect with a tensile stress induced increase of electron trapping in the Si/SiO_2 interface and subsequent hole accumulation due to a surface potential shift. The resulting increase of charge carries exceeds the p-type bulk piezoresistive effect and decreases the resistivity of the silicon nanobeam.

The trapped charges at the surface act like a wrapped gate on the nanowire controlling the conductivity inside the nanowire. By applying an external back gate voltage on the nanowire the surface gate effect can be amplified or extenuated resulting in an increase or decrease of the gauge factor [17].

Finally Winkler et al. [58] measured the piezoresistive behavior of suspended intrinsic nanowires in a gate all around field effect transistor configuration with a transparent gate stack, demonstrating that giant and anomalous piezoresistance effects in VLS grown silicon nanowires are mainly determined by the filling or depopulation of surface states due to the stress induced modulation of the surface potential. By controlling the nature and density of these surface states via passivation the intrinsic piezoresistance of the nanowires is found to be a result of stress-induced carrier mobility change and comparable with that of bulk silicon.

2.5 Strain determination by Raman spectroscopy

The Raman effect, discovered in 1928 by Raman and Krishnan [59], relies on inelastic scattering of monochromatic light, usually from a laser source. The laser light interacts with optical phonons in solids or with molecular vibrations in gases or liquids, resulting in scattered light with shifted photon frequencies (Stokes and Anti-Stokes scattering) next to scattered photons with the same frequency (Rayleigh scattering) as the incident light. The frequency shifts of the scattered photons in comparison to the incident photon frequency represent the material specific energies of rotation-, vibration- and phonon processes and can be therefore used to determine physical properties of the material.

The Raman effect only occurs when the polarizability of the material changes with the rotation-, vibration- and phonon processes. A dipole moment p induced to a material by an external field E coming from a monochromatic light source can be described by:

$$p(t, E) = \alpha \; E_0 \; \cos(\omega_i t) \tag{2.57}$$

with ω_i the light frequency of the incident light and α the polarizability of the material. Since the polarizability is dependent on its current vibration state, it can be written as vibration normal mode $q_n(\alpha = \alpha(q_n))$. By performing a Taylor series expansion around $q_n = 0$ and describing q_n with a harmonic oscillator ($q_n = q_0 \; \cos(\omega_n t)$), the dipole moment is given by:

$$\begin{aligned} p(t, E) \; &= \alpha_0 E_0 \; cos(\omega_i t) \\ &+ \frac{1}{2} \left(\frac{\partial \alpha}{\partial q_n} \right)_0 \; q_{n0} E_0 \; \cos((\omega_i - \omega_n)t) \\ &+ \frac{1}{2} \left(\frac{\partial \alpha}{\partial q_n} \right)_0 \; q_{n0} E_0 \; \cos((\omega_i + \omega_n)t) \end{aligned} \tag{2.58}$$

The first term represents the Rayleigh scattering, the second term represents the Stokes scattering and the third term represents the Anti-Stokes scattering. For further, detailed information about the Raman effect, a textbook like Weber and Merlin [60] is recommended.

In silicon, first-order processes (i.e. processes involving a single phonon) access only excitations near the Γ-point ($q_n \approx 0$). Figure 2.17 shows the corresponding Raman spectrum of bulk silicon with the first-order (Anti-Stokes) Raman peak at 520 $rel.\,cm^{-1}$. Here the optic phonon is threefold degenerated. Such first-order Raman peaks can be fitted by Lorentz distribution functions.

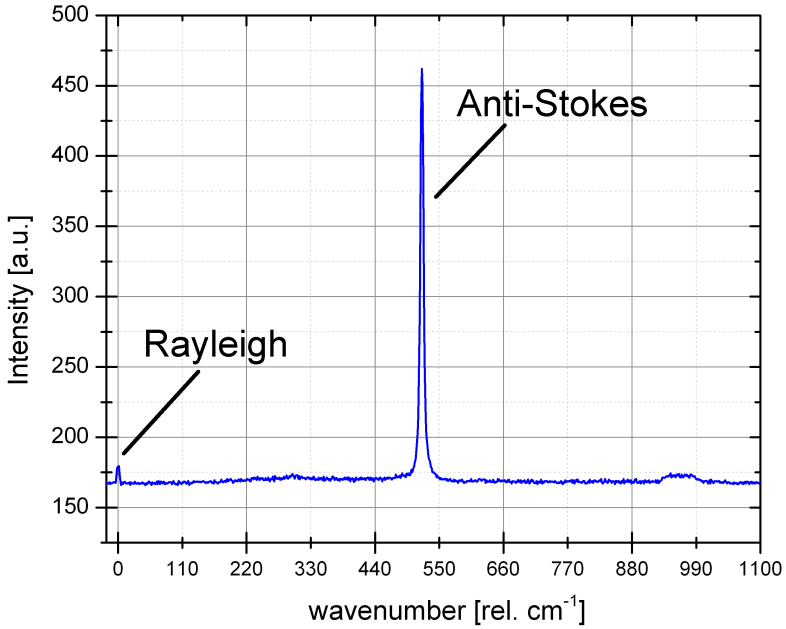

Figure 2.17: *Raman spectrum of bulk silicon with the Rayleigh peak at and the first-order optical phonon (Anti-Stokes) Raman peak at* 520 $rel.\,cm^{-1}$.

For uniaxial stress applied along the [111] crystallographic direction the threefold degeneracy of the $q_n \approx 0$ optical phonon is split into a singlet Ω_s with eigenvector parallel to the direction of the stress and a doublet Ω_d with eigenvectors perpendicular to the direction of the stress [61] which are given by:

$$\begin{aligned} \Omega_s &= \omega_0 + \Delta\Omega_H + \frac{2}{3}\Delta\Omega \\ \Omega_d &= \omega_0 + \Delta\Omega_H - \frac{1}{3}\Delta\Omega \end{aligned} \tag{2.59}$$

where ω_0 is the optical phonon frequency of relaxed silicon ($\omega_{0,Si} = 520\ rel.\,cm^{-1}$). $\Delta\Omega_H$ and $\Delta\Omega$ are the stress induced frequency shifts for the hydrostatic stress component and shear stress component, respectively which are given by:

$$\begin{aligned}\Delta\Omega_H &= \frac{P\omega_0}{6}(K_{11}+2K_{12})(S_{11}+2S_{12}) \\ \Delta\Omega &= \frac{P\omega_0}{2}K_{44}S_{44}\end{aligned} \tag{2.60}$$

where P is the uniaxial stress (see equation 2.43), S_{ij} are the elastic compliance constants of silicon and K_{ij} are the normalized phonon deformation potentials. With 2.59 and 2.60 it is obvious that optical phonon frequency shift and therefore the first-order silicon Raman peak shift is linear proportional to the applied stress. The proportionality factor k for silicon is given in literature with values in the range of $k = -336\ cm^{-1}$ to $k = -343\ cm^{-1}$ [62].

$$\Delta\Omega_s = \varepsilon_{[111]} \cdot k \tag{2.61}$$

Hence strain determination is feasible by measuring the first-order Raman peak shift. Tensile strain along the <111> directions of silicon causes a shift of the Raman peak to lower wavenumbers while compressive strain shifts the Raman peak to higher wavenumbers.

2.5.1 Temperature dependency of the Raman shift

Aside of strain the temperature influences the optical phonon frequency and thus the Raman peak shift [63]. As shown in figure 2.18, the first-order optical phonon frequency shifts to lower wavenumbers for increasing temperature. This temperature dependent Raman shift can easily be misinterpreted as a strain dependent Raman shift.

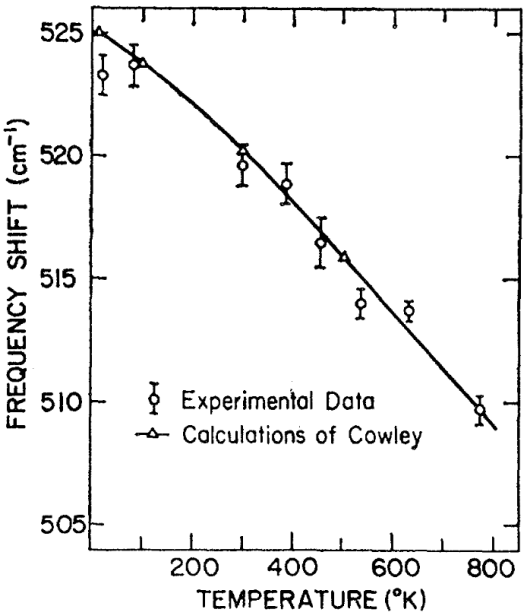

Figure 2.18: *First-order optical phonon frequency shift as function of the temperature. [63]*

The excitation laser light introduces energy into the silicon which will transformed mostly to thermal energy and heats up the silicon. Hence the silicon heating is dependent on the laser power. Since bulk silicon acts as a heat sink the induced heat is fast distributing over the whole silicon, a local heating due to the laser light and therefore a Raman shift can be neglected for moderately laser powers. For suspended silicon nanowires, the laser light induced heat can be dissipated only insufficient [64]. The local temperature increase results in a Raman peak shift and thus biased strain measurements. Therefore the excitation laser power has to be kept below 50 μW for strain measurements on nanowires via Raman spectroscopy to avoid laser induced nanowire heating.

2.6 Principle of MEMS actuation technology

This section is focused on the basic principles of an electrostatic comb drive actuator. For further information about this and other actuator types textbooks like "Micromachined Transducers Sourcebook" from Kovacs [65] and "The MEMS Handbook" from Gad-el Hak [66] are recommended.

One of the most common actuator types for MEMS devices is the electrostatic comb drive actuator. Figure 2.19 shows a SEM image of such a comb drive actuator. It comprises two interlocking comb-shaped structures where the comb on the top is fixed and the comb below is movable.

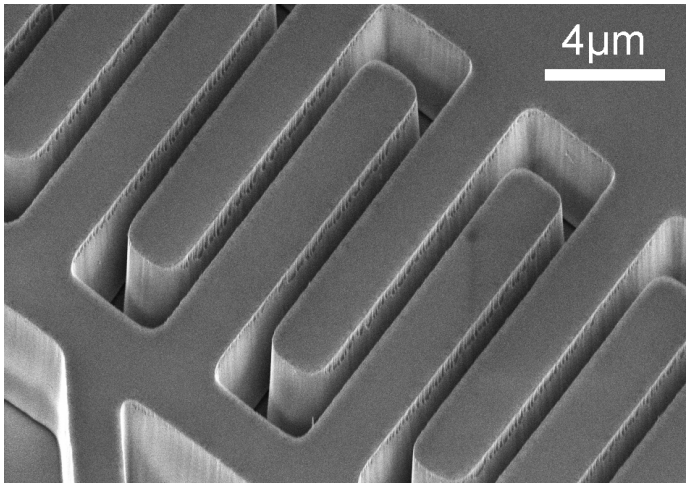

Figure 2.19: *SEM image of comb drive actuator elements of a MEMS device with the fixed comb on the top and the movable comb below.*

It utilizes the attractive Coulomb force between two differently charged bodies can be derived from the capacity plate model. For a constant voltage V, an energy W is stored between two parallel plates which is given by:

$$W = \frac{\epsilon A V^2}{2y} \tag{2.62}$$

where ϵ is the dielectric constant of free space ε_0 multiplied with the relative dielectric constant ϵ_r for the material between the plates. A is the area of a plate and y the distance between the two plates. The attractive force F between the plates is thus given by:

$$F = -\frac{\partial W}{\partial d} = \frac{\epsilon A V^2}{y^2} \tag{2.63}$$

Since the Coulomb force is proportional to $1/y^2$, it rapidly decreases with increasing gap distance.

If the two plates are shifted to each other next to the normal directed force also a tangential directed force will act on the plates as shown in figure 2.20.

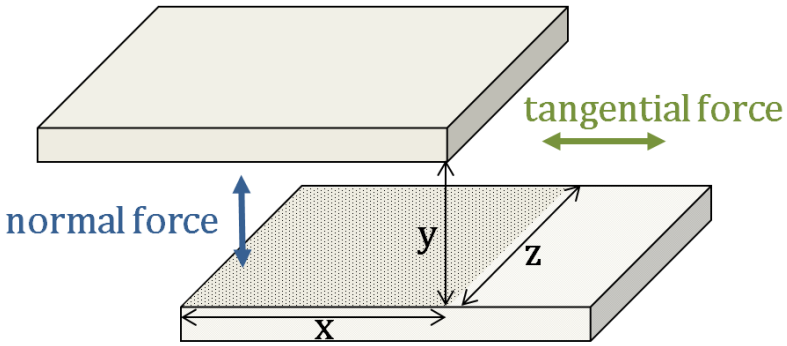

Figure 2.20: *Schematic of the resulting Coulomb forces for two plates shifted apart from each other and a constant voltage is applied between the plates.*

By substituting the area A with the product of the lateral dimensions x and z the energy of the tangential component is given by:

$$W = \frac{\epsilon x z V^2}{2y} \tag{2.64}$$

and the resulting tangential directed force is

$$F = \frac{\partial W}{\partial x} = \frac{\epsilon z V^2}{2y} \tag{2.65}$$

.

Hence, the tangential force is not dependent on the lateral position x.

Figure 2.21 shows a schematic of a comb drive actuator element. Due to the symmetry in a comb drive actuator the normal directed plate forces, which are marked with blue arrows, are compensating each other. Therefore the green marked tangential directed forces together with the red marked normal directed forces attributed to the comb end fronts, generate a movement of the movable comb part towards the fixed comb part. The final actuator force F_a is given by:

$$F_a = N_c \epsilon h \left(\frac{1}{d_1} + \frac{w}{(d_2 - \partial_a)^2} \right) V_{Act}^2 \tag{2.66}$$

with N_c is the total number of comb actuator elements, d_1 the gap distance between two combs, d_2 the distance between the tip of the comb to the opposite comb electrode in the initial state, V_{Act} is the voltage applied to the actuator. ∂_a is the comb actuator displacement from the initial position, h and w are the height and width of the comb, respectively.

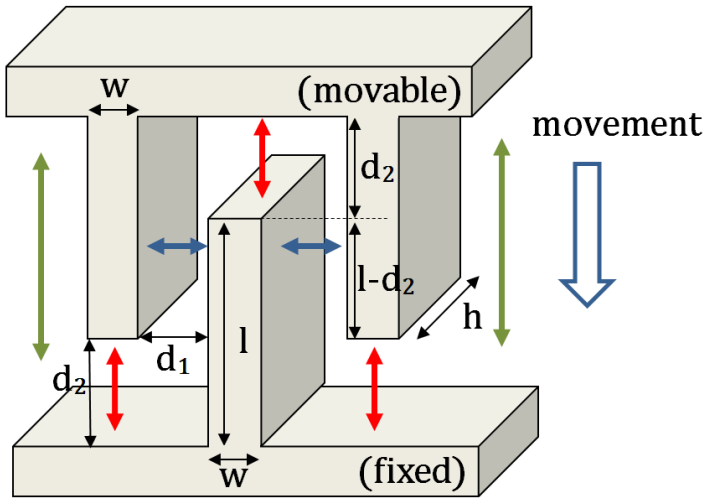

Figure 2.21: *Schematic of a comb drive actuator element. The green arrows display the tangential directed forces, the blue arrows indicate the normal directed plate forces and the red arrows denotes the forces normal to the comb end fronts, which are resulting from a constant voltage applied between the combs.*

Due to the deflection of the cantilever beams which are holding the movable comb drive structures, a restoring force F_{beam} contrary to the actuator force F_a has to be considered as shown in figure 2.22.

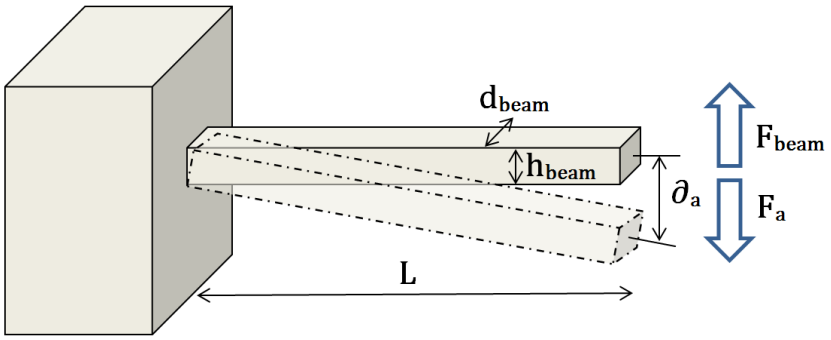

Figure 2.22: *Schemactic of a silicon beam bended due to the attractive comb drive force F_a. A restoring force F_{beam} contrary to F_a is forming.*

The restoring beam force F_{beam} is given by:

$$F_{beam} = N_{beam}\, Y\, h_{beam}\, d_{beam}^3 \frac{\partial_a}{4L^3} \tag{2.67}$$

where N_{beam} is the total number of cantilever beams, Y the Young's modulus of the beam material, L the length of the beam, ∂_a the cantilever tip displacement from the initial state, h_{beam} and d_{beam} the height and thickness of the beam, respectively.

Chapter 3

Experimental

This chapter describes the MEMS straining device, the fabrication process and the experimental methods and procedures for the synthesis, device integration and characterization of strained nanowires.

3.1 The Electrostatic-Actuated-Straining-Device

For all straining experiments on silicon nanowires the comb drive actuated EASD was used. In this section the basic elements of the MEMS straining device will be introduced followed by an explanation of the stabilizing structures and design parameters for efficient nanowire straining. The calibration of the ESAD to guarantee sufficient straining of average silicon nanowires for high strain experiments will end this section.

3.1.1 Design of the EASD

As shown in figure 3.1, the MEMS device consists of three basic parts marked with different colors. The electrostatic comb drive actuator is composed of sections of the actuator (red)- and the stage (green) part. The silicon nanowire is monolithically integrated between stage part and the fixed specimen (purple) part. Each part is connected with a macroscopic silicon pad suitable for wire bonding. The comb drive actuator is designed with two rows of comb drive elements to increase the total number of elements and therefore the attainable actuator force. The section of the stage part which is part of the actuator is suspended to provide the movability of the actuator combs. Due to an applied voltage on the actuator part, the suspended stage part can be attracted toward the actuator part and in the same way, it will be pulled apart from the specimen part. Hence the nanowire integrated between stage and specimen part will be strained tensile and uniaxial.

In the following listing the three parts are described in detail.

- **Actuator part:** The actuator part constitutes one part of the comb drive actuator. It contains the fixed combs of the comb drive actuator which are directly attached on the actuator silicon pad for the second comb drive row (2). The combs of the first row (1) are connected with the pad by a feeder structure (A). The feeder structure is dimensioned in a way that it will not be under-etched during the MEMS device fabrication process.
- **Stage part:** Apart from the fixed silicon pad, the stage part is mainly composed of the suspended and therefore movable part. The suspended stage part comprises the movable combs of the comb drive actuator. Also one end of the integrated nanowire is connected to the suspended stage part . Furthermore the suspended stage part is electrically connected to the fixed silicon pad by two suspended silicon beams adjacent to the first comb drive row. For better stability of the moveable stage part, the second comb drive row is connected by two equivalent silicon beams to isolated pads (B) which will not be under-etched during MEMS fabrication process. To reduce the mass of the movable stage part and to guaranty an uniform etching, the stage is designed as a silicon grid structure. Such a grid structure grants the stage sufficient stiffness to avoid bending of the stage itself. Hence only the four silicon beams which are supporting the suspended stage will be bended during actuation. The movable combs of the comb drive are directly attached on the stage grid. As designated site for the nanowire integration, a trapeze-shaped structure is attached on the stage part, opposite to the specimen part.

- **Specimen part:** At the fixed specimen part the other end of the nanowire is integrated. As designated integration site again a trapeze-shaped structure is intended. Thus the silicon pad of the specimen part is stepwise reducing to a final trapeze-shaped structure opposite to the trapeze on the stage part. The nanowire is integrated between the two trapeze structures. These trapeze structures promote a selective metal colloid deposition by dielectrophoresis since an electric field enhancement appears at this area in comparison to the surrounding structures. As gap distance between the two trapeze structures 3 μm is chosen. Smaller gap distances will hinder Raman measurements on the nanowire since reflections on the trapeze structure edges will disturb the excitation laser light. Larger gap distances require longer nanowires and thus the total nanowire growth time increases followed by an increased deposition of undesired uncatalytic silicon.

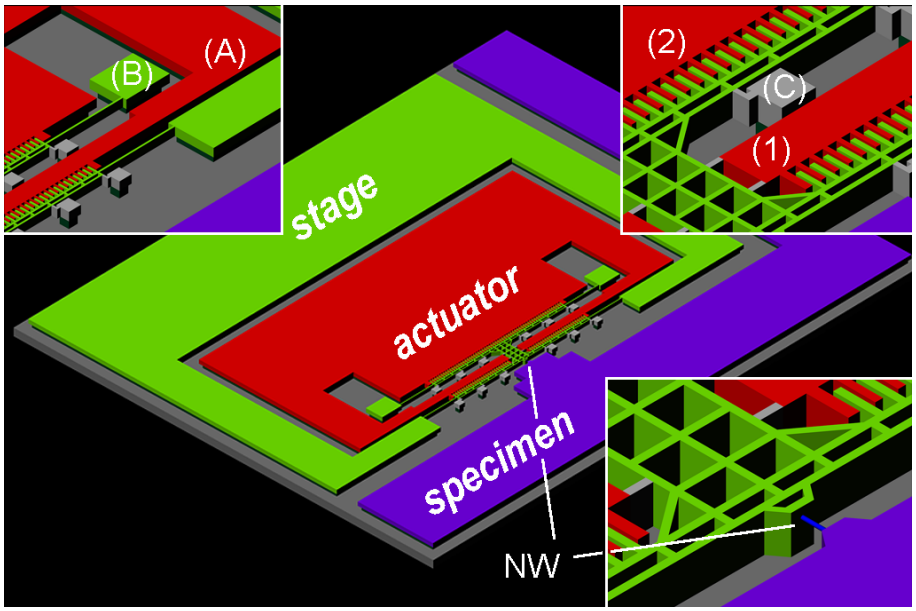

Figure 3.1: *Schematic of the EASD with the red colored actuator part, the green colored stage part and the purple colored specimen part. The inset shows a magnification of the gap between stage and specimen part with the monolithically integrated silicon nanowire (blue).*

Hydro-adhesive forces can lead to a sticking of the suspended EASD parts on the underlying substrate. Especially wet chemical processes during device fabrication and nanowire integration involve risk for such sticking. Therefore the suspended stage part is supported by silicon beams connected to the actuator part and isolated pads (C) at sixteen positions. These beams prevent the suspended stage part from sticking on the bulk substrate to during the whole fabrication process and nanowire

integration. Previous to the straining experiments the beams will be removed by FIB cutting as shown in figure 3.2. After the removal of the supporting beams the stage part is fully movable but the device is from now on incompatible to any kind of wet processes.

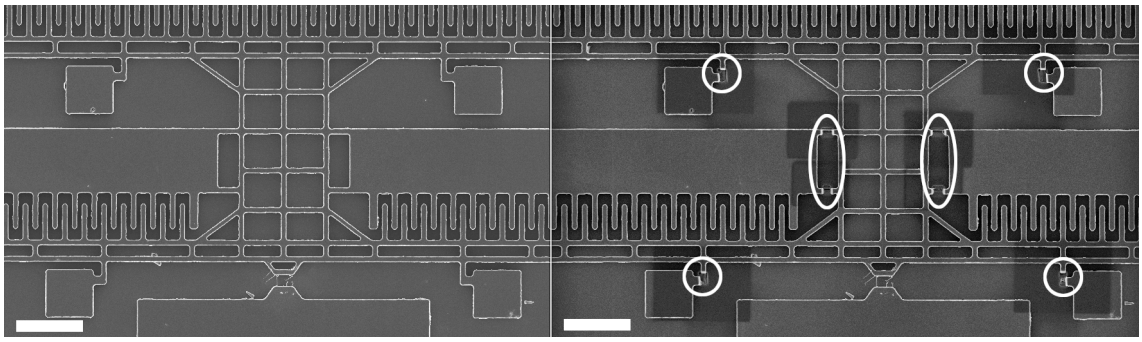

Figure 3.2: *SEM image of an EASD before (left) and after (right) FIB cutting of the supporting beams. The white circles are marking the cut supporting beams. The scale bar equates to* 20 μm.

3.1.2 Fabrication of the EASD

The EASDs are fabricated using a silicon-on-insulator (SOI) wafer with (110) device layer orientation diced to pieces with the size of 10 mm $\times$ 10 mm. The device layer as well as the buried oxide (BOX) layer of the SOI have a thickness of 2 μm, the handle layer a thickness of 500 μm. The main process steps of the EASD fabrication are illustrated in figure 3.3.

After cleaning the substrate by sonification in acetone and subsequently rinsing with isopropanol a photoresist is deposited by spin coating. The resist is exposed with the EASD design pattern by direct laser writing. The pattern is oriented with respect to the device layer orientation, that the facets of the trapeze gap structures are oriented in <111> direction (see figure 3.3(a)). The resist is developed and the sample is subsequently covered with a 60 nm thick layer of chromium by magnetron sputtering. After a lift off process with acetone a chromium hard mask pattern of the MEMS device remains on the sample as shown in figure 3.3(b). With an anisotropic reactive ion etching (RIE) process at cryogenic temperature, silicon is etched anisotropically down to the oxide layer. Finally the chromium hard mask is removed with a chromium etchant (see figure 3.3(c)). By etching the sample in buffered hydrofluoric acid (BHF) under constant stirring for 30 minutes the BOX under the movable stage part is etched to release the grid structure. An about

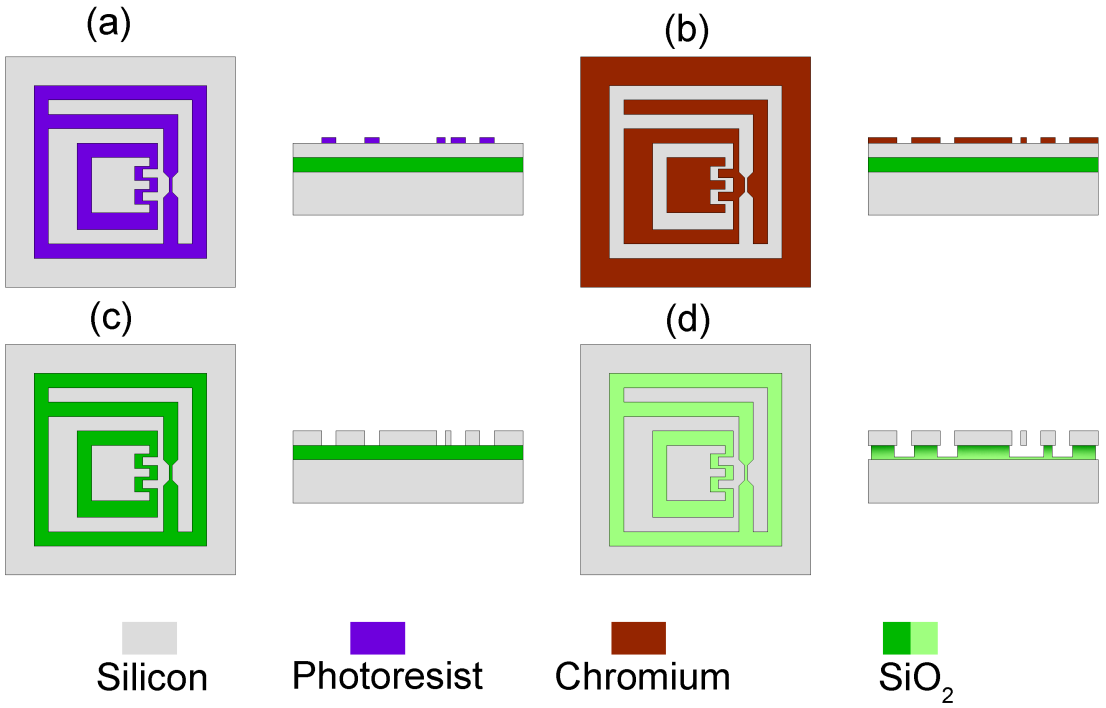

Figure 3.3: *Schematic illustration of the main process steps for the fabrication of an EASD. (a): Structuring of photoresist with the MEMS pattern by direct laser writing. (b): Hard mask formation by chromium deposition and subsequently lift off procedure. (c) Structuring of the device layer by anisotropic RIE. (d) Release of the movable stage part by BHF etching of the BOX.*

200 nm thick SiO_2 layer is left on the handle layer to avoid shortcuts between the structured device layer and the handle layer due to silicon residuals from the RIE etch process (see figure 3.3(d)). The process parameters for the EASD fabrication are listened in section 5.

Hence, the silicon nanowire can be integrated into the EASD by monolithic integration or via pick and place technique. Both methods are described in detail in section 3.2.3. After nanowire integration the sample is glued on a 170 μm thick quartz glass plate which itself is further glued on a copper plate. Next to the sample a circuit board with solder contacts for a connector is glued on the copper plate. By aluminum wire bonding the silicon pads of the sample are connected with the circuit board. At this point the movable parts of the EASD can be fully released by cutting the supporting silicon beams via FIB. Therefore all pins of the connector are connected to a grounded stub inside the FIB system. This prevents a FIB induced charging of the EASD structures and thus undesired attraction toward the handle

layer substrate. During the whole FIB milling process an exposure of the nanowire with the FIB has to be avoided. Otherwise an amorphization of crystalline nanowires would occur. Figure 3.4 shows an image of a sample ready for measurement. The silicon chip contains a matrix of 4 × 4 MEMS devices where only one is connected to the circuit board by wire bonding.

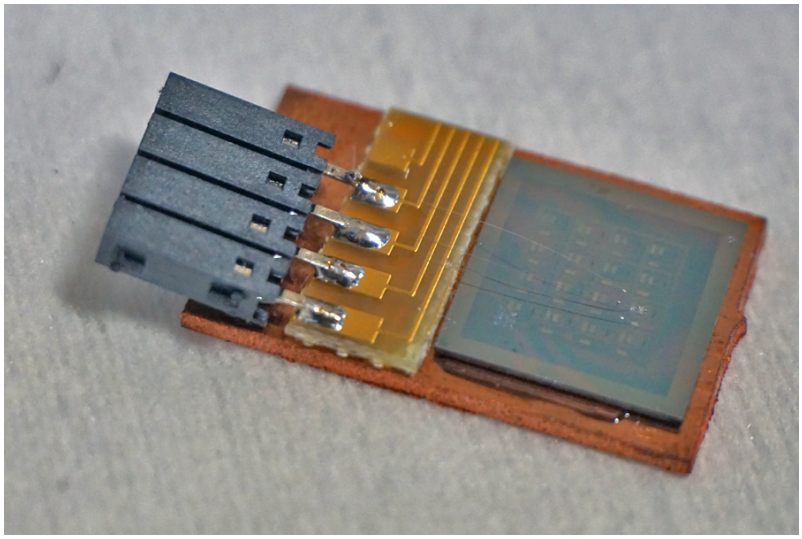

Figure 3.4: *MEMS device chip with 4 × 4 devices mounted next to a circuit board on a copper plate. One device is connected with the circuit board by aluminum wire bonding.*

3.1.3 Benchmarking of the EASD

In this section, the capability of the EASD is demonstrated under consideration of the employed design parameters. The derivation of the used equations are described in section 2.6.

The force and thus the strain acting on the integrated nanowire is an interaction of the attractive actuator force F_a and the restoring force F_{beam}. Both forces are also dependent on the current state of stage displacement. The length of the four silicon beams supporting the movable stage part is chosen to $L = 94\ \mu m$. With the Young's modulus of silicon in [111] $Y_{111} = 187\ GPa$, a chosen beam thickness of $d_{beam} = 2\ \mu m$ and the beam height h_{beam} (which is given by the device layer thickness), the total beam force as function of the beam deflection (similar to the stage displacement) ∂_a is calculated by using equation 2.67) to

$$F_{beam} = 3.39 \cdot 10^{-4} \cdot \partial_a \; [N] \tag{3.1}$$

The actuator force can be calculated with equation 2.66. The utilized design parameters are the total number of combs $N_c = 226$, a comb width of $w = 2\ \mu m$, a distance between two combs of $d_1 = 1\ \mu m$ and the distance between comb tip and opposite structure of $d_2 = 3\ \mu m$. Thus the actuator force dependent on the actuator voltage $V_{Act}$and the actuator displacement ∂_a is calculated to

$$F_a = \left(4 \cdot 10^{-9} + \frac{8.01 \cdot 10^{-21}}{(3 \cdot 10^{-6} - \partial_a)^2}\right) \cdot V_{Act}^2 \; [N] \tag{3.2}$$

As mentioned above the force acting on the nanowire is an interaction of actuator force and restoring beam force. It can be described as $F_{NW} = F_a - F_{beam}$. According the definition of stress in section 2.4.1.2, the stress P applied on the nanowire is given by F_{NW} per the nanowire cross section area $A_{NW} = \pi r_{NW}^2$. This stress P is proportional to the applied strain ε_{111} with the Young's modulus Y_{111} of the nanowire as proportional constant (see equation 2.45). Hence the strain applied on the nanowire equals the interaction of the displacement dependent actuator force and beam force. The strain on the nanowire is defined as change of the nanowire length ∂_a per initial nanowire length l_{NW} and is therefore also dependent on the stage displacement. Thus the whole system is given by

$$\varepsilon_{111} = \frac{\partial_a}{l_{NW}} = \frac{F_{NW}}{Y_{111} A_{NW}} \tag{3.3}$$

Typical dimensions of a silicon nanowire integrated into the MEMS device are a length of $l_{NW} = 3\ \mu m$ and a diameter of $d_{NW} = 100 - 150\ nm$.

This system can be described by a cubic function $f(\partial_a)$. By solving equation 3.3 for ∂_a with a numeric calculation tool and utilizing only the physically relevant solution, the system converges for the respective actuator voltage V_{Act} to force values F_{NW} and the strain values ε_{111} as shown in figure 3.5.

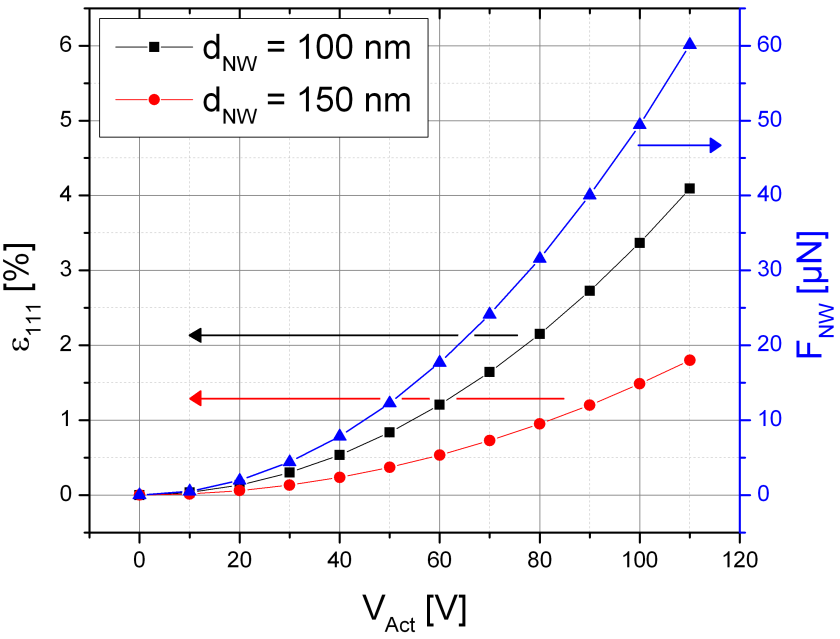

Figure 3.5: *Calculated force and strain generated by the EASD applied on a 3 µm long silicon nanowire as a function of the actuator voltage V_{Act} for two different nanowire diameters.*

Stress and thus strain which can be applied on the nanowire is inverse proportional to the square of the nanowire diameter d_{NW}. Hence, a reduction of the nanowire diameter increases the straining performance of the EASD for a certain actuator voltage drastically. While for a 150 nm thick nanowire and 100 V actuator voltage a theoretically strain value of 1.49% is reached, for a nanowire with 100 nm diameter and the same actuator voltage a theoretical strain value of 3.37% can be achieved. Nevertheless with generated forces up to 60 μN at 110 V actuator voltage the EASD is predestined for high strain experiments on silicon nanowires. The generated force is almost quadratic dependent on the actuator voltage and can approximately described by:

$$F_{NW} = 4.94908 \cdot 10^{-9} \cdot V_{Act}^2 \; [N] \tag{3.4}$$

The strain values achieved from a real-life EASD can differ from the calculated values because the EASD fabrication underlies tolerances which vary the design parameter dimensions. Furthermore the nanowires did not have an uniform diameter. Therefore strain is not distributed homogeneously along the nanowire.

3.2 Nanowire synthesis

3.2.1 LPCVD system

Silicon nanowire synthesis is performed in a LPCVD reactor, utilizing the VLS mechanism with silane as precursor gas and gold as catalyst. Figure 3.6 shows an image of the LPCVD reactor as well as a schematic of the main components of the system.

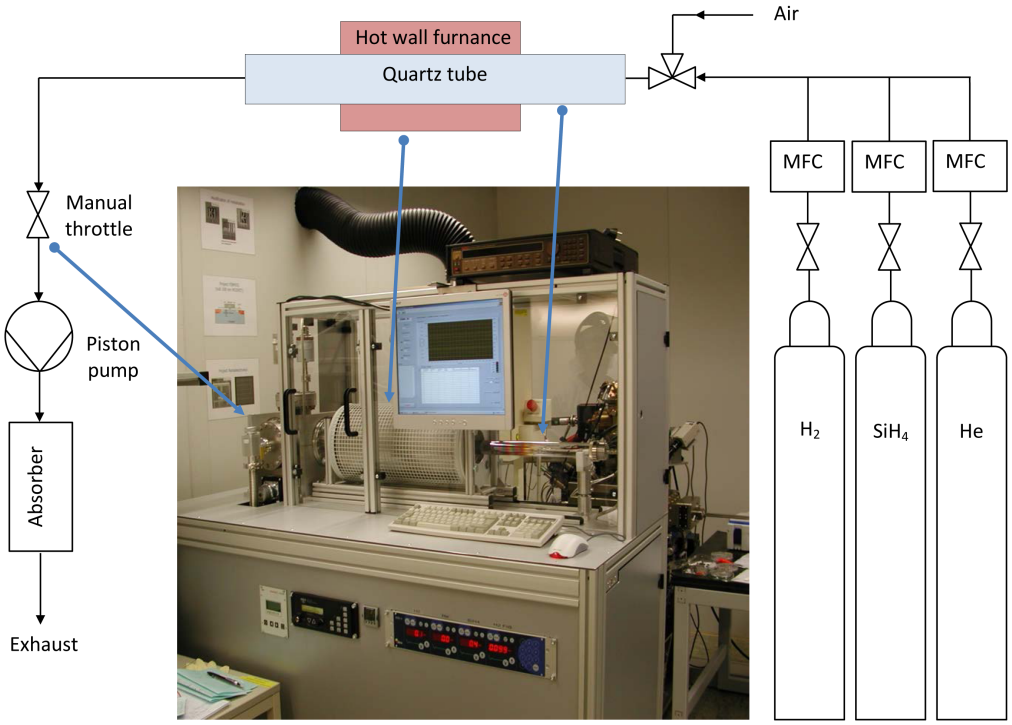

Figure 3.6: *LPCVD system, for VLS synthesis of silicon nanowires. The system consists of a process gas supply, the reactor tube with the surrounding furnace and a piston pump to evacuate the reactor. The gas flow is controlled by MFCs in the gas lines and the pressure inside the reactor is controlled by a manual throttle after the reactor tube.*

The reactor consists of a quartz tube surrounded by a movable tubular hot wall furnace. On the one end the gas supply is connected and on the other end a vacuum system is located. The gas supply is carried out by high pressure gas cylinders of the process gases followed by pressure reducers for each line. The flows of each line are controlled by separate mass flow controllers (MFC) and are subsequently mixed to one line which is connected over a two-way hand valve to the reactor tube.

Depending on the hand valve position, either the growing gases or ambient air for venting the tube, passes the valve.

The vacuum system consists of an oil-free piston pump for the reactor tube evacuation and a manual throttle between pump and tube, which regulates the pressure inside the reactor. After the pump the extracted gases are neutralized by an absorber.

To load the LPCVD reactor with a sample the two-way hand vale can be unscrewed via a screw cap and the sample will be moved to the right position inside the tube with a quartz glass hook. The oven will be moved that the sample is positioned at the center of the tubular furnace.

3.2.2 Silicon nanowire growth

3.2.2.1 Synthesis of <111> oriented silicon nanowires

For VLS synthesis optimization, nanowires are grown on silicon (111) cut samples. Therefore a silicon dice is cleaned by sonification in acetone and isopropanol, dipped in BHF for 5 s to remove the native SiO_2 layer and subsequently rinsed with deionized (DI) water. To deposit the catalytic gold colloids with diameter of 80 nm, 10 μl of the colloid solution solved in DI water with a mixing ratio of 1:5 is dropped on the silicon dice. The sample is dried on a hot plate, once again dipped in BHF for 10 s and subsequently rinsed in DI water. The second BHF dip is required to remove the oxide from the gold collide surface originating by silicon diffusion through the gold [67].

Immediately afterward the sample is introduced into the LPCVD reactor and the reactor tube is evacuated to a pressure of 0.05 mbar to prevent re-oxidation of the silicon. After evacuation the tube is purged with 70 sccm He and the oven is heated up with a ramp of 60 K/min to the final growth temperature of 793 K. During the heating the pressure is regulated to 3 mbar with the manual throttle. After the growth temperature is reached, the He flow is stopped and the process gases, 10 sccm H_2 and 100 sccm diluted SiH_4 (2% SiH_4 in He) are started. The temperature will be kept constant for the whole growth duration time. After completion of a 45 min growth duration time the gas flows are stopped and the tube is purged with He during the cool down of the furnace.

At a temperature of about 573 K the sample is removed from the LPCVD reactor. A typical growth rate of silicon nanowire under the given growth conditions is about 110 nm/min, thus for a growth duration of 45 min the nanowires will have a length of 5 μm in average.

3.2.2.2 Synthesis of <112> oriented silicon nanowires

In principle <112> oriented silicon nanowires are grown similar to <111> nanowires as described in the section above 3.2.2.1. The deviations from the processes described above are elaborated in the following sentences. First a (112) oriented silicon substrate is used for the nanowire synthesis. Since some of the epitaxial grown <112> nanowires are directed perpendicular to the substrate and therefore easier to pick and place on the EASD. Total process gas pressure is increased to 15 mbar to synthesize <112> oriented nanowires [38] and finally the growth temperature is increased to 808 K to achieve nanowire lengths of more than 20 μm for a growth duration of 45 min. Nanowire lengths of more than 15 μm are necessary for the employed pick and place nanowire transfer technique.

3.2.3 Nanowire integration

3.2.3.1 Monolithic integration of nanowires in the MEMS device

For most straining experiments the silicon nanowires are monolithically integrated into the EASD. To deposit the catalytic colloids on the facets of the trapeze-shaped structures of the EASD, the dielectrophoresis technique is employed. At this technique the colloids in the solution are arranged along the electric field lines of an alternating electric field applied between stage part and specimen part of the EASD. Once they come in contact with the silicon surface, they are bonded on it and will not be rinsed away by following rinsing steps. To make sure that only the trapeze structures are coming in contact with the colloid solution, first the whole EASD is covered with a total of three layers of photoresist. Afterward the region around the trapeze structures is exposed with a 12×12 μm^2 sized window by direct laser writing and developed to remove the exposed resist. Next to the window at the gap where the nanowires will growth, about 100×2000 μm^2 sized windows are exposed and developed on the silicon pads of the EASD to apply the alternating voltage, necessary

for the dielectrophoresis, with needle probes. Figure 3.7 shows microscope images of the resist windows for the silicon pads 3.7(a) and the nanowire gap 3.7(b).

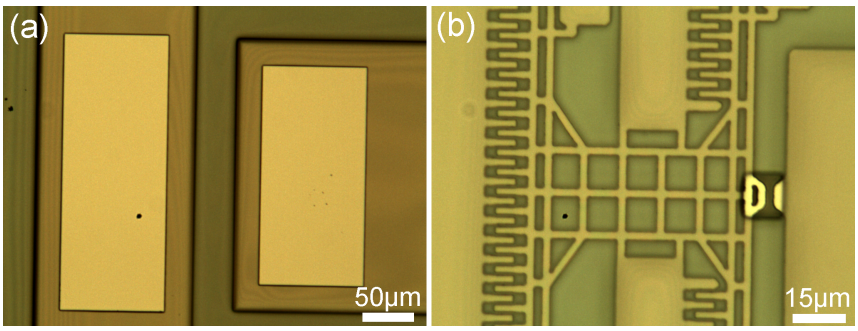

Figure 3.7: *Microscope images of the resist windows on the EASD for catalytic colloid deposition by dielectrophoresis. (a)* $100 \times 2000\ \mu m^2$ *sized windows on the silicon pads for needle probes. (b)* $12 \times 12\ \mu m^2$ *sized window to make sure that colloids are only attached on the silicon surface at the nanowire gap.*

After a 5 s BHF dip to remove the native oxide the same colloid mixture as described in the section above is dropped on the resist window at the gap and needles of a needle probe station are placed on the opened silicon pads of the specimen and stage part. By applying a sinusoidal AC voltage of $V_{pp} = 15\ V$ with a frequency of 100 kHz combined and a DC offset voltage of $V_{bias} = 3\ V$ for 5 s, few gold colloids of the colloid mixture are intentionally placed on the (111) oriented sidewall facet of the gap trapeze structures. Afterward the excess colloid solution is blown away with nitrogen and the resist layer covering the silicon structures is removed by rinsing the sample with acetone and isopropanol. After removing resist residuals in oxygen plasma for 15 min, the MEMS device is once again dipped in BHF and silicon nanowire synthesis is started as described in the section above (3.2.2). Since the epitaxial silicon nanowire growth in <111> direction is starting from the (111) facet of the gap structure, the nanowire is growing perpendicular from one facet bridging the gap and forming a self-aligned contact on the opposite facet as shown in figure 3.8(a).

Such defect free nanowire/bulk silicon contacts show a high mechanical robustness and an excellent electric behavior with contact resistivity about two orders of magnitude lower than for comparable Au/Ti contacts [68–70].

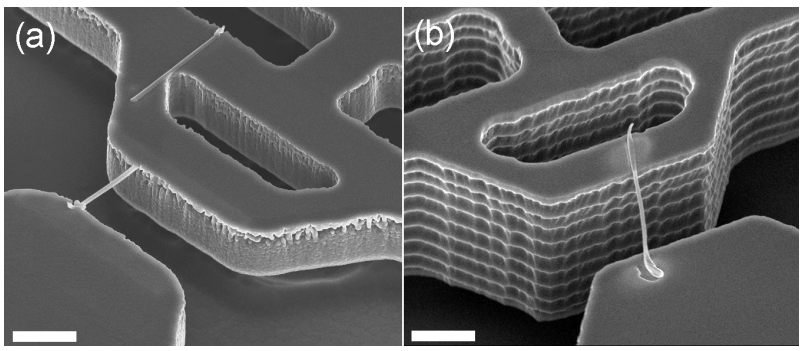

Figure 3.8: *SEM images of silicon nanowires integrated into an EASD. a) Monolithic integrated nanowire. b) Nanowire integrated with pick and place technique and EBID tungsten fixation. Scale bar equals* 2 μm.

3.2.3.2 Pick and place integration of nanowires in the EASD

Alternative to the monolithic integration of <111> oriented silicon nanowire, a <112> oriented nanowire is integrated into an EASD by pick and place technique using a dual beam (SEM-FIB) system. Therefore special glue was deposited on the tip of a nano-manipulator. After approaching the tip of an individual <112> silicon nanowire with the tip of the nano-manipulator, the glue is hardened with an electron beam with the current of 1 nA for one minute. After the fixation of the nanowire on the manipulator tip the nanowire is separated at base from the growing substrate by a fine FIB cut. After placing the nanowire over the gap of the EASD, both ends of the nanowire are fixed by electron beam induced deposition (EBID) of tungsten. Finally the nanowire is cut from the nano-manipulator by FIB. Figure 3.8(b) shows a silicon nanowire integrated on an EASD by pick and place technique.

3.3 Measurement setup

3.3.1 Confocal micro-Raman microscopy

Micro Raman spectroscopy measurements are executed with a WITec alpha300 confocal microscope system shown in figure 3.9.

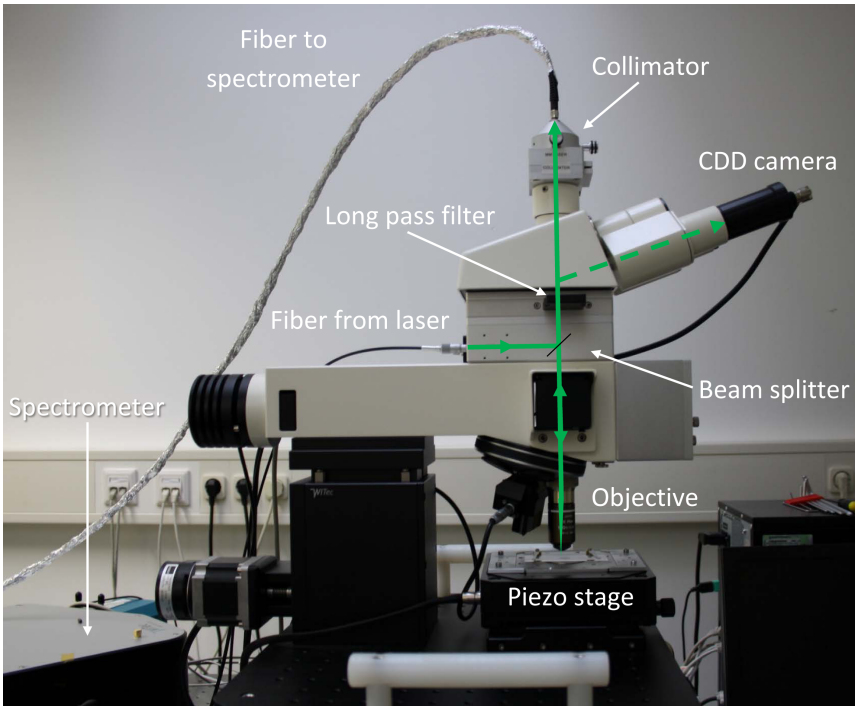

Figure 3.9: *Image of the Raman spectroscopy setup.*

A frequency doubled Nd:YAG laser emitting linearly polarized light at 532 nm, fiber-coupled to the system, is used as excitation light source. The laser light passes a beam splitter and is focused on the sample to a spot size of about 300 nm with a Zeiss LD EC Epiplan-Neofluar 100x objective (NA = 0.75; WD = 4 mm) or about $1\mu m$ with a Nikon EPI EPlan 20x objective (NA = 0.4; WD = 3.8 mm). The scattered light is then collected by the same objective and passes a filter to blank the excitation wavelength. Spectral analysis is performed by a WITec UHTS300 spectrometer specified for wavelengths from 400 nm to 1100 nm. The filtered light is coupled to a fiber by a collimator, guiding the light to the spectrometer. The light can also be redirected to a CCD camera build in the microscope ocular for sample imaging.

System configuration used for the Raman spectroscopy is:

- Dichroic beam splitter
- 532 nm long pass filter (light with wavenumbers beyond approx. 60 $rel.\ cm^{-1}$ passes the filter)
- 100 μm single mode fiber to the spectrometer
- WITec UHTS300 spectrometer: 600 and 1800 g/mm gratings with 0.5 μm blaze wavelength, 300 mm focal length, f/4 aperture ratio
- Andor iDus DV401A-BV CCD detector

The sample is mounted on a piezo-actuated stage enabling a positioning of the sample in x, y and z direction in 10 nm steps. The stage is computer controlled with the associated WITech software enabling fully automated data acquisition from the spectrometer measuring the spectrum of a single spot or performing a line scan over a chosen path.

3.3.1.1 Calibration of strain measurements in nanowires

The quantification of strain in the nanowires for the piezoresistance measurements with the EASD is realized by Raman spectroscopy measurements. Therefore the shift of the first-order Raman peak is measured which is proportional to the applied strain by a constant k, as described in section 2.5. Hence, to utilize the Raman spectroscopy for strain measurement, first the factor k has to be determined accurately. Therefore the elongation of a nanowire, monolithic integrated in an EASD, was measured in situ with SEM at different actuator voltages (see figure 3.10(a)). With the measured elongations, the respective strain was calculated with $\varepsilon = \Delta l / l_0$ where Δl is the elongation and l_0 is the length of the unstrained nanowire. In the next step the Raman peak shift of the same nanowire was measured for the same actuator voltages (see figure 3.10(b)). Thereby a low excitation laser power ($< 50\ \mu W$) was used to avoid unintentional heating of the nanowire, and therefore a temperature induced peak shift. The strain value can thus be correlated to the Raman peak shift for each actuator voltage (see figure 3.10(c)). The slope of the function "peak shift over strain" corresponds with the factor k (see figure 3.10(d)). The proportional factor was determined to $k = 326$ in good agreement with literature [62, 71].

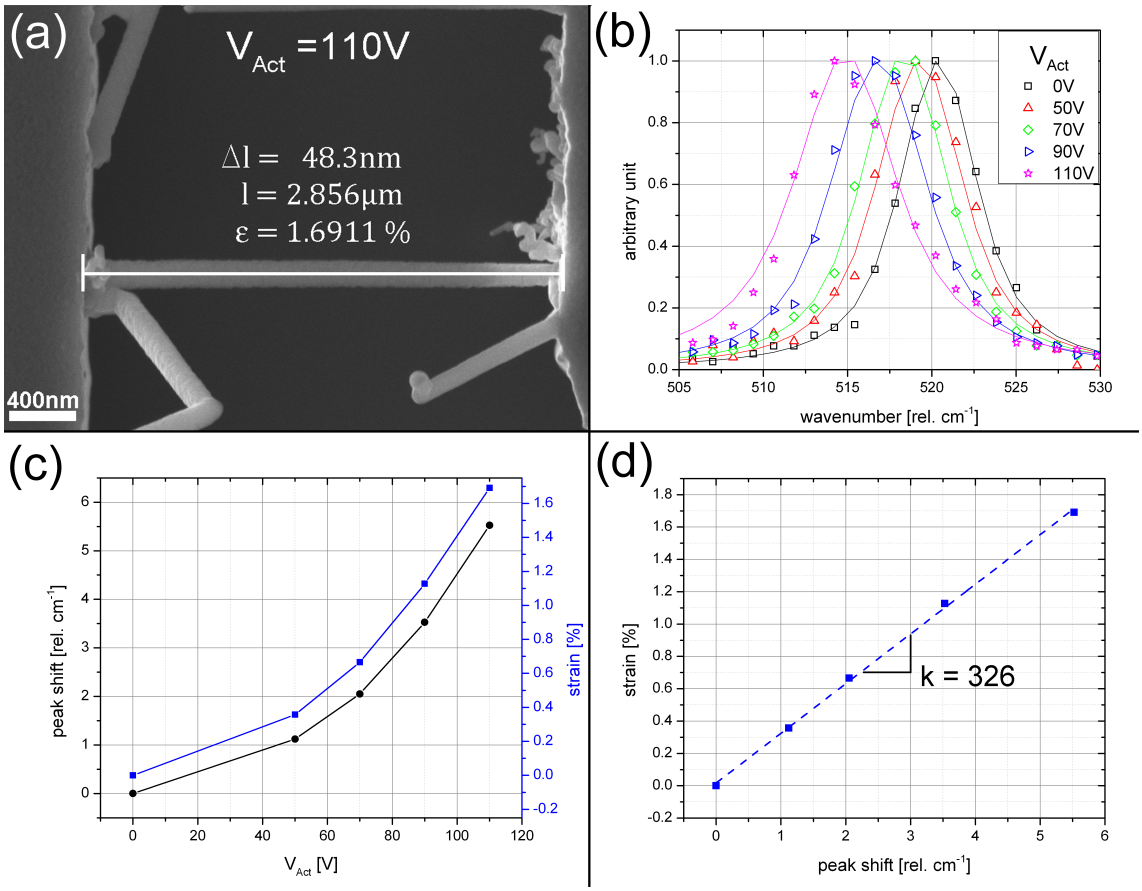

Figure 3.10: *Determination of the proportionality factor k of VLS grown silicon nanowires. (a) Direct determination of strain measuring the nanowire elongation in-situ with SEM for various actuator voltages. (b) Raman peak shift measured at the same actuator voltages. (c) Strain values and dedicated peak shifts for different actuator voltages. (d) Strain over dedicated peak shift. The slope of the linear fit corresponds to the factor k = 326.*

3.3.2 Electrical characterization of semiconductor nanowire

Electrical characterization of the nanowires is carried out with low-noise source monitor units (SMU) embedded in a HP4156B semiconductor parameter analyzer. The wired MEMS device as shown in figure 3.4 is connected with the SMUs via coaxial cables. In order to identify parasitic shunting resistances in the device, both voltage and current are monitored in all utilized SMUs during I/V sweeps.

Typically resistance of an integrated intrinsic silicon nanowire is $R_{NW} \approx 10^9\ \Omega$ so that a measurement circuit as showed figure 3.11 has to be employed for high resistance measurements in voltage source mode.

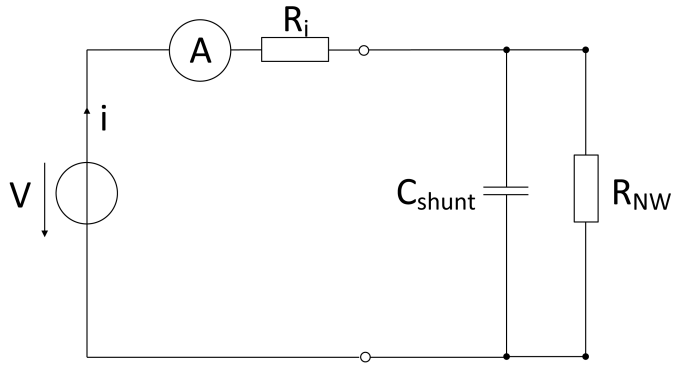

Figure 3.11: *Schematic of the measurement circuit in voltage source mode. R_i is the internal resistance, C_{shunt} the parasitic capacitance from the cables and setup and R_{NW} the nanowire resistance.*

For piezoresistance measurement the nanowire voltage V_{NW}, applied between the specimen part and stage part, is swept from negative to positive voltages while both currents, I_{NW} into specimen part and I_{GND} from the stage part, are measured. The voltage sweep is repeated for various stepwise increasing actuator voltages V_{Act}, applied between the actuator and stage part. Stage part and handle substrate are connected to ground to prevent an attraction of the movable part to the handle substrate due to leakage current induced charging of the substrate. Wiring of an EASD is illustrated in the figure 3.12.

The device layer of the SOI wafer, used for the EASD fabrication, is heavy p-doped. Furthermore the aluminum bonding wires are forming a near ohmic contact with the silicon pads [72] and the rest of the current path to the SMUs is conducted with low resistance cables. Due to the high nanowire resistance, the comparatively small contact resistances of the silicon pads can be neglected for the I/V measurements.

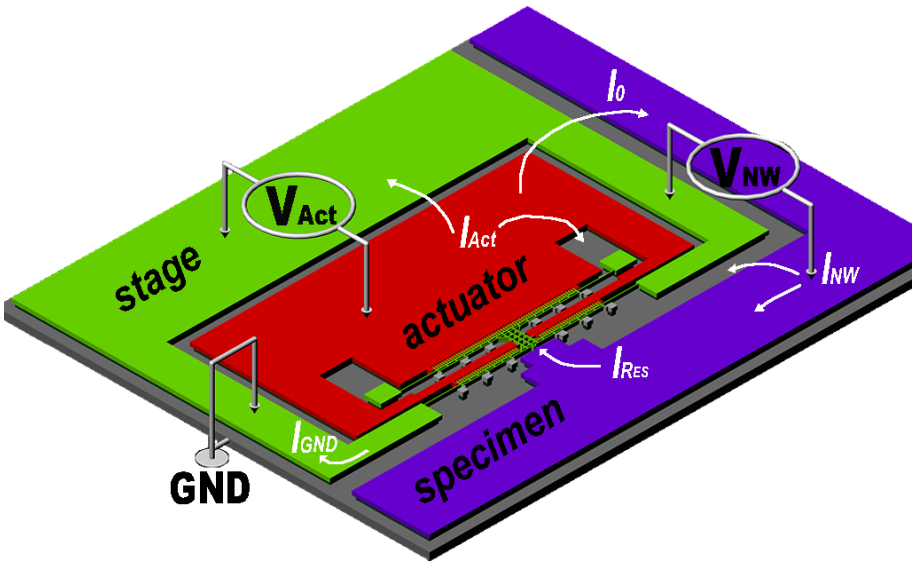

Figure 3.12: *Schematic of the EASD with the applied voltages and resulting currents during electrical characterization of a silicon nanowire. The induced currents can flow between the different part of the EASD due to parasitic resistances of the uncatalytic deposited silicon layer.*

Timing parameters of an I/V sweep has to be carefully chosen. The time constant of the circuit is given by $\tau = (R_i//R_{NW})C_{shunt} \cong R_i C_{shunt}$ since the internal resistance is much lower than the nanowire resistance. With typically values $R_i = 1 - 10\ \Omega$ and $C_{shunt} = 100\ pF$ settling time is about 1 ns. Nevertheless, contact resistance, parasitic device capacitance and charging of slow surface states can lead to significant larger time constants. Therefore a delay time of 1 s between two V_{NW} steps and a hold time of 10 s for each V_{Act} step was chosen for all electrical measurements.

During the monolithic nanowire integration into the EASD, the whole EASD will be covered by an uncatalytic deposited amorphous silicon layer which acts as parasitic resistances interconnecting the silicon pads with the handle substrate. Therefore part of the specimen current I_{NW} is flowing directly to the handle substrate. The part flowing over the silicon nanowire is measured at the stage part. Further, the high actuator voltages up to 110 V lead to leaking currents up to a few μA flowing over the parasitic resistances to the stage part and to the substrate silicon. Therefore the current I_{GND} measured at the stage part is disturbed, especially at higher actuator voltages. The current at the specimen part will not be disturbed by the crosstalk since the specimen part is shielded from the actuator part by the

grounded stage part. Due to the parasitic resistances, a negative offset current I_0, dependent on V_{Act} originating from the handle substrate, can be measured on the specimen part which is constant over a V_{NW} voltage sweep. Hence the current I_{Res} for the nanowire resistance calculation is determined by following equation:

$$I_{Res}(V_{Act}) = I_{GND,0V} + \Delta I_{NW}(V_{Act}) \tag{3.5}$$

with

$$\Delta I_{NW}(V_{Act}) = (I_{NW}(V_{Act}) - I_0(V_{Act})) - I_{NW,0V} \tag{3.6}$$

where $I_{GND,0V}$ is the current flowing over the nanowire at $V_{Act} = 0\ V$ and $I_{NW,0V}$ the current induced to the specimen part at $V_{Act} = 0\ V$. Therefore the current over the nanowire is a sum of the undisturbed $I_{GND,0V}$ and the V_{Act} and thus strain related change of I_{NW}.

For the nanowire resistance calculation, the differential resistance $\delta V_{NW}/\delta I_{Res}$ around $V_{NW} = 0\ V$ is utilized. To minimize an error due to noise inflicted distortion of single data points, a set of differential resistances are calculated with varying voltage ranges for δV_{NW}. As the final result for the nanowire resistance R_{NW}, the median of the various differential resistances is used. Hence, the error, caused by disturbed data points, is statistically reduced.

For the piezoresistance measurement of the nanowire integrated by pick and place technique, I_{NW} can directly be used for R_{NW} calculation due to the lack of parasitic resistances caused by uncatalytic silicon deposition.

All electrical measurements are executed with all light sources in the room turned off to avoid light induced currents which alter the measurement results.

3.3.3 Electrical measurements at cryogenic temperatures

The measurement of the silicon nanowire piezoresistance at cryogenic temperatures is carried out with the cryostatic temperature regulator setup shown in figure 3.13.

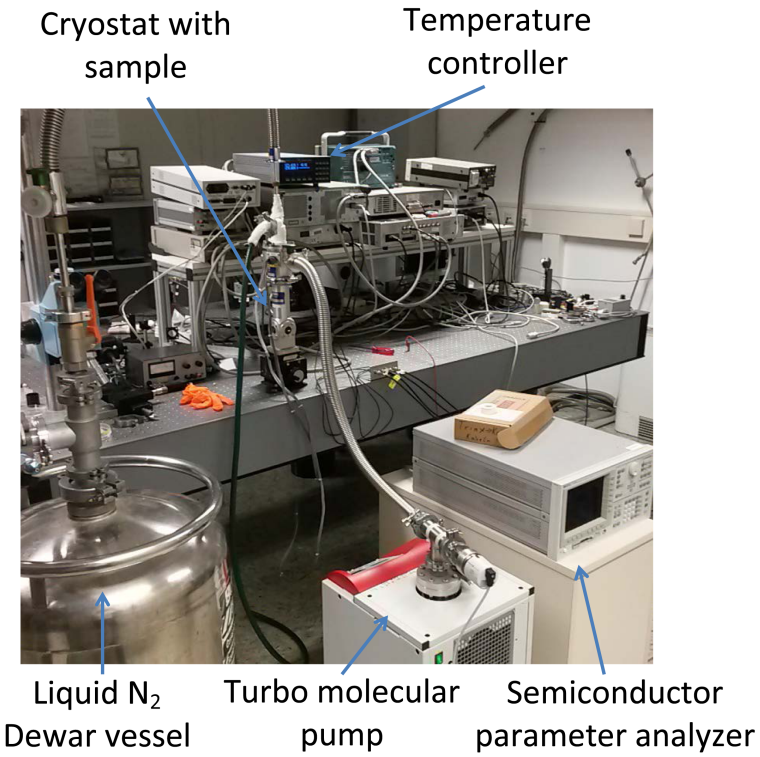

Figure 3.13: *Image of the cryostatic temperature regulator setup used for the piezoresistance measurements of silicon nanowires at cryogenic temperatures.*

Therefore the EASD with integrated nanowire is mounted inside a cryostat which is evacuated with a turbo molecular pump to a base pressure $< 3 \cdot 10^{-6}$ $mbar$. The cryostat is cooled with liquid nitrogen from a Dewar vessel. A temperature is regulated with a controller by heating the cryostat until the desired temperature is set. The temperature variation during a piezoresistivity measurement at a certain temperature is kept below $\Delta T = 0.05$ K to avoid a temperature related resistance fluctuations.

3.3.4 Electrical measurements under laser light excitation

To investigate the strain dependency of the electrical properties in intrinsic silicon nanowires under 532 nm laser light excitation, the EASD with an integrated nanowire is embedded into the micro-Raman spectroscopy setup (see section 3.3.1) and connected to the semiconductor parameter analyzer. With the 20x magnification objective, the FWHM of the laser spot is about 1 μm. Hence, only a part of the nanowire is excited with the laser light during the electrical characterization as shown in figure 3.14. The structures of the EASD were unaffected by the laser light excitation.

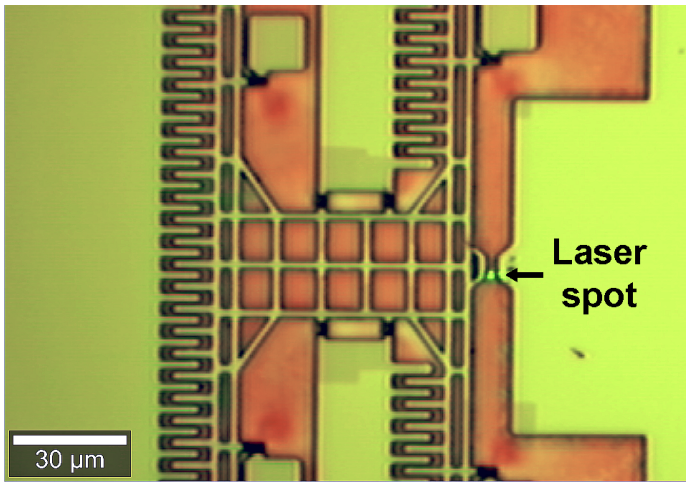

Figure 3.14: *Microscope image of the EASD with NW 2 using the 20x magnification objective of the micro-Raman spectroscopy setup. The nanowire is excited with the green excitation laser (532 nm) of the micro-Raman spectroscopy setup. With the 20x magnification objective, the laser spot size is about* 1 μm. *Thus only a part of the nanowire is excited while the EASD structures are unaffected by the laser light.*

Excitation laser power is measured directly under the 20x magnification objective before and after the electrical characterization. The utilized laser powers 25 μW, 50 μW and 100 μW correlate to laser power densities of 4.85 kW/cm^{-2}, 9.7 kW/cm^{-2} and 19.4 kW/cm^{-2}, respectively.

Photocurrent measurements on nanowires are performed as illustrated in figure 3.15. First a piezoresistivity measurement as described in section 3.3.2 is executed with the excitation laser turned off 3.15(a). No charge carriers are photo-generated, hence the dark current is measured. Afterward the measurement is repeated with the excitation laser turned on 3.15(b). Now an additional, photo-generated current will be measured. Since the laser is focused by the microscopy objective only the

nanowire is excited by laser light. A comparison of the measurement data with and without laser light exhibits the laser light induced nanowire photocurrent.

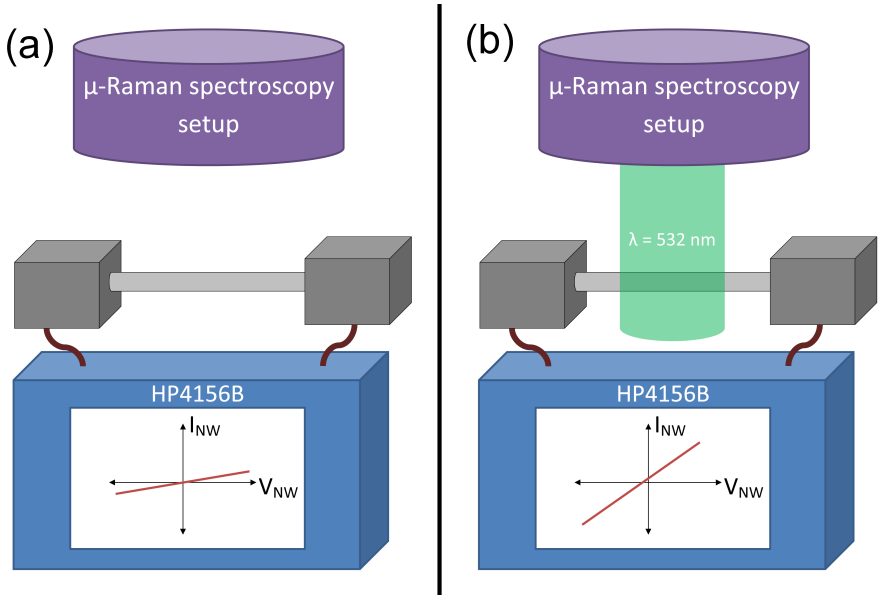

Figure 3.15: *Schematic of the photocurrent measurement on a silicon nanowire utilizing the micro-Raman spectroscopy setup. (a) First electrical characterization of the nanowire is done with the laser turned off. (b) Afterward the measurement is repeated with the laser turned on. The laser light induced photocurrent results from a comparison of the two measurements.*

Chapter 4

Results and Discussion

In this chapter the results of the strain engineering experiments are presented and analyzed with the main focus on the piezoresistive behavior of the intrinsic silicon nanowires. First the results for <111> oriented silicon nanowires are shown including piezoresistivity measurements under ambient condition, vacuum condition and low temperature as well as measurements under laser light excitation. The influence of strain on the I-V characteristic and the photocurrent of the nanowires are presented. Afterward the origin of the atypical piezoresistive behavior of intrinsic silicon nanowire are discussed. Finally the piezoresistive measurements on a <112> oriented nanowire are shown and discussed.

4.1 Strain related measurements on <111> oriented silicon nanowires

4.1.1 micro-Raman spectroscopy on <111> oriented silicon nanowires

Since the silicon nanowires integrated in the EASD are slightly tapered, i.e. the diameter is reducing from the base to the tip of the nanowire, an non-uniform strain distribution along the nanowire can be expected. By performing line scans along a strained nanowire with the micro-Raman spectroscopy setup 3.3.1 the spatial resolved strain mapping of the nanowire can be achieved.

For low strain levels the strain along the nanowire was evenly distributed. Under high strain with peak value above 1%, the strain mapping showed a gradient in strain along the nanowire. Figure 4.1 shows the spatial resolved strain distribution along a silicon nanowire for various actuator voltages and therefore strain levels.

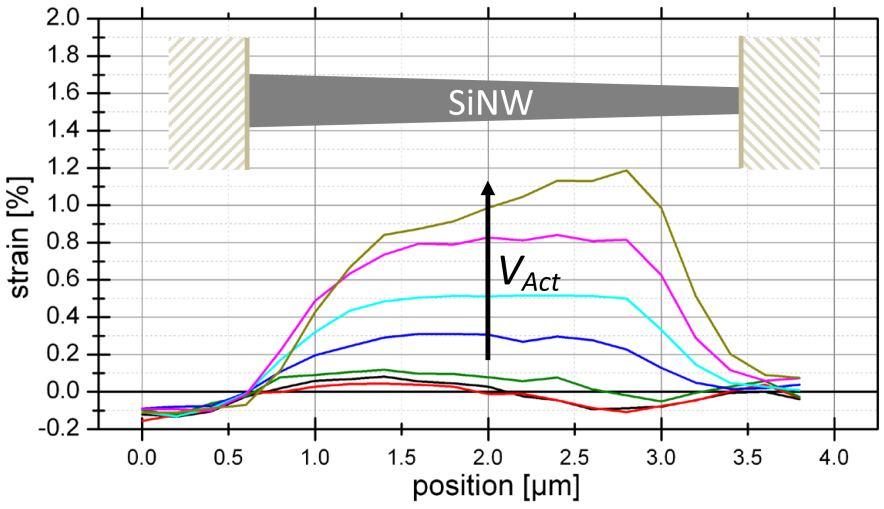

Figure 4.1: *Raman strain mapping of a tapered silicon nanowire. At low actuator voltages the strain is homogeneously distributed along the nanowire. For high strain levels a strain gradient, with strain decreasing from the thinner nanowire end towards the thicker end, occurs.*

The highest strain level occurred at the thinner end of the nanowire and was con-

tinuously decreasing towards the thicker end. Hence, electrical properties, e.g. band gap and thus carrier density, are expected to be inhomogeneous along the nanowire at high strain levels. For all further investigations the strain value measured at the half length of the nanowire was used. This value corresponds roughly to the average of all strain values along the nanowire.

4.1.2 Electrical characterization of <111> nanowires

The measurement procedures for the electrical measurement are thoroughly explained in section 3.3.2.

The current-voltage (I-V) characteristics of a 3.2 μm long and slightly tapered silicon nanowire integrated in an EASD is shown in figure 4.2. The diameter of the nanowire varies from 125 nm at the base to 100 nm at the tip which is connected to the stage part. In figure 4.2(a) the measured values of the nanowire current I_{Res} and in 4.2(b) the semilogarithmic plot for the unstrained nanowire, at 1% tensile strain and at 3% tensile strain as well as the respective fourth order polynomial fits are shown.

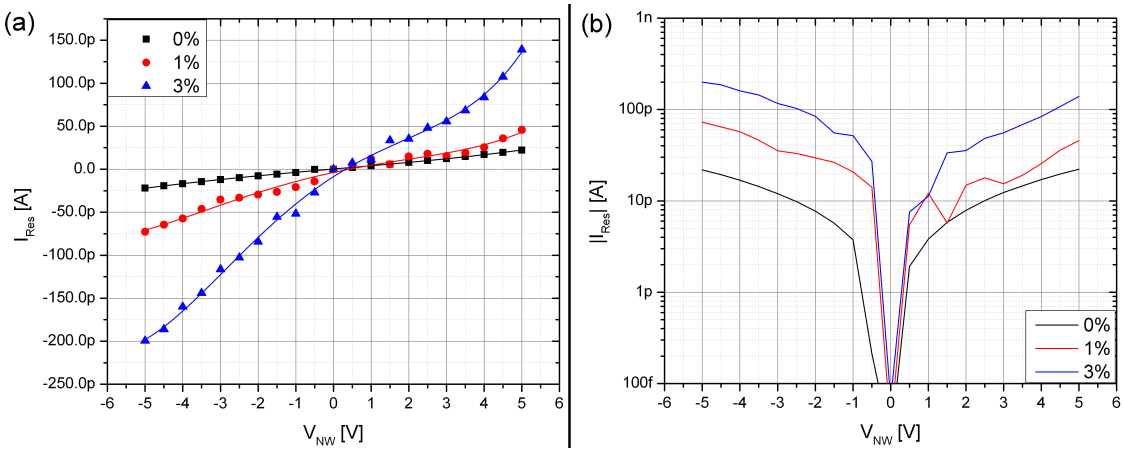

Figure 4.2: *Typical I-V characteristics of a silicon nanowire under increasing strain conditions. (a) I-V plot showing the rising asymmetry with increasing strain. (b) Semilogarithmic I-V plot showing an increase in current of about one decade due to the applied strain of 3%.*

The nanowire I-V characteristic is slightly non-linear. As origin of the non-linearity, imperfect contacts are assumed. With increasing strain the current increases by about one order of magnitude at 3% strain and exhibits an enhanced

non-linearity. Furthermore the I-V characteristic is ambipolar, i.e. an asymmetry between the positive and negative biased current was observed with a lower resistance for negative voltages. Generally the asymmetry can be dedicated to the tapered geometry of the nanowire and thus asymmetric contact interfaces. The contact resistance of a monolithically integrated nanowire is dependent on the nanowire diameter [69]. While without applied strain the ambipolar characteristic is vanishingly small, at high strain levels the ambipolar characteristic is significant. When the nanowire is highly strained an non-uniform strain distribution along the nanowire occurs as shown in the section above. Hence, the thinner nanowire/EASD interface is more stressed than the thicker one. It seems that this stress alters the electrical properties of the nanowire contacts leading to the enhanced non-linearity and the ambipolarity of the I-V characteristic at high strain.

The fourth order polynomial fittings of the currents in figure 4.2(a) indicated an small offset current at $V_{NW} = 0\ V$ which originated from the subtraction of a slightly disturbed offset current I_0 (see equation 3.6). Since the nanowire resistance was calculated using the differential resistance this offset had no impact on the final result.

4.1.3 Piezoresistivity of <111> oriented silicon nanowires

The I-V measurements exhibited a high strain dependency of the nanowire resistance as expected for semiconductors. In the following plots the relative resistance change $(R_{NW,strained} - R_{NW,unstrained})/(R_{NW,unstrained})$is used. This allows a piezoresistive behavior comparison of nanowires with different initial resistances. In semiconductors the relative change of resistance can be assumed as equivalent to the relative change of resistivity (see section 2.4.2).

Measurement data from two silicon nanowires are shown in the following plots, which will be further denoted as NW 1 and NW 2 for reasons of simplicity. Physical dimensions of the two nanowires are given in table 4.1.

denotation	length	min. diameter	max. diameter
NW 1	3.2 μm	100 nm	125 nm
NW 2	3 μm	110 nm	140 nm

Table 4.1: *Physical dimensions of the silicon nanowires used for piezoresistivity measurements*

4.1.3.1 Piezoresistivity measurements at room temperature

IThe semilogarithmic plot in figure 4.3 the relative resistance changes of NW 1 and NW 2 as a function of the applied strain. The green and the blue line represents the piezoresistive behavior of moderately p- and n-doped <111> oriented bulk silicon calculated by Kanda [13], respectively. Both nanowires where measured under ambient conditions and room temperature. A maximum strain of 3.07% was measured for NW 1 by Raman spectroscopy at 125 V actuator voltage which equals an applied stress of 5.74 GPa. Beyond $V_{Act} = 125\ V$, NW 1 ruptured which corresponds to reporeted fracture stress values of <111> oriented silicon nanowires in literature [10, 23].

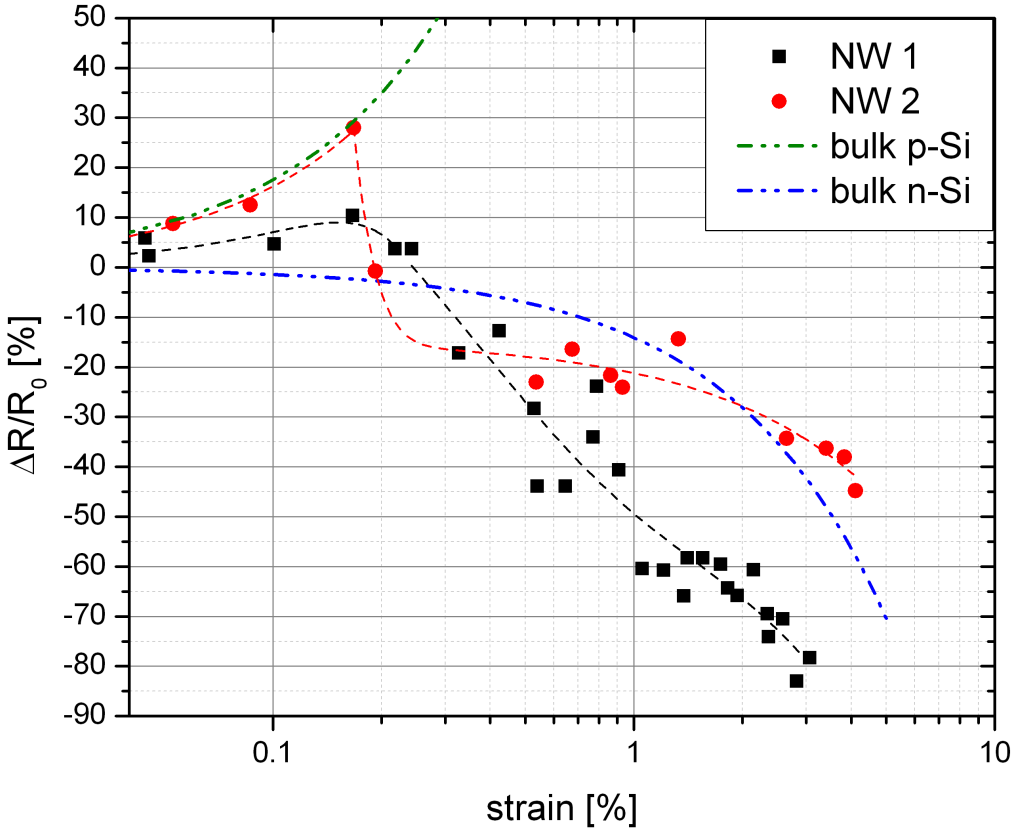

Figure 4.3: *Semilogarithmic plot of the relative resistance change of silicon nanowires as a function of applied strain. Measurements were executed under ambient conditions and room temperature. The green and blue dot dashed trend lines indicate piezoresistive behavior of <111> oriented moderately p- and n-doped bulk silicon, respectively.*

For NW 2 a maximum actuator voltage 100 V was applied to prevent a premature fracture of the nanowire. A maximum tensile strain of 4.1% was applied which corresponds to a stress of 7.67 GPa. Since straining the NW 2 up to 4.1% was reproducible, we suppose that the nanowire was strained within the elastic deformation range. The higher robustness of NW 2 was unexpected because a larger nanowire diameter normally means a lower fracture stress limit [10]. Micro defects in the bulk/nanowire tip interface of NW 1 could be a possible reason for the earlier fracture. Nevertheless, NW 1 withstood an about two times higher strain level as reported for bulk silicon.

The measurement data of both nanowires in figure 4.3 showed an increase in resistance for low tensile strain levels. Such a behavior is common for p-type silicon with stress applied in <111> direction. With increasing strain the trend changed and the nanowire resistances were decreasing. The increase of the relative nanowire resistance change of NW 1 slowly flattened with increasing strain reaching the peak value at 0.15%. Beyond 0.24% strain the relative resistance values inverted to negative values, i.e. the nanowire resistance under strain became lower than for the unstrained nanowire. In contrast, resistance of NW 2 increases linearly with an abrupt inversion of the trend and decreasing resistance for strain levels beyond 0.19%. A decrease of the resistance with increasing tensile strain is typical for n-type silicon. The relative resistance of NW 1 changed up to about -80% which is a five times lower resistance compared to the unstrained nanowire resistance. The relative resistance of NW 2 changed up to -45% which means a nearly bisection of the initial nanowire resistance.

For a better comparability of the nanowire piezoresistivity behavior with that of bulk silicon, the piezoresistive coefficients where calculated by dividing the relative change of nanowire resistance by the applied stress. In figure 4.4 the piezoresistive coefficients of NW 1 and NW 2 are plotted as a function of the applied strain on the nanowires. Again the bulk silicon values are marked with green and blue dot dashed trend lines.

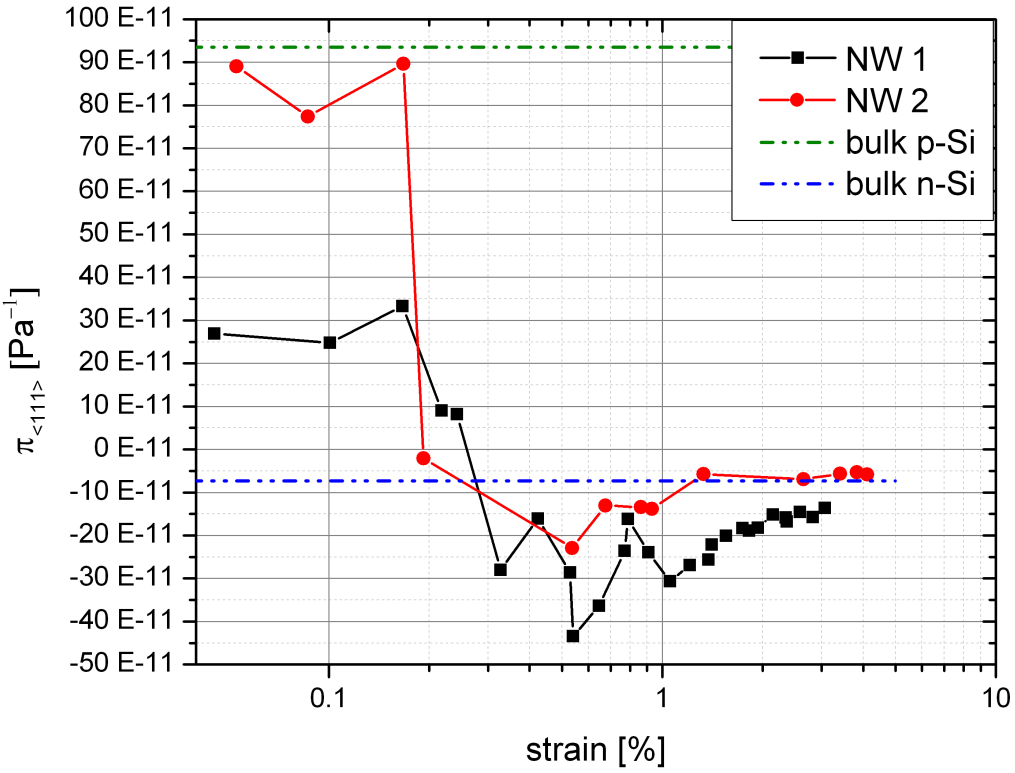

Figure 4.4: *Semilogarithmic plot of the piezoresistive coefficients of two different silicon nanowires as a function of applied strain. Measurements were executed under ambient conditions and room temperature. The green and blue dot dashed lines indicate the piezoresistive coefficients of <111> oriented moderately p- and n-doped bulk silicon, respectively.*

For NW 1 at strain levels below 0.16% the piezoresistive coefficient was about $+30{\cdot}10^{-11}\ Pa^{-1}$ while for higher strain levels up to 1% the coefficient was fluctuating around $-30 \cdot 10^{-11}\ Pa^{-1}$. Beyond 1% strain the piezoresistive coefficient of NW 1 was continuously converging to a value of $-14 \cdot 10^{-11}\ Pa^{-1}$. Hence, at low strain the piezoresistive coefficient of NW 1 was below the bulk value and for high strain above the bulk value of moderately p- and n-doped silicon, respectively.

Furthermore, the piezoresistive coefficient of NW 2 at low strain levels was around $+90 \cdot 10^{-11}\ Pa^{-1}$ and dropped instantly to values about $-13 \cdot 10^{-11}\ Pa^{-1}$ until 1% strain and $-6 \cdot 10^{-11}\ Pa^{-1}$ beyond 1% strain. Hence, the piezoresistive coefficient of NW 2 was close to the bulk value of moderately p-doped silicon for low strain levels and close to the bulk value of moderately n-doped silicon for high strain levels. In the intermediate regime from about 0.2% to 1% strain, the piezoresistive coefficient was slightly higher than the bulk value.

4.1.3.2 Piezoresistivity measurements at cryogenic temperatures

In this section the results to the temperature dependent piezoresistivity measurements of NW 2, measured in 25 K steps from 200 K to 300 K under vacuum conditions, are presented. The measurements were performed with the cryostatic temperature regulator setup described in section 3.3.3. To guarantee a constant temperature during the measurement at a defined temperature, the measurement duration was reduced by increasing the steps of V_{Act} from 5 V to 20 V.

At the investigated temperature regime, the extrinsic silicon carrier concentration and thus resistivity are dominated by the doping concentration (see section 2.3.2.1). Hence, the contact resistance of the highly p-doped silicon pads can still be neglected. Figure 4.5 shows the semilogarithmic plot of the relative resistance change of NW 2 as a function of the applied strain measured at different temperatures.

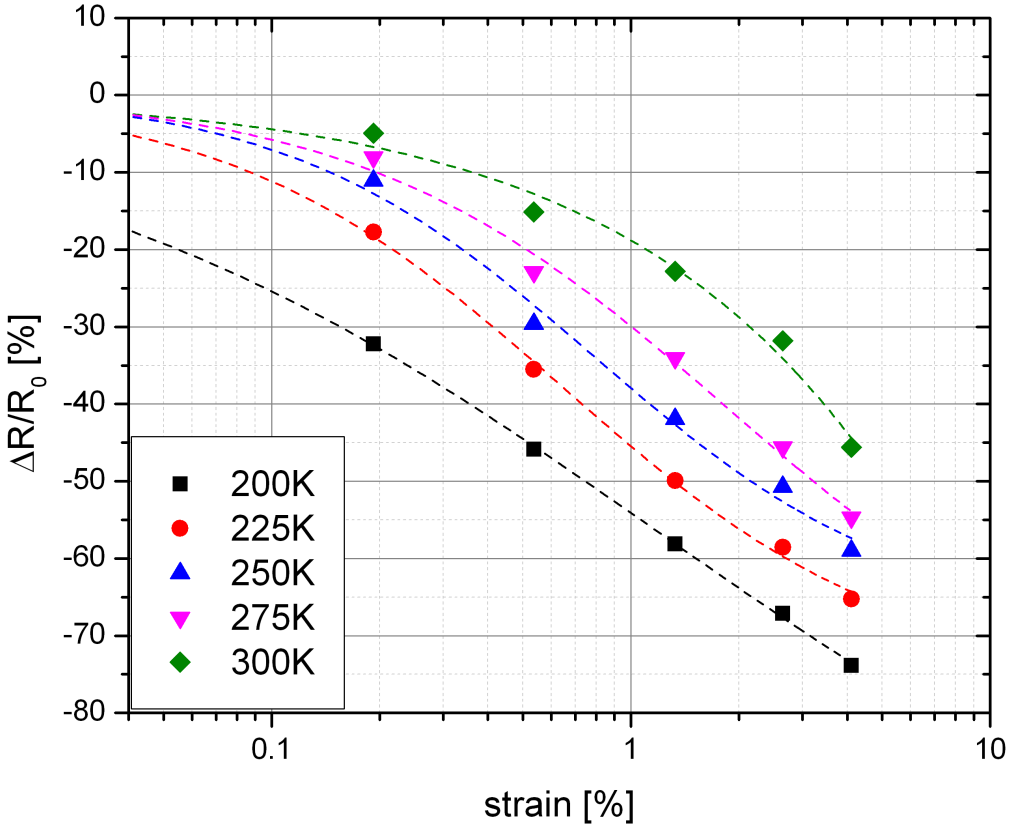

Figure 4.5: *Semilogarithmic plot of the relative resistance changes of NW 2 over the applied tensile strain for different temperatures. Measurements were executed under vacuum condition.*

For all temperature in vacuum a decrease of the resistance was observable with increasing tensile strain. Beyond 0.2% strain the relative resistance change measured at 300 K in vacuum was similar to the result measured at room temperature and ambient condition. With decreasing temperature the value of the relative resistance change at 0.2% strain was decreased from -4.9% at 300 K down to -32.1% at 200 K. The relative resistance change characteristics of all temperatures ran almost parallel for strain values above 0.5% and showed an n-type bulk silicon behavior.

The semilogarithmic plot of the piezoresistive coefficients as a function of the strain (see figure 4.6) exhibits the temperature dependency of the negative piezoresistive coefficient on applied strain, especially for small strain values.

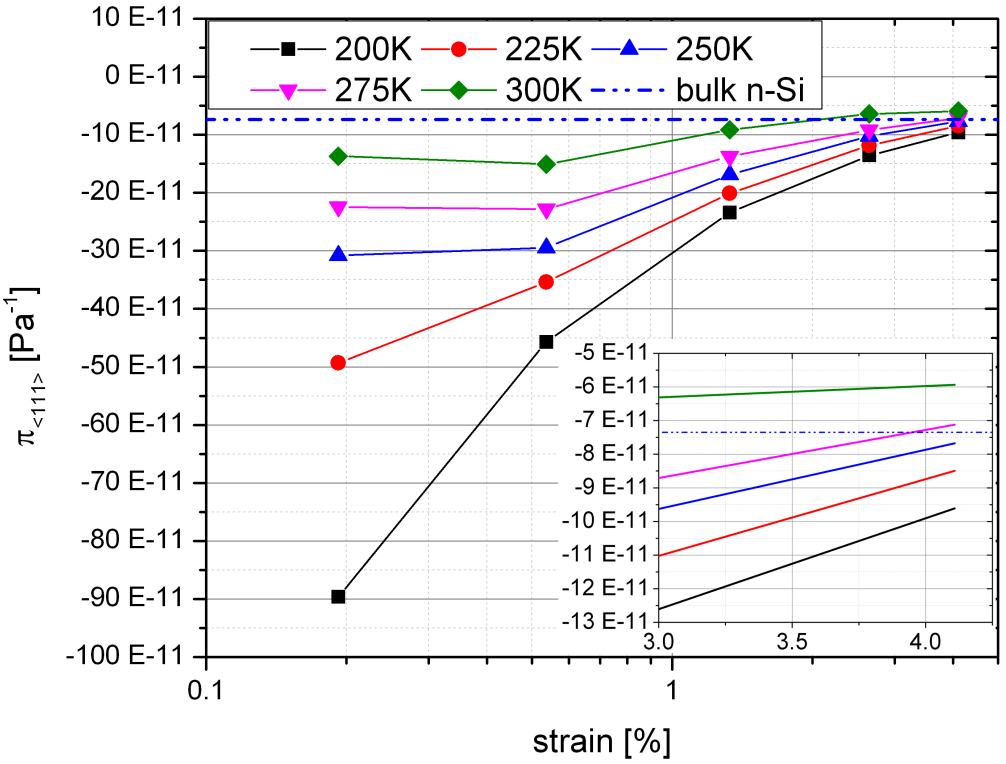

Figure 4.6: *Semilogarithmic plot of the piezoresistive coefficient of NW 2 as a function of the applied strain and the n-doped bulk silicon value for comparison. The inset shows a magnification of the high strain region with linear scale.*

While for 300 K and 0.2% strain the piezoresistive coefficient of NW 2 is about $-14 \cdot 10^{-11}\ Pa^{-1}$, at 200 K the piezoresistive coefficient is $-90 \cdot 10^{-11}\ Pa^{-1}$ which is six times higher than at 300 K and about ten times higher than the bulk silicon value. Nevertheless with increasing strain, the piezoresistive coefficients for each temperature were approaching to values common for n-type bulk silicon. In the

temperature range of 300 K to 250 K the piezoresistive coefficients were nearly constant up to 0.5% strain. Afterward the negative piezoresistive coefficient values started to decrease. For lower temperatures the negative piezoresistive coefficients were decreasing continuously with increasing strain.

In table 4.2 the piezoresistance multiplication factors P(T) of NW 2 at 4.1% tensile strain are given in comparison to the values calculated by Kanda [13] (see figure 2.13) for moderate doped n-type bulk silicon.

temperature [K]	this work	Kanda
300	1	1
275	1.20	1.10
250	1.29	1.21
225	1.43	1.35
200	1.62	1.52

Table 4.2: *Comparison of the piezoresistance multiplication factors P(T) measured on NW 2 at 4.1% tensile strain with values calculated by Kanda [13] for moderate doped n-type bulk silicon.*

The results for piezoresistance multiplication factor are in a good agreement with the calculations of Kanda.

4.1.4 Nanowire characterization under laser light excitation

Laser light excited measurements were performed on NW 2 utilizing the micro-Raman spectroscopy setup as described in section 3.3.4.

4.1.4.1 Influence of laser light excitation on the piezoresistivity

Figure 4.7 shows the semilogarithmic plot of the relative resistance change of NW 2 as a function of applied tensile strain for different laser excitation powers.

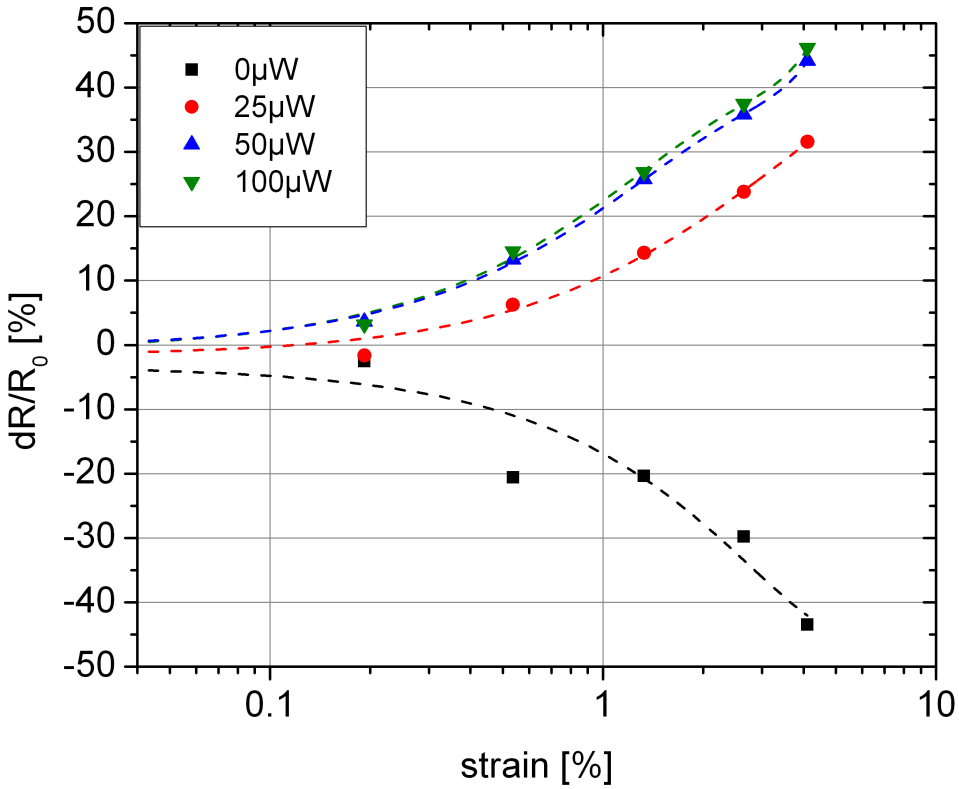

Figure 4.7: *Semilogarithmic plot of the relative resistance change of NW 2 as a function of the applied tensile strain at different laser excitation powers.*

Without excitation the nanowire showed qualitatively the same piezoresistive behavior as discussed before at comparable temperatures (see section 4.1.3). Under laser excitation the nanowire exhibited an increase in resistance with increasing strain over the whole applied strain range. The relative resistance change at 25 μW

excitation power reached a maximum value of 31.5% at 4.1% strain. By increasing the excitation power to 50 μW the relative resistance change increases to a maximum value of about 44%. A further increase of the laser power to 100 μW did not increase the piezoresistivity appreciable. The relative resistance change saturates at about 46% for a strain value of 4.1% although the overall resistance of the unstrained nanowire was continuously decreasing with increasing laser excitation power. The decrease of the unstrained nanowire resistance with increasing laser power is caused by the photo current, i.e. electron hole pair generation due to absorbed photons with energy higher than the bandgap of silicon.

The semilogarithmic plot of the piezoresistive coefficient as a function of the applied strain (figure 4.8) reveals that the piezoresistive coefficient values measured under laser excitation are approaching to a value around $5 \cdot 10^{-11}\ Pa^{-1}$ which is about twenty times smaller than the value of moderately p-doped bulk silicon.

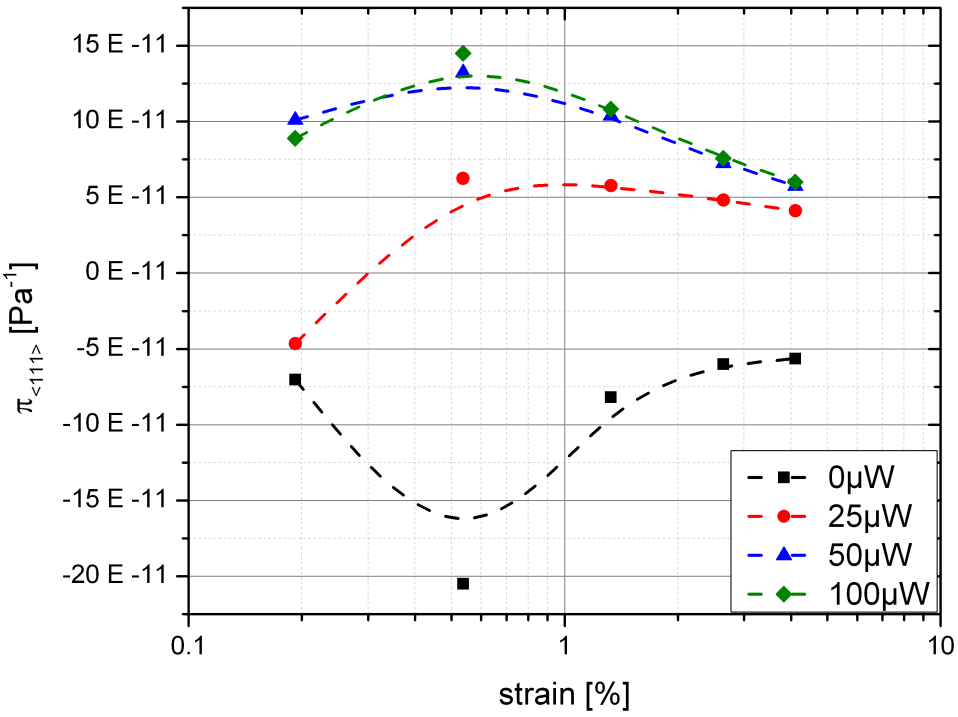

Figure 4.8: *Semilogarithmic plot of the piezoresistive coefficients of NW 2 as a function of the applied tensile strain for different laser excitation powers.*

4.1.4.2 Strain dependency of the photocurrent

As mentioned in the section above, the resistivity and thus the current over the nanowire is sensitive to the light excitation. With the electrical characterization of the nanowire under laser light, the photo current induced by the laser can be investigated (see section 3.3.4).

In figure 4.9 the influence of strain on the photocurrent for laser excitation with different laser powers is presented.

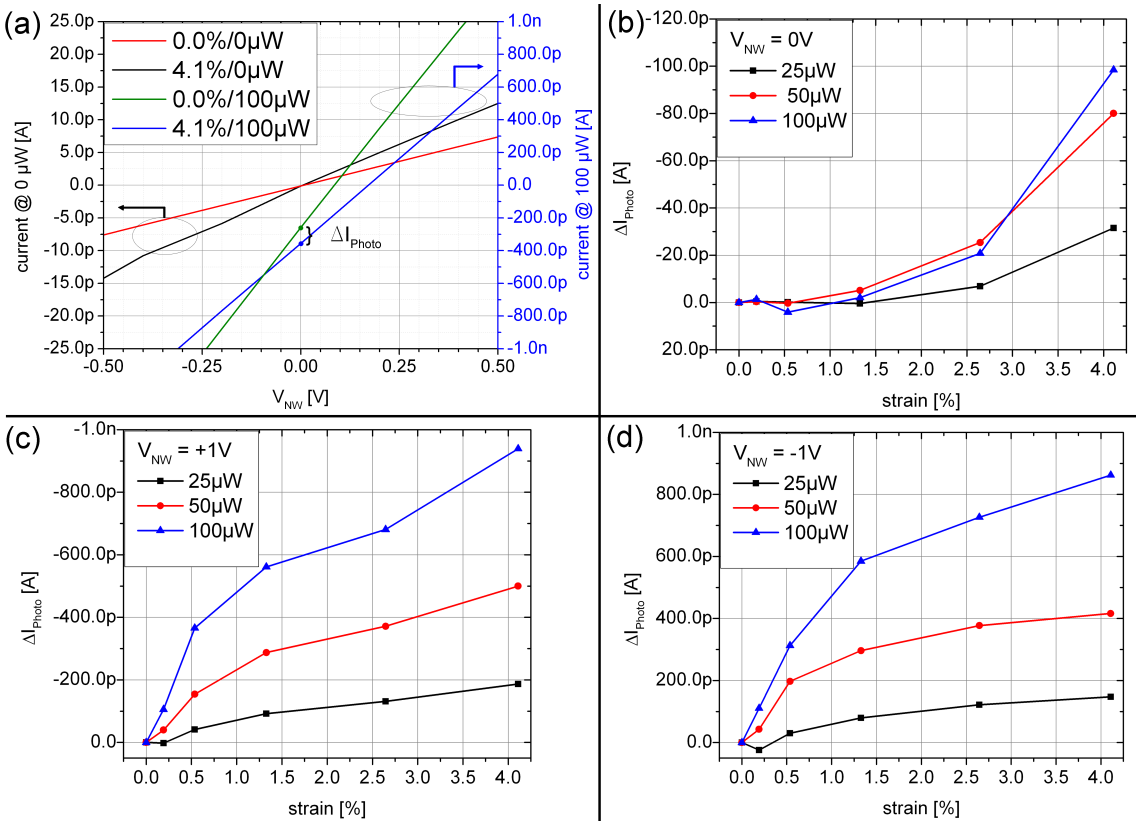

Figure 4.9: *The influence of strain in a silicon nanowire on the photocurrent at laser excitation with different laser powers. (a) Effect of 4.1% strain and 100 μW laser excitation on the I-V characteristic of NW 2. In (b), (c) and (d) ΔI_{photo} is plot as a function of the strain for $V_{bias} = 0\ V$, $V_{bias} = +1\ V$ and $V_{bias} = -1\ V$, respectively. While with bias voltage the photocurrent changes instantly with the strain, without bias voltage, changes of the photocurrent appear for strain levels higher than 1%.*

Figure 4.9(a) shows the I-V characteristic of NW 2 with and without applied strain of 4.1% as well as with and without laser excitation of 100 μW. Without

excitation the applied strain caused a decrease of the nanowire resistivity, observable by the increased slope of the nanowire current (black line) . Both strained (black) and unstrained (red)current trend lines have their intercept with the current axis at 0 V, indicating that no photocurrent was induced. Under laser excitation the slope of the unstrained nanowire current (green line) was higher than the slope of the strained nanowire current (blue line), which indicates a strain induced enhancement of the nanowire resistance. Strained as well as unstrained measurement of the nanowire under laser excitation showed a photocurrent even at $V_{bias} = 0\ V$, i.e. without an applied external field. To obtain photocurrents without applied external electric field, a carrier separation by a built-in voltage due to a gradient in the valence and conduction band is necessary [73, 74]. The homojunction interfaces of the intrinsic silicon nanowire monolithically integrated into the highly p-doped silicon structures of the EASD, provides such gradients in the bands. The photo current flow direction depends on which interface is illuminated. When both interfaces are illuminated than the photo currents cancel each other out. Hence, only one interface of NW 2 was illuminated, since a negative net photo current was measured without applied strain on the nanowire. Also the adsorbed molecules on the nanowire surface leads to a surface charge induced band bending coming along with a hole accumulation in the valence band [47]. These band bending leads to a high photoresponsivity of the nanowire, since the photogenerated electrons will recombine with surface states while the holes will be confined to the center of the nanowire [75]. The band bending at the depleted region of the nanowire cross section and thus the carrier concentration inside the nanowire is dependent on the nanowire diameter. Since the nanowire has a slightly tapered geometry a band gradient due to non-homogeneous carrier concentration along the nanowire can be expected.

The difference between the photo current at strained and at unstrained state is marked in figure 4.9(a) and is further denoted with ΔI_{photo}. In figure 4.9(b), (c) and (d) the change of the photo currents ΔI_{photo} without external electrical field ($V_{bias} = 0\ V$), at $V_{bias} = +1\ V$ and at $V_{bias} = -1\ V$ are shown as a function of the strain for different excitation laser powers. While without a bias voltage the photocurrent did not change significant before a strain level of about 1% was reached, with an applied external field the photocurrent altered instantly with the tensile strain. As shown before in figure 4.1, the strain along the nanowire for strain levels below 1% is homogeneously distributed. However with rising actuation of the EASD the strain distribution becomes inhomogeneous with higher strain at the thinner tip end of the nanowire than at the base. Since the bandgap of <111> oriented silicon narrows with tensile strain, a strain gradient over the nanowire occurs which is equivalent to an energy band gradient along the nanowire. Thus the change of the photo current without bias voltage can be associated to the inhomogeneously strain distribution at high strain levels beyond 1%.

In the case of an applied bias voltage, the generated photo current is already high due to charge carrier separation by the external electrical field. Thus the strain induced energy band modifications affect the photocurrent even at small strain levels.

4.1.5 Influence of the measurement conditions on the nanowire resistivity

An overview of the resistivity of NW 2 as a function of the applied tensile strain for different measurement conditions is given in figure 4.10.

The perfect agreement of the measurement result at room temperature with the about one week later measured result at $LP = 0\ \mu W$ demonstrates the reliability of the EASD technique. The nanowire resistivity of the unstrained nanowire was determined to be at 21.5 $k\Omega\,cm$ and decreased to about 12 $k\Omega\,cm$ for 4.1% strain. In vacuum at 300 K, the resistivity of the unstrained NW 2 was with 24 $k\Omega\,cm$ and for 4.1% with 12.5 $k\Omega\,cm$, about 10% higher than the resistivity of the same nanowire measured in air. This resistivity increase is attributed to the lack of absorbed molecules on the nanowire surface in vacuum. Without the adsorbed molecules, the surface doping effect due to hole accumulation in the valence band as described in section 2.3.5.1 is nonexistent. The absent resistance increase at low strain levels verifies this explanation.

The low temperature measurements under vacuum condition showed a strong increase of the resistivity with decreasing temperature. This increase is a result of the intrinsic nature of the nanowire (see equation 2.6) whereby carrier concentration is strongly dependent on the temperature. A reduction of the temperature is equivalent to a reduction in the carrier concentration. Due to piezoresistive effects, with increasing strain the resistivity was decreasing as shown in section 4.1.3.2.

Furthermore, with the generation of free charge carriers by laser excitation, the resistivity of NW 2 was reduced by two orders of magnitude. The higher the excitation laser power, the more charge carriers are generated and the lower is the nanowire resistivity. With increasing strain the resistivity was increasing as shown in section 4.1.4.1.

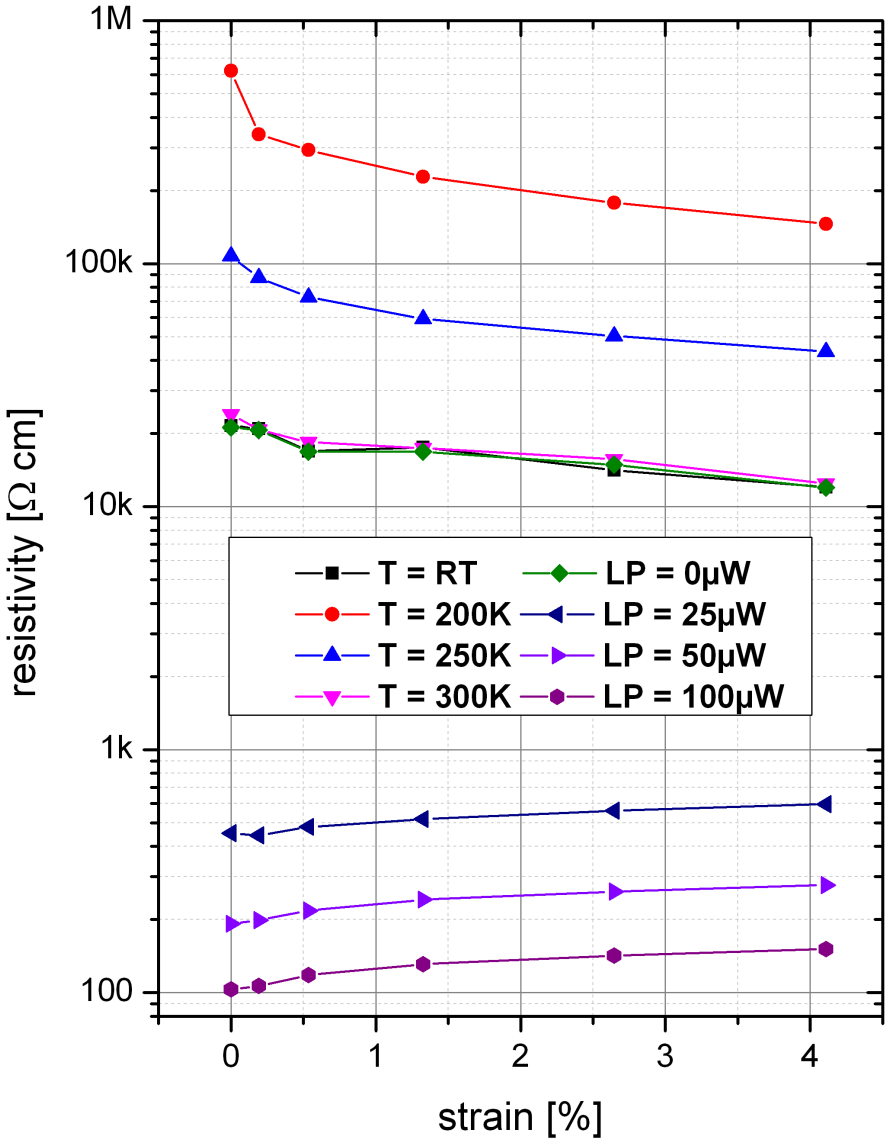

Figure 4.10: *Semilogarithmic plot of the resistivity of NW 2 as a function of tensile strain under different measurement conditions. The temperature dependent measurements $T = 300$ K, $T = 250$ K and $T = 200$ K were executed under vacuum and the measurements with different excitation laser powers (LP) were executed under ambient condition at room temperature.*

4.1.6 Discussion of the piezoresistivity of intrinsic <111> silicon nanowires

This section discusses the piezoresistive measurements dependent on temperature, ambient conditions and laser light excitation. A comparison of the different results exhibits that the atypical piezoresistive behavior of intrinsic nanowires has its origin in surface related effects.

As described in section 2.4.3, piezoresistive effects in bulk silicon are mainly determined by the majority charge carrier type.

- If transport is carried out mainly by holes, the hole transfer from the light hole band to the heavy hole band due to uniaxial tensile strain in <111> oriented silicon leads to a reduction of the mobility and thus to an increase of the resistance.
- For tensile strained <111> oriented n-type silicon, a narrowing of the bandgap leads to a increase of carrier concentration and thus to a reduction of the resistivity.
- For nanowires, the surface mainly determines the resistivity and thus piezoresistive effects. Strain caused modifications of trap state levels and the surface potential changes the carrier concentration in the nanowire and thus the resistivity significantly [16, 57].

The electrical measurements of the silicon nanowires revealed, that the piezoresistive behavior is affected by the listed piezoresistive effects, depending on the amount of strain applied on the nanowire and the prevailed measurement conditions.

At ambient conditions, adsorbed water molecules on the nanowire surface lead to additional surface charges and trap states with energies below the midgap of the silicon nanowire which cause electron trapping and thus Fermi level pinning below the midgap and subsequently band bending along the depleted surface region. As a result, an accumulation of holes in the valence band of the nanowire take place, leading to p-type behavior of intrinsic silicon nanowires [20, 40, 49]. Hence the intrinsic nanowire resistance rose with applied tensile strain up to 0.19%-0.25% (see section 4.1.3.1) due to the p-type piezoresistive effect. In comparison with work of Kanda [13], the thicker nanowire NW 2 had a piezoresistive coefficient similar to moderately p-doped bulk silicon. The piezoresistive coefficient of the thinner

nanowire NW 1 was about 3 times smaller than for NW 2 which equals highly p-doped bulk silicon (see figure 2.13). Due to the depletion layer for thinner nanowires, the charge carriers are highly concentrated in the inner of the nanowire with a carrier concentration similar to highly p-doped bulk silicon and thus leading to a reduced piezoresistive coefficient [46, 76]. Since the conducting area of the nanowire is also reduced, the resistivity of NW 1 was even two times higher than the resistivity of NW 2.

With increasing strain beyond 0.25%, a strong descent of the nanowire resistance occurred. Such pronounced changes in resistivity have been reported by He and Yang [14], Yang and Li [57] and were denoted as a giant piezoresistive effect. This giant piezoresistive effect results due to stress induced modulation of the trap state levels and thus surface potentials, leading to a filling or depopulation of the trap states [16]. The energy levels of the surface states at the Si/SiO_2 interface varies with changing bonding parameters such as bond lengths and bond angles of the dangling bonds and bonds with molecules adsorbed nearby [56]. Hence a deformation of the crystal lattice due to strain changes the surface state levels and thus the surface potential. The measurements suggest that tensile strain leads to a depopulation of the Si/SiO_2 interface traps and the adsorbed molecule trap states. Such mechanical stress induced modulation of the trapping/de-trapping behavior of the interface traps has been reported in MOSFET and memory devices [77, 78]. Particularly the surface potential is shifting with strain, resulting in a reduced depletion layer i.e. the traps become depopulated. Some of the de-trapped electrons recombine with the holes in the valence band and the others act as free charge carriers in the conduction band. Thus the charge carrier concentration increases and results in the fast descent of the nanowire resistance.

After reaching a strain level of about 1%, the resistance of NW 2 decreased slowly with a piezoresistive coefficient typical for moderate n-type bulk silicon. The piezoresistive coefficient of NW 1 converged to this value with increasing strain. The charge transport is now dominated by the de-trapped electrons from the Si/SiO_2 interface. An increasing strain leads to a narrowing of the bandgap and thus to an increase of the charge carrier concentration which again leads to a steady decreasing resistance.

Under vacuum conditions during the cryogenic measurements on NW 2 we observed no increase of resistance for small strain levels. Thus we assume that the accumulation of holes due to adsorbed water molecules did not occur without ambient air. At 300 K and below 1% strain the negative piezoresistive coefficient was slightly higher than for bulk silicon. The larger piezoresistive coefficient can be attributed again to a surface potential shift resulting in a release of additional free electrons from the surface traps and the piezoresistive coefficient approached the bulk value of n-type silicon.

At cryogenic temperatures a rapid decrease of resistance was observed for small strain levels and beyond a certain strain level the resistance was decreasing with a rate typical for n-type bulk silicon. This strain level determines the point where most of the trap states are depopulated. With decreasing temperature the depopulation strain level became lower and the relative change of resistance before the this strain level became larger. It seems that a reduction of the thermal energy due to cooling is reducing the capability of the Si/SiO_2 interface to trap electrons.

In the case of laser light excitation (see section 4.1.4.1) the nanowire is flooded with photo-generated electrons and holes. Thus, due the high amount of free charge carriers, the carriers released from the surface trap states, play a minor role for the nanowire piezoresistivity and the piezoresistive behavior of the nanowire is mainly determined by n- and p-type bulk piezoresistive effects. Since the p-type bulk piezoresistive effect has a stronger impact on the resistance of <111> oriented silicon than the n-type bulk piezoresistive effect, the nanowire exhibited a slightly positive piezoresistive coefficient. The identical piezoresistive behavior of the nanowire for 50 μW and 100 μW laser power verifies that resistance change over strain is dominated by piezoresistive effects and not by photo current related effects.

4.2 Strain related measurements on a <112> oriented silicon nanowire

This section is attended to the electrical characterization of an intrinsic <112> oriented silicon nanowire under tensile strain. The nanowire was synthesized on a silicon substrate and subsequently transferred to the EASD by pick and place technique as described in section 3.2.3.2. The diameter of the nanowire was increasing from 120 nm at the thinner end to 135 nm at the thicker end and the total length of the nanowire was 4 μm. Accidentally, the nanowire was placed 20° off, to the perpendicular of the gap facets. Hence applied strain on the nanowire was not pure uniaxial.

4.2.1 micro-Raman spectroscopy on <112> oriented silicon nanowires

Typical <112> oriented silicon nanowires exhibit {111} planar stacking faults along the growth axis [79]. These stacking faults give the nanowires next to the diamond cubic structure (3C) local domains of polytype structures depending on the periodic stacking fault arrangement. As the most common polytypes diamond hexagonal (2H) or rhombohedral (9R) silicon can be found [80]. The diverse local domains of polytype structures have different lattice constants and thus biaxially stresses surrounding domains, leading to variations of Raman peak positions and additional Raman peaks depending on the fraction of the diverse polytypes [81].

By executing a Raman spectroscopy line scan along the <112> oriented silicon nanowire integrated into the EASD the variation of Raman peak positions and additional Raman peaks were observed. Figure 4.11 shows the Raman spectra of an unstrained <111> , an unstrained <112> and a strained <112> oriented silicon nanowire.

The first-order Raman peak of the unstrained <112> oriented silicon nanowire is shifted in respect to the unstrained <111> oriented silicon nanowire peak. This shift changes with measurement position on the nanowire. Also an additional Raman peak appears at about 495 $rel.cm^{-1}$ originated from the 2H and 9R polytype structures. When strain is applied on the <112> oriented silicon nanowire both

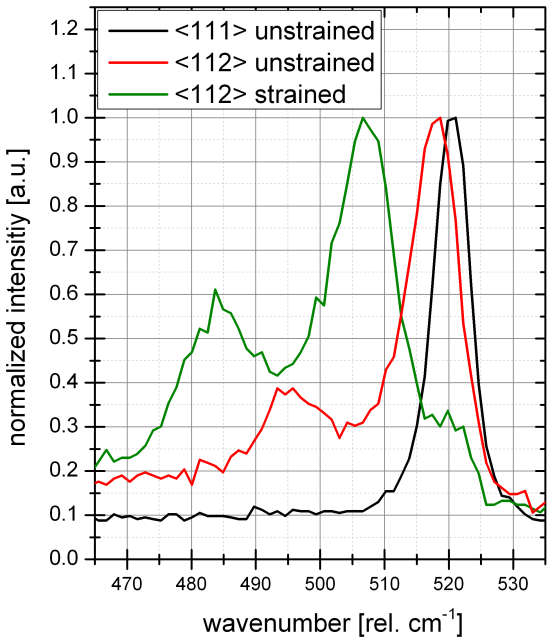

Figure 4.11: *Raman spectra of an unstrained <111> , an unstrained <112> and a strained <112> oriented silicon nanowire.*

first-order Raman peak and the additional Raman peak are shifting.

To determine the tensile strain depended Raman peak shifts, several line scans were performed for different actuator voltages measuring the Raman peak position the threefold degenerate first-order Raman peak of cubic silicon (see figure 4.12(a)). Subtracting the wavenumbers of the strained nanowire Raman peak with the wavenumbers of the unstrained nanowire for each spatial position result in the strain related peak shifts.

With equation 2.61 and knowing the factor k, the strain on the nanowire can be calculated from the peak shifts. A SEM calibration was not performed for the <112> oriented nanowire and the literature research was not successful. Hence, a factor k 333 cm^{-1} was assumed or further calculation which lies in between factors of <110> and <111> oriented silicon nanowires. In figure 4.12(b) the actuator voltage depended Raman peak shifts and the related strain values along the nanowire are depict. As strain value for the further calculations, the maximum strain values of the thinner nanowire end position $x = 2\ \mu m$ were used. The determined strain values have be treated with attention, since the influence of the applied tensile strain on the internal biaxial strain, caused by the polytype structure domains, and thus on the Raman peak shift is not fully clarified.

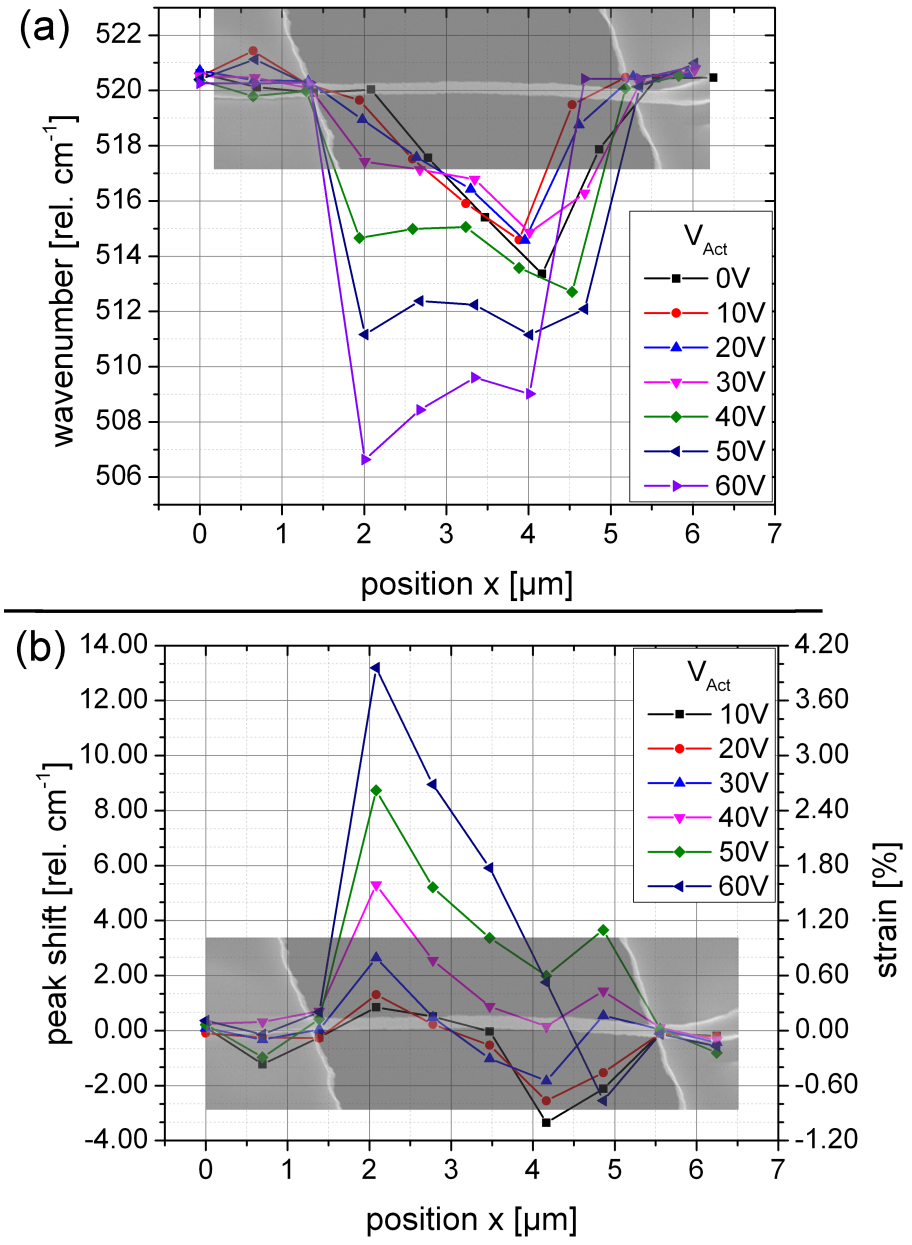

Figure 4.12: *(a) Raman peak position over the spatial position along a <112> silicon nanowire for different actuator voltages. (b) Strain caused Raman peak shifts as a function of the spatial position along the nanowire. A SEM image of the <112> silicon nanowire underlies both plots.*

4.2.2 Electrical characterization of a <112> nanowire

The pick and place integrated <112> silicon nanowire exhibits a near ohmic characteristic as shown in figure 4.13.

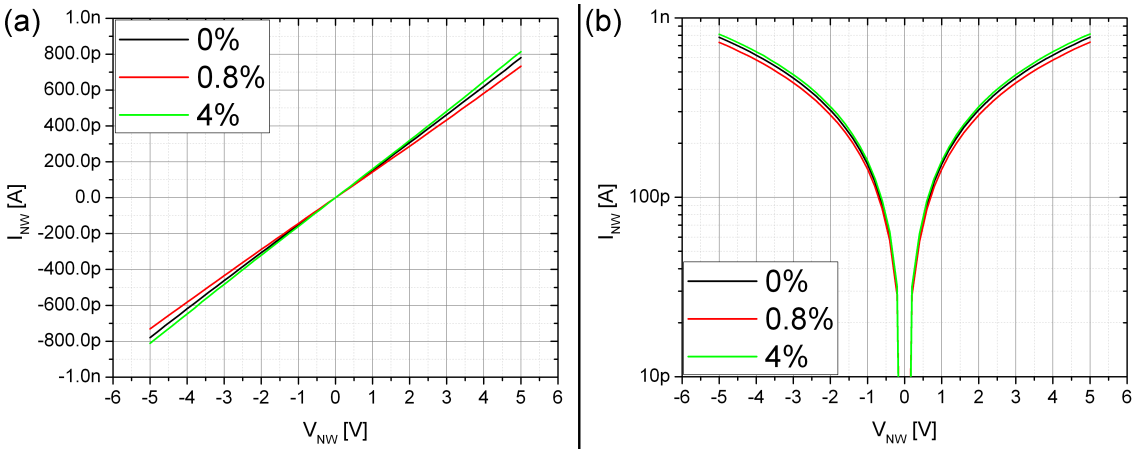

Figure 4.13: *(a) Linear and (b) semilogarithmic I-V plot of the <112> oriented silicon nanowire integrated into the EASD for different applied strain levels.*

Contrary to the <111> silicon nanowires the I-V characteristic remained symmetric and linearity of the I-V characteristic was not altered under tensile strain since the tungsten metal contacts fixing the nanowire are not effected by the strain. The resistivity of the unstrained <112> oriented nanowire was about 10 times smaller compared to the <111> oriented intrinsic silicon nanowires.

4.2.3 Piezoresistivity of a <112> oriented silicon nanowire

In figure 4.14 the relative change of resistance (black circles) as well as the piezoresistive coefficient (blue squares) are plotted as a function of the applied tensile strain. With increasing strain the resistance of the nanowire increased up to a strain level of about 1.5% with a maximum relative resistance change of 10.3%. Beyond that strain level the resistance decreased with increasing strain. For an applied strain higher than 3.6% the resistance became smaller than the initial resistance of the unstrained nanowire.

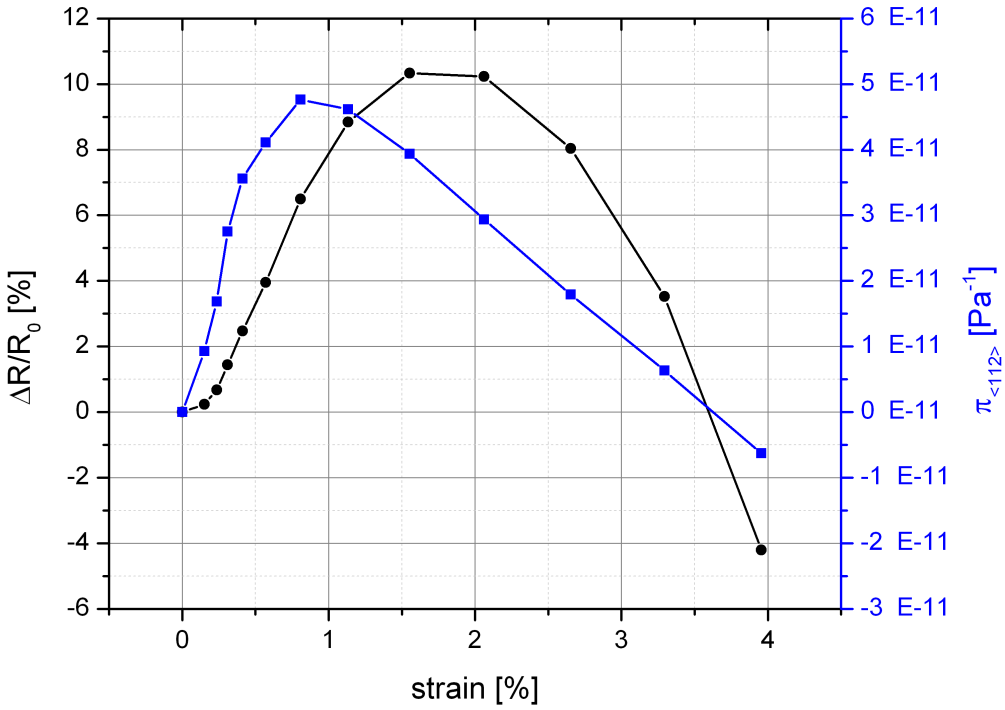

Figure 4.14: *Plot of the relative change of resistance (black circles) as well as the piezoresistive coefficient (blue squares) as a function of the applied tensile strain.*

The piezoresistive coefficient of the <112> silicon nanowire reached a maximum value of $4.8 \cdot 10^{-11}\ Pa^{-1}$ at 0.8% strain. At higher strain the piezoresistive coefficient was decaying linearly with the applied strain to a negative value of $-6 \cdot 10^{-12}\ Pa^{-1}$ at 4% strain.

Since the nanowire was not integrated exact in actuation direction of the EASD, a transverse strain component next to the longitudinal strain component had to be considered. Transverse stress has a big impact on the piezoresistivity of p-type silicon, reducing the resistance with increasing strain. In <112> oriented n-type silicon, the effect of strain on the resistance is also bigger than in <111> oriented silicon since a conduction band valley splitting (see section 2.4.3.1) appears similar to <110> oriented silicon. Hence, next the carrier concentration alteration due to the bandgap modification, an effective mass and thus electron mobility change affects the resistance. In table 4.3 the transverse and longitudinal piezoresistive coefficients of n- and p-type silicon given by Kanda [13] are listed.

doping type	n-type	p-type
$\varrho\ [\Omega\, cm]$	11.7	7.8
$\pi_{<112>l}$	-30	+70
$\pi_{<112>t}$	-5	-45

Table 4.3: *Tensile piezoresistive coefficients* $[10^{-11}\ Pa^{-1}]$ *for n-doped and p-doped <112> silicon in longitudinal (l) and transverse (t) direction at room temperature.*

With a ratio of 0.364 between transverse and longitudinal component of strain the effective piezoresistive coefficients are calculated to $28.14 \cdot 10^{-11}\ Pa^{-1}$ and $-20.9 \cdot 10^{-11}\ Pa^{-1}$ for p- and n-type silicon, respectively. It seems that the piezoresistive response of the <112> silicon nanowire was an interaction of electron and hole carrier transport. With increasing strain beyond the 1% strain level the electron transport was slightly preferred. The influence of the surface adsorbed molecules on the resistivity played a minor role which could be also an effect of the larger nanowire diameter. The strain shifted the surface potential, thus releasing free electrons from to Si/SiO_2 interface traps resulting in n-type piezoresistive behavior. The effect of the polytype structures inside the nanowire and the thus induced initial biaxial stress can also have a huge influence of the nanowire resistance and has to be investigated in more detail. The about 10 times smaller resistivity of the <112> nanowire in comparison to the <111> nanowires could have its origin in the internal biaxial strain.

Chapter 5

Conclusion

Silicon nanowires are intensively investigated since twenty years but still exhibit interesting effects. One of them is the atypical piezoresistive behavior in comparison to bulk silicon. Anomalous piezoresistivity and giant piezoresistive effects have a huge potential to find application e.g. in highly sensitive strain gauges. Since the nanowire surface has a big influence on the resistivity also applications as chemical sensors are given. While piezoresistive effects in doped silicon nanowires have been intensely investigated, intrinsic nanowires and their piezoresistive behavior have been largely overlook up to now.

The scope of this thesis was the investigation of the anomalous piezoresistivity of intrinsic silicon nanowires and its origin by measuring the electrical properties of the nanowire under different measurement conditions. Therefore a dedicated electrostatic actuated MEMS straining device (EASD) was developed and manufactured to satisfy the requirements of executing high strain experiments in several different measurement setups, i.e. SEM, Raman spectroscopy and cryostatic measurements. Monolithically integration of the nanowires into such an EASD was performed and the piezoresistive behavior was measured in ambient conditions and vacuum at different temperatures. Also the influence of laser light excitation on the nanowire piezoresistivity and the dependency of tensile strain on the photocurrent have been investigated.

After a short introduction, chapter two treats the theoretical aspects of the work. The basic properties of silicon as well as the VLS based nanowire synthesis with the

most important parameters to control the synthesis, are presented. A section about the electronic properties of silicon, including the carrier concentration of intrinsic as well as doped silicon is reviewed and the derivation of the resistivity within the framework of the Drude model for electric transport is given. A section about carrier generation and recombination with attention on trap states and the influence of the nanowire surface on the electrical transport finishes the electrical properties section. Here the amphoteric nature of the Si/SiO_2 interface states and the influence of the trap states on effective nanowire diameter and carrier concentration as well as the effect of adsorbed molecules on the nanowire surface are described. The next section the definitions of stress and strain in a crystal lattice are given, followed by a description of the piezoresistivity in generally. The origin of piezoresistive effects in n- and p-doped bulk silicon and atypical piezoresistive effects in silicon nanowires are summarized and a quantitative model, i.e. the deformation potential theory, for the prediction of strain-induced energy level shifts was given. The next section includes an introduction of the Raman effect and the dependency of the Raman shift on strain. The chapter is closed the derivation of equations to calculate the actuation forces of comb drive actuated MEMS devices.

Chapter three takes attention on the experimental procedures used for this work. First the functionality of the EASD and its basic parts are described as well as all relevant design features. Thereafter the fabrication of an EASD is explained in detail. Also an estimation of generated actuation force and applied strain on typical nanowires is given utilizing the set of equations from chapter two and the applied geometric design parameters. With $60\mu N$ inducing about 4% strain in a 100 nm diameter nanowire at 110V actuator voltage the EASD is predestined for high strain experiments on silicon nanowires. In the next section the synthesis of <111> and <112> oriented nanowires is described in detail as well as the two methods for nanowire integration into the EASD, i.e. the monolithic integration and the pick and place technique. Furthermore the measurement setups and measurement methods to characterize the nanowires under several environment conditions are presented including the mathematical calculations to extract current and resistance values from the raw data for piezoresistance determination. Finally the measurement of the k factor to correlate strain and Raman shift is shown.

In chapter four the results of the measurements are presented and discussed. This chapter is divided into measurements on two monolithically integrated <111> silicon nanowire and measurements on a pick and place integrated <112> silicon nanowire. The first part started with Raman investigation the I-V characteristic of a <111> oriented nanowire exhibiting a slightly non-linear behavior in the unstrained state. Under strain an ambipolar I-V characteristic occurs attributed to asymmetric stress on the monolithic contacts. Under ambient conditions and small strain

levels the resistance of the nanowire was increases with a piezoresistive coefficient similar to the value of p-type bulk silicon. With increasing strain the resistance radically dropped and beyond 1% strain the resistance of the nanowire decreases with a piezoresistive coefficient typical for n-type bulk silicon. The low strain p-type behavior of the nanowire is a result of holes accumulation due to adsorbed molecules. With increasing strain the surface potential shifts, resulting in a reduction of the depletion radius and releases free electrons into the nanowire. Hence the nanowire resistance decreases. In vacuum only a strain induced lowering of the resistance is measurable due to the lack of holes generated by adsorbed molecules.

By reducing temperature, the strain level is reduced which is necessary to shift the surface potential above the midgap and release electrons from the trap states, since electron trapping capability of the Si/SiO_2 interface is reduced with reduced thermal energy. Under laser excitation the nanowire exhibites an interplay of p- and n-type piezoresistive effects since the nanowire is flooded with both photo-generated holes and electrons. Surface effects play a minor role in comparison to unexcited nanowires. Furthermore a laser power and strain depended photo current is measured even at zero bias voltage. Thereby charge carrier separation is attributed to an non-uniform strain distribution along the nanowire and band bending at the nanowire/bulk interfaces.

Part two of this chapter treats the electrical characterization of a <112> silicon nanowire under strain. Raman spectroscopy revealed the existence of polytype structures inside the nanowire due to stacking fault formation. The strain experiment with the EASD shows a weak anomalous piezoresistivity, originating in the interplay of transverse and longitudinal piezoresistive effects since the applied strain on the nanowire is not uniaxial. The influence of the surface states on the piezoresistivity of the nanowire is not that distinct as for the <111> nanowires.

Summarizing, the developed MEMS device proved to be an ideal strain engineering platform to perform high strain experiments on silicon nanowires under several measurement conditions. The anomalous piezoresistivity of intrinsic silicon nanowires could be investigated with different measurement setups revealing its origin in surface related effects combined with bulk piezoresistive effects. The versatile utilizability of the MEMS device opens the way for further strain related applications on miscellaneous nanostructures.

List of Abbreviations

AFM	Atomic Force Microscopy
Al_2O_3	Aluminum oxide
BHF	Buffered Hydrofluoric Acid
BOX	Buried Oxide
DI water	De-Ionized water
EASD	Electrostatic Actuated Straining Device
EBID	Electron Beam Induced Deposition
FET	Field Effect Transistor
FIB	Focused Ion Beam
Ge	Germanium
HH	Heavy Hole
I-V	Current-Voltage
LH	Light Hole
LP	Laser Power
LPCVD	Low Pressure Chemical Vapor Deposition
MEMS	Micro Electro Mechanical System
MFC	Mass Flow Controller
NA	Numeric Aperture
NW	Nanowire
RIE	Reactive Ion Etching
sccm	Standard Cubic Centimeters per Minute
SEM	Scanning Electron Microscopy
Si	Silicon
SiO_2	Silicondioxide
SMU	Source Monitor Unit
SOI	Silicon-On-Insolator
VLS	Vapor-Liquid-Solid
WD	Working Distance

List of EASD processing parameters

Lithography

MEMS pattern

- resist spin-coating: AZ5214 (1:1) 35 s with 9000 rpm
- pre-bake: 1 minute at 100 C
- direct laser writing: 2mm write head; Energy 10; Defoc 1800; 10% filter
- resist development: 25 s in MIF726

Dielectrophoresis pattern

- resist spin-coating: AZ5214 (1:1) 35 s with 3000 rpm
- pre-bake: 1 minute at 100 C
- resist spin-coating: AZ5214 (1:0) 35 s with 3000 rpm
- pre-bake: 1 minute at 100 C
- resist spin-coating: AZ5214 (1:0) 35 s with 5000 rpm
- pre-bake: 1 minute at 100 C

- direct laser writing: 4mm write head; Energy 100; Defoc 1700; 50% filter
- resist development: 50 s in MIF726

Chromium mask deposition by magnetron sputtering

- layers: 3
- power: 50 W
- duration per layer: 60 s
- rate: 20 nm / min

RIE parameters for anisotropic silicon etching

- temperature: -110 C
- pressures: work 10 mtorr, strike 35 mtorr
- gas flows: O_2 10 sccm, SF_6 50 sccm, He 5sccm
- powers: RF 15 W, ICP 100 W
- etch rate: ca. $1\mu m$ / min

Bibliography

[1] J. Bardeen and W. Shockley. Deformation potentials and mobilities in non-polar crystals. *Phys. Rev.*, 80:72–80, Oct 1950. doi: 10.1103/PhysRev.80.72.

[2] C. S. Smith. Piezoresistance effect in germanium and silicon. *Phys. Rev.*, 94: 42–49, Apr 1954. doi: 10.1103/PhysRev.94.42.

[3] R. Craddock. Sensors based on silicon strain gauges. In *Sensing Via Strain, IEE Colloquium on*, pages 5/1–5/4, Oct 1993.

[4] C. Y.-P. Chao and S. L. Chuang. Spin-orbit-coupling effects on the valence-band structure of strained semiconductor quantum wells. *Phys. Rev. B*, 46: 4110–4122, Aug 1992. doi: 10.1103/PhysRevB.46.4110.

[5] M. V. Fischetti, F. Gámiz, and W. Hänsch. On the enhanced electron mobility in strained-silicon inversion layers. *Journal of Applied Physics*, 92(12):7320–7324, 2002. doi: 10.1063/1.1521796.

[6] S. E. Thompson, G. Sun, Y. S. Choi, and T. Nishida. Uniaxial process induced strained Si: extending the CMOS roadmap. *Electron Devices, IEEE Transactions on*, 53(5):1010–1020, May 2006. ISSN 0018-9383. doi: 10.1109/TED.2006.872088.

[7] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, and M. Bohr. A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors. In *Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International*, pages 11.6.1–11.6.3, Dec 2003. doi: 10.1109/IEDM.2003.1269442.

[8] M. L. Lee, E. A. Fitzgerald, M. T. Bulsara, M. T. Currie, and A. Lochtefeld. Strained Si, SiGe, and Ge channels for high-mobility metal-oxide-semiconductor

field-effect transistors. *Journal of Applied Physics*, 97(1), 2005. doi: 10.1063/1.1819976.

[9] S. M. Hu. Critical stress in silicon brittle fracture, and effect of ion implantation and other surface treatments. *Journal of Applied Physics*, 53(5):3576–3580, 1982. doi: 10.1063/1.331137.

[10] Y. Zhu, F. Xu, Q. Qin, W. Y. Fung, and W. Lu. Mechanical properties of vapor-liquid-solid synthesized silicon nanowires. *Nano Letters*, 9(11):3934–3939, 2009. doi: 10.1021/nl902132w.

[11] S. Hoffmann, I. Utke, B. Moser, J. Michler, S. H. Christiansen, V. Schmidt, S. Senz, P. Werner, U. Gösele, and C. Ballif. Measurement of the bending strength of vapor-liquid-solid grown silicon nanowires. *Nano Letters*, 6(4):622–625, 2006. doi: 10.1021/nl052223z.

[12] L. T. Ngo, D. Almécija, J. E. Sader, B. Daly, N. Petkov, J. D. Holmes, D. Erts, and J. J. Boland. Ultimate-strength germanium nanowires. *Nano Letters*, 6 (12):2964–2968, 2006. doi: 10.1021/nl0619397.

[13] Y. Kanda. A graphical representation of the piezoresistance coefficients in silicon. *Electron Devices, IEEE Transactions on*, 29(1):64–70, Jan 1982. doi: 10.1109/T-ED.1982.20659.

[14] R. He and P. Yang. Giant piezoresistance effect in silicon nanowires. *Nat Nano*, 1(1):42–46, Oct 2006. doi: 10.1038/nnano.2006.53.

[15] J. X. Cao, X. G. Gong, and R. Q. Wu. Giant piezoresistance and its origin in si(111) nanowires: First-principles calculations. *Phys. Rev. B*, 75:233302, Jun 2007. doi: 10.1103/PhysRevB.75.233302.

[16] A. C. H. Rowe. Silicon nanowires feel the pinch. *Nat Nano*, 3(6):311–312, Jun 2008. doi: 10.1038/nnano.2008.108.

[17] P. Neuzil, C. C. Wong, and J. Reboud. Electrically controlled giant piezoresistance in silicon nanowires. *Nano Letters*, 10(4):1248–1252, 2010. doi: 10.1021/nl9037856.

[18] J. S. Milne, A. C. H. Rowe, S. Arscott, and Ch. Renner. Giant piezoresistance effects in silicon nanowires and microwires. *Phys. Rev. Lett.*, 105:226802, Nov 2010. doi: 10.1103/PhysRevLett.105.226802.

[19] A. C. H. Rowe. Piezoresistance in silicon and its nanostructures. *Journal of Materials Research*, 29:731–744, 2014. doi: 10.1557/jmr.2014.52.

[20] A. Lugstein, M. Steinmair, A. Steiger, H. Kosina, and E. Bertagnolli. Anomalous piezoresistance effect in ultrastrained silicon nanowires. *Nano Letters*, 10 (8):3204–3208, 2010. doi: 10.1021/nl102179c.

[21] A. San Paulo, J. Bokor, R. T. Howe, R. He, P. Yang, D. Gao, C. Carraro, and R. Maboudian. Mechanical elasticity of single and double clamped silicon nanobeams fabricated by the vapor-liquid-solid method. *Applied Physics Letters*, 87(5):053111, 2005. doi: 10.1063/1.2008364.

[22] C.-L. Hsin, W. Mai, Y. Gu, Y. Gao, C.-T. Huang, Y. Liu, L.-J. Chen, and Z.-L. Wang. Elastic properties and buckling of silicon nanowires. *Advanced Materials*, 20(20):3919–3923, 2008. ISSN 1521-4095. doi: 10.1002/adma.200800485.

[23] J. W. Ma, W. J. Lee, J. M. Bae, K. S. Jeong, Y. S. Kang, M. H. Cho, J. H. Seo, J. P. Ahn, K. B. Chung, and J. Y. Song. Effects of surface chemical structure on the mechanical properties of si1-xgex nanowires. *Nano Letters*, 13 (3):1118–1125, 2013. doi: 10.1021/nl304485d.

[24] J. Greil, A. Lugstein, C. Zeiner, G. Strasser, and E. Bertagnolli. Tuning the electro-optical properties of germanium nanowires by tensile strain. *Nano Letters*, 12(12):6230–6234, 2012. doi: 10.1021/nl303288g.

[25] Z. Yong, L. Xinyu, R. Changhai, L. Z. Yan, D. Lixin, and S. Yu. Piezoresistivity characterization of synthetic silicon nanowires using a MEMS device. *Microelectromechanical Systems, Journal of*, 20(4):959–967, Aug 2011. doi: 10.1109/JMEMS.2011.2153825.

[26] J. M. Chen and N. C. MacDonald. Measuring the nonlinearity of silicon piezoresistance by tensile loading of a submicron diameter fiber using a microinstrument. *Review of Scientific Instruments*, 75(1):276–278, 2004. doi: 10.1063/1.1633005.

[27] R. A. Bernal, T. Filleter, J. G. Connell, K. Sohn, J. Huang, L. J. Lauhon, and H. D. Espinosa. In situ electron microscopy four-point electromechanical characterization of freestanding metallic and semiconducting nanowires. *Small*, 10(4):725–733, 2014. doi: 10.1002/smll.201300736.

[28] M. E. Weeks. The discovery of the elements. xii. other elements isolated with the aid of potassium and sodium: Beryllium, boron, silicon, and aluminum. *Journal of Chemical Education*, 9(8):1386, 1932. doi: 10.1021/ed009p1386.

[29] J. Singh. *Semiconductor devices: basic principles*. Wiley, 2001. ISBN 9780471362456.

[30] M. A. Green. Intrinsic concentration, effective densities of states, and effective mass in silicon. *Journal of Applied Physics*, 67(6):2944–2954, 1990. doi: 10.1063/1.345414.

[31] M. Morita, T. Ohmi, E. Hasegawa, M. Kawakami, and M. Ohwada. Growth of native oxide on a silicon surface. *Journal of Applied Physics*, 68(3):1272–1281, 1990. doi: 10.1063/1.347181.

[32] Z. Huang, H. Fang, and J. Zhu. Fabrication of silicon nanowire arrays with controlled diameter, length, and density. *Advanced Materials*, 19(5):744–748, 2007. doi: 10.1002/adma.200600892.

[33] Y.Y. Wong, M. Yahaya, M. Mat Salleh, and B. Yeop Majlis. Controlled growth of silicon nanowires synthesized via solid-liquid-solid mechanism. *Science and Technology of Advanced Materials*, 6(3-4):330–334, 2005. ISSN 1468-6996. doi: 10.1016/j.stam.2005.02.011.

[34] R. S. Wagner and W. C. Ellis. Vapor-liquid-solid mechanism of single crystal growth. *Applied Physics Letters*, 4(5):89–90, 1964. doi: 10.1063/1.1753975.

[35] J. Westwater, D. P. Gosain, S. Tomiya, S. Usui, and H. Ruda. Growth of silicon nanowires via gold/silane vapor-liquid-solid reaction. *Journal of Vacuum Science & Technology B*, 15(3):554–557, 1997. doi: 10.1116/1.589291.

[36] Y. Cui, L. J. Lauhon, M. S. Gudiksen, J. Wang, and C. M. Lieber. Diameter-controlled synthesis of single-crystal silicon nanowires. *Applied Physics Letters*, 78(15):2214–2216, 2001. doi: 10.1063/1.1363692.

[37] M. S. Gudiksen, J. Wang, and C. M. Lieber. Synthetic control of the diameter and length of single crystal semiconductor nanowires. *The Journal of Physical Chemistry B*, 105(19):4062–4064, 2001. doi: 10.1021/jp010540y.

[38] A. Lugstein, M. Steinmair, Y. J. Hyun, G. Hauer, P. Pongratz, and E. Bertagnolli. Pressure-induced orientation control of the growth of epitaxial silicon nanowires. *Nano Letters*, 8(8):2310–2314, 2008. doi: 10.1021/nl8011006.

[39] V. Schmidt, S. Senz, and U. Gösele. Diameter-dependent growth direction of epitaxial silicon nanowires. *Nano Letters*, 5(5):931–935, 2005. doi: 10.1021/nl050462g.

[40] Y. Cui, X. Duan, J. Hu, and C. M. Lieber. Doping and electrical transport in silicon nanowires. *The Journal of Physical Chemistry B*, 104(22):5213–5216, 2000. doi: 10.1021/jp0009305.

[41] J. E. Sutherland and J. R. Hauser. A computer analysis of heterojunction and graded composition solar cells. *Electron Devices, IEEE Transactions on*, 24(4): 363–372, Apr 1977. doi: 10.1109/T-ED.1977.18742.

[42] J. E. Allen, E. R. Hemesath, D. E. Perea, J. L. Lensch-Falk, Y. Liz, F. Yin, M. H. Gass, P. Wang, A. L. Bleloch, R. E. Palmer, and L. J. Lauhon. High-resolution detection of au catalyst atoms in si nanowires. *Nat Nano*, 3(3): 168–173, March 2008. doi: 10.1038/nnano.2008.5.

[43] Y. Dan, K. Seo, K. Takei, J. H. Meza, A. Javey, and K. B. Crozier. Dramatic reduction of surface recombination by in situ surface passivation of silicon nanowires. *Nano Letters*, 11(6):2527–2532, 2011. doi: 10.1021/nl201179n.

[44] V. Schmidt, S. Senz, and U. Gösele. Influence of the Si/SiO_2 interface on the charge carrier density of si nanowires. *Applied Physics A: Materials Science & Processing*, 86(2), 2006. doi: 10.1007/s00339-006-3746-2.

[45] N. Yoshio, T. Kiyoshi, and O. Atsushi. Study of silicon-silicon dioxide structure by electron spin resonance ii. *Japanese Journal of Applied Physics*, 11(1):85, 1972. doi: 10.1143/JJAP.11.85.

[46] M. T. Björk, H. Schmid, J. Knoch, H. Riel, and W. Riess. Donor deactivation in silicon nanostructures. *Nature nanotechnology*, 4(2):103–107, 2009. doi: 10.1038/nnano.2008.400.

[47] J. Jie, W. Zhang, G. Peng, K.and Yuan, C. S. Lee, and S.-T. Lee. Surface-dominated transport properties of silicon nanowires. *Advanced Functional Materials*, 18(20):3251–3257, 2008. doi: 10.1002/adfm.200800399.

[48] U. Kumar Bhaskar, T. Pardoen, V. Passi, and J.-P. Raskin. Surface states and conductivity of silicon nano-wires. *Journal of Applied Physics*, 113(13):134502, 2013. doi: 10.1063/1.4798611.

[49] B. Salem, F. Dhalluin, T. Baron, H. Jamgotchian, F. Bedu, H. Dallaporta, P. Gentile, N. Pauc, M. I. Den Hertog, J. L. Rouviere, et al. Chemical-vapour-deposition growth and electrical characterization of intrinsic silicon nanowires. *Materials Science and Engineering: B*, 159:83–86, 2009. doi: 10.1016/j.mseb.2008.09.011.

[50] Y. Sun, S.E. Thompson, and T. Nishida. *Strain Effect in Semiconductors: Theory and Device Applications*. Springer US, 2009. ISBN 9781441905529.

[51] J. J. Wortman and R. A. Evans. Young's modulus, shear modulus, and poisson's ratio in silicon and germanium. *Journal of Applied Physics*, 36(1):153–156, 1965. doi: 10.1063/1.1713863.

[52] W. A. Brantley. Calculated elastic constants for stress problems associated with semiconductor devices. *Journal of Applied Physics*, 44(1):534–535, 1973. doi: 10.1063/1.1661935.

[53] C. Herring and E. Vogt. Transport and deformation-potential theory for many-valley semiconductors with anisotropic scattering. *Physical Review*, 101(3):944, 1956.

[54] C. G. Van de Walle. Band lineups and deformation potentials in the model-solid theory. *Phys. Rev. B*, 39:1871–1883, Jan 1989. doi: 10.1103/PhysRevB.39.1871.

[55] P. Kleimann, B. Semmache, M. Le Berre, and D. Barbier. Stress-dependent hole effective masses and piezoresistive properties of *p*-type monocrystalline and polycrystalline silicon. *Phys. Rev. B*, 57:8966–8971, Apr 1998. doi: 10.1103/PhysRevB.57.8966.

[56] T. Sakurai and T. Sugano. Theory of continuously distributed trap states at Si-SiO2 interfaces. *Journal of Applied Physics*, 52(4):2889–2896, 1981. doi: 10.1063/1.329023.

[57] Y. Yang and X. Li. Giant piezoresistance of p-type nano-thick silicon induced by interface electron trapping instead of 2D quantum confinement. *Nanotechnology*, 22(1):015501, 2011. doi: 10.1088/0957-4484/22/1/015501.

[58] K. Winkler, E. Bertagnolli, and A. Lugstein. Origin of anomalous piezoresistive effects in VLS grown Si nanowires. *Nano letters*, 15(3):1780–1785, 2015. doi: 10.1021/nl5044743.

[59] C. V. Raman and K. S. Krishnan. A new type of secondary radiation. *Nature*, 121(3048):501–502, 1928. doi: 10.1038/121501c0.

[60] W. H. Weber and R. Merlin. *Raman Scattering in Materials Science*. Physics and astronomy online library. Springer, 2000. ISBN 9783540672234.

[61] E. Anastassakis, A. Pinczuk, E. Burstein, F. H. Pollak, and M. Cardona. Effect of static uniaxial stress on the Raman spectrum of silicon. *solid state Communications*, 8(2):133–138, 1970. doi: 10.1016/0038-1098(93)90294-W.

[62] F. Ureña, S. H. Olsen, and J.-P. Raskin. Raman measurements of uniaxial strain in silicon nanostructures. *Journal of Applied Physics*, 114(14):144507, 2013. doi: 10.1063/1.4824291.

[63] T. R. Hart, R. L. Aggarwal, and Benjamin Lax. Temperature dependence of Raman scattering in silicon. *Phys. Rev. B*, 1:638–642, Jan 1970. doi: 10.1103/PhysRevB.1.638.

[64] A. Torres, A. Martín-Martín, O. Martínez, A. C. Prieto, V. Hortelano, J. Jiménez, A. Rodríguez, J. Sangrador, and T. Rodríguez. Micro-raman spectroscopy of Si nanowires: Influence of diameter and temperature. *Applied Physics Letters*, 96(1):011904, 2010. doi: 10.1063/1.3284647.

[65] G.T.A. Kovacs. *Micromachined Transducers Sourcebook*. McGraw-Hill series in electrical and computer engineering. WCB/McGraw-Hill, 1998. ISBN 9780072907223.

[66] M. Gad-el Hak. *The MEMS Handbook, Second Edition - 3 Volume Set*. Mechanical and Aerospace Engineering Series. Taylor & Francis, 2005. ISBN 9780849321061.

[67] A. Lugstein, Y. J. Hyun, M. Steinmair, B. Dielacher, G. Hauer, and E. Bertagnolli. Some aspects of substrate pretreatment for epitaxial Si nanowire growth. *Nanotechnology*, 19(48):485606, 2008. doi: 10.1088/0957-4484/19/48/485606.

[68] M. S. Islam, S. Sharma, T. Kamins, and R. S. Williams. A novel interconnection technique for manufacturing nanowire devices. *Applied physics A*, 80(6):1133–1140, 2005. doi: 10.1007/s00339-004-3177-x.

[69] A. Chaudhry, V. Ramamurthi, E. Fong, and M. S. Islam. Ultra-low contact resistance of epitaxially interfaced bridged silicon nanowires. *Nano Letters*, 7 (6):1536–1541, 2007. doi: 10.1021/nl070325e.

[70] A. Lugstein, M. Steinmair, C. Henkel, and E. Bertagnolli. Scalable approach for vertical device integration of epitaxial nanowires. *Nano Letters*, 9(5):1830–1834, 2009. doi: 10.1021/nl803776a.

[71] C.-Y. Peng, C.-F. Huang, Y.-C. Fu, Y.-H. Yang, C.-Y. Lai, S.-T. Chang, and C. W. Liu. Comprehensive study of the raman shifts of strained silicon and germanium. *Journal of Applied Physics*, 105(8):083537, 2009. doi: 10.1063/1.3110184.

[72] H. C. Card. Aluminum-silicon schottky barriers and ohmic contacts in integrated circuits. *Electron Devices, IEEE Transactions on*, 23(6):538–544, Jun 1976. doi: 10.1109/T-ED.1976.18449.

[73] J. Greil, S. Birner, E. Bertagnolli, and A. Lugstein. Nanowires enabling strained photovoltaics. *Applied Physics Letters*, 104(16):163901, 2014. doi: 10.1063/1.4871458.

[74] Y. Ahn, J. Dunning, and J. Park. Scanning photocurrent imaging and electronic band studies in silicon nanowire field effect transistors. *Nano Letters*, 5(7):1367–1370, 2005. doi: 10.1021/nl050631x.

[75] A. Zhang, H. Kim, J. Cheng, and Y.-H. Lo. Ultrahigh responsivity visible and infrared detection using silicon nanowire phototransistors. *Nano Letters*, 10(6): 2117–2120, 2010. doi: 10.1021/nl1006432.

[76] I. Kimukin, M. S. Islam, and R. S. Williams. Surface depletion thickness of p-doped silicon nanowires grown using metal-catalysed chemical vapour deposition. *Nanotechnology*, 17(11):S240, 2006. doi: 10.1088/0957-4484/17/11/S03.

[77] A. Hamada and E. Takeda. Hot-electron trapping activation energy in PMOSFET's under mechanical stress. *Electron Device Letters, IEEE*, 15(1):31–32, Jan 1994. doi: 10.1109/55.289471.

[78] R. Arghavani, N. Derhacobian, V. Banthia, M. Balseanu, N. Ingle, H. MSaad, S. Venkataraman, E. Yieh, Z. Yuan, L.-Q. Xia, Z. Krivokapic, U. Aghoram, K. MacWilliams, and S. E. Thompson. Strain engineering to improve data retention time in nonvolatile memory. *Electron Devices, IEEE Transactions on*, 54(2):362–365, Feb 2007. doi: 10.1109/TED.2006.888827.

[79] F. M. Davidson, D. C. Lee, D. D. Fanfair, and B. A. Korgel. Lamellar twinning in semiconductor nanowires. *The Journal of Physical Chemistry C*, 111(7): 2929–2935, 2007. doi: 10.1021/jp0672205.

[80] F. J. Lopez, E. R. Hemesath, and L. J. Lauhon. Ordered stacking fault arrays in silicon nanowires. *Nano Letters*, 9(7):2774–2779, 2009. doi: 10.1021/nl901315s.

[81] F. J. Lopez, U. Givan, J. G. Connell, and L. J. Lauhon. Silicon nanowire polytypes: Identification by Raman spectroscopy, generation mechanism, and misfit strain in homostructures. *ACS Nano*, 5(11):8958–8966, 2011. doi: 10.1021/nn2031337.

Own publications and conference contributions

1. S. Wagesreither, E. Bertagnolli, S. Kawase, Y. Isono, A. Lugstein: Electrostatic actuated strain engineering in monolithically integrated VLS grown silicon nanowires; *Nanotechnology*, 25 (2014), 45; S. 455705-1 - 455705-6

2. S. Wagesreither, A. Lugstein, E. Bertagnolli: Anisotropic lithiation behavior of crystalline silicon; *Nanotechnology*, 23 (2012), S. 4957161 - 4957164

3. S. Wagesreither, E. Bertagnolli, S. Kawase, Y. Isono, A. Lugstein: Investigations on the Piezoresistivity of Monolithically Integrated VLS Grown Silicon Nanowires by Electrostatic Actuation with a MEMS Device; MRS Fall Meeting 2014, Boston, MA, USA; 30.11.2014 - 05.12.2014

4. S. Wagesreither, K. Winkler, A. Lugstein, Y. Isono, E. Bertagnolli: Tunable Straining of Silicon Nanowires Integrated in a MEMS Device by Electrostatic Actuation; Smart Systems Integration (SSI) 2014, Vienna, Austria; 26.03.2014 - 27.03.2014

5. S. Wagesreither, A. Lugstein, Y. Isono, E. Bertagnolli: Tuning the Tensile Strain in Silicon Nanowires by an Electrostatic Actuated MEMS Device; MRS Fall Meeting 2013, Boston, MA, USA; 01.12.2013 - 06.12.2013

6. S. Wagesreither, A. Lugstein, E. Bertagnolli: Ultra Fast and Anisotropic Diffusion of Lithium in Silicon Nanostructures; DPG-Frühjahrstagung 2012 (Spring Meeting of the Condensed Matter Section), Berlin, Germany; 25.03.2012 - 30.03.2012

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