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Diploma Thesis / Diplomarbeit

Power Amplifier and Low Phase Noise Synthesizer for L-DACS1

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Abstract

L-DACS1 is the future digital communication system for the European civil air traffic. It is OFDM-based with a bandwidth of 498 kHz and operates in the L-band around 1 GHz with a peak transmit power of 53 dBm $\hat{=}$ 200 W. To verify the technical feasibility of the specifications and the compatibility with existing systems like GPS, a transmitter prototype is needed. Hardware is built and verified that upconverts a 70 MHz intermediate frequency signal to the 1 GHz band, including a local oscillator synthesizer satisfying the low phase noise requirements of L-DACS1. The power amplifier chain is linearized using digital predistortion to meet the very rigorous spectral mask that requires −76 dBc outside a bandwidth of only 1544 kHz. The linearity requirement is the main challenge as it is on the edge of feasibility.

Kurzfassung

L-DACS1 ist das zukünftige digitale Kommunikationssystem für die europäische Zivilluftfahrt. Es basiert auf OFDM mit einer Bandbreite von 498 kHz und arbeitet im L-Band bei 1 GHz mit einer Spitzenleistung von 53 dBm $\hat{=}$ 200 W. Um die Umsetzbarkeit der Spezifikationen und die Verträglichkeit mit bestehenden Systemen wie GPS zu überprüfen, ist ein Sender-Prototyp notwendig. Hardware wird gebaut und verifiziert, die ein 70 MHz Zwischenfrequenz-Signal in das 1 GHz-Band umsetzt, inklusive eines Synthesizers für den lokalen Oszillator, der den Anforderungen von L-DACS1 an das Phasenrauschen genügt. Die Leistungsverstärker-Kette wird mit digitaler Vorverzerrung linearisiert, um der sehr strengen spektralen Maske gerecht zu werden, die −76 dBc außerhalb einer Bandbreite von nur 1544 kHz verlangt. Diese Linearitätsanforderung ist am Rande der Umsetzbarkeit und daher die wesentliche Herausforderung.

Contents

1 Introduction

1.1 Motivation

On December 7th, 1944, the "Convention on International Civil Aviation" was signed by 52 states. Also called the "Chicago Convention" it set up a code of conduct and established the International Civil Aviation Organization (ICAO) to regulate and coordinate international aviation. Annex 10 specifies the speech radio system, an AM-based analog design that operates in the very high frequency band (VHF, 30 to 300 MHz) that is still used to date [1].

Being the only means of communication between tower and aircraft, the analog voice channels quickly became crowded as air traffic increased rapidly. The airspace over the densely-populated EU area is especially busy so congestion was prevalent.

As a counter-measure, the channel spacing was reduced several times from 200 kHz to ultimately 8.33 kHz, significantly increasing the number of channels available (table 1.1).

Year	Used frequencies	Channel spacing	Number of available channels
1947	118-132 MHz	200 kHz	70
1958	118-132 MHz	100 kHz	140
1964	118-136 MHz	50 kHz	360
1972	118-136 MHz	25 kHz	720
1995	118-137 MHz	8.33 kHz	2280

Table 1.1: ICAO speech radio standards [2]

Additionally, the airspace was segmented into smaller cells with a control station in each one to permit frequency reuse in non-adjacent cells. However, finer segmentation leads to an increase in handover traffic that at some point outweighs the capacity increase. The way out is to make the communication more bandwidth-efficient. As the channel spacing for the analog speech channel cannot be decreased significantly more, the speech dialogues have to be replaced by digital messages.

Digital aeronautical telecommunication started in the late 1970s with the advent of ACARS (Aircraft Communications Addressing and Reporting System) in North America, also operating in the VHF band and providing 300 bits/s. While ACARS initially provided AOC (airline operational control) services such as flight status reporting for the airlines, it was later used to offload simple repetitive dialogues (clearances) between tower and aircraft from the crowded voice channels to the data channel.

CPDLC (Controller Pilot Data Link Communications) extends the use-cases of the data channel for more air traffic control tasks, saving more speech radio time. This

digital interface is mandatory for all new aircraft in the EU since January 1, 2011 [3].

The next-generation European air traffic management (ATM) system is developed in the SESAR program (Single European Sky ATM Research). By unifying the European airspace, switching to end-to-end trajectory planning with a high degree of computer support and automation, and several organizational improvements, the program aims to reach ambitious goals [4]:

- Triple the European air-space capacity (flight traffic is expected to increase by 50% until 2020)
- Improve safety by a factor of ten
- Decrease fuel consumption by 10% per flight by using optimal paths
- Reduce ATM costs by 50%

The L-DACS1 (L-Band Digital Aeronautical Communication System) transmission technology aims to provide enough bandwidth to the European air traffic of the future. It complements the speech channels in the VHF band with a fast digital data link that operates in the L-band around 1 GHz. This band, however, is shared with a number of other services, the most prominent being satellite navigation and distance measurement equipment (DME). L-DACS1 is designed to not disturb these existing services.

To verify compatibility of the L-DACS1 system with these other services and also to demonstrate the technical feasibility of implementing the specification, a prototype transmitter is needed. Prototype hardware for L-DACS1 has already been built by the DLR (Deutsches Zentrum für Luft- und Raumfahrt – German Aerospace Center) delivering good results [5]. However, the DLR prototype transmitter delivered a significantly lower output power than required by the L-DACS1 specification.

1.2 Scope of this Thesis

In the course of this thesis, the upconversion and power amplifier (PA) part of a transmitter prototype is built by the author, one of the four building blocks of the overall system prototype that is shown in figure 1.1. The baseband unit is provided by Frequentis AG. Reference receiver and receiver are both built at the EMCE by Michael Zaisberger and Reinhard Koeppner, respectively. Both receiver and transmitter contain a microcontroller board that provides a serial control interface to set the power level, the frequency channel etc. The final transmitter and receiver prototypes are housed in industry-standard 19 inch (482.6 mm) rack-mount cases.

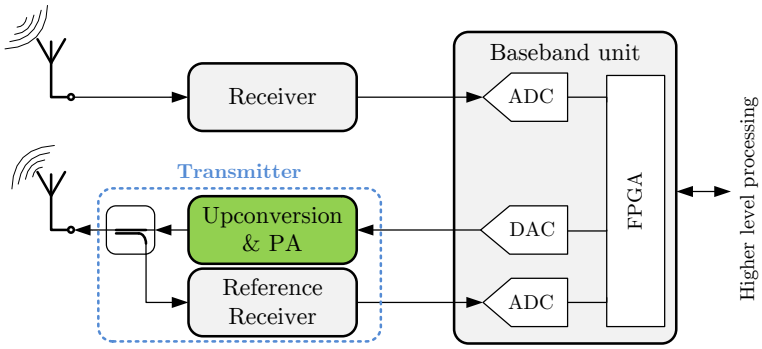


Figure 1.1: Overall system diagram - subject of this thesis are upconversion and PA

The upconversion and PA part includes a single-sideband quadrature upconverter, gain stages, a local oscillator synthesizer, a driver amplifier, and a power amplifier that delivers the full output power required by the L-DACS1 specification of 53 dBm peak. It also includes linearisation of the transmit chain using digital predistortion (DPD).

1.3 Main Challenges

The average RF output power is 42 dBm or 16 W. L-DACS1 is an OFDM system and inherits the property of a high PAPR (peak to average power ratio). With the PAPR at 11 dB, the peak output power of the power amplifier is 53 dBm. Including a system margin for connector losses, the power amplifier is designed to provide 53.5 dBm or 224 W peak RF power (42.5 dBm average).

The main challenge is to fulfill the very tight spectral mask at this output power (fig. 1.2, with f_0 denoting the center frequency). From the edge of the signal bandwidth (498 kHz), the spectral mask falls off to −76 dBc only 523 kHz away from the band edge. This is a requirement at the edge of feasibility. As this is the critical point, every part of the design aims to provide the best possible linearity.

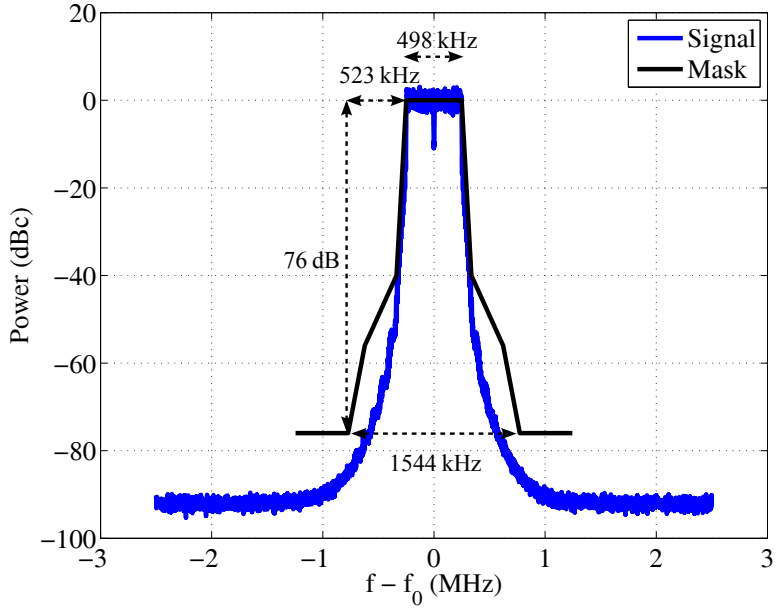


Figure 1.2: Spectrum of the baseband signal compared to the spectral mask

2 Device Nonlinearity

Components that are not strictly passive, like electronically controlled attenuators, introduce nonlinearities. The dominating contributions usually come from the amplifiers, especially from the final stages outputting high power levels. This chapter focuses on the nonlinearity of amplifiers and modeling their behavior.

2.1 Power Series Model

The ideal amplifier is linear, time-invariant, and memory-less and has the simple transfer function,

$$y(t) = ax(t). \tag{2.1}$$

A real amplifier has a more complicated transfer function. For the model used here, only the assumption of linearity is dropped, equivalent to assuming a *static/memory-less nonlinearity*. A common approach to approximate the transfer function is using a power series model:

$$y(t) = a_1 x(t) + a_2 x(t)^2 + a_3 x(t)^3 + \dots \tag{2.2}$$

Note that the existence of even-order powers implies that the transfer function is asymmetric in the sense that negative voltages are transferred differently than positive voltages.

In the frequency domain, the multiplications map to convolutions:

$$Y(j\omega) = a_1 X(j\omega) + a_2 X(j\omega) * X(j\omega) + a_3 X(j\omega) * X(j\omega) * X(j\omega) + \dots \tag{2.3}$$

2.2 The Two-Tone Experiment

Amplifier data sheets usually do not provide the coefficients a_n used in the power series model (equ. 2.2) but the third-order intercept-point (IP3) that is based on the two-tone experiment.

In the two-tone experiment, two sinusoidal carriers with equal amplitude spaced a small frequency offset apart are used as the input signal:

$$x(t) \quad = b\left(\cos(\omega_1 t) + \cos(\omega_2 t)\right) \tag{2.4}$$

with $|\omega_1 - \omega_2| \ll \omega_0 = \frac{\omega_1+\omega_2}{2}$.

Assuming a transfer function containing only the first and third power,

$$\tilde{y}(t) = a_1 x + a_3 x^3 \tag{2.5}$$

the resulting signal is

$$\begin{aligned} y(t) &= a_1 x + a_3 x^3 \\ &= \left[b\tfrac{a_1}{2} + b^3\tfrac{9a_3}{8}\right] \quad \left[\cos(\omega_1 t) + \cos(\omega_2 t)\right] \\ &+b^3\tfrac{3a_3}{8} \quad \Big[\cos((2\omega_1 - \omega_2)t) + \cos((2\omega_2 - \omega_1)t) \\ &\qquad + \cos((2\omega_1 + \omega_2)t) + \cos((2\omega_2 + \omega_1)t)\Big] \\ &+b^3\tfrac{a_3}{8} \quad \left[\cos(3\omega_1 t) + \cos(3\omega_2)t)\right]. \end{aligned} \tag{2.6}$$

The spectrum is shown in figure 2.1.

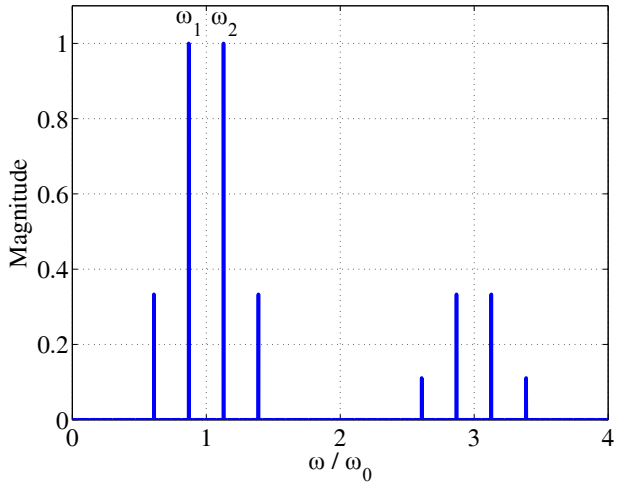


Figure 2.1: Third-order harmonics in the two-tone experiment

As the spectrum of the fundamental signal is discrete, the convolutions reduce to a summation and the output spectrum is discrete again. The third-order nonlinearity generates new frequency components at $2\omega_1 \pm \omega_2$, $2\omega_2 \pm \omega_1$, $3\omega_1$ and $3\omega_2$. A N-th order nonlinearity generates the frequencies

$$n\omega_1 + m\omega_2 \quad \forall \quad n, m \in \mathbb{Z} \quad | \quad |n| + |m| = N. \tag{2.7}$$

In the case of a third-order nonlinearity, the magnitude of the fundamental frequencies at the output linearly depends on the magnitude of the input. The third-order harmonics show a cubic dependency. This is the basis for measuring the IP3.

2.3 The Third-order Intercept Point (IP3)

The IP3 is the most important metric concerning linearity. It can be measured easily using two continuous wave (CW) generators, whose outputs are combined using a power

combiner, and a spectrum analyzer: The two CW carriers are spaced a small offset frequency apart to realize a two-tone experiment. On the spectrum analyzer, the power of the fundamental frequencies and the harmonics can be read. As the power level of both fundamental carriers is equal, either one can be measured. A frequency of $2\omega_1 - \omega_2$ or $2\omega_2 - \omega_1$ is selected to read the power of the third-order harmonics.

Having the amplifier "sufficiently far away from compression" (to be defined below), 1 dB of input power change results in 1 dB of output power change for the fundamental signal. The third-order harmonics have a slope of 3 dB/dB. Fitting straight lines yields an intersection point, called the third-order intercept point (fig. 2.2).

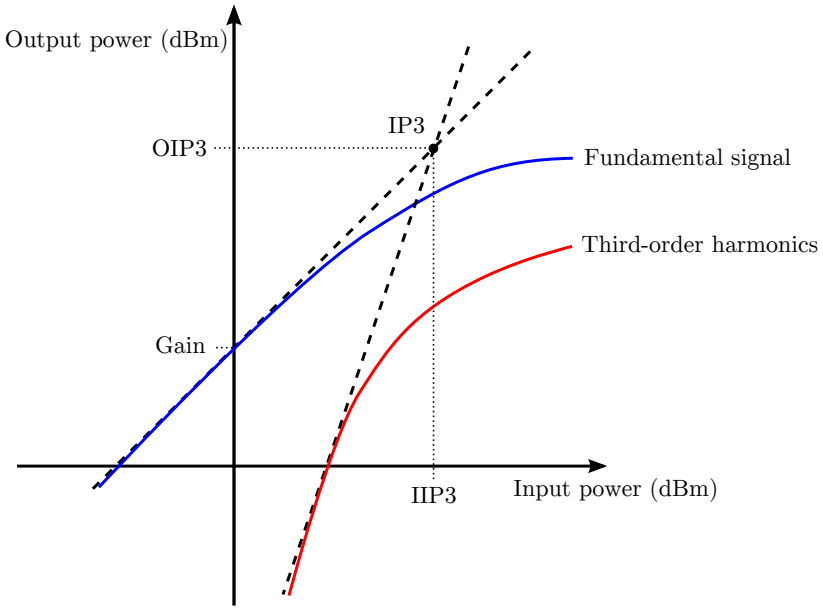


Figure 2.2: Definition of input-IP3 (IIP3) and output-IP3 (OIP3)

The coordinates of the IP3 can be stated in terms of input or output power yielding the input-IP3 (*IIP3*) or the output-IP3 (*OIP3*), respectively. Being two equivalent descriptions, the transformation is (in dB scale),

$$OIP3 = IIP3 + Gain. \tag{2.8}$$

Manufacturers tend to prefer the OIP3, not least because it gives higher numbers, and call it just IP3. This convention will be also used in this thesis.

What does "sufficiently far away from compression" mean? Looking at equation 2.6, it is seen that the signals at frequencies ω_1 and ω_2 carry the factor $b\frac{a_1}{2} + b^3\frac{9a_3}{8}$, that is, they depend linearly *and* cubically on the input signal's amplitude b. "Far away" means that $b\frac{a_1}{2} \gg b^3\frac{9a_3}{8}$ or equivalently $b^2 \ll \frac{a_1}{a_3}\frac{4}{9}$. Then, the cubic component at the fundamental frequencies can be neglected. This is up to a factor of 3 the relation connecting the a_n coefficients and the IP3:

$$IIP3 = \frac{a_1}{a_3}\frac{4}{3}. \tag{2.9}$$

Notably, this point can neither be reached practically nor theoretically. Practically, both slopes become gentler as the amplifier enters compression, eventually reaching 0 dB/dB. Theoretically, the minimal ratio between fundamental and harmonics magnitude is (equ.2.6)

$$\lim_{b\to\infty} \frac{b\frac{a_1}{2} + b^3\frac{9a_3}{8}}{b^3\frac{3a_3}{8}} = 3, \tag{2.10}$$

or 9.54 dB.

2.4 Inter-modulation Distance and Shoulder Distance

The inter-modulation distance (IMD) is defined as ratio of the power of the fundamental signal and the strongest odd-order harmonic. In a dB-scaled plot, this is simply the geometrical distance as shown in figure 2.3.

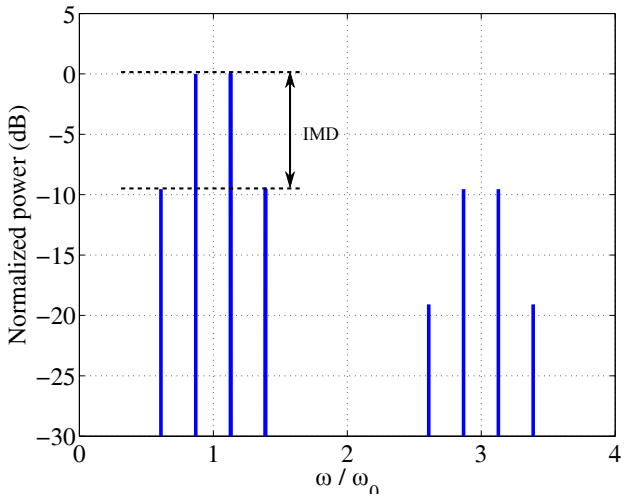


Figure 2.3: Inter-modulation distance in the two-tone experiment

In the two-tone experiment, the IMD can be calculated from IP3 and output power (in dB) as

$$IMD = 2(OIP3 - P_{\text{out}}). \tag{2.11}$$

The shoulder distance is a similar measure for band-pass signals. In a dB-scaled plot, it is the distance between the fundamental signal and the "shoulder" of the nonlinear products. Unlike the IMD, the shoulder distance cannot be easily predicted from the IP3.

2.5 Band-Pass Signals

The L-DACS1 transmission system uses a narrow pass-band signal – a case that is not modeled properly in the two-tone experiment.

The band-pass signal $x(t)$ is set to have a rectangular spectrum of bandwidth B_0 centered at ω_0. The real signal $x(t)$ can be described using a complex, band-limited to $\left[-\frac{B_0}{2}, \frac{B_0}{2}\right]$ baseband signal $x_\mathrm{b}(t)$ as

$$x(t) = \mathrm{Re}\left\{2x_\mathrm{b}(t)e^{j\omega_0 t}\right\} = x_\mathrm{b}(t)e^{j\omega_0 t} + \overline{x_\mathrm{b}}(t)e^{-j\omega_0 t} \tag{2.12}$$

with the factor 2 added without loss of generality to simplify the formulas. The notation $\overline{x_\mathrm{b}}(\,)$ denotes the complex conjugate of $x_\mathrm{b}(\,)$.

Using the binomial theorem, for integer powers l, $x(t)^l$ can be calculated as

$$x(t)^l = \sum_{k=0}^{l} \binom{l}{k} x_\mathrm{b}(t)^{l-k}\overline{x_\mathrm{b}}(t)^k e^{j\omega_0 t(l-2k)}. \tag{2.13}$$

With a continuous spectrum, each convolution involves actual integration and changes in the shape of the spectrum. The first convolution (corresponding to a second-order nonlinearity) yields a triangular shape and further convolutions grind down the slopes more and more broadening the spectrum.

Considering harmonics up to the 5$^{\mathrm{th}}$ order we obtain the spectrum shown in figure 2.4.

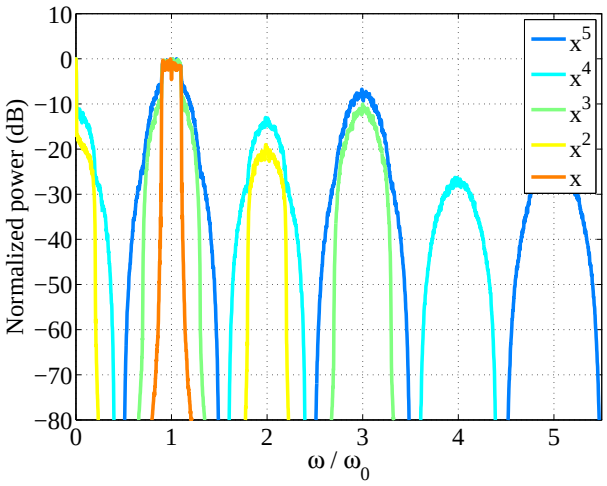


Figure 2.4: Spectra of the harmonic components of a band-pass signal distorted by a 5$^{\mathrm{th}}$-order nonlinearity

The important properties are:

- The originally rectangular spectrum of the signal becomes rounded as the order of the harmonic increases. Each convolution applied to the spectrum decreases the slope of the edges and increases the width of the base. An N^{th}-order harmonic has a bandwidth of NB_0.
- The even-order components (right column in figure 2.4) generate the frequencies 0 (DC), $2f_0$, $4f_0$ etc. They do not interfere with the fundamental signal at f_0. As

there is a large gap between f_0 and the first harmonic component ($B_0 \ll f_0$!), they can be filtered out after the amplifier relatively easily.

- The odd-order components generate the frequencies f_0, $3f_0$, $5f_0$ etc. They directly overlap the fundamental signal at f_0 and cannot be filtered out. Also, the broadening of the spectrum cannot be compensated by using a narrow filter as f_0 may not be fixed to a particular frequency but can be any value in a frequency band that is significantly wider than B_0. The odd-order components have to be reduced by making the amplifier itself as linear as possible.

Comparing the output spectrum with the spectral mask makes the intention of its designer clear: To allow for third-order distortion but not for fifth and above (fig. 2.5).

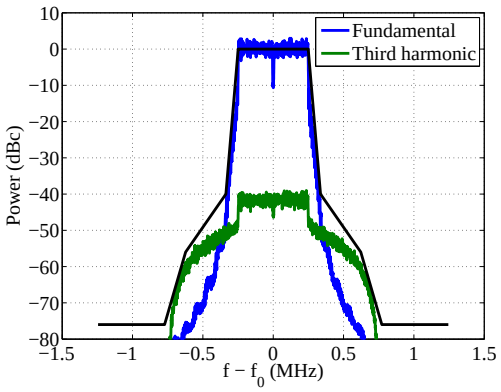


Figure 2.5: Third-order harmonics fitting into the spectral mask

2.6 Equivalent Complex Baseband

For the realization of a digital pre-distortion (DPD) system (chapter 3), it is not possible or even necessary to consider the full bandwidth of the signal including all harmonics (multiples of f_0, i.e. a sample rate of many GHz). The output of the system is usually, and specifically in the case of L-DACS1, filtered by a high-order band-pass. This filter removes the harmonics that do not fall onto the fundamental frequency f_0 and, therefore, these can then be disregarded also for the purpose of the DPD [6, sec. 2.1.1].

A band-pass signal that is strictly band-limited to NB_0, with N being the order of the nonlinearity and B_0 the fundamental signal bandwidth, remains.

Revisiting equation 2.13,

$$x(t)^l = \sum_{k=0}^{l} \binom{l}{k} x_\mathrm{b}(t)^{l-k} \overline{x_\mathrm{b}}(t)^k e^{j\omega_0 t(l-2k)},$$

applying a pass-band filter at ω_0 means that only the terms with $l - 2k = \pm 1$ or equivalently $k = \frac{l \mp 1}{2}$ survive. For an even l this is no term at all, for an odd l two terms

remain:

$$\mathrm{BP}\left\{x(t)^l\right\} = \binom{l}{\frac{l-1}{2}} x_\mathrm{b}(t)^{\frac{l+1}{2}} \overline{x_\mathrm{b}}(t)^{\frac{l-1}{2}} e^{j\omega_0 t} + \binom{l}{\frac{l+1}{2}} x_\mathrm{b}(t)^{\frac{l-1}{2}} \overline{x_\mathrm{b}}(t)^{\frac{l+1}{2}} e^{-j\omega_0 t}. \tag{2.14}$$

Now the signal is mixed down to baseband by multiplying with $e^{-j\omega_0 t}$,

$$\mathrm{BB}_1\left\{x(t)^l\right\} = \binom{l}{\frac{l-1}{2}} x_\mathrm{b}(t)^{\frac{l+1}{2}} \overline{x_\mathrm{b}}(t)^{\frac{l-1}{2}} + \binom{l}{\frac{l+1}{2}} x_\mathrm{b}(t)^{\frac{l-1}{2}} \overline{x_\mathrm{b}}(t)^{\frac{l+1}{2}} e^{-j2\omega_0 t}. \tag{2.15}$$

A digital low pass filter removes the component at $2\omega_0$, finally yielding, for odd l

$$\mathrm{BB}_2\left\{x(t)^l\right\} = \binom{l}{\frac{l-1}{2}} x_\mathrm{b}(t)^{\frac{l+1}{2}} \overline{x_\mathrm{b}}(t)^{\frac{l-1}{2}}, \tag{2.16}$$

or, for more clarity with $l = 2m+1$, $m \in \mathbb{N}$,

$$\mathrm{BB}_2\left\{x(t)^{2m+1}\right\} = \binom{2m+1}{m} x_\mathrm{b}(t)^{m+1} \overline{x_\mathrm{b}}(t)^m. \tag{2.17}$$

Each of the m $x(t)\overline{x_\mathrm{b}}(t)$ pairs can be written as $|x_\mathrm{b}(t)|^2$,

$$\mathrm{BB}_2\left\{x(t)^{2m+1}\right\} = \binom{2m+1}{m} x_\mathrm{b}(t)|x_\mathrm{b}(t)|^{2m}. \tag{2.18}$$

The overall *equivalent complex baseband* output signal is

$$y_\mathrm{b}(t) = x_\mathrm{b}(t) \sum_{m=0}^{\lfloor\frac{N-1}{2}\rfloor} a_{2m+1} \binom{2m+1}{m} |x_\mathrm{b}(t)|^{2m} = x_\mathrm{b}(t) g\left(|x_\mathrm{b}(t)|\right). \tag{2.19}$$

Actual processing and modeling takes place in the digital domain (chapter 3), that is, the signals are discrete in time and value. The value discretization is neglected here, i.e., the signal is assumed to be sampled at high resolution. As the signal is strictly band-limited it can be reconstructed without information loss if the sample-rate is chosen high enough. We obtain (dropping the "b" index),

$$y[n] = x[n] g\left(|x[n]|\right). \tag{2.20}$$

The power series model limits $g(\,)$ to be real. Actual power amplifiers additionally show an amplitude-dependent phase shift that cannot be modeled by the simple power series. This limitation is lifted by allowing $g(\,)$ to take any complex value.

$g\left(|x[n]|\right)$ can then be interpreted as a complex gain factor that only depends on the amplitude of input signal. This must be the case as the reduction to odd-order powers force the transfer function to be symmetric with respect to the origin. The interpretation as a complex gain factor leads to two classical distortion measures described in the next section.

2.7 AM-AM and AM-PM Distortion

AM-AM (amplitude-amplitude) and AM-PM (amplitude-phase) distortion are common measures to characterize a nonlinear device without memory. The complex gain factor $g(|x[n]|)$ only depends on the amplitude of the input signal, coining the "AM-" part of AM-AM or AM-PM. Splitting g into magnitude and phase gives the two measures.

With respect to equation 2.20, AM-AM is defined as [7]

$$amam(|x[n]|) = |y[n]| = |x[n]||g(|x[n]|)|, \tag{2.21}$$

output amplitude over input amplitude. Using $x[n]$ instead of $|x[n]|$ as the argument allows the function to be used directly as a transfer function,

$$amam(x[n]) = x[n]|g(|x[n]|)|. \tag{2.22}$$

AM-PM is defined as

$$ampm(|x[n]|) = \arg(y[n]) - \arg(x[n]) = \arg(g(|x[n]|)), \tag{2.23}$$

an amplitude-dependent phase shift.

Equation 2.20 can be written equivalently using the AM-AM / AM-PM pair,

$$amam(x[n])e^{jampm(|x[n]|)} = x[n]|g(|x[n]|)|e^{j\arg(g(|x[n]|))} = x[n]g(|x[n]|) = y[n], \tag{2.24}$$

which will be used in the next chapter.

3 Digital Predistortion (DPD)

The very stringent spectral mask of L-DACS1 can only be fulfilled with signal processing external to the amplifier. The state-of-the art method is to preprocess the signal in the digital domain – digital predistortion (DPD). DPD adds considerable complexity to the system, as it requires an additional receiver for the loop-back path and additional base-band processing.

The static memory-less nonlinear model extended by a phase shift (sec. 2.1) is used for modeling the power amplifier. This simple model makes system identification quite easy. The actual pre-distortion can be implemented in an efficient manner in a field-programmable gate array (FPGA), as detailed in section 3.5.

3.1 Principle of Operation

DPD compensates the effect of the nonlinearity in advance. It operates in the equivalent complex baseband domain as defined in section 2.6 and uses the AM-AM / AM-PM pair to model the nonlinearity (sec. 2.7). Figure 3.1 visualizes the process of compensating the AM-AM distortion, using the normalized AM-AM function $amam_{\mathrm{n}}(\,)$ to be defined in a moment (equ. 3.4).

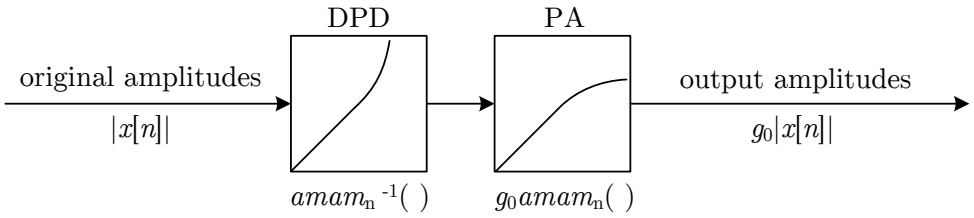


Figure 3.1: Compensation of AM-AM distortion

Revisiting equation 2.20,

$$y[n] = x[n]g\left(|x[n]|\right),$$

it is seen that the model includes the amplifier gain in $g(\,)$. With g_0 as the gain and $g_{\mathrm{n}}(\,)$ the remaining normalized distortions, $g(\,)$ can be split according to

$$g\left(|x[n]|\right) = g_0 g_{\mathrm{n}}(|x[n]|). \tag{3.1}$$

With P_x and P_y the powers of $x[n]$ and $y[n]$, respectively,

$$g_0^2 = \frac{P_y}{P_x}. \tag{3.2}$$

As the gain is irrelevant for the DPD, it can be removed,

$$y_{\mathrm{n}}[n] = \frac{y[n]}{g_0} = x[n] g_{\mathrm{n}}(|x[n]|), \tag{3.3}$$

normalizing the AM-AM function (equ. 2.22) to

$$\begin{aligned} amam(|x[n]|) &= |x[n]|\,|g\,(|x[n]|)\,| = g_0\,|x[n]|\,|g_{\mathrm{n}}(|x[n]|)| \\ &=: g_0 amam_{\mathrm{n}}(|x[n]|). \end{aligned} \tag{3.4}$$

The inverse, $amam_{\mathrm{n}}^{-1}(\,)$, assuming that it exists,[1] compensates for the effect of AM-AM distortion, in the sense that

$$amam\left(amam_{\mathrm{n}}^{-1}(|x[n]|)\right) = g_0 amam_{\mathrm{n}}\left(amam_{\mathrm{n}}^{-1}(|x[n]|)\right) = g_0\,|x[n]|\,. \tag{3.5}$$

Peak amplitudes are typically compressed by the power amplifier and have to be expanded by the DPD. This causes an even higher PAPR at the power amplifier input and all previous stages. As the expanded peaks will be compressed even more, DPD causes a slight gain reduction.

To additionally compensate for AM-PM distortion, the inverse of $ampm(\,)$ is not needed. The original phase can be restored by simply adding the expected phase distortion in advance.

Both $amam_{\mathrm{n}}^{-1}(\,)$and $ampm(\,)$ can be estimated from the known original signal $x[n]$ and a recording of the distorted signal after the amplifier $y_{\mathrm{n}}[n]$. In the test setup, the estimation is done in Matlab code as shown in figure 3.2.

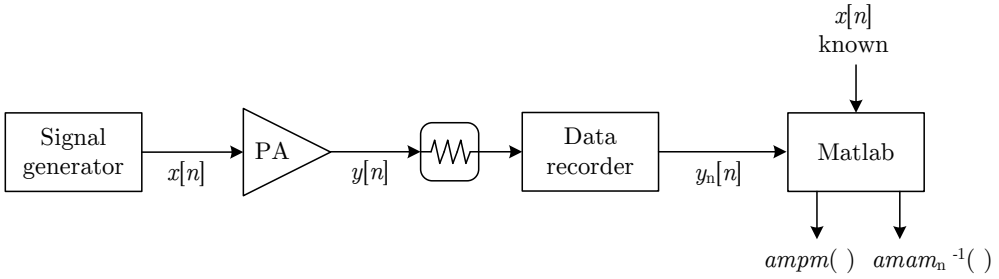


Figure 3.2: Model estimation

The actual implementation involves additional steps that are detailed in the following sections:

1. Time-alignment of the recorded $y[n]$ with the known $x[n]$ (section 3.2)
2. Estimating the (inverse) model parameters (section 3.3)
3. Applying the inverse model onto the signal $x[n]$ (sections 3.4 and 3.5)

[1] The inverse exists if the AM-AM function is strictly monotonic. This will be verified by measurements in chapters 8 and 9.

3.2 Time-Alignment

While the sample rate of signal generator and data recorder can be easily synchronized by using a shared reference frequency – here, 10 MHz – the start of a recording can only be coarsely synchronized with the start of playback by using a trigger. Coarsely means that recording and playback are a few samples off. For the purpose of the DPD, $x[n]$ and $y[n]$ need to be aligned very accurately down to sub-sample precision to allow for an accurate estimation of AM-AM and AM-PM.

The problem is attacked by assuming $x[n]$ and $y[n]$ to be of length L and be identical up to a cyclic time delay of d samples. This approach ignores the distortion introduced by the amplifier but has proven to give good results for the amplifiers used. Input and output are

$$\begin{aligned} y[n] &= x[(n-d) \mod L] \\ &\xrightarrow{\text{FFT}} \\ Y[n] &= X[n]e^{-\frac{j2\pi nd}{L}}. \end{aligned} \tag{3.6}$$

The frequency-domain time delay transfer function H_d can be found by dividing X and Y,

$$H_\mathrm{d}[n] = e^{-\frac{j2\pi nd}{L}} = \frac{Y[n]}{X[n]}, \tag{3.7}$$

with exemplary results from the power amplifier (to be presented in chapter 8) shown in figure 3.3. Ideally, the magnitude of this function is constant one and the phase has a

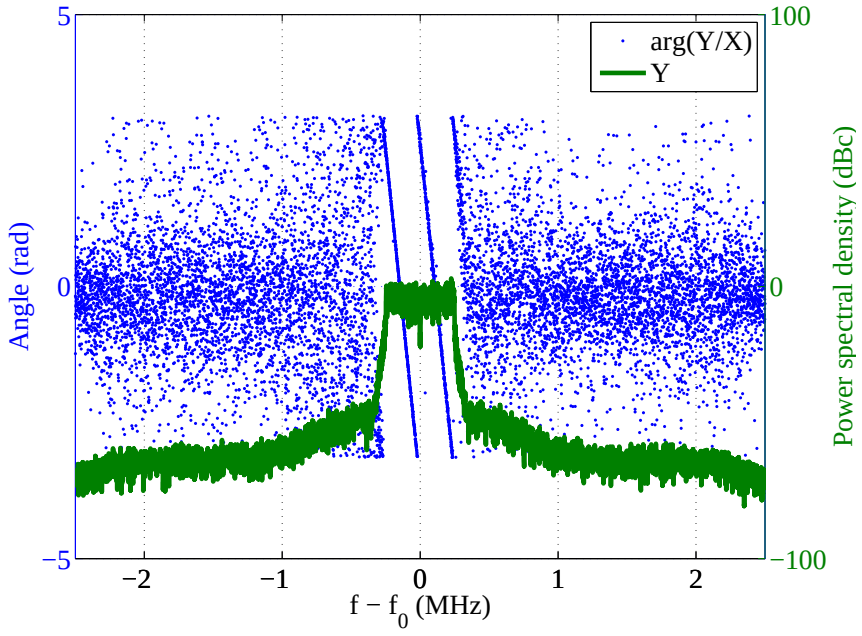


Figure 3.3: Phase versus signal power

constant slope proportional to d.

However, values outside the signal bandwidth are useless because the SNR is too low to extract phase information. Useful data is available only within the signal bandwidth.

To get the slope, first, the gradient is calculated. Remaining 2π jumps are removed using a simple unwrapping algorithm: With u_n and p_n the original and unwrapped phase gradient, respectively,

$$u_n = \begin{cases} p_n & , |p_n| \leq \pi \\ p_n + 2\pi & , p_n < \pi \\ p_n - 2\pi & , p_n > \pi. \end{cases} \tag{3.8}$$

The difference to Matlab's `unwrap( )` function is that `unwrap( )` effectively applies each addition of $\pm 2\pi$ cumulatively to all following points.

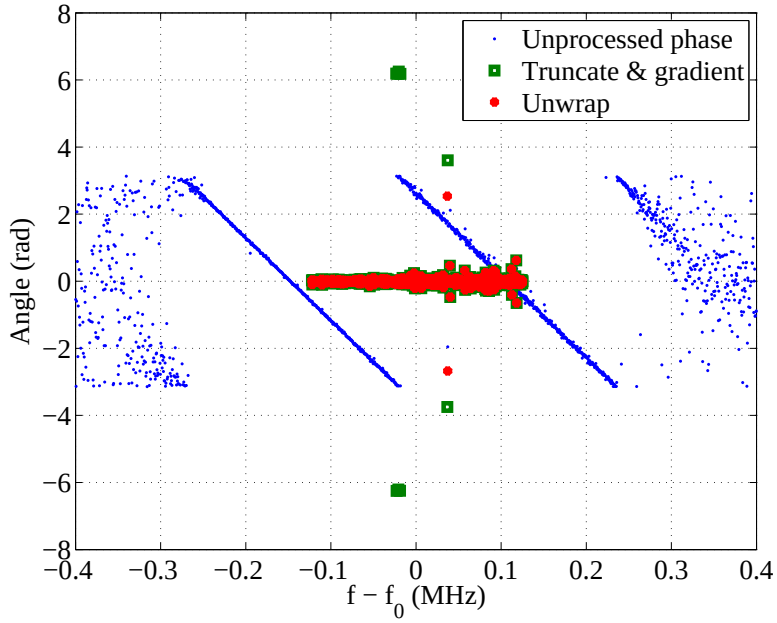


Figure 3.4: Steps in processing the phase

Figure 3.4 shows the steps of truncation to the high-SNR region, calculation of the gradient and the removal of steps in the gradient (unwrapping).

The delay in samples can now be calculated using the mean of the unwrapped phase gradient u_n. With $\bar{u}$ denoting the mean value of u_n and L the original (not truncated) signal length,

$$d = \frac{\bar{u}}{2\pi L}. \tag{3.9}$$

The delay is compensated in the frequency domain using a time advance element,

$$H_\mathrm{a}[n] = \frac{1}{H_\mathrm{d}[n]} = e^{+\frac{j2\pi nd}{L}} \tag{3.10}$$

and the time-aligned $\tilde{Y}$ is obtained from

$$\tilde{Y}[n] = Y[n]H_{\mathrm{a}}[n] = X[n]e^{-\frac{j2\pi nd}{L}}e^{+\frac{j2\pi nd}{L}} = X[n]. \tag{3.11}$$

In a real DPD system, the assumption that $y[n]$ is a cyclically-shifted version of $x[n]$ (3.6) does not hold as $x[n]$ and $y[n]$ are overlapping but different segments of a non-repetitive fundamental signal (figure 3.5, the black bars symbolize the L-DACS1 frame structure). The cyclic shift applied by $H_{\mathrm{a}}[n]$ leads to different signals at the start (or end, if d is negative) of $x[n]$ and $\tilde{y}[n]$. A practical solution is to chop off at least d samples from the *start* of both processed signals. If d is negative, the samples have to be removed from the *end* of the signals instead.

However, this also means that the estimation of d is partly based on "garbage" data. As the time shifts that are practically seen in the test setup are very small compared to the recorded signal length and will be even lower when implemented in the FPGA (sec. 3.5), the introduced uncertainty is considered negligible.

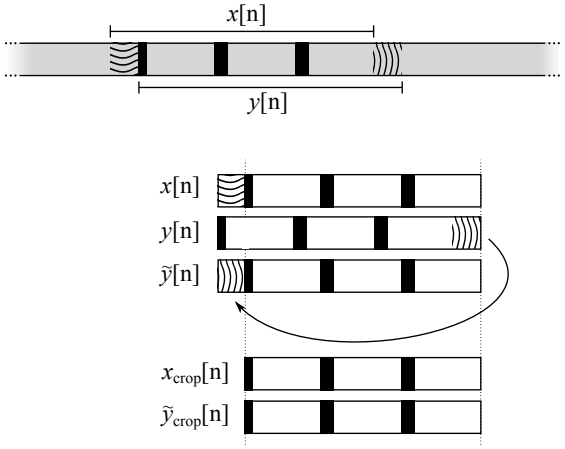


Figure 3.5: Time aligning overlapping but different segments

3.3 Parameter Estimation

Now, $x[n]$ and $y[n]$ are the time-aligned and truncated original and distorted signal as shown in figure 3.2. Their values are copied into the $L \times 1$ vectors $\underline{x}$ and $\underline{y}$. Additionally, both signal powers are normalized to 1. Disregarding the power change from the nonlinear distortion, this is equivalent to normalizing a_1 in equation 2.19 to 1 and scaling the other coefficients accordingly. This normalization removes the linear gain of the amplifier and does not influence the output spectrum and is, therefore, without loss of generality for the purpose of the DPD.

Plotting $|\underline{y}|$ over $|\underline{x}|$ (equation 2.23) gives the AM-AM characteristic ("Recorded data" in figure 3.6). At high power levels, compression is visible. For low power levels, the points spread out as the SNR decreases. The point cloud is fitted by a polynomial

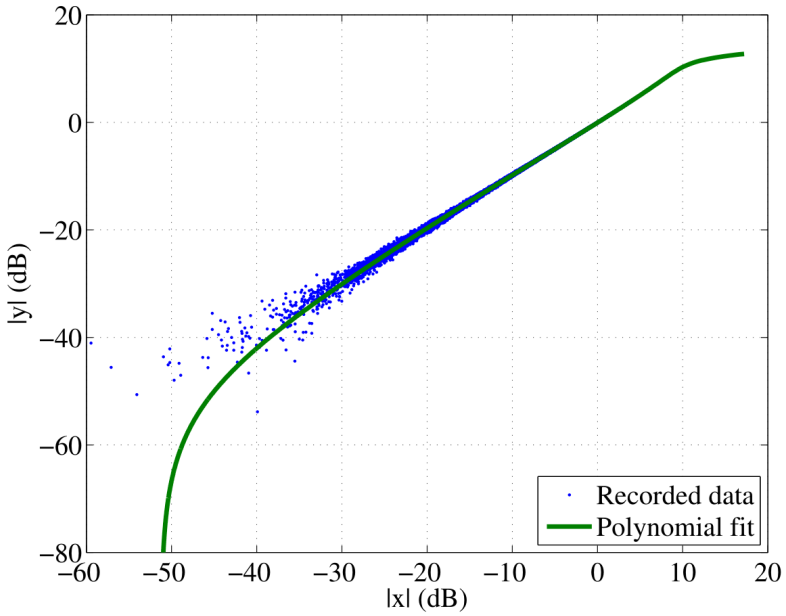


Figure 3.6: AM-AM distortion

using Matlab's `polyfit( )` function. With $\underline{y} = f(\underline{x})$, `polyfit`$(\underline{x}, \underline{y}, n)$ returns polynomial coefficients of degree n that approximate $f(\,)$ in a least-squares sense. Reversing $\underline{x}$ and $\underline{y}$ as in `polyfit`$(\underline{y}, \underline{x}, n)$ returns coefficients for $f^{-1}(y)$. In this case the function of interest is $amam_{\mathrm{n}}{}^{-1}(|y|)$,

$$\underline{c}_{amam^{-1}} = \texttt{polyfit}(|\underline{y}|, |\underline{x}|, n). \tag{3.12}$$

The resulting polynomial with coefficients $\underline{c}_{amam^{-1}}$ is shown in figure 3.6 for $n = 8$, which has proven to give good results. The fit is poor below $-40\,\mathrm{dB}$. This is, however, insignificant as few points are affected that each carry a very low power.

AM-PM is visualized by plotting $\Delta\rho = \mathrm{mod}(\arg(\underline{\mathrm{x}}) - \arg(\underline{\mathrm{y}}), 2\pi)$ over $|x|$. Using Matlab's `polyfit( )` function for fitting this curve is found to be insufficient as it produces a poor match for high amplitudes. This is because these peak values occur very rarely and carry the strongest phase shift. However, because these points carry a high power, they have a big impact on the spectrum and a good match is absolutely needed. The solution is to to use a weighted least-squares fit (fig. 3.7).

The classical linear regression problem, with the $L \times 1$ "y data" vector $\underline{b}$, the $1 \times N$ coefficient vector $\underline{c}$ and the $L \times N$ design matrix A is

$$A\underline{c} = \underline{b}. \tag{3.13}$$

For a polynomial regression of degree n, A is set to

$$A = \begin{pmatrix} \underline{1} & \underline{a} & \underline{a}^2 & \underline{a}^3 & \underline{a}^4 & \cdots & \underline{a}^n \end{pmatrix}, \tag{3.14}$$

with $\underline{a}$ denoting the "x data" vector. of If $\underline{b}$ is longer than $\underline{c}$, which is the case for the DPD ($L \gg N$), the system is overdetermined and can be solved in the sense of least

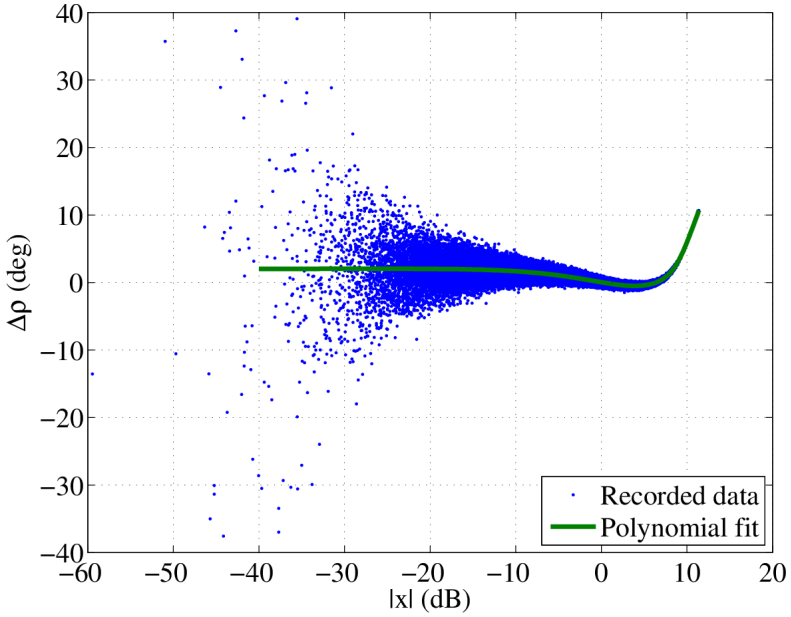


Figure 3.7: AM-PM distortion

square error using the pseudoinverse[2] A^+ of A,

$$\underline{c} = A^+ \underline{b}. \tag{3.15}$$

The weighted version of the problem is created by multiplying both sides by the diagonal $L \times L$ weighting matrix W,

$$WA\underline{c} = W\underline{b} \tag{3.16}$$

and the least-squares solution is

$$\underline{c} = (WA)^+ (W\underline{b}). \tag{3.17}$$

Some care must be taken when implementing this, as L is very large ($L \approx 300.000$). A fully-populated W consumes over 700 gigabytes ($2 \cdot 4 \cdot L^2$ bytes) of memory. One option in Matlab is to use the `spdiags( )` function to create W as a sparse matrix. Another equivalent approach is using the $L \times 1$ weighting vector $\underline{w}$ and using the element-wise matrix product (Hadamard product)[3] "$\circ$",

$$A_w \underline{c} = \underline{b}_w, \tag{3.18}$$

with

$$A = \left(\begin{array}{cccccc} \underline{1} & \underline{a} \circ \underline{w} & \underline{a}^2 \circ \underline{w} & \underline{a}^3 \circ \underline{w} & \cdots & \underline{a}^n \circ \underline{w} \end{array} \right), \tag{3.19}$$

[2] An efficient implementation in Matlab would use the backslash operator, $\underline{c} = A \backslash \underline{b}$.
[3] In Matlab, this operator is written as ".*"

$$\underline{b}_w = \underline{b} \circ \underline{w}. \tag{3.20}$$

As experiments show, a good choice of $\underline{w}$ with regard to a good fit at the rare maximum amplitudes is the absolute value of x,

$$\underline{w} = |\underline{x}|, \tag{3.21}$$

with $\underline{x}$ containing the L values of $x[k]$ written in a $L \times 1$ vector. As the purpose is to fit $\Delta\rho$ over $|x|$,

$$\underline{a} = |\underline{x}|, \tag{3.22}$$

$$\underline{b} = \Delta\rho, \tag{3.23}$$

$$\underline{c}_{ampm} = A_w^+ \underline{b}_w. \tag{3.24}$$

A resulting fit is shown in figure 3.7, the good quality (judging visually) of the fit is confirmed by spectral measurements.

3.4 Applying the Correction

With the coefficients vectors $\underline{c}_{ampm}$ and $\underline{c}_{amam^{-1}}$, the pre-distorted signal can be generated. To evaluate the polynomial defined by the coefficients $\underline{c}$ at points in vector $\underline{x}$, the Matlab function polyval($\underline{c}, \underline{x}$) is used.

The AM-AM correction has to be applied first, as the AM-PM correction has to take into account the corrected (higher) amplitudes. The AM-AM corrected $|x'[n]|$ is calculated by evaluating the polynomial defined by the coefficients $\underline{c}_{amam^{-1}}$ at $|x[n]|$. Using Matlab's `polyval( )` function,

$$|x'[n]| = \texttt{polyval}(\underline{c}_{amam^{-1}}, |x[n]|). \tag{3.25}$$

The lost phase information is applied together with the AM-PM correction $\Delta\rho[n]$:

$$\Delta\rho[n] = \texttt{polyval}(\underline{c}_{ampm}, |x[n]|) \tag{3.26}$$

$$x''[n] = x'[n] e^{j(\Delta\rho[n] + \arg(x[n]))}. \tag{3.27}$$

Now, $x''[n]$ can be sent to the amplifier and should result in an output identical to a scaled version of the original signal $x[n]$. Actual output spectra are presented in chapter 10.

3.5 Limited-Precision Implementation

The DPD performed in the course of this thesis is an offline (non-real-time) implementation. In the final transmitter system (including the FPGA board from Frequentis AG), the pre-distortion has to be applied to the input signal in real time. The task is split into two parts:

1. Applying the inverse model onto the data. This is done in real-time in the baseband processing unit provided by Frequentis in an FPGA.
2. Estimating the inverse model and calculating look-up tables. This is done periodically every few seconds in a controller PC that is external to the transmitter unit.

Selection and simulation of the FPGA algorithm is also in the scope of the thesis, while the implementation in VHDL is not. A simulation of both (1) and (2) written in Matlab exists and works.

The key difference between a Matlab implementation and the FPGA setup is the used data type. Matlab by default uses 64 bit double precision floating point numbers, while the FPGA will use, in accordance to the resolution of DAC and ADC, 16 bit integers.

To provide the real-time capability and to avoid the use of floating point math, look-up tables (LUTs) are used instead of direct evaluation of the polynomials. As the tables contain fewer entries than possible amplitude values, linear interpolation is used. Equivalently, this is a piecewise-linear approximation of the polynomials. The look-up tables are computed on the controller PC using floating point math.

The overall FPGA algorithm flow is shown in figure 3.8. It only requires two polar↔Cartesian conversions and two staged table lookups[4] with interpolation[5].

The bit width of the table indices determines the number of supporting points for the piecewise linear approximation. The necessary width is determined experimentally using the power amplifier that will be covered in detail in chapter 8. Figure 3.9 shows the spectrum of the digital data that is to be sent to the power amplifier using a range of index widths for the integer implementation and the implementation using double variables as reference. For index widths of 6 bits and above, the difference to the implementation with double precision numbers can be considered negligible. The only significant deviation happens below $-80\,\mathrm{dBc}$, which is already below the spectral mask and therefore insignificant. For comparison, also the spectrum of the original signal (without DPD) is shown. The DPD causes the spectrum of the *input signal* to the power amplifier to broaden. Actually, the spectrum of the baseband signal with DPD applied looks very similar to the spectrum of the power amplifier output signal without DPD (chap. 10).

After discussion with Frequentis, it is decided to use a 10 bit index, as the resulting look-up table fits exactly into one RAM page of 4 KB. All spectra presented in chapter 10 use the algorithm presented above with 10 bit look-up tables implemented in Matlab. The output spectrum is verified to be identical to the implementation using double variables.

[4] AM-AM and AM-PM table could be merged into a single table, which would save one lookup and result in a shorter pipeline. The advantage of having two separate tables is easier calculation of the tables and an algorithm that is essentially identical to the Matlab double implementation, which makes verification of the correctness easier.

[5] There is also the explicit addition shown in figure 3.8. As the interpolations already implicitly contain several additions and multiplications it is omitted here.

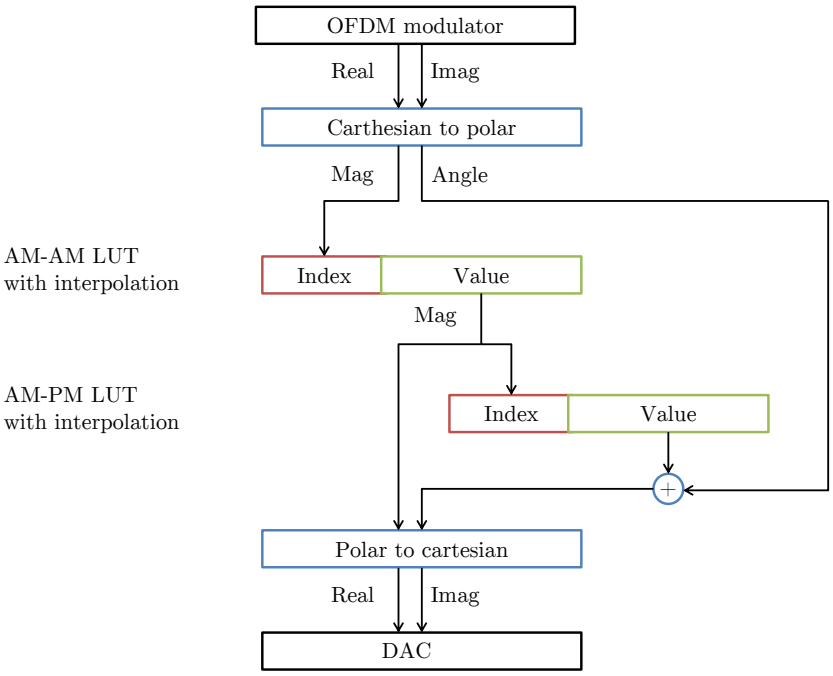


Figure 3.8: FPGA algorithm

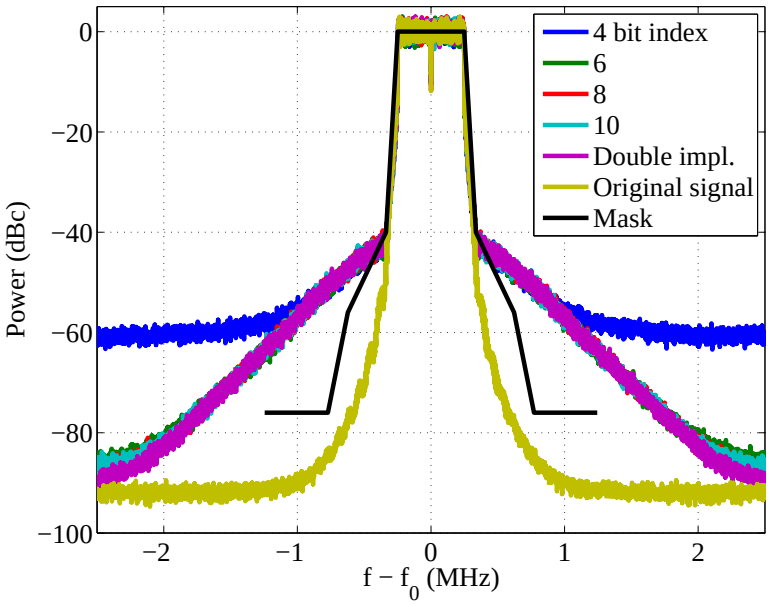


Figure 3.9: Spectrum of the baseband signal with DPD applied for a range of index widths

4 Signal Generation and Spectrum Measurement

The spectral mask required by the L-DACS1 specification is challenging not only in terms of building a power amplifier that can fulfill it. Just generating and measuring the signal with the required dynamic range is not easily done, even with state-of-the art signal generators and spectrum analyzers.

4.1 Comparison of Spectrum Analyzers

Two spectrum analyzers are permanently available at the lab:

1. Agilent E4446A PSA Series Spectrum Analyzer
2. Rohde & Schwarz FSEK 30 Spectrum Analyzer

As per the L-DACS1 specifications, the spectra are measured with a resolution bandwidth (RBW) of 10 kHz and a video bandwidth of 30 kHz. To get a stable reading, averaging is used, where care is taken that it is always in RMS mode to get realistic values. The attenuator is manually set to examine the effect on linearity and noise floor.

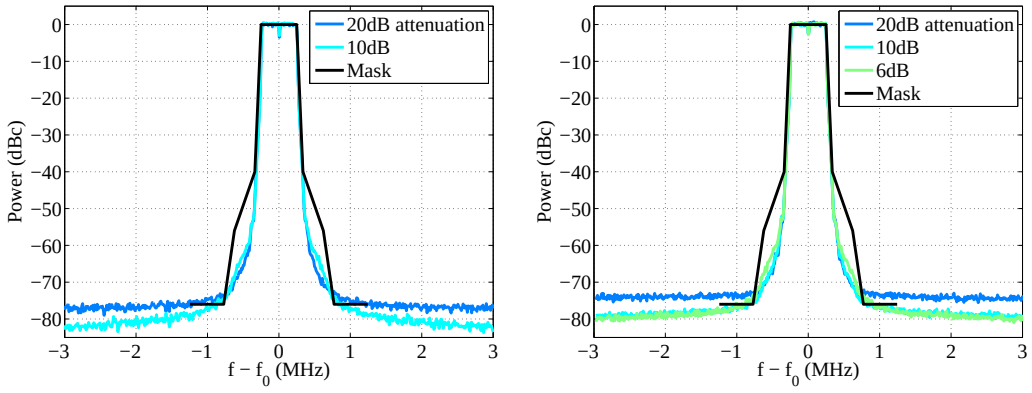
Directly connecting a Rohde & Schwarz (R&S) SMBV100A signal generator to both spectrum analyzers gives the spectra shown in figure 4.1. The center frequency is set to 1 GHz and the output power of the generator is 0 dBm.

For the FSEK, the attenuator can be set in 10 dB steps, where 10 dB is the lowest setting that does not give an overload warning. The PSA attenuator can be set in 2 dB steps where 6 dB was the lowest setting without an overload warning. Both spectrum analyzers show third-order inter-modulation for the lowest attenuation settings. For both analyzers, the best compromise between linearity and noise floor is obtained at 10 dB attenuation. Comparing the two (fig. 4.2) shows that the FSEK has a lower noise floor while the PSA shows better linearity. The PSA is chosen as the main tool for spectral measurements for several reasons:

1. Better linearity
2. Easy export of trace data (CSV files that can be transferred by FTP)
3. Integrated data recording functionality (used for the digital pre-distortion)

4.2 Comparison of Signal Generators

The Rohde & Schwarz SMBV100A is the only signal generator permanently available for the lab testing. While it offers good-quality signal generation and a respectable set



(a) R&S FSEK spectrum analyzer

(b) Agilent PSA spectrum analyzer

Figure 4.1: Spectrum of the signal from the SMBV signal generator for FSEK and PSA, various attenuator settings

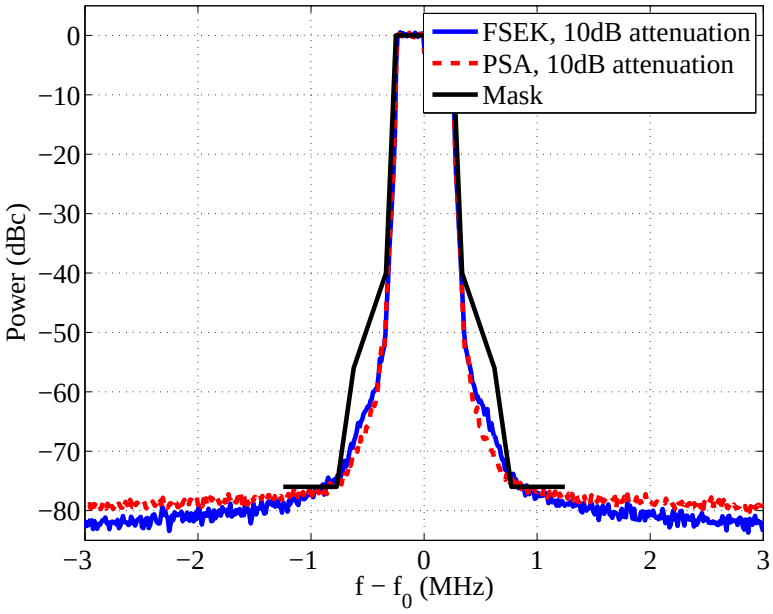


Figure 4.2: Best spectrum for both analyzers compared

of features, the SMBV series is the compact line of signal generators from R&S. For comparison purposes, R&S' flagship signal generator, the SMU, and Agilent's flagship generator, the MXG, are temporarily obtained. Additionally, Agilent's top-of-the-line spectrum analyzer, the Agilent N9030A PXA Signal Analyzer (successor of the PSA series) is obtained for this test. The results, again for a resolution bandwidth of 10 kHz and equal output powers for both signal generators, are shown in figure 4.3.

While the difference in the spectra between SMBV and SMU are of quantitative nature,

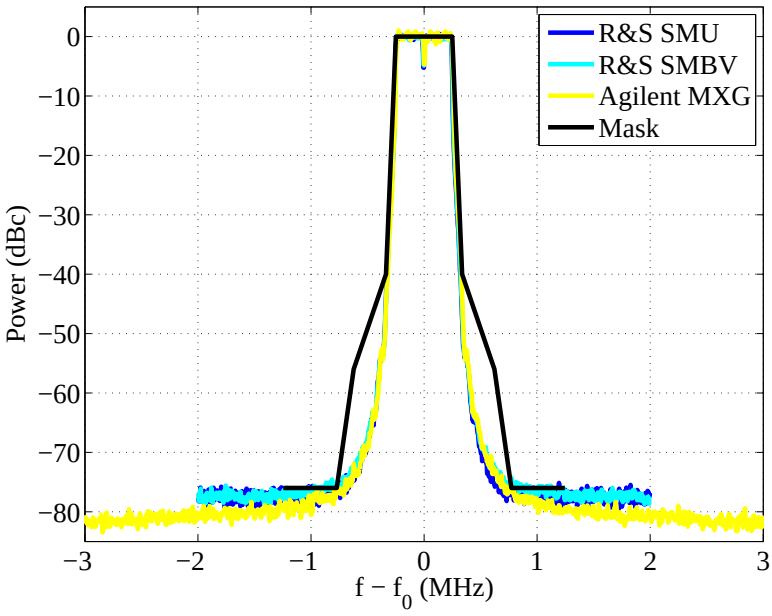


Figure 4.3: Comparison of SMBV and SMU signal generators at the PXA spectrum analyzer

the MXG shows several dB of improvement starting at 1 MHz from the center.

All the spectra touch the spectral mask at the −76 dBc edge.

4.3 Conclusion

The spectral mask is indeed at the edge of feasibility, even in terms of generating and measuring the signal. Flagship equipment from Rohde & Schwarz and Agilent lead to readings that already touch the spectral mask.

It is seen that the equipment primarily used in the laboratory testing, the Agilent PSA und the Rohde & Schwarz SMBV, do not fall significantly behind the best equipment currently available.

5 Transmitter Design

This chapter details the requirements for the transmitter and the design of the transmit chain.

5.1 System Overview

L-DACS1 specifies an output power of 42 dBm average. A system margin of 0.5 dB is included to account for losses after the amplifier, leading to a targeted output power of 42.5 dBm. The signal to transmit is OFDM with a bandwidth of 498 kHz and a PAPR of 11 dB, giving a peak output power of 53.5 dBm. The frequency bands the transmitter operates in are shown in section 5.3.

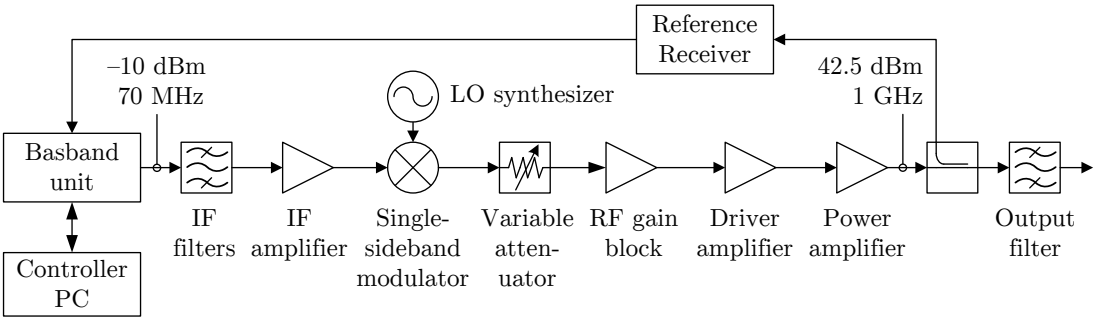


Figure 5.1: Transmitter block diagram

A block diagram of the transmitter is shown in figure 5.1. It includes the following elements:

- Baseband unit (provided by Frequentis AG, section 6.1)
- Controller PC (provided by Frequentis AG, standard rack-mount PC controlling the baseband unit)
- 70 MHz IF interface (section 5.6)
- IF filters (section 6.2)
- IF amplifier (section 6.3)
- LO synthesizer (chapter 7)
- Single-sideband modulator (section 6.4)
- RF gain blocks (section 6.5)

- Driver amplifier (chapter 9)
- Power amplifier (chapter 8)
- Reference receiver (built by Michael Zaisberger)
- Output filters (section 5.5)

The link budget for the whole path is shown in section 5.2.

5.2 Link Budget

Table 5.1 shows the link budget design of the upconversion & PA path. The row output power shows the *mean* output power after the device. At the interface from the baseband unit, 3 dBm peak power is expected (sec. 6.1). The original signal's PAPR of 11 dB is expanded by DPD to 13 dB (worst-case assumption), giving an average power of −10 dBm at the interface. The PAPR is reduced by the power amplifier back to 11 dB. As no measurements are possible between driver and power amplifier for reasons outlined in chapter 10, so neither the PAPR nor the gain is known at this point in the chain. As the power amplifier is closer to its IP3, it can be assumed to be dominant in PAPR reduction, and the PAPR after the driver amplifier can be assumed to be close to but below 13 dB. The gain of the driver amplifier plus power amplifier chain is known: 41 dB. In the table, this gain is simply split into 20.5 dB each.

The total required gain is 52.5 dB (row "Chain gain" in the table). As the L-DACS1 specification also requires the possibility for the output power to be reduced by up to 50 dB, two digital attenuators (Mini-Circuits DAT-31R5-SP) with a range of 30 dB each are included after the single-sideband modulator.

The design tries to back-off from the IP3 of the devices by at least 40 dB. This constraint is violated for the driver and the power amplifier, where there is no other option, and also the second RF gain block (discussed in section 6.5). The fixed attenuator after the IF gain block is needed to precisely adjust the input power level for the single-sideband modulator (discussed in section 6.4). Individual parts are discussed in the sections mentioned in section 5.1.

										
	Base-band unit	IF filters	IF gain block	Fixed attenua-tor	Single-sideband modula-tor	Variable attenua-tor	RF gain block	Transit losses	Driver ampli-fier	Power ampli-fier
Device	Provided by Fre-quentis	2x BPF-C70+	ADL 5535	II atten-uator	TRF 370317	2x DAT-31R5-SP	ADL 5602	Cabling	MRF6V 10010N	MRF6V 12250H
IP3 (dBm)	-	-	43.5	-	26.5	52.0	40.0	-	50.0	64.0
Gain (dB)	-	−13.0	16.0	−6.0	−1.0	−2.5	20.0	−2.0	20.5	20.5
Output power (dBm)	−10.0	−23.0	−7.0	−13.0	−14.0	−16.5	3.5	1.5	22.0	42.5
PAPR (dB)	13	13	13	13	13	13	13	13	<13	11
Chain gain (dB)	-	−13.0	3.0	−3.0	−4.0	−6.5	13.5	11.5	32.0	52.5
IP3 backoff (dB)	-	-	50.5	-	40.5	68.5	36.5	-	28.0	21.5

Table 5.1: Link budget

5.3 Frequency Bands

L-DACS1 uses 500 kHz channel spacing, which is part of the reason for the rigorous spectral mask.

Band #	Range (MHz)	Bandwidth (MHz)	Number of channels
1	**963.5-970.5**	**7**	**14**
2	985.5-1008.5	23	36
3	**1048.5-1071.5**	**23**	**36**
4	1149.5-1156.5	7	14

Table 5.2: L-DACS1 frequency bands.

Two deployment options are discussed in the L-DACS1 prototype specifications: Band 2&3 (frequency division duplex) and 1&4 (tab. 5.2). However, it was decided to order filters (sec. 5.5) for band 1&3 for this phase of the project. Because of that, development of the prototype focuses on band 1&3, marked bold in the table.

5.4 Spurious Emissions

In addition to the in-band spectral mask, the L-DACS1 specification also has strong requirements regarding spurious emissions. The spurious domain is specified to start 1245.125 kHz from the carrier frequency.

The spurious emission limit is specified as −36 dBm for the ground transmitter and −60 dBm for the airborne transmitter. As the prototype has to be able to play both roles, the −60 dBm limit is used.

The spurious emission power is measured in a bandwidth that depends on the frequency: Below 1 GHz, the measurement bandwidth is 100 kHz while it is 1 MHz above 1 GHz. For this design, the more stringent limit for the region above 1 GHz is also used for band 1 (table 5.2) even if it is fully below 1 GHz.

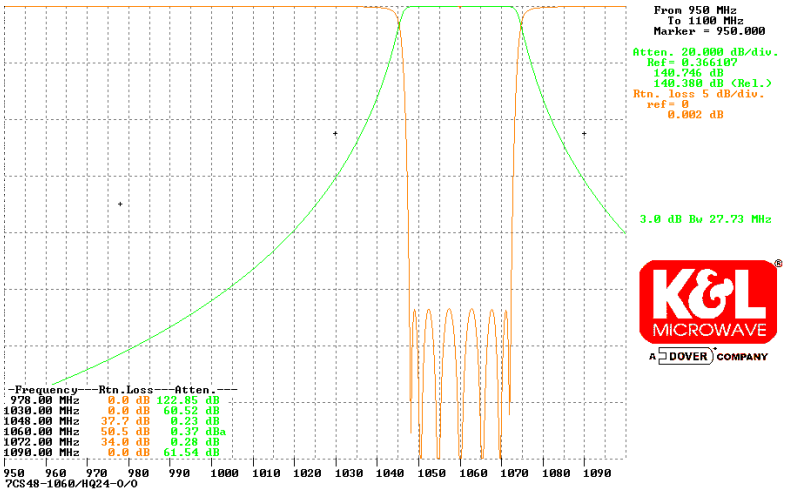
At an output power of 42.5 dBm, −60 dBm means that the other sideband and the LO has to be suppressed by at least 102.5 dB compared to the useful band.

5.5 Output Filters

The properties of the output filter that comes after the power amplifier are fully characterized by the L-DACS1 specification. It is custom-built by an external supplier, K&L filters. Only two filters (of four) are ordered for this phase of the project, covering the bands 1 and 3 (tab. 5.2). The filters are not shipped yet, though the vendor has provided frequency response simulations (fig. 5.2).

As each filter covers a whole band, it will not help in terms of achieving the spectral mask. It does help to remove spurious emissions outside the band. Unfortunately, the vendor simulations only show a frequency range of less than 200 MHz. The rejection

(a) Band 1



(b) Band 3

Figure 5.2: Output filter frequency response, vendor simulation, 20 dB/division

outside that range is assumed to be at least as high as at the edge of the shown range. For the band 3 filter, the frequency response is also assumed to be reasonably symmetric around the center frequency.

Under these assumptions, spurious products at multiples of the carrier frequency are strongly suppressed by at least 80 dB. Concerning the single-sideband upconverter, there are two spurious products that have to be taken into account: The other side-band at a distance of two time times the intermediate frequency from the carrier ($2 \cdot f_{\mathrm{IF}}$) and the local oscillator that is f_{IF} away from the carrier. As will be justified in section 6.1, 70 MHz is chosen as the intermediate frequency f_{IF}, setting LO and the other sideband at an offset of 70 MHz and 140 MHz, respectively. For band 3, both are rejected by at least 80 dB. This is also the case for band 1 if the LO is above the useful band, that is, if

a high LO is used. This is taken into account for the PLL design (chap. 7).

5.6 Intermediate Frequency

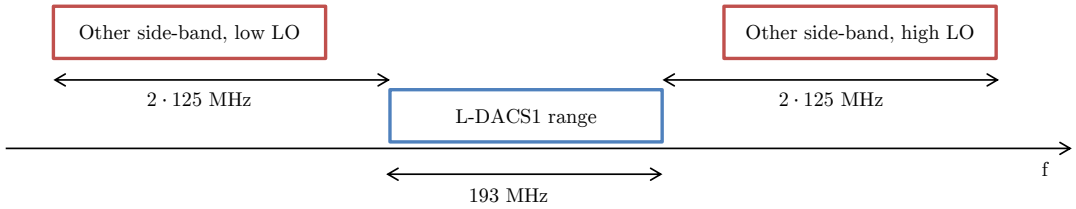
For the choice of the intermediate frequency (IF), 70 MHz and 125 MHz were evaluated.

The higher frequency of 125 MHz has the advantage of the large frequency offset of $2 \cdot 125\,\text{MHz} = 250\,\text{MHz}$ of the other side-band. The total frequency range over all bands is 193 MHz (table 5.2). As $193\,\text{MHz} < 2 \cdot 125\,\text{MHz} = 250\,\text{MHz}$, this means that the other side-band would always be located outside the L-DACS1 frequency range (fig. 5.3a). A single band-pass filter could be used to suppress the other side-band for all channels within the band. Still, the local oscillator (LO) can fall into the L-DACS1 range as $1 \cdot 125\,\text{MHz} < 193\,\text{MHz}$.

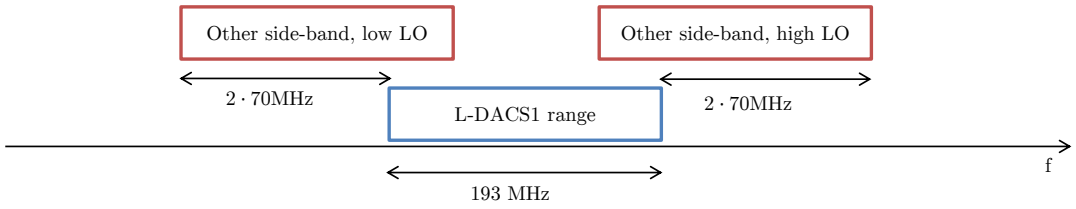
The good availability of band-pass filters and measurement equipment that accept 70 MHz IF is advantageous for this frequency. Compared to the 125 MHz IF, LO and side-band are closer to the useful band. As the side-bands are withing the L-DACS1 frequency range, a single band-pass filter cannot be used to suppress them. The LO falls into the L-DACS1 frequency range as in the case for the 125 MHz IF.

As discussed (sec. 5.5), both LO and the other side-band are suppressed by at least 80 dB by the output filters, even for the 70 MHz IF. Also considering a side-band and LO suppression provided by the mixer that should be higher than 20 dB, the spurious emission requirements are achieved.

After discussion with Frequentis, it was decided to use 70 MHz as the IF.



(a) 125 MHz IF



(b) 70 MHz IF

Figure 5.3: Location of the other side-bands (high and low) for the two IF choices

6 Quadrature upconversion

The IF signal is directly generated by a DAC at the baseband unit (digital IF). The signal is provided as is without any filtering, the anti-aliasing has to be done on the upconversion board. This chapter covers the DAC used by Frequentis, the IF filters, the single-sideband mixer, and gain stages up to (but not including) the power amplifiers.

6.1 Baseband Unit

Baseband signal generation is done in an FPGA driving a dual-channel DAC. The DAC used by the baseband is the Texas Instruments DAC5682z. Relevant features are [8]:

- Dual-channel 16 bit, 1 GSPS
- Internal 4x interpolation, selectable high-pass or low pass interpolation filter
- Internal Hilbert transform
- 0 dBm of mean output power for a 70 MHz sinus

The high available sample rate combined with internal interpolation and Hilbert transform makes it well-suited for the digital intermediate IF design. One channel is used for the IF signal and the other for the Hilbert-transformed (90° shifted) version of the IF signal to allow for single-sideband upconversion.

The sampling frequency is chosen by Frequentis to be 160 MHz. This is a somewhat unfortunate choice, as the first image frequency generated by the DAC is at $160\,\text{MHz} - 70\,\text{MHz} = 90\,\text{MHz}$, or only 20 MHz away from the 70 MHz carrier. This component is suppressed by the $\sin(x)/x$ characteristic by only 2.2 dB. This value is confirmed by a measurement conducted by Frequentis where the DAC outputs a sinus carrier at 70 MHz at the sample rate of 160 MHz (table 6.1).

Frequency (MHz)	Power (dBm)
70	0.64
90	-1.62

Table 6.1: DAC output power measurement provided by Frequentis

The 20 MHz spacing between the useful frequency and the first image is actually less than the width of band 2 and 3 which take up 23 MHz. This means that the output filter, depending on the selected channel, may not suppress this component at all! As the choice of the sampling frequency has withstood extensive discussion with Frequentis, the image frequency has to be suppressed solely by the IF filters.

As the measured power levels are average and a CW carrier has a PAPR of 3 dB, the peak output power of the DAC is over 3 dBm. With a realistic estimate for the PAPR of the L-DACS1 signal after the DPD of 13 dB, −10 dBm of mean output power for the actual signal is expected.

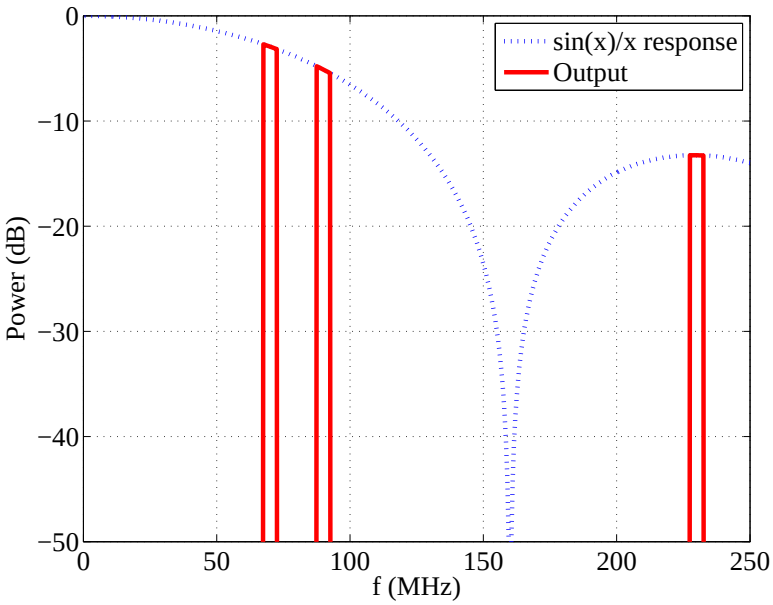


Figure 6.1: 70 MHz DAC output at 160 MHz sample rate

6.2 IF Filters

As stated in section 5.4, the targeted spurious rejection is at least 102.5 dB. Subtracting the 2.2 dB provided by the $\sin(x)/x$ characteristic at 90 MHz requires 100.3 dB of suppression from the IF image rejection filters. 70 MHz filters are available in surface-acoustic wave (SAW) and also lumped-element type.

TriQuint is, at time of this writing, one of the most popular manufacturers of SAW filters. Their filters are evaluated and are found to have a common drawback: While the filters provide very steep slopes, the out-of-band rejection is modest at about 50 dBr (relative to the pass-band loss). The pass-band loss of SAW filters is also found to be high with at least 7.5 dB. As several filters have to be used connected in series, the pass-band loss would drive the noise figure through the roof. A practical concern is that these filters need external matching.

The lumped-element Mini-Circuits BPF-C70+ is instead selected for providing modest pass-band loss of 6 dB and very high out-of-band rejection (66 dBr). The frequency response of a single filter and a two-filter series setup is shown in figure 6.2. For the two-filter setup, rejection at 90 MHz reaches 132 dBr, which exceeds the requirement. Practically, the coupling between the transmission lines leading to and from the filters

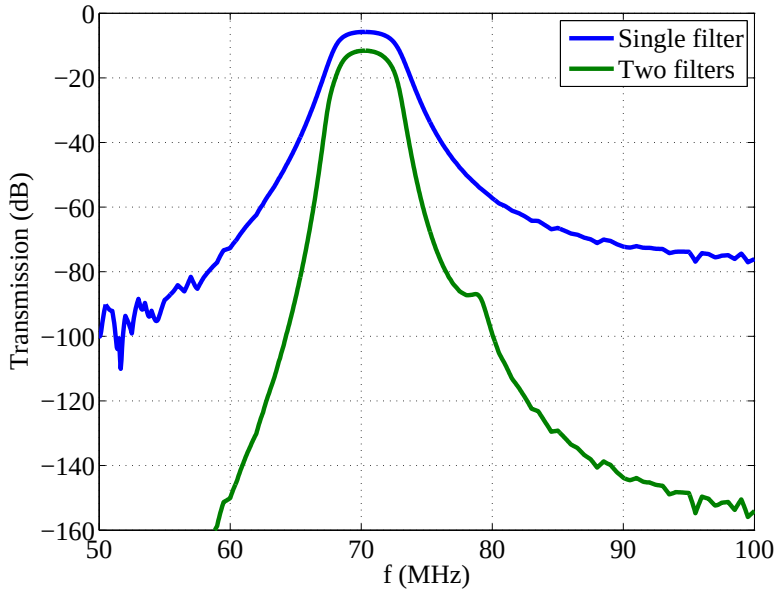


Figure 6.2: Mini-Circuits BPF-C70+ frequency response (vendor-provided S-parameters, simulation)

may be stronger than −132 dB. Section 6.6 shows several PCB design details to tackle the issue. The pass-band loss of 11.6 dB is still significant and is compensated using an IF amplifier after the filter stage.

6.3 IF Amplifier

The IF amplifier is needed to compensate the filter losses and provide the optimal power level to the mixer.

The selected Analog Devices ADL5535 is internally matched and provides 16.5 dB gain. The high OIP3 of 43.5 dB means that it is operated at over 50 dB of IP3 backoff (table 5.1) and will not contribute significant nonlinearity.

A fixed attenuator is used after the amplifier to set the exact signal level. This attenuator is placed *after* the amplifier to not further deteriorate the noise figure.

6.4 Single-Sideband Modulator

A Texas Instruments TRF370317 I/Q modulator is used for the upconversion. Outstanding features are [9]:

- OIP3 of 26.5 dBm
- Noise floor of −163 dBm/Hz

- LO feedthrough of −40 dBm (note that this value is independent of the signal power and also the LO power)
- Side-band suppression of 45 dBc
- Differential baseband inputs

The functional block diagram of the mixer is shown in figure 6.3. As the mixer baseband inputs are differential and the IF interface is single-ended, a balun is needed. The balun is also used to provide the DC bias that is needed on the baseband inputs.

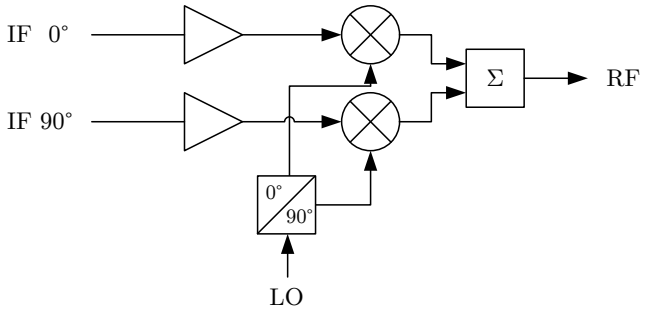


Figure 6.3: Mixer functional block diagram

Every differential amplifier has some DC offset between each line of the differential pair. The offset at the input amplifiers of the mixer is the fundamental cause for LO feedthrough as it causes a DC voltage on the mixers. To get rid of the LO feedtrough, a process called carrier nulling can be used [10]. The offset between the differential lines of both the inphase (0°) and the quadrature (90°) input are adjusted iteratively until the minimal LO feedthrough is found. The offset voltages are very small, on the order of µV, which makes the process very sensitive.

Figure 6.4 shows the process of carrier nulling, going through three passes. In the third pass, the LO feedthrough is reduced to less than −70 dBm, an improvement of over 30 dB. The slopes at the minimum are already very steep at this point. Further passes may be able to temporarily reduce the feedtrough even further, but also make the slopes even steeper. The slightest change in environmental parameters (temperature, supply voltage, device aging, ...) would cause the LO feedtrough to shoot up again. Another practical limit is the resolution the offset voltage can be adjusted with.

As shown in the link budget (table 5.1), the mean output power of the mixer is −14 dBm. With the datasheet LO feedthrough of −40 dBm, this is a distance of just 26 dB. To fulfill the spurious emissions specification (sec. 5.4), 22.5 dB are absolutely needed, to provide a total rejection of 102.5 dB together with the output filter that provides 80 dB.

To be able to improve the LO feedthrough, carrier nulling circuitry is integrated into the biasing circuit (fig. 6.5). A center-tapped transformer acts as a balun, DC blocked by capacitors C37 and C38 and RF terminated by R3 (the mixer has high-impedance inputs). Through the four-channel DAC1 both collective biasing and the differential offset

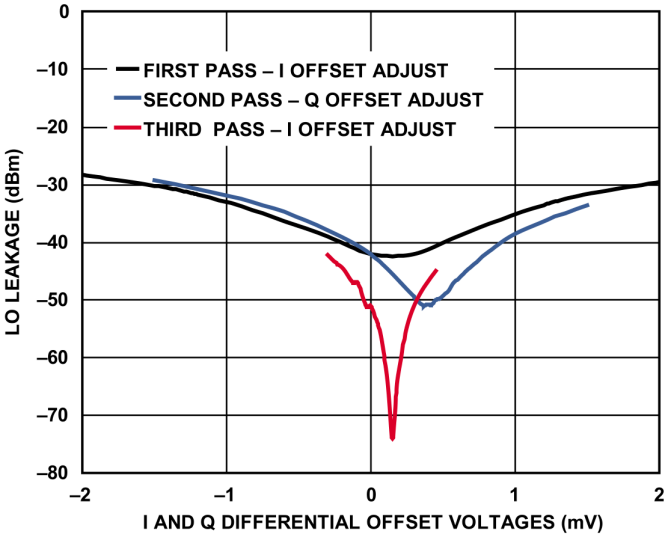


Figure 6.4: Iterative carrier nulling. Source: [10]

are controlled for the 0° and the 90° input (only the 0° part is shown). Output VOUTA controls the collective bias. Output VOUTB can shift one leg of the differential pair through resistor R23 which is much larger than R19. Using this setup, even a 12 bit DAC as is used here (Texas Instruments DAC7574) can control the offset with high resolution.

In terms of input power, a compromise has to be found between the introduced noise level (fixed noise floor) and the generated nonlinearity. Using the setup shown in figure 6.6, different power levels are empirically evaluated: The SMBV signal generator's baseband outputs are fed to the mixer's I and Q inputs. While the available RF bandwidth is 120 MHz (software option SMBV-B10), this translates to only 60 MHz on the baseband outputs. This makes testing at the real IF of 70 MHz impossible using the setup. The test is instead conducted at 60 MHz, which is assumed to be close enough to reflect the behavior at 70 MHz.

An alternative is to use the RF output of *two* phase-coherent SMBVs, allowing arbitrary output frequencies. Two problems are found with this approach:

1. Low quality of coherence. Even using a passive combiner with 180° out-of-phase signals, suppression above 30 dB is hardly achieved. Additionally, the suppression ratio is found to be time-varying. The results are not reproducible in the sense that switching the modulator on and off can lead to vastly different results. This suggests an internal problem in the baseband synchronization between the SMBVs.
2. High noise floor at the RF output. At 70 MHz, the noise floor is significantly worse than at 1 GHz, where it is already almost touching the spectral mask.

Overall, using the baseband output at 60 MHz is considered to be the better option for this test.

Shown in figure 6.7 is the output spectrum of the mixer for two power levels in comparison with the SMBV RF output. The output spectrum at −17.5 dBm shows a

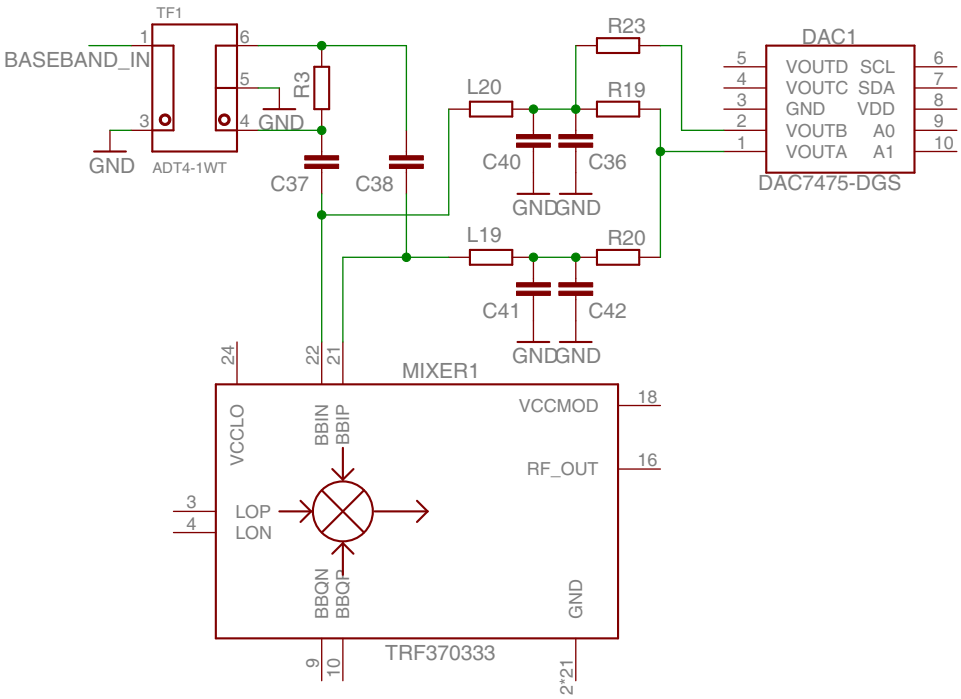


Figure 6.5: Simplified schematic of the baseband input biasing

lower noise floor, but also some nonlinearity. The mixer input level can be fine-tuned on the PCB using the Π-attenuators. As shown in the link budget, −14 dBm is found to be a good setting as the nonlinearity introduced by the mixer is small compared to the contributions of the gain blocks.

Interestingly, the SMBV's RF output is significantly outperformed by the mixer's output at −17.5 dBm. This means that the SMBV engineers favored linearity over noise floor.

6.5 RF Gain Blocks

Internally matched gain blocks are convenient to use as they require only a few external components and no tuning. As the whole upconversion happens on a single PCB, the selection is limited to SMD devices. However, SMD gain blocks are available only up to a certain power level. A selection of high-IP3 gain blocks is presented in table 6.2. The P1dB is about 20 dBm, including the PAPR of at least 11 dB this means that the mean output power is limited to roughly 10 dBm. The rest of the necessary gain up to 42.5 dBm has to be provided by the driver and the power amplifier.

The first design planned to use two ADL5602 connected in series. This configuration is tested with two ADL5602 on test-PCBs connected through a variable attenuator

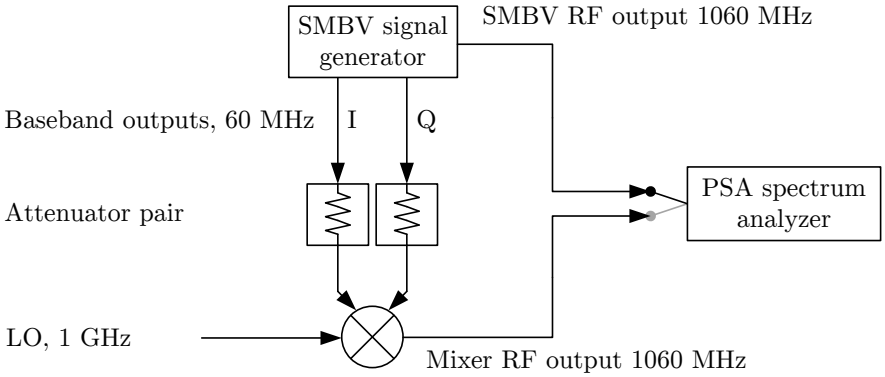


Figure 6.6: Test setup for determining the optimal power level

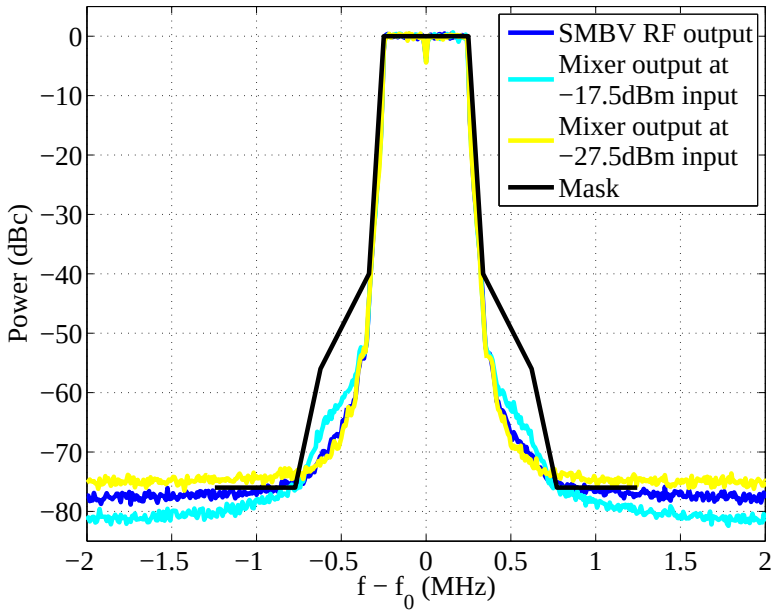


Figure 6.7: Mixer output spectrum vs input power (10 kHz RBW)

Supplier	Part name	Gain (dB)	P1dB (dBm)	IP3 (dBm)
Mini-Circuits	HXG-122+	15.20	23.75	40.83
Mini-Circuits	HXG-242+	15.75	23.10	43.22
Analog Devices	ADL5601	15	18	42
Analog Devices	ADL5602	20	20	40

Table 6.2: High-IP3 gain blocks datasheet specifications compared at 1 GHz and 5 V DC supply

(Rohde & Schwarz RSG) as shown in figure 6.8. The output spectrum is very good, even at power levels above the necessary 4 dBm (fig. 6.9). The relatively high noise floor comes from the mixer stage that is driven at an input power level of only -27.5 dBm for best linearity and matches the noise floor shown in figure 6.7.

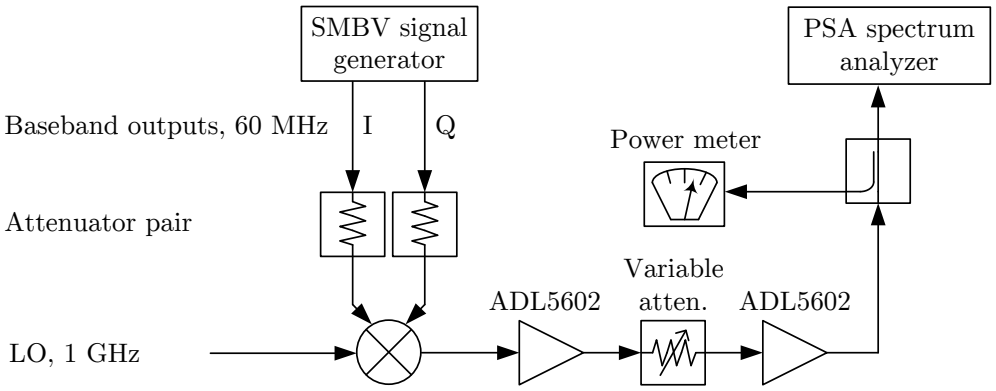


Figure 6.8: Test setup for the ADL5602

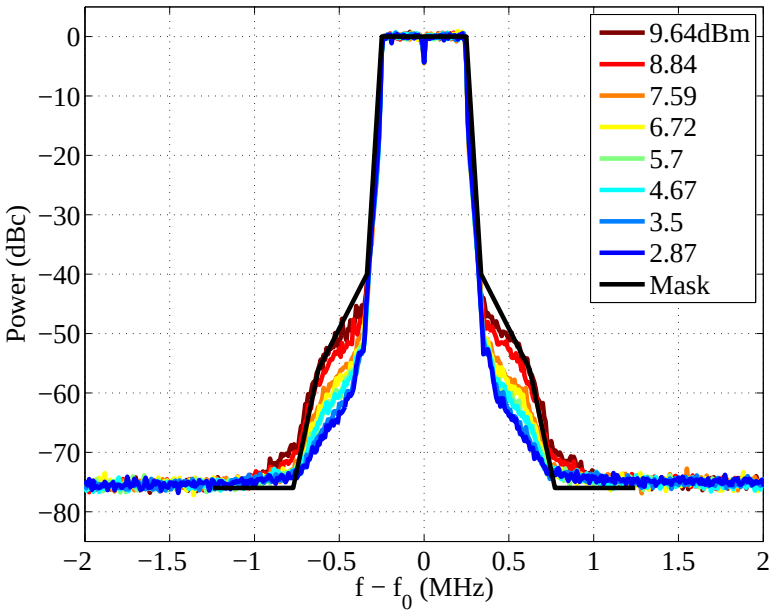


Figure 6.9: Spectrum at the output of ADL5602 in series for different output powers (10 kHz RBW)

As the mixer input power level in the final system is significantly higher, the ADL5602 can be substituted by an ADL5601 that provides lower gain at an higher IP3. This combination is tested on the complete PCB (sec. 6.6). The test setup block diagram is shown in figure 6.10. The PCB is equipped with test-points along the signal path, so

the change of the spectrum through the chain can be tracked. As the 70 MHz IF filters are in place on the PCB, the test cannot be conducted at 60 MHz any longer. Instead, the RF output of two phase-coherent SMBV signal generators is used for generating the 70 MHz 0° and 90° signal. The output power of the 2nd ADL5601 is 4.9 dBm.

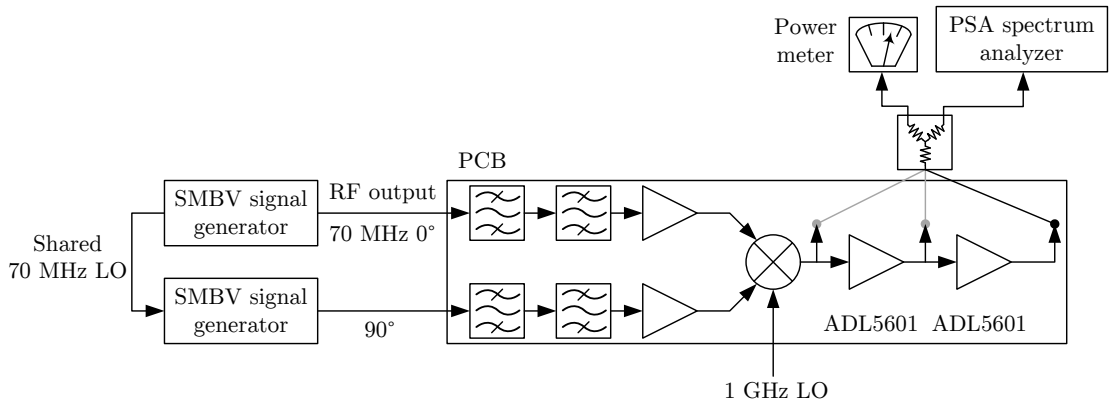


Figure 6.10: PCB block diagram

Analyzing the spectra (fig. 6.11), performance is worse than expected from the ADL5602 test. The signal after the 2nd ADL5601 has third- and fifth-order products that significantly violate the spectral mask. For comparison, an external ADL5602 is used instead of the two ADL5601. At an output power of 5.36 dBm, the spectrum shows considerable improvement. It is also noted that the noise floor at the mixer output is actually lower than at the SMBV output. This is because the narrow input filters suppress the noise outside the desired signal bandwidth.

6.6 Upconversion PCB

Figure 6.12 shows the populated upconversion PCB. The placement of the parts is roughly equivalent to figure 6.10.

Five solder pads for square shielding enclosures are provided around each functional block. To combat the problem of coupling between IF filter input and output transmission lines mentioned in section 6.2, the first and second stage of the filter bank is shielded separately.

As this is a four layer design, the IF lines are moved to an inner layer to shield them additionally. The IF signal enters the PCB at the SMA connectors at the left and immediately dives into the inner layer.

At the bottom right the blue 10-pin connectors provide power supply and digital control over an I^2C bus. Each PCB in the transmitter prototype carries two connectors to allow arbitrary daisy-chaining of the boards.

As the digital attenuators are SPI-controlled, an I^2C-to-parallel converter is used to provide SPI-over-I^2C. The converter is placed outside the shielding next to the blue

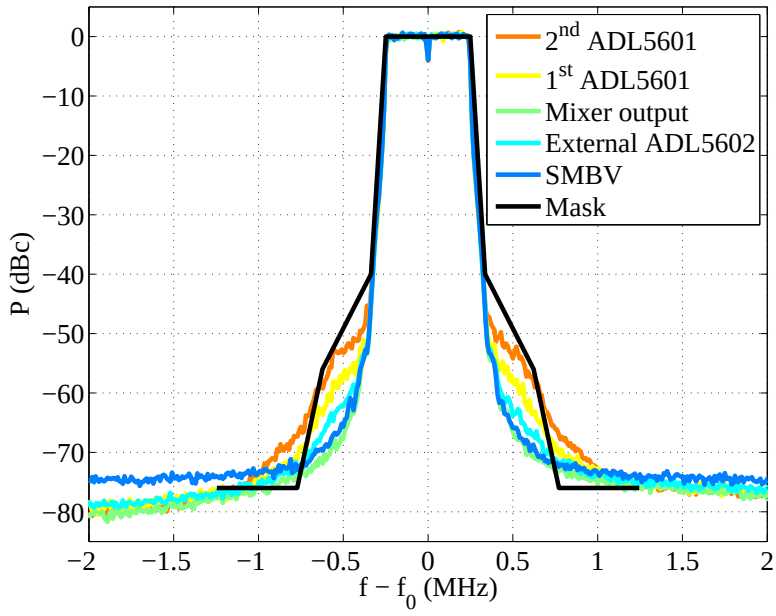


Figure 6.11: Spectrum at different points in the chain (10 kHz RBW)

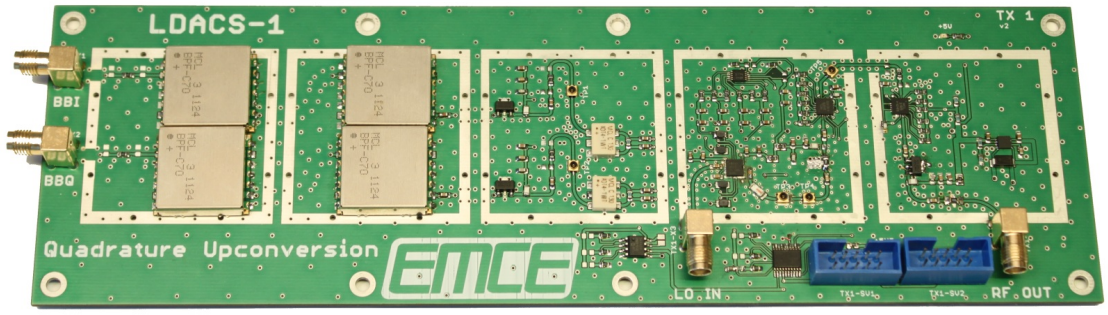


Figure 6.12: Populated upconversion PCB

connectors.

Power is provided to the PCB by a 5.5 V switching-mode power supply. A high PSRR (power supply ripple rejection) low-dropout linear regulator, seen on the right above the "RF OUT" connector, is used to provide a stable supply voltage.

7 LO Synthesizer

Although a local oscillator (LO) synthesizer is needed both in the transmitter and in the receiver prototype, it is associated to the upconversion path and also within the scope of this thesis.

7.1 Requirements

The most important performance parameters for an LO synthesizer are phase noise and frequency switchover time (in the following simply called *lock time*).

The L-DACS1 specification does not have a strict specification for the LO phase noise. It does, however, have a recommendation [11, p. 103]. The LO synthesizer is designed to meet these recommendations as displayed in table 7.1, in the following called the *phase noise mask*.

Δf	Phase noise (dBc/Hz)
1 kHz	−88
10 kHz	−90
100 kHz	−118
1 MHz	−135
10 MHz	−140
100 MHz	−140

Table 7.1: L-DACS1 recommended LO phase noise

The L-DACS1 specification proposes four frequency bands (sec. 5.3). However, these are different deployment options and only two of them will be used, one for the uplink and one for the downlink, as L-DACS1 is a frequency-division duplex (FDD) system. Each receiver and each transmitter will be fixed to a single band. This means that the "frequency switchover time", that is specified to 5 ms [11, p. 58], concerns switching within one frequency band.

The LO synthesizer designed here supports all bands. It also supports arbitrary switching across bands, however, the lock time requirement may not be met in that case.

7.2 Measuring Oscillator Noise

The ideal oscillator generates a perfect sine wave at it's nominal frequency as modeled by

$$V(t) = V_0 \sin(2\pi f_0 t). \tag{7.1}$$

In the frequency domain, this is a single Dirac peak. A real oscillator, on the other hand, suffers from several imperfections:

- Random amplitude fluctuations
- Long-term drift of V_0
- Random phase fluctuations (jitter)
- Long-term drift of f_0

Slight long-term drift of the amplitude V_0 is usually insignificant. On the other hand, drift of the mean frequency f_0 is a severe problem for a reference oscillator as it causes the whole system to transmit (or receive) at a wrong frequency. The long-term stability of oscillators is usually given in parts per million (ppm) per time-interval or even indefinitely. The L-DACS1 standard states a stability for the 10 MHz reference oscillator of 0.1 ppm (indefinitely).

The short-term random fluctuations can be modeled as [12]

$$V(t) = (V_0 + \epsilon(t)) \sin(2\pi f_0 t + \Phi(t)), \tag{7.2}$$

with $\epsilon(t)$ and $\Phi(t)$ denoting the amplitude and phase fluctuations, respectively. These fluctuations translate into an overall broadening of the spectral line. A typical power spectral density plot of a real oscillator is shown in figure 7.1.

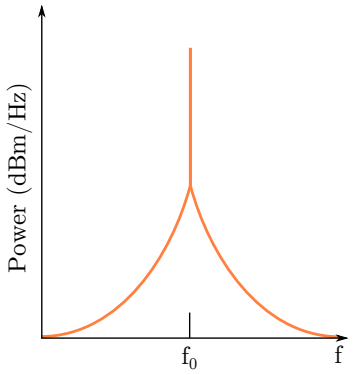


Figure 7.1: Example power spectral density for a real oscillator [12, p. TN-196]

The side-bands seen on either side of the mean frequency f_0 are the superposition of the components created by amplitude fluctuations and phase fluctuations (the phase noise). Only the phase noise is usually specified in oscillator datasheets. The phase noise is the important component because the amplitude noise is usually suppressed by the nonlinear operation of the mixer. Phase noise usually propagates unchanged through the chain.

The term *phase noise* usually means the power spectral density originating from the phase fluctuations of the oscillator and is usually expressed as dBm/Hz or, to make it independent of the output power, as dBc/Hz.

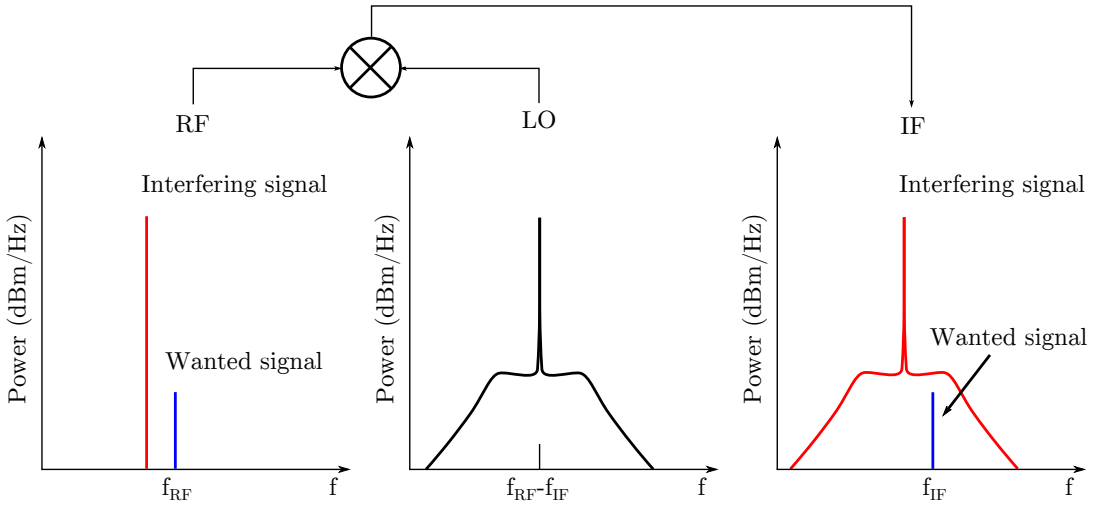


Figure 7.2: Effect of phase noise in a receiver [13]

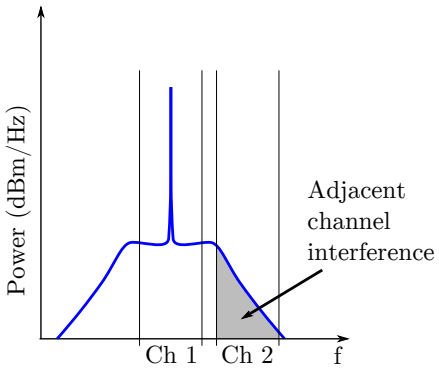


Figure 7.3: Effect of phase noise in a transmitter. Source: [13, fig. 1]

In an RF receiver, phase noise determines the selectivity (fig. 7.2), whereas in a transmitter, phase noise causes interference for the adjacent channels (fig. 7.3). Both figures assume that a PLL-stabilized oscillator is used for the LO (hence the shape of the spectrum), which is usually the case in practice. Section 7.4 discusses the spectrum in detail.

Phase noise can be measured using signal source analyzers like the Agilent E5052B. Such a signal source analyzer is unfortunately not available at the lab. The overall power spectral density can be directly measured using a spectrum analyzer. This approach, however, has two drawbacks:

1. The spectrum analyzer cannot separate amplitude and phase noise and displays both components.
2. The selectivity of a spectrum analyzer is determined by its own internal local oscillator (LO). The spectrum that is displayed is the sum of the spectra of the

oscillator under test (OUT) and the internal LO. Accurate measurements are only possible if the spectrum analyzer's LO is significantly better than the one of the OUT. For high-quality OUTs this is typically not the case, which is why signal source analyzers operate on a different principle.

Still, measurements using a spectrum analyzer can be used as a pessimistic estimate for the phase noise.

7.3 PLL Operation

Voltage-controlled oscillators (VCOs) have a tuning input port that controls the output frequency within some limits set by its design. This tuning voltage is provided by the phase-locked loop (PLL) IC.

Figure 7.4 shows a synthesizer including the PLL IC, the loop filter and the VCO. The reference frequency, in this design 10 MHz, is divided by the R counter to the phase-frequency detector (PFD) frequency $f_{\mathrm{PFD}} = \frac{f_{\mathrm{ref}}}{R}$ and is fed into the the PFD. The VCO output at f_{out} is fed back through the N counter also into the PFD. Once the PLL is locked, $f_{\mathrm{PFD}} = \frac{f_{\mathrm{out}}}{N}$ or equivalently,

$$\frac{f_{\mathrm{out}}}{N} = \frac{f_{\mathrm{ref}}}{R}. \tag{7.3}$$

The R and N counter work as frequency dividers by counting input signal cycles. From a configured initial value, they count down to zero. At this point, a positive digital pulse is output and the counter is reset to the initial value. Left and right-hand side of equation 7.3 represent the *pulse rate* for the N and the R counter, respectively.

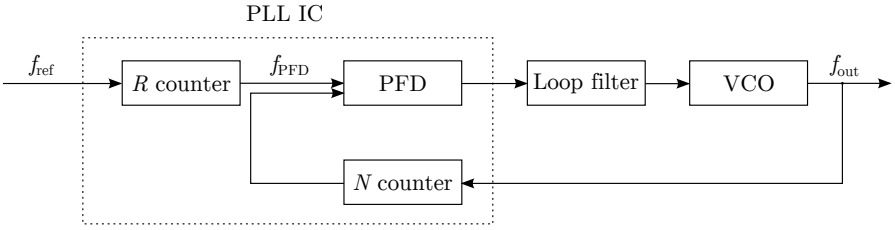


Figure 7.4: Synthesizer block diagram [14, fig. 1]

The PFD includes a charge pump that can either output a precisely defined positive or negative current or it can switch to a high-impedance state (tri-state). Through the loop filter it is connected to the VCO's tuning input.

The operation of the PFD is conceptually very simple: It contains a state machine with three states transitioning upon the pulses from the N and R counters [15]. A pulse from the N counter transitions the state to the left, while a pulse from the R counter transitions to the right (fig. 7.5). An example for a transition sequence is shown in figure 7.6.

Assuming the VCO runs too fast, the pulse rate of the N counter is higher than that of the R counter ($\frac{f_{\mathrm{out}}}{N} > \frac{f_{\mathrm{ref}}}{R}$). This keeps the charge pump alternating between sink

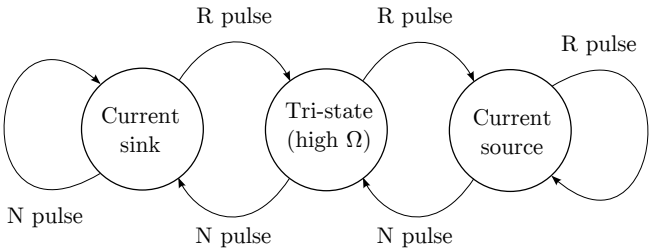


Figure 7.5: PFD state transition diagram [15, fig. 3.2]

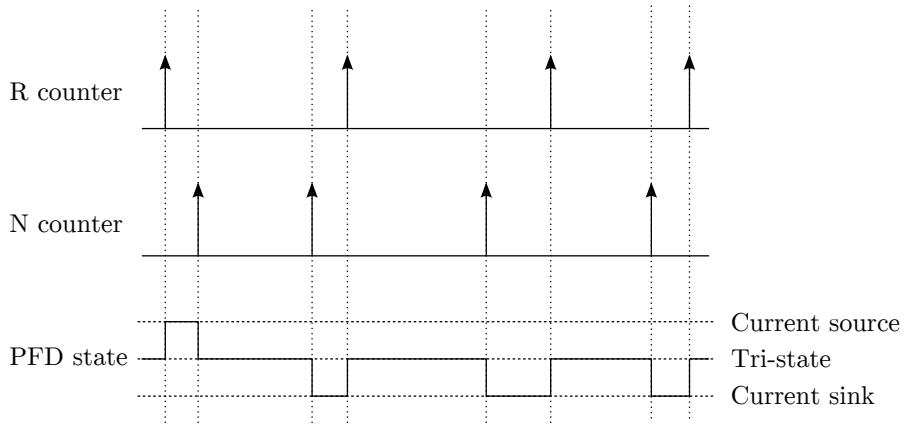


Figure 7.6: PFD operation example [15, fig. 3.3]

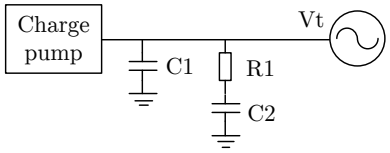
and tri-state mode, never reaching source mode. The average current output is negative, which causes the voltage at the VCO tuning port to drop, reducing the VCO frequency (VCOs usually have a positive frequency-voltage characteristic). This process continues until N and R output pulses at the same rate. Now, the phase difference between N and R determines the average current. If the N counter is ahead of R, the VCO will be slowed down until the phases are synchronized. At this point, the average current becomes zero and the PLL is locked.

7.4 The Loop Filter and PLL Noise

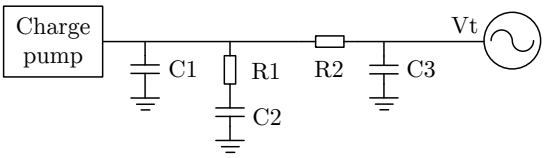
The loop filter converts the rectangular current pulses from the charge pump to a continuous tuning voltage. Its integrator characteristic removes high-frequency components from the PFD output. Two popular passive topologies are shown in figure 7.7. Active designs introduce additional noise but are needed if the tuning voltage for the VCO is higher than what the charge pump can provide [15, p. 198].

Higher-order loop filters provide better suppression of spurious products generated by charge pump operation. However, the series resistors needed for third order and higher (R3 in figure 7.7b) add additional thermal noise. For the design laid out in detail in section 7.7, a second order loop filter as shown in figure 7.7a is chosen, as it introduces

the least thermal noise [15, p. 174].



(a) Second order loop filter



(b) Third order loop filter

Figure 7.7: Passive loop filter topologies

The loop filter bandwidth B_{LF} sets the maximum VCO phase noise frequency the PLL can compensate. Outside the loop filter bandwidth the VCO behaves as if it was free-running.

The VCO noise is usually known from the vendor datasheet and decreases when moving away from the carrier frequency until it reaches a noise floor (fig. 7.1). Under some constraints[1], the noise from the PLL charge pump can be modeled to be white. Its power level can be estimated from the 1 Hz normalized synthesizer phase noise floor, $PN_{1\,\mathrm{Hz}}$, that is usually stated in the vendor datasheet.

The actual synthesizer phase noise PN_{synth} can be modeled as [15, equ. 14.2]

$$PN_{\mathrm{synth}} = PN_{1\,\mathrm{Hz}} + 20\log(N) + 10\log\left(\frac{f_{\mathrm{PFD}}}{1\,\mathrm{Hz}}\right). \tag{7.4}$$

Using the fact that the N counter $N = f_{\mathrm{out}}/f_{\mathrm{PFD}}$, equation 7.4 can be rewritten as

$$\begin{aligned} PN_{\mathrm{synth}} &= PN_{1\,\mathrm{Hz}} + 20\log\left(\frac{f_{\mathrm{out}}}{f_{\mathrm{PFD}}}\right) + 10\log\left(\frac{f_{\mathrm{PFD}}}{1\,\mathrm{Hz}}\right) \\ &= PN_{1\,\mathrm{Hz}} + 20\log\left(\frac{f_{\mathrm{out}}}{1\,\mathrm{Hz}}\right) - 10\log\left(\frac{f_{\mathrm{PFD}}}{1\,\mathrm{Hz}}\right). \end{aligned} \tag{7.5}$$

For a fixed output frequency f_{out}, doubling f_{PFD} (equivalently, halving the N divider value) reduces the noise by 3 dB. In other words, a high PFD frequency f_{PFD} is desirable. This is one of the reasons fractional PLLs were developed (sec. 7.5).

The overall phase noise at the output of a PLL synthesizer is the combination of several components:

[1] Moving very close to the carrier ($\Delta f < f_{\mathrm{PFD}}$), $1/f$ noise becomes dominant [15, p. 101], which restricts the validity of the white noise model to $\Delta f > f_{\mathrm{PFD}}$.

- Inside the loop filter bandwidth B_{LF}, the white noise from the PLL charge pump PN_{synth} is seen.
- Outside B_{LF}, the free-running VCO noise is dominant.

Figure 7.8 shows the components for the optimal choice of B_{LF}. This choice of B_{LF} is optimal in the sense that it leads to the lowest total phase noise. It is set to the carrier offset Δf of the crossover point between VCO noise and PLL noise.

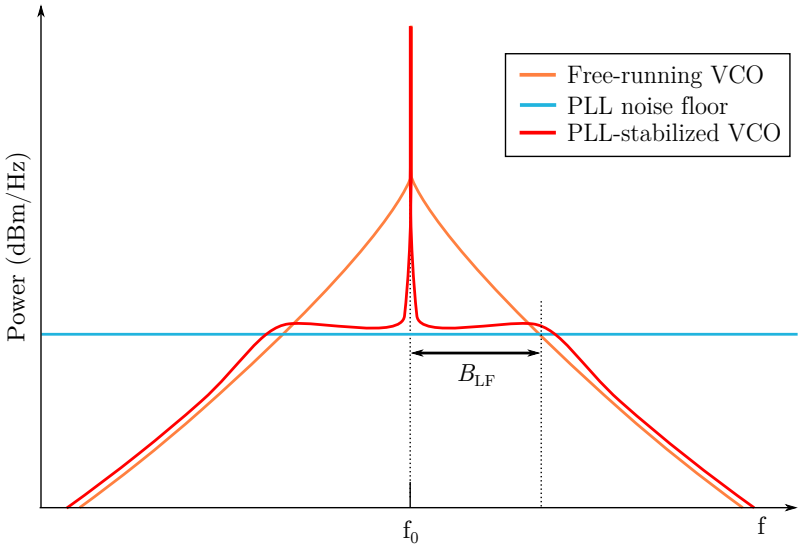


Figure 7.8: Free-running and PLL-stabilized VCO

Two more factors have to be taken into consideration when designing the loop filter bandwidth:

- Lock time. The time it takes for the PLL to lock to a new frequency t_{lock} can be roughly approximated as [15, p. 128]

$$t_{\mathrm{lock}} = \frac{4}{B_{\mathrm{LF}}}. \tag{7.6}$$

  The lock time requirement sets a lower limit for the loop filter bandwidth B_{LF}.
- Spurious emissions. In addition to white noise, periodicity in the charge pump operation causes frequency spikes in the output spectrum. This problem is more prominent in fractional PLLs (sec. 2.6) and can be mitigated by using a higher-order loop filter or reducing the loop filter bandwidth.

7.5 Fractional and Integer PLLs

PLLs are available in two variants: fractional and integer. The difference between fractional and integer is in the N counter, that can take fractional values in the case of a fractional PLL.

For an integer PLL, the output frequency is an integer multiple of the PFD frequency:

$$f_{\text{out}} = N \cdot f_{\text{PFD}}. \tag{7.7}$$

As one usually wants to tune to channels on a grid spaced by f_{sp}, this means that the maximum f_{PFD} is f_{sp}. The grid may, however, be offset by f_{o}. Additionally, f_{ref} must be an integer multiple of f_{PFD}. Summarizing,

$$f_{\text{PFD}} = \frac{f_{\text{out}}}{N} = \frac{f_{\text{ref}}}{R}, \quad \forall \quad f_{\text{out}} = n \cdot f_{\text{sp}} + f_{\text{o}}. \tag{7.8}$$

Thus, f_{PFD} is normally set to the greatest common divisor of f_{ref} and $f_{\text{sp}} + f_{\text{o}}$. For some combinations, this is a very small value. As shown in equation 7.4, a low f_{PFD} leads to high phase noise and should, therefore, be avoided.

Fractional PLLs solve this problem by allowing rational values for N. With a fractional PLL, one can usually run the PFD at full f_{ref}, some even feature internal frequency multipliers to run the PFD at $2 \cdot f_{\text{ref}}$. Aside from the gained flexibility, equation 7.4 suggests an improvement in phase noise.

The problem with fractional PLLs is spurious emissions [14, p. 3]: The fractional N counter is actually implemented using an integer counter. In an integer PLL, the counter is reset to a fixed value once is has reached zero. In a fractional PLL, the reset value cycles through a list of integer numbers to give the desired rational N value on average. That means that the N counter actually fires at a slightly wrong moment every time, causing constant charge pump activity. The periodic cycling through the list of integer numbers causes frequency spikes at fractions *and* multiples of the PFD frequency. The actual frequency of these spikes depends on the length of the list, meaning that it may change when switching channels. Some PLLs offer a low spur mode that dithers the list entries to make the spurs effectively look like white noise. Unfortunately, this causes a strong degradation of the PLL noise floor (up to 10 dB [16, p. 19]).

Even though the spur performance of fractional PLLs has greatly improved recently, simulations using ADIsimPLL show that the problem is still prevalent for this use case and fractional PLLs are disregarded in favor of an integer PLL solution.

7.6 Integrated Synthesizer Solution

Integrated synthesizers combine a VCO and a PLL into a single package. The only external component is the loop filter. Even though the performance usually falls behind discrete solutions, they are convenient to use and it should be evaluated if an integrated solution fulfills the requirements.

The ADF4350 is a high-performance integrated wide-band synthesizer. It achieves the extremely wide output frequency range of 137 to 4400 MHz by internally switching between three VCOs where each can be switched to 16 frequency bands. Frequencies below 2200 MHz are generated using a programmable output frequency divider. In simulation, the synthesizer tightly fulfills the phase noise mask (fig. 7.9).

After discussion with Frequentis, it is decided to go for the best possible performance and build the synthesizer from discrete components, as detailed in the next section.

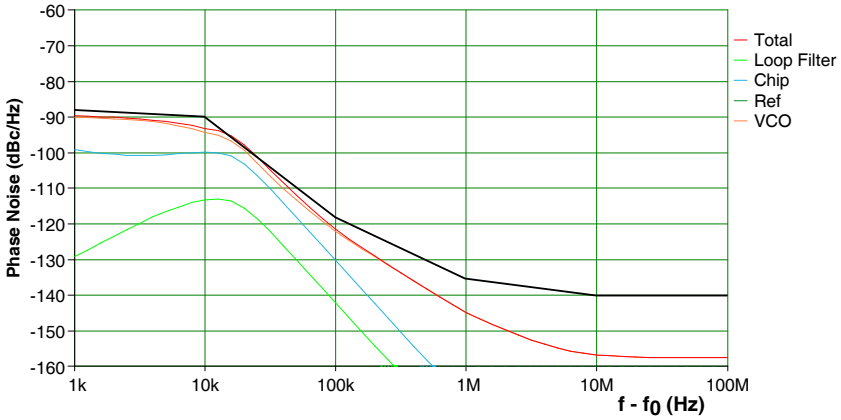


Figure 7.9: Simulated phase noise for the integrated synthesizer ADF4350 (phase noise mask in black)

7.7 Final Design

Narrow-band VCOs are available with very low phase noise. Wide-band VCOs sacrifice some phase noise performance to cover a wider band. For this high-performance design, two narrow-band VCOs are switched on demand to cover all channels. The selected VCOs are shown in table 7.2.

#	Manufacturer	Model	Frequency range (MHz)	Phase noise @ 10kHz (dBc/Hz)	Phase noise @ 100kHz (dBc/Hz)	Tuning voltage range (V)
1	Crystek	CVCO55CL-1030-1090	1030–1090	−110	−131	0.5–4.5
2		CVCO55CL-1090-1145	1090–1145	−108	−130	0.3–4.7

Table 7.2: Specifications of selected VCOs [17, 18]

The lowest L-DACS1 channel is at 963.5 MHz (in band 1) and the highest is at 1156.5 MHz (in band 4, see table 5.2). This is a range of 193 MHz, while the VCOs only cover 1030 MHz − 1145 MHz = 115 MHz. This works if the highest band uses a low LO while the others use a high LO. The alternative to using a mixed high/low LO configuration would be to introduce a third VCO. Compared to the mixed high/low configuration that only requires software changes, this option is deemed excessive. The final LO band diagram is shown in figure 7.10.

For the PLL, the Analog Devices ADF4106 integer PLL is selected. Outstanding features are:

- Low normalized synthesizer phase noise floor, $PN_{1\,\mathrm{Hz}} = -219\,\mathrm{dBm/Hz}$.

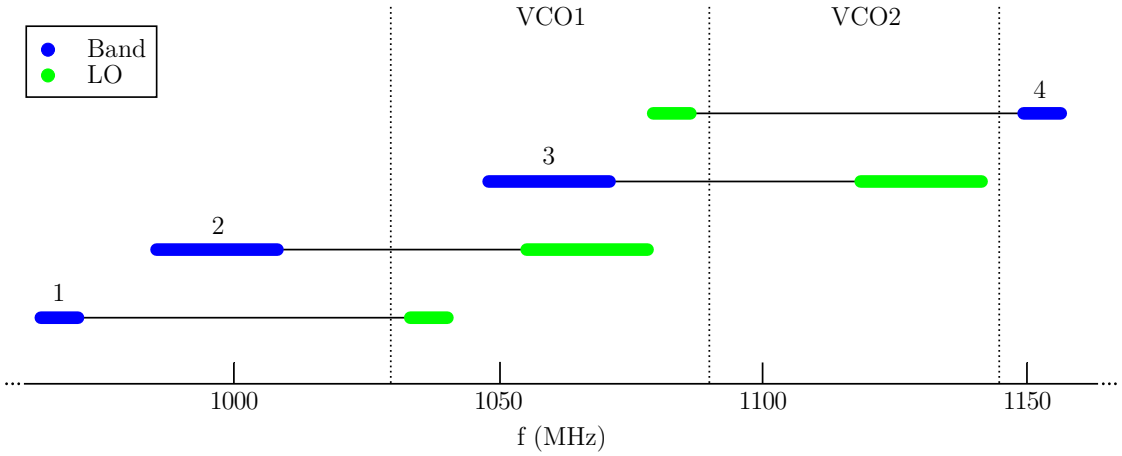


Figure 7.10: LO band overview

- Charge pump operation up to 5.5 V (separate supply voltage for the charge pump). This is needed because the tuning voltage range exceeds the standard 3.3 V supply voltage.

A second-order loop filter with a bandwidth $B_{\mathrm{LF}} = 5\,\mathrm{kHz}$ is used. Equation 7.6 predicts $t_{\mathrm{lock}} = \frac{4}{500\,\mathrm{kHz}} = 800\,\mu\mathrm{s}$, which is roughly consistent with the time to reach 1 Hz accuracy (see below).

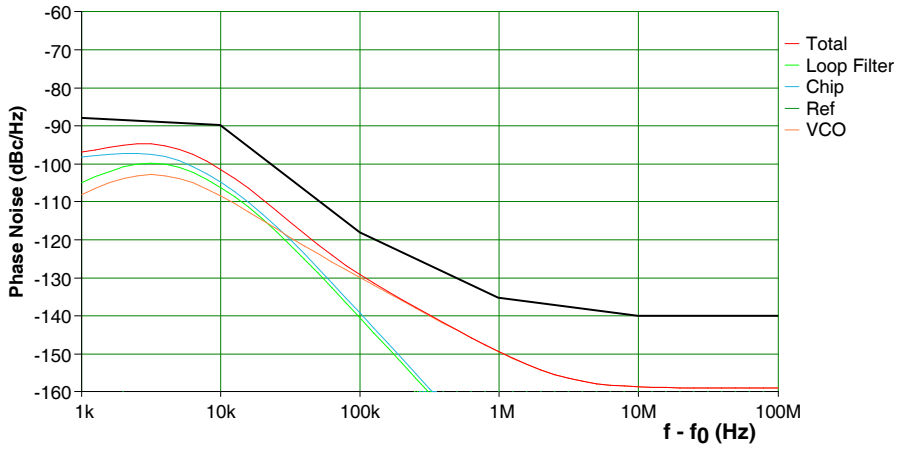


Figure 7.11: Simulated phase noise (spectral mask in black)

Phase noise and lock time for both VCOs are simulated using ADIsimPLL. For the lock time simulation, a switch from the lowest VCO frequency to the highest one is used as a worst-case scenario. The simulation results for VCO1 are shown in figure 7.12. Results for VCO2 are virtually identical and therefore omitted. The phase noise requirements are fulfilled with a margin of at least 5 dB. The lock detect output that is integrated in the PLL (top right image in figure 7.12) goes high again after only $t_{\mathrm{LD}} \approx 330\,\mu\mathrm{s}$. If the

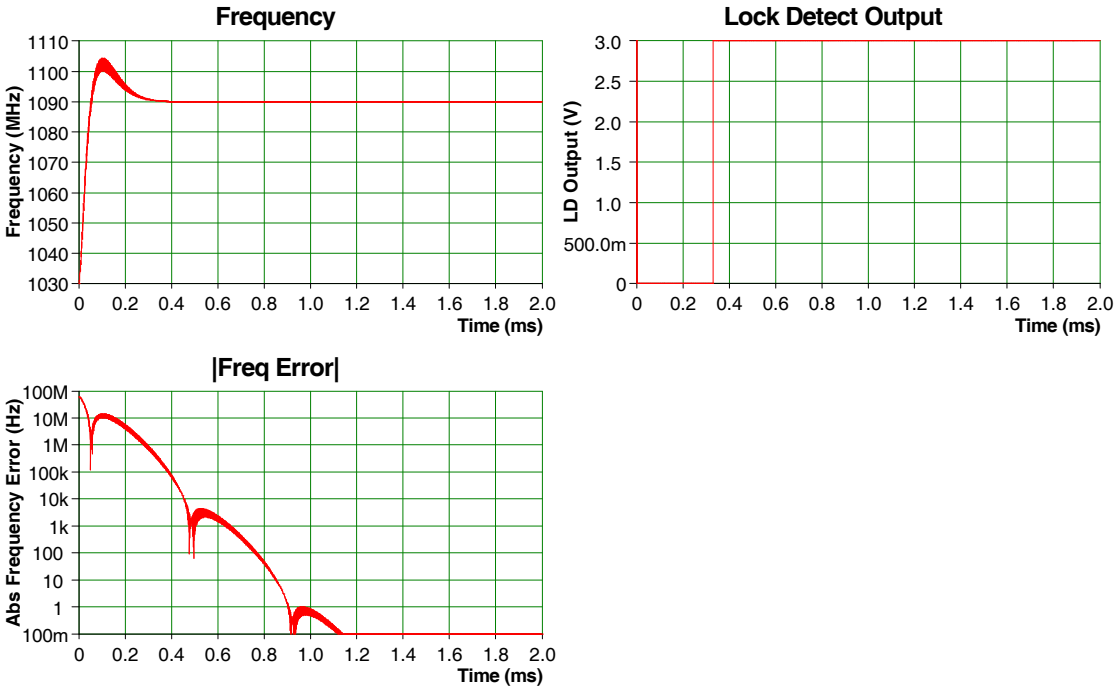


Figure 7.12: Lock time simulation

lock time is defined in a stricter sense as the time until the frequency error is below 1 Hz, the lock time is roughly 1 ms $\approx 3 \cdot t_{\mathrm{LD}}$ which is well below the 5 ms requirement.

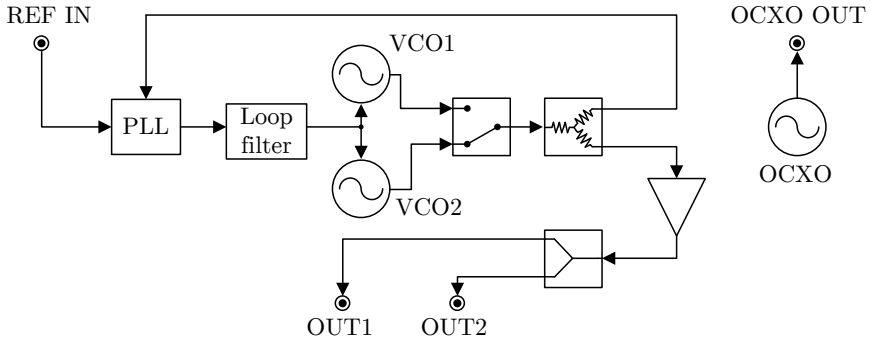


Figure 7.13: Synthesizer PCB block diagram

Both VCOs share a common PLL and loop filter. Both VCOs' tuning ports are connected to the loop filter at all times, though the unused VCO's supply voltage is turned off to prevent spurious emissions. As the transmitter needs two LO outputs (upconverter, reference receiver), a gain block is included before the power splitter to boost the LO power (fig. 7.13). An oven-controlled crystal oscillator (OCXO) is used as the 10 MHz reference. An OCXO is the only possibility to reach the stability of 0.1 ppm

that is required by the L-DACS1 specification. It is not internally connected at the PCB as the OCXO is the shared master oscillator for upconversion path, the reference receiver, the baseband unit and the receiver. The 10 MHz clock is distributed using a clock distribution unit integrated into the baseband unit provided by Frequentis.

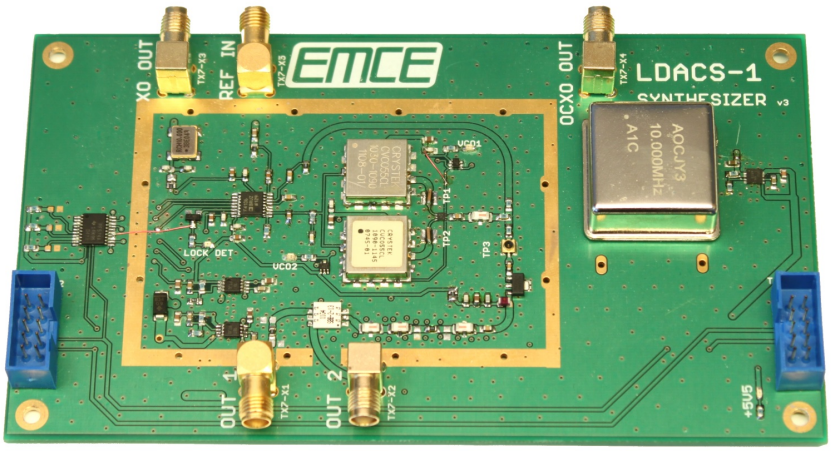


Figure 7.14: Populated synthesizer PCB

The PCB including the OCXO (right side) is shown in figure 7.14. The block diagram 7.13 reflects the layout on the board. A solder pad for a shielding enclosure is provided to help prevent interference. Like the upconversion PCB, it includes two 10-pin connectors for power an I²C I/O (left and right edges). The 5.5 V input is converted using high-PSRR low-dropout linear regulators to the required 5 V and 3.3 V supply voltage. An I²C to parallel converter is used to communicate with the PLL IC that uses SPI.

7.8 Measurement Results

Phase noise measurements are taken, in absence of a source signal analyzer (sec. 7.2), using the Agilent PSA spectrum analyzer and its noise marker function:

- VCO1 is measured at 1060 MHz, which is the center of its frequency range,
- VCO2 only contains one band (fig. 7.10). Therefore, the measurements are taken at the middle of this band, at 1160 MHz.

Figure 7.15 shows the measured phase noise for both VCOs. At $\Delta f = 100\,\text{kHz}$, the phase noise of the PSA, which is almost 10 dB higher than the simulation results, clearly is the limiting factor. At $\Delta f > 10^7\,\text{Hz} = 10\,\text{MHz}$, the noise floor of the PSA is reached. The performance of VCO2 is worse than expected for $\Delta f \leq 10^4\,\text{Hz} = 10\,\text{kHz}$, but still, the phase noise mask is fulfilled for both VCOs.

The lock time for both VCOs is measured by switching between their lowest and highest specified frequency (tab. 7.2) and monitoring the VCO tuning voltage and the PLL's lock detect output.

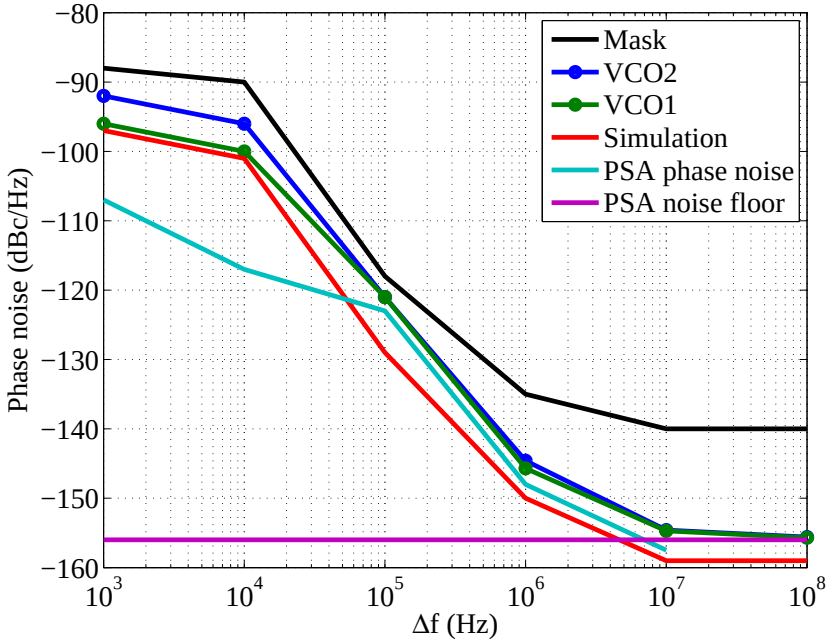


Figure 7.15: Measured phase noise

After setting the new frequency (actually, a new N counter value is set), the lock detect output goes low. It goes high again (with t_{LD} designating the time that has passed) once the phase error between R and N counter is lower than 15 ns for five consecutive PFD cycles [19, p. 10]. From the ADIsimPLL simulations it follows that the frequency error is below 1 Hz after $3 \cdot t_{\mathrm{LD}}$. Figures 7.16 and 7.17 show the results. The colored curves show the slower transition, for VCO1 this is switching from high to low frequency. With ADIsimPLL predicting a t_{LD} of about 330 μs, the longest measured lock time is 406 μs (low to high transition for VCO2). With $3 \cdot t_{\mathrm{LD}} = 3 \cdot 406\,\mu\mathrm{s} = 1.218\,\mathrm{ms}$, the result is well below the requirement of 5 ms. No change in the tuning voltage (lower curves) can be seen after $1 \cdot t_{\mathrm{LD}}$.

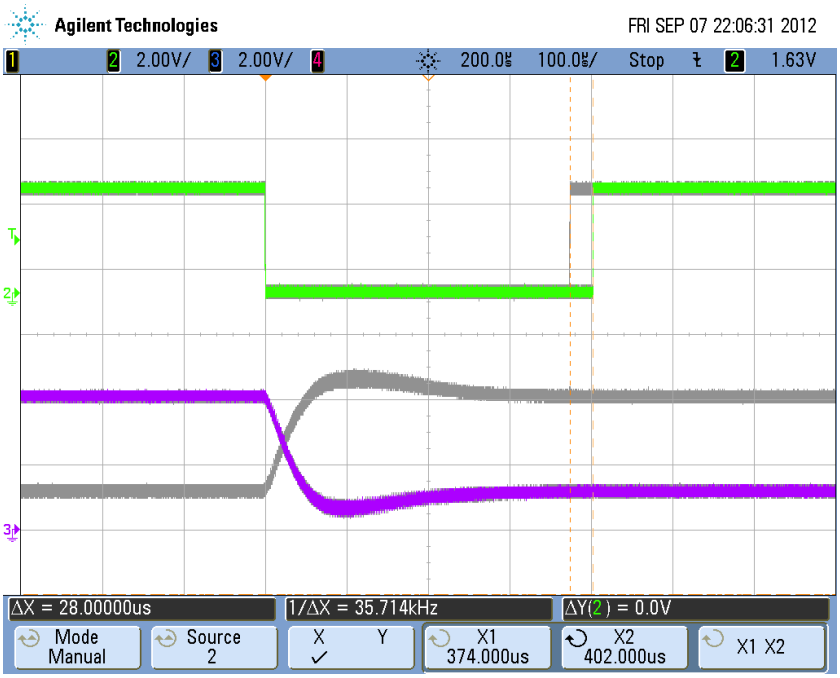


Figure 7.16: VCO1 switching between 1030 MHz and 1090 MHz (upper curves: lock detect, lower curves: tuning voltage)

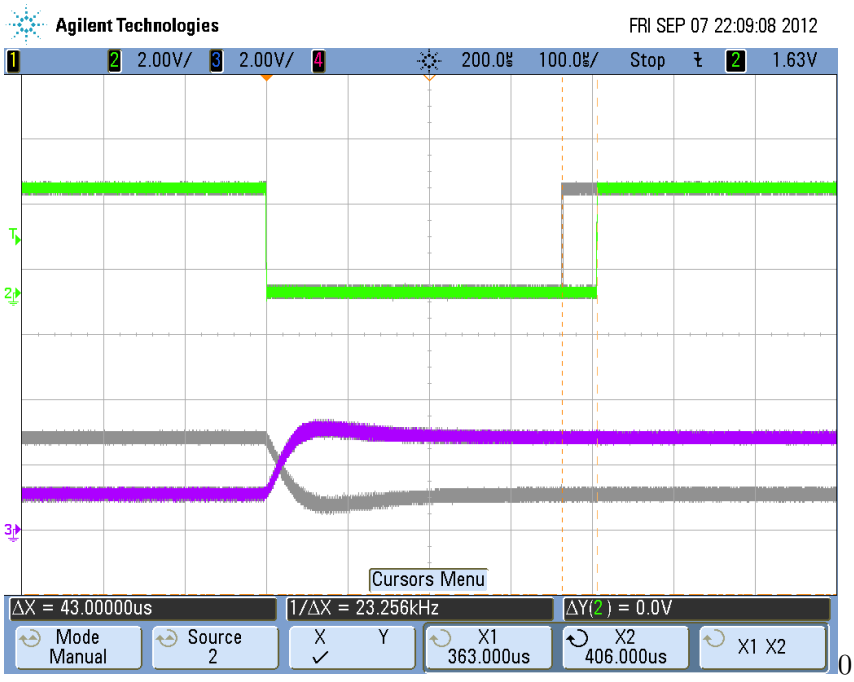


Figure 7.17: VCO2 switching between 1090.5 MHz and 1145 MHz (upper curves: lock detect, lower curves: tuning voltage)

8 Power Amplifier

8.1 Component Selection

High power amplifiers (PAs) designed for the aerospace L-band range of 960–1160 MHz are not yet available from many manufacturers. At the time of the selection, only Freescale was a viable option.

Two RF transistors are selected for testing, the MRF6V12250H 275 W device and the MRF6V12500H 500 W device. Both are manufactured in the rugged LDMOS technology and operate at 50 V drain voltage (tab. 8.1). The datasheet suggests that these devices are destined for use in pulsed applications, candidates being DME (distance measurement equipment) or ADS-B (advanced dependent surveillance - broadcast). While an OFDM signal is strictly speaking continuous, its high PAPR property makes it similar to a pulsed signal. This is why these devices are seen as a good match for the L-DACS1 requirements.

Manu-facturer	Device	P1dB (W)	P3dB (W)	Broadband power gain (dB)	Frequency range (MHz)	Drain voltage (V)
Freescale	MRF6V12250H	299	338	19.8	960–1215	50
	MRF6V12500H	511	575	18.5		

Table 8.1: Datasheet specifications of the selected power amplifiers

Both devices feature an identical ceramic package (fig. 8.1).

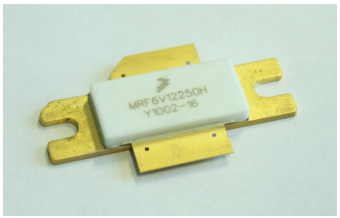


Figure 8.1: RF transistor screw-mount ceramic package

8.2 Evaluation Module

For both power amplifiers, evaluation modules including a matching PCB, a heatsink and connectors could be obtained from Freescale. The PCB provides matching from the

very low input and output impedance of a few Ω up to 50 Ω.

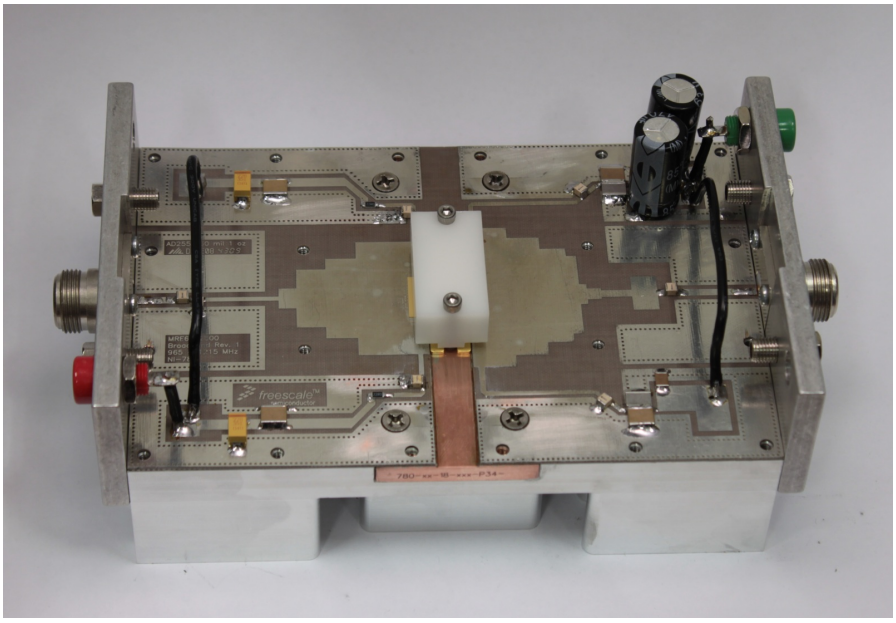


Figure 8.2: Populated evaluation board on heatsink

The bare PCB is soldered to a copper heat spreader, which is in turn is screwed to a aluminum base that also provides side walls for mounting the N connectors and the ports for gate and drain voltage (fig. 8.2). The amplifier itself is clamped to the PCB using a plastic holder that provides firm pressure for good electrical and thermal contact.

8.3 Test Setup

For all power amplifier measurements, a very similar setup is used (fig. 8.3).

The output power is constantly monitored and the input power is adjusted to obtain an average output power of 42.5 dBm at all times. The path between the amplifier under test (AUT) and the output power meter (cables, attenuators and directional coupler) is compensated by configuring an offset at the output power meter.

To measure the transducer gain of the AUT, the input power meter monitors the input of the AUT. The loss of the directional coupler is compensated by applying an offset to the input power meter.

Assuming 20 dB gain for the AUT, the required peak input power is 43.5 dBm + 11 dB − 20 dB = 34.5 dBm. Accounting for some cable and connector losses, the practically required power will be somewhat higher. As the maximum output power of the SMBV signal generator is 30 dBm, a pre-amplifier is needed. The Mini-Circuits ZHL-30W-252+ is operated in sufficient backoff from it's IP3 of 52 dBm to not introduce significant nonlinearity. Verifying the spectrum after the pre-amplifier, it is found to be virtually identical to the output spectrum of the signal generator.

The output spectrum of the AUT is monitored using the PSA spectrum analyzer. The current consumption is read from the power supply's integrated display.

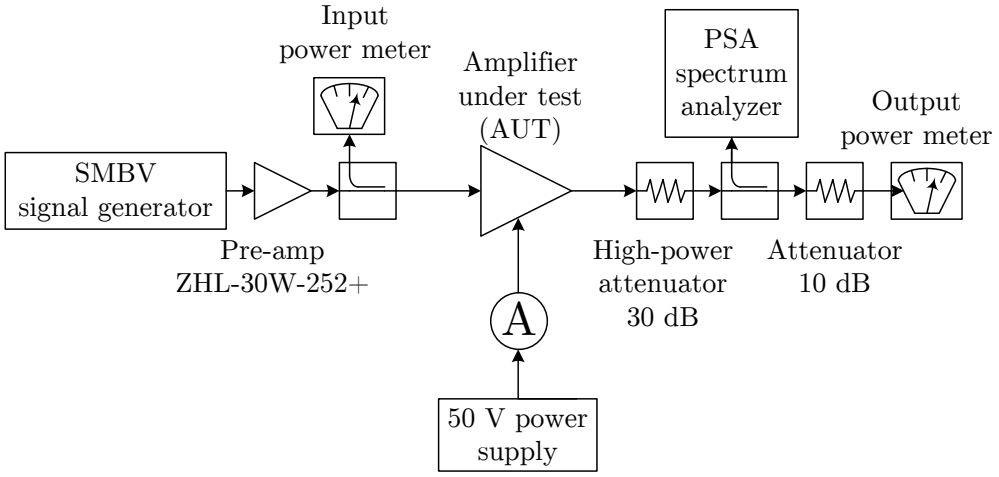


Figure 8.3: PA test setup

8.4 Optimum Bias Current

Adjusting the bias current is an essential standard procedure to get reasonable performance out of an RF amplifier. The bias current setting I_{Dq} changes the gain, linearity, and even input and output impedance of an amplifier. Figure 8.4 shows the output spectrum of the 500 W amplifier at the datasheet's suggested value of $I_{\mathrm{Dq}} = 200\,\mathrm{mA}$ and a sweet spot at 1750 mA. The sweet spot is the bias current setting that gives the output spectrum with the highest linearity. It is experimentally found by monitoring the output spectrum (fig. 8.3) while iteratively adjusting the bias current.

At the same time gain and linearity go up, efficiency goes down. The datasheet bias current seems to be optimized for efficiency. Tuning to the sweet spot leads to a dramatic improvement of the shoulder distance from just 20 dB to 45 dB.

The behavior of the 275 W device is similar as shown in the next section.

8.5 Comparison of 275 W and 500 W Device

The peak RF power of 224 W can be, even with a small margin, handled by the smaller 275 W device. The 500 W device is also evaluated because it may provide better linearity because of the bigger backoff from its IP3. This advantage could translate to a better spectrum after DPD.

The drawbacks of using the 500 W device are cost, gain and power efficiency: It is about 63 % more expensive (Digi-Key prices as of Oct. 2012). In terms of RF performance, the datasheet values suggest a smaller gain for the 500 W device (table 8.1). Using oversized RF amplifiers generally leads to poor power efficiency.

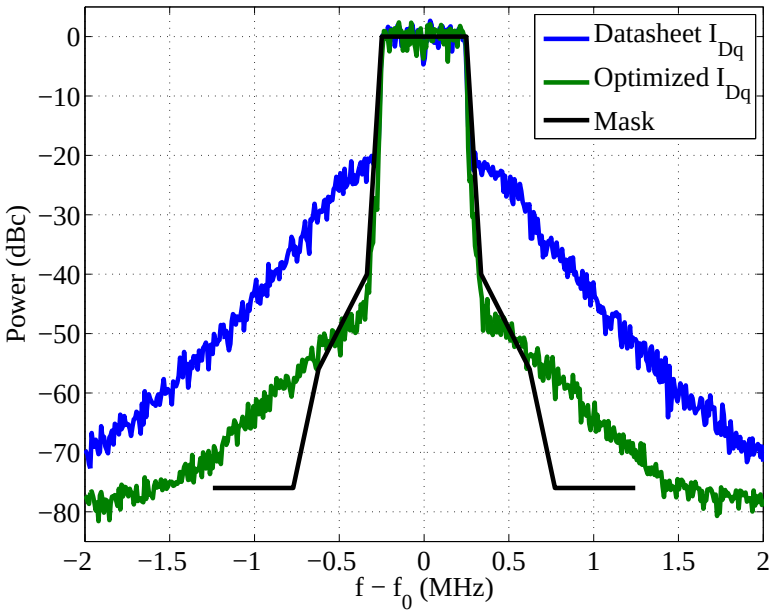


Figure 8.4: Idle current optimization for the 500 W device (10 kHz RBW)

A range of bias currents is tested for both amplifiers (tables 8.2 and 8.3), starting from the datasheet recommended value up to (or slightly beyond) the sweet spot. Input power is adjusted to give an output power of 42.5 dB for every bias current setting.

The test confirms that the gain of the 500 W amplifier is significantly lower than that of the 275 W amplifier, for every bias current setting. At the sweet spot, the thermal losses[1] of the 500 W amplifier are two times the losses of the 275 W device.

	I_{Dq} (mA)	Gain (dB)	DC input power (W)	Thermal losses (W)	η (%)	PAE (%)
Datasheet →	100	20.0	72	54	24.7	24.5
	200	20.5	74	57	23.9	23.7
	500	21.6	84	66	21.2	21.0
Sweet spot →	**940**	**22.6**	**95**	**77**	**18.7**	**18.6**
	1000	22.5	96	78	18.5	18.4

Table 8.2: 275 W device performance for a range of bias currents

Linearity is the key requirement that voids all other concerns. Figure 8.5 compares the output spectra of both amplifiers at their sweet spot. As expected, the linearity of the 500 W device is better without DPD. Surprisingly, the 275 W device outperforms the 500 W device once DPD is activated. The peaks seen on the lower 275 W curve (275 W device with DPD) are an artifact of the early version of DPD algorithm used for this test

[1] Drain efficiency is defined as $\eta = \frac{P_{\mathrm{RF,Out}}}{P_{\mathrm{DC,in}}}$. Power-added efficiency is defined as $PAE = \frac{P_{\mathrm{RF,Out}} - P_{\mathrm{RF,In}}}{P_{\mathrm{DC,in}}}$.

	I_{Dq} (mA)	Gain (dB)	DC input power (W)	Thermal losses (W)	η (%)	PAE (%)
Datasheet →	200	15.7	111	94	16.0	15.4
	400	16.5	120	102	14.9	14.6
	600	17.0	128	110	13.9	13.7
	800	17.4	134	116	13.3	13.0
	1000	17.6	140	122	12.7	12.5
	1200	18.0	144	127	12.3	12.1
	1400	18.1	152	134	11.7	11.5
	1600	18.4	159	141	11.4	11.3
Sweet spot →	**1750**	**18.4**	**160**	**143**	**11.1**	**10.9**

Table 8.3: 500 W device performance for a range of bias currents

that left some rare but drastic phase shifts uncompensated. The flaw is corrected in the current version of the algorithm, for which spectra are shown in chapter 10.

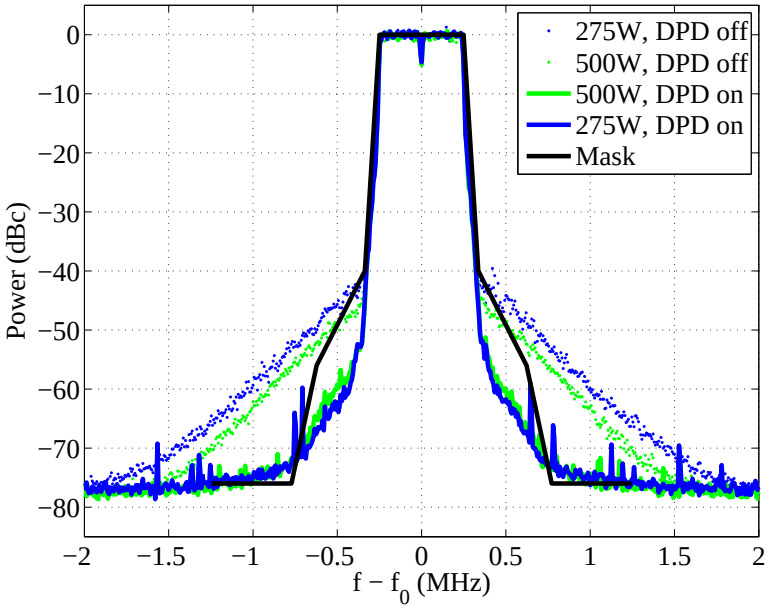


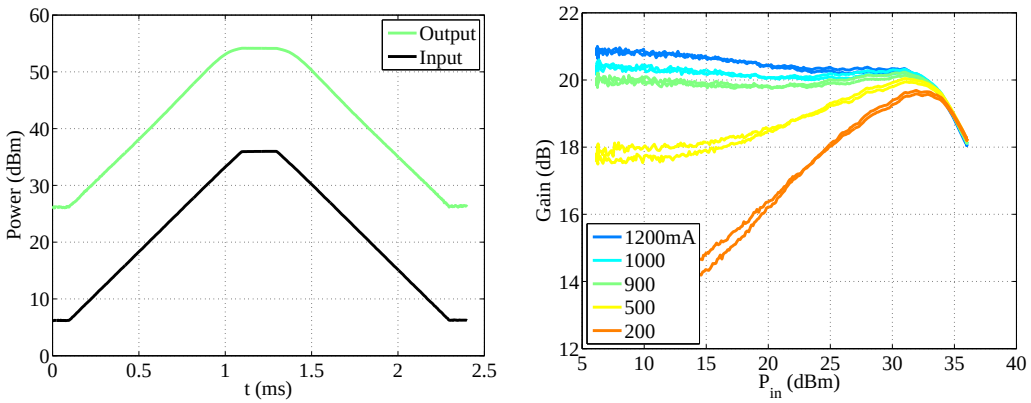
Figure 8.5: Output spectra of 275 and 500 W amplifiers, without and with DPD (10 kHz RBW)

Summing up, the 275 W amplifier has higher gain, better efficiency, and a better output spectrum with DPD.

After discussion with Frequentis, the 275 W device is selected to be used in the prototype and all further testing. All measurements involving the power amplifier in the following sections refer to the 275 W device.

8.6 AM-AM Measurements

While a spectrum measurement allows to find the optimal bias points, it does not give understanding of the underlying nonlinear behavior. Using a simple setup, a signal generator and a spectrum analyzer, the AM-AM distortion can directly be measured. A power ramp from the signal generator is measured by the spectrum analyzer in zero-span mode. The amplifier is inserted and the power ramp is measured again (fig. 8.6a). The difference between the two measurements is the gain, which can now be plotted over the input power.



(a) Power ramp in the time domain at 900 mA bias current

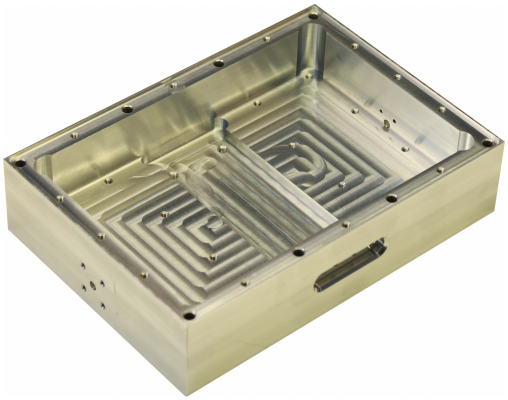
(b) AM-AM for a range of bias currents

Figure 8.6: Direct AM-AM measurement for the PA in the in milled enclosure

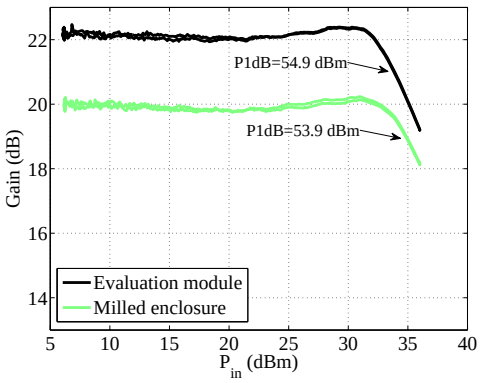
Figure 8.6b shows the resulting curve set for a range of bias currents. In agreement with the spectrum measurements, a bias current of roughly 900 mA shows the flattest response. As expected, the PA show gain *compression* at high power levels.

8.7 Enclosure

The evaluation module (fig. 8.2) is not suitable for direct use in the prototype because it lacks shielding. For that reason, aluminum enclosures are CAD-designed by Holger Arthaber and milled from solid blocks of raw material (fig. 8.7a). Also the test fixture PCBs provided by Freescale are reproduced, courtesy of Reinhard Koeppner.



(a) Milled enclosure



(b) AM-AM characteristics of evaluation module and milled enclosure at 900 mA

Figure 8.7: Effect of the milled power amplifier enclosure

The changed environment also affects the RF performance of the amplifier. Although great care is taken to reproduce the layout as is on the same PCB substrate and to use the same components as those provided by Freescale, the gain is 2 dB lower. Unfortunately, the P1dB is also 1 dB lower (fig. 8.7b). Chapter 10 will lay out that a good spectrum is achieved nevertheless.

9 Driver Amplifier

9.1 Component Selection

As the power amplifier provides a gain of roughly 20 dB, the driver amplifier has to provide an output power of 42.5 dBm − 20 dB = 22.5 dBm $\hat{=}$ 0.2 W mean or, including the worst-case PAPR of 13 dB, 33.5 dBm $\hat{=}$ 3.5 W peak.

To avoid introducing another power supply unit, the 50 V DC voltage is also used for the driver amplifier.

The Freescale MRF6V10010 is selected as it provides ample headroom in terms of $P_{1\,\mathrm{dB}}$, is manufactured in the same rugged technology as the PA (LDMOS), and matches the PA's frequency range and supply voltage (tab. 9.1).

Manufacturer	Device	$P_{1\,\mathrm{dB}}$ (W)	$P_{3\,\mathrm{dB}}$ (W)	Pulsed power gain (dB)	Frequency range (MHz)	Drain voltage (V)
Freescale	MRF6V10010	10.4	11.65	25	960–1400	50

Table 9.1: Datasheet specifications of the selected driver amplifier

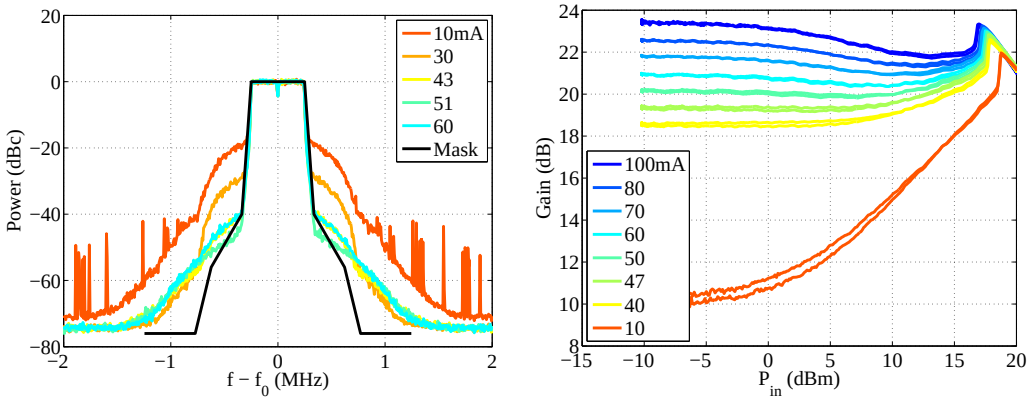
9.2 Optimum Bias Current

As for any power amplifier (sec. 8.4), the bias current has to be optimized to get reasonable linearity. In the frequency domain, a sweet spot is found at $I_{\mathrm{Dq}} = 50\,\mathrm{mA}$. The datasheet value of 10 mA is clearly not optimized for good linearity. The spikes are caused by discontinuities in the output signal that are introduced by the strong nonlinearity at the 10 mA operating point.

9.3 AM-AM Measurements

Using the method presented in section 8.6, the result obtained in the frequency domain is validated using the AM-AM distortion (fig. 9.1).

As the frequency domain results have predicted, at roughly 50 mA the flattest response is obtained. Interestingly, the driver amplifier shows gain *expansion* at this operating point. This compensates some of the compression introduced by the PA. Because of the gain expansion, the PAPR after DPD has been observed to be actually *lower* at the input of the driver-PA chain than at its output.



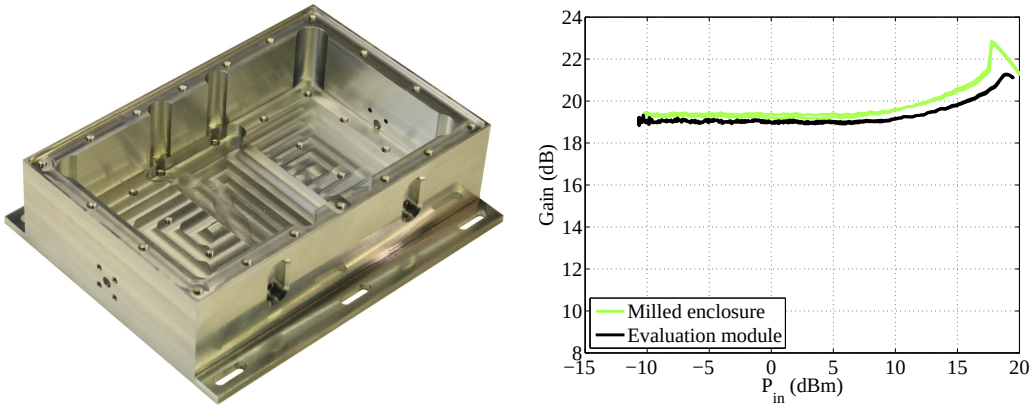
(a) Output spectra (10 kHz RBW)

(b) AM-AM measurements

Figure 9.1: Driver amplifier in milled enclosure tested for a range of bias currents

9.4 Enclosure

The driver amplifier is provided with an evaluation module similar to that of the PA that lacks shielding. A milled aluminum enclosure is manufactured to provide shielding and cooling (fig. 9.2a) and the PCB is reproduced.



(a) Milled enclosure

(b) AM-AM characteristics of evaluation module and milled enclosure at 50 mA

Figure 9.2: Effect of the milled driver amplifier enclosure

The gain does not show a big change compared to the test fixture (fig. 9.2b). The behavior of the evaluation module is, however, significantly more good-natured. The sharp kink in the characteristic of the milled enclosure is challenging for the DPD algorithm as it introduces strong phase distortions (see chap. 10).

10 Amplifier Chain

Chaining multiple amplifiers can lead to unexpected results up to instability. In an individual test, both source and load have a high return loss. Power amplifiers are usually modestly well matched at their input and reflect a significant part of the power back to the previous amplifier in the chain.

This chapter examines the chain of driver amplifier and power amplifier, the crucial part of the overall transmit system.

10.1 Test Setup

The electrical length between the amplifiers rotates the impedances around the Smith chart. A directional coupler between the amplifiers yields better understanding of the physical processes as the power transfer can be observed. The change in electrical length, however, is found to vastly change the behavior of the system. It is decided that the system, therefore, should be evaluated in the configuration as it will operate in the prototype unit with driver amplifier and power amplifier connected directly (figs. 10.1, 10.2).

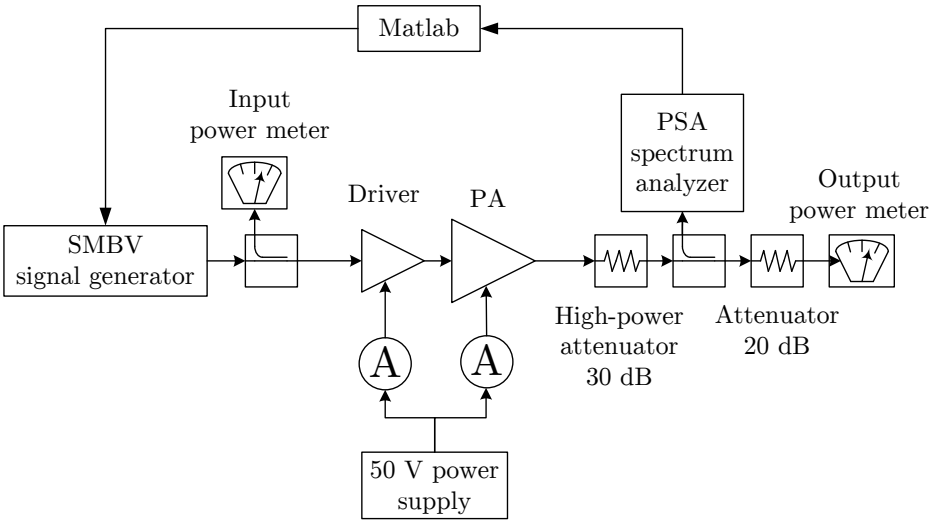


Figure 10.1: Test setup block diagram

The PSA is used as the data recorder and Matlab closes the DPD loop. The output power of the SMBV is adjusted to get a PA output power of 42.5 dBm.

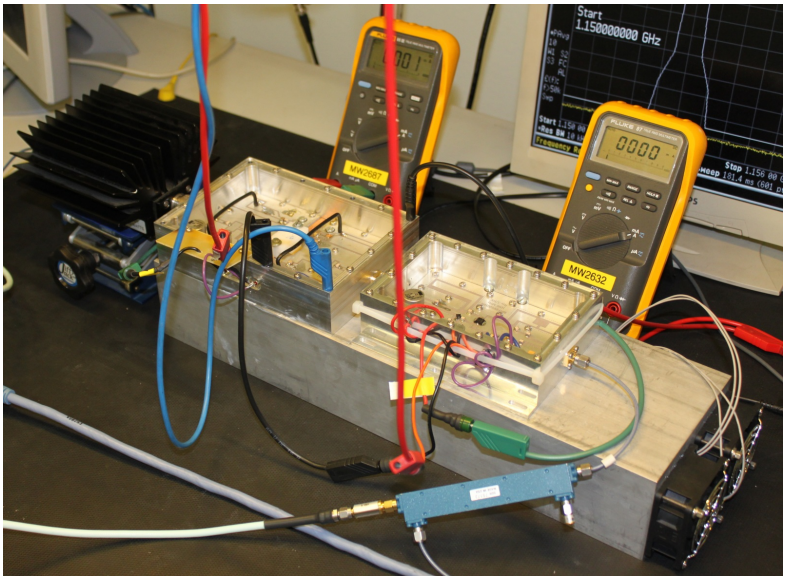


Figure 10.2: Test setup

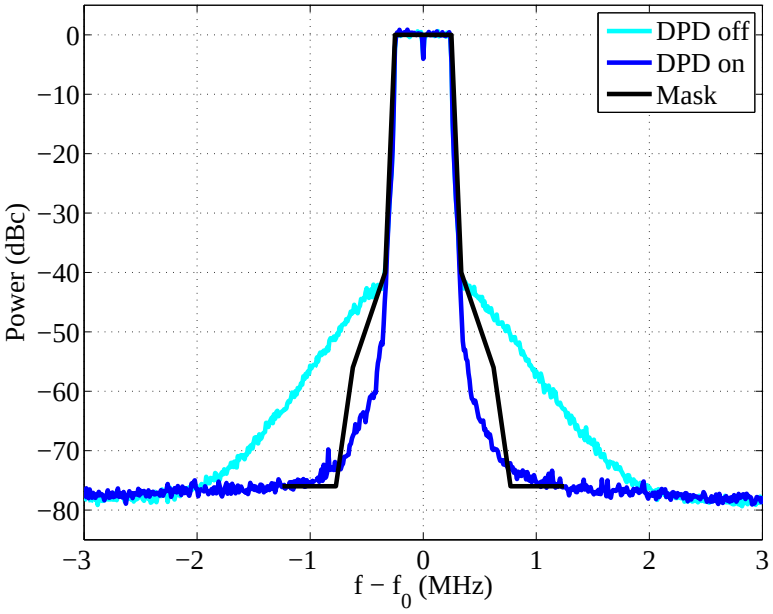
The test is conducted for band 1 ($963.5 - 970.5\,\text{MHz}$) and 3 ($1048.5 - 1071.5\,\text{MHz}$) as they are the focus of the prototype (sec. 5.3). For each band, the bias current of both driver and PA is optimized at the center of the band. Measurements are performed at the center and at the edges of the bands, with and without DPD.

10.2 Measurement Results

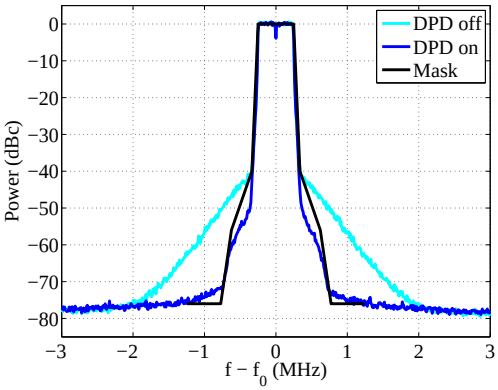
Band 1 is only 7 MHz wide, so the properties of the amplifier change little when moving from the center to the band edges. The DPD setting is obtained at the band center and reused at the upper and lower edge. Although at the band edges more third-order nonlinearity is visible, this is allowed by the spectral mask (fig. 10.3). Independent DPD iterations could reduce the spectrum to the one seen at the band center.

Band 3 is 27 MHz wide and the DPD setting obtained at the band center could not be reused. Instead, the DPD is executed independently (fig. 10.4). Spikes are seen in the original spectrum. These are caused by strong phase shifts that effectively make the signal discontinuous. The DPD can still provide a very clean spectrum.

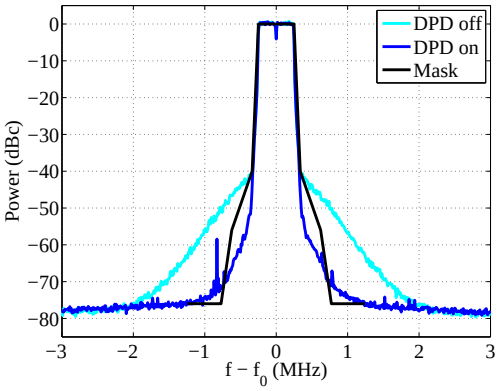
For both bands, the spectral mask is violated. Unfortunately, this is expected as even without the driver amplifier (fig. 8.5) the spectral mask could not be met. However, the chain of driver and power amplifier provides a spectrum that is virtually identical to the spectrum of the power amplifier alone.



(a) 967 MHz (center)

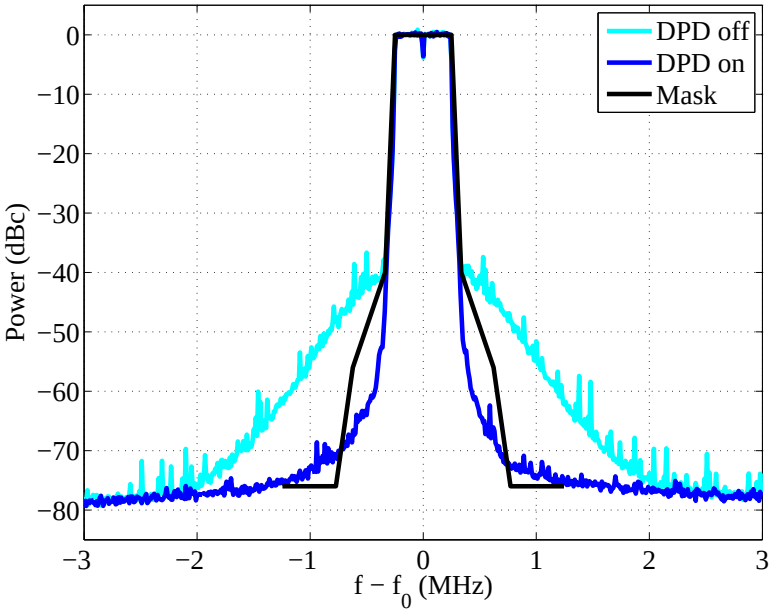


(b) 963.5 MHz (lower edge)

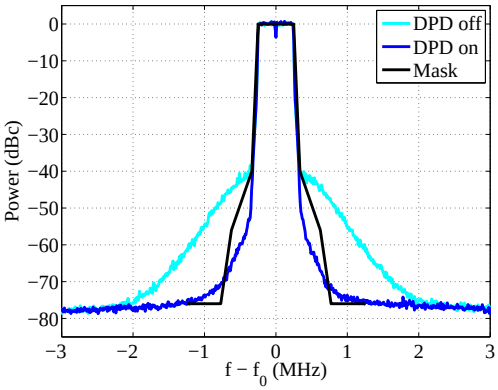


(c) 970.5 MHz (upper edge)

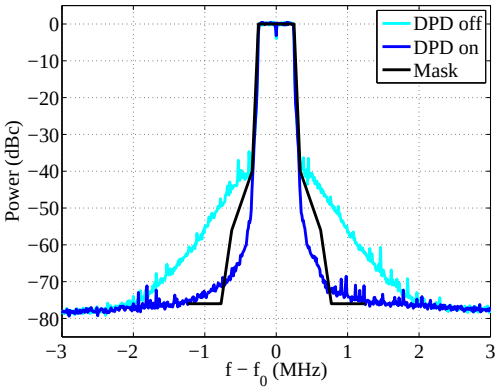
Figure 10.3: Results for band 1 (10 kHz RBW)



(a) 1060 MHz (center)



(b) 1048.5 MHz (lower edge)



(c) 1071.5 MHz (upper edge)

Figure 10.4: Results for band 3 (10 kHz RBW)

11 Assembled Transmitter Prototype

Figure 11.1 shows the transmitter prototype assembled in its 19 inch rack-mount case.

Figure 11.1: Populated rack-mount case

Some wiring is missing but all the functional units are included:

- In the back left corner, the two power supply units are seen, the 48–56 V 5 A supply for power amplifier and driver amplifier and the slim 5–5.5 V supply for all other digital and analog parts.
- On the left side, the upconversion PCB is seen (sec. 6.6).
- The right side is occupied by the milled enclosures of the power amplifier (back) and the driver amplifier (front) mounted to the heatsink (chap. 10).
- Two directional couplers are mounted to the heatsink, one for the forward wave (for the DPD) and one for the reflected wave (for detection of a missing output termination). Both signals are processed by the reference receiver whose role was shown in fig. 5.1.
- Between the directional couplers, the vertically-mounted PCB contains DACs to control the gate voltage of driver and power amplifier (built by Michael Zaisberger).

- The PCB on the back in the center is the microcontroller board that is built by Michael Zaisberger.
- The PCB stack contains (bottom to top) the synthesizer (sec. 7.7), the reference receiver and the accompanying filter board built by Michael Zaisberger.
- Almost hidden in the front right corner is a pre-match board built by Reinhard Koeppner. This board may be needed to support the other two frequency bands (bands 2 and 4). It is not used for bands 1 and 3 that are in the scope of this thesis (sec. 5.3).

12 Conclusion

Upconversion path, LO synthesizer, driver, and power amplifier for the L-DACS1 system, that operates around 1 GHz and uses 498 kHz OFDM carriers, were built and the performance was verified by measurements.

In the upconversion path, linearity of the selected single-sideband upconverter Texas Instruments TRF370317 is excellent, exceeding the performance of the the R&S SMBV100A signal generator. A bottleneck in terms of linearity is found in the final gain block (Analog Devices ADL5602), suggesting a replacement with a higher IP3 device (Mini-Circuits HXG-242+) in a future design iteration.

The LO synthesizer uses a high-performance PLL IC (Analog Devices ADF4106), two narrow-band low-noise VCOs (Crystek CVCO55CL series) that are switched depending on the sub-band. The synthesizer satisfies the requirements both in terms of phase noise and switchover time.

For the driver and power amplifier, Freescale 50 V LDMOS RF transistors are used. The power amplifier delivers the full output power required by L-DACS1 in addition to a 0.5 dBm system margin, giving 53.5 dBm $\hat{=}$ 234 W peak output power. It is linearized using digital predistortion (DPD), improving the shoulder distance by 30 dB and virtually eliminating 3^{rd}-order intermodulation. The DPD is implemented in Matlab, additionally an algorithm suitable for real-time implementation in an FPGA is presented. The algorithm is verified in a Matlab simulation (using integer variables) to provide equivalent results. Despite the linearity improvement, the -76 dBc edge (that does not take 5^{th} and higher-order distortion into consideration) of the spectral mask is violated by about 5 dB. As even directly measuring the output spectrum of a state-of-the-art signal generator fulfills the spectral mask only tightly at the -76 dBc edge, the requirement must be considered to be indeed at the very edge of feasibility.

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