DISSERTATION

Ultra-Thin InAlN/AlN Barrier Enhancement-Mode High Electron Mobility Transistors

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It is meant to answer a few questions but raise many more

Abstract

For the last two decades, significant and rapid advances in the growth and technology of III-N related semiconductors have yielded exciting performance for optical and electronic devices. Laser diodes from green to ultra-violet and light-emitting diodes based on gallium nitride and related wide band materials are already in mass production. Electron devices have shown outstanding results by high electron mobility transistors (HEMTs) utilizing the strong polarization from the III-N wurzite crystal structure. The excellent electronic properties such as high electric field strength due to the large bandgap, high saturation and overshoot electron velocity, and good thermal conductivity, make GaN-based transistors ideal for high power, high speed, and high temperature applications in harsh environments. In order to improve the efficiency, circuit design and safety of today's power amplifiers and converters, HEMTs with high current density, low on-state resistance, high breakdown voltage, operation in enhancement mode (E-mode, normally-off), and reliable surface passivation to minimize electron trapping are highly desired.

The main subject of this work is the design and realization of a high electron mobility transistor with a barrier thickness (2 nm) much below conventional devices, attaining enhancement-mode operation. The thinnest stress-free barrier could be realized using lattice-matched InAlN on GaN. The usual trade-off in enhancement-mode devices between the on-resistance and the threshold voltage has been extended by developing a novel passivation scheme using a highly doped GaN cap layer together with a selective recess process for the gate. This cap layer provides a state-of-the-art carrier density in the access region and shields the device channel from charge variations at the surface. This unique independency of surface traps was proven to be free of drain current dispersion without additional passivation, promising excellent device reliability. Another important design parameter for enhancement-mode devices is the surface potential of the barrier layer. Due to the lack of exact measurement methods of the surface potential, new characterization techniques have been developed allowing the investigation of the effective potential at Schottky and metal-oxide gates. Integration of those results led to an improved design of the ultra-thin barrier device with gate insulation, achieving a threshold voltage above +2V and a maximum feasible gate bias of 10V.

The thin barrier allows detailed analysis of the gate stack, which led to the discovery of a gate sinking effect for GaN devices. This effect was linked to diffusion of oxygen from an interfacial layer into the iridium gate metal and could be utilized to fabricate devices with record transconductance of 640 mS/mm for GaN HEMTs in normally-off operation.

Zusammenfassung

Die rasante Entwicklung von III-N Halbleitern während der letzten zwei Jahrzehnte begründet sich durch in die drastischen Erfolge in der Herstellung von optischen und elektrischen Bauteilen auf diesem Materialsystem. Laserdioden vom grünen bis zum ultravioletten Spektralbereich sowie Leuchtdioden (LEDs) haben bereits ihre Tauglichkeit für die Massenproduktion bewiesen. Im Bereich der elektronischen Bauteile überzeugt der High-Electron Mobility Transistor (HEMT) mit außerordentlichen Leistungen dank der starken Polarisation des Wurzitkristalls von III-N Materialien. Die hohe elektrische Durchbruchsfestigkeit, die große Bandlücke, sowie die hohe Sättigungsgeschwindigkeit der Elektronen und gute Wärmeleitfähigkeit versprechen gute Anwendbarkeit von GaN Bauteilen im Hochleistungs-, Hochfrequenz- und Hochtemperaturbereich. Für die Verbesserung der Effizienz und der Sicherheit moderner Leistungsverstärker bzw. -konverter sind Bauteile mit hohen Stromdichten, niedrigen Durchlasswiderständen, hohen Durchbruchsspannungen und zuverlässigen Oberflächenpassivierungen erwünscht. Besonders gesucht sind dabei Transistoren die sich ohne Schaltspannung am Gate im ausgeschalteten Zustand befinden (Anreicherungstyp, normally-off, enhancement-mode).

Der Hauptteil dieser Arbeit beschäftigt sich mit der Entwicklung und Fertigung von GaN Transistoren (HEMT) mit sehr dünnen Barrierendicken (2 nm), welche eine positive Schwellspannung möglich machen. Die Barriere besteht dabei aus InAlN, welches bei entsprechendem Indiumanteil die gleiche Gitterkonstante besitzt wie GaN und daher zu keinen Verspannungen im Bauteil führt. Der übliche Kompromiss zwischen Durchlasswiderstand und Schwellspannung konnte durch die Entwicklung einer hoch dotierten GaN Schicht über der Barriere und dem dazu notwenigem Ätzprozess für den Gatefuß erweitert werden. Diese Schicht dient nicht nur dazu, den Elektronenkanal hochleitend zu machen, sondern schirmt ihn auch vor äußeren elektrischen Einflüssen ab. Aufgrund der Unabhängigkeit von Oberflächenzuständen zeigt der Kanalstrom dieses Bauelementes keinerlei Dispersionseffekte und verspricht daher ausgezeichnete Zuverlässigkeit. Ein weiterer wichtiger Parameter für das Design von GaN Transistoren mit positiven Schwellspannungen ist das Oberflächenpotential der Barriere. Da in der Praxis keine exakten Messmethoden am bestehenden Bauteil existieren, wurden im Rahmen dieser Arbeit neue Wege zur Charakterisierung entwickelt. Diese können dazu verwendet werden, das Oberflächenpotential unter dem Gate und an der Grenzfläche zu Oxiden zu berechnen. Durch die Anwendung dieser Methoden konnte das oben beschriebene Design durch zusätzliche Isolationsschichten des Gates verbessert werden, wodurch Vorwärtsspannungen am Gate bis zu 10 V ermöglicht wurden.

Die Möglichkeit der präzisen Herstellung dieser 2 nm dünnen Barrieren ermöglichte weiters die genaue Analyse der parasitären Gatekapazitäten. Dadurch wurde der Ef-

fekt des “Gate Sinkings” entdeckt, welcher in ähnlicher Form bereits von GaAs Bauelementen bekannt ist. Durch elektrische und materialtechnische Untersuchungen wurde herausgefunden, dass sich zwischen Gatemetall und Barriere eine Sauerstoffhaltige Zwischenschicht bildete, welche bei höheren Temperaturen in das Gatemetall hineindiffundiert. Durch Ausnutzung dieses Effektes konnte die bis dahin höchste je gemessene Steilheit von 640 mS/mm bei GaN Transistoren mit positiven Schwellspannungen erreicht werden.

Contents

1 Introduction

Energy has become the number one issue in our society triggering new political and economical conflicts and processes. Increasing population and the ongoing request for market growth in order to increase or sustain social wealth has driven us into higher energy production and created new challenges for our local and global environment. Several alternative energy production solutions have been developed but are currently often too expensive or not sufficient to achieve significant market relevance and therefore sometimes have been replaced by conservative methods [1]. In addition to new methods for power generation, a lot of research and development has been done to increasing the efficiency along the whole power supply chain including the production, distribution, transformation, and the power conversion in consumer products. This issue has become very dominant as today's total energy efficiency, concerning the released energy from burning gas or the potential energy of water in comparison to the final service provided at the consumer, as extracted light or heated water, is typically below 10% [2].

The majority of today's electronic applications uses semiconductor devices replacing conventional electronic parts due to their improvement in complexity and capacity [3]. On one hand, these new technologies led to smaller, faster, and more energy efficient solutions. On the other hand, the increase of modern services in information technology caused also a rise of the total power consumption. Therefore, the efficiency of semiconductor devices has an enormous impact on the amount of required energy.

A very promising group of materials for this challenge are nitride-based wide bandgap semiconductors. The market penetration of high power nitride-based light-emitting diodes (LEDs) has been only the beginning of new electronic devices increasing the energy efficiency compared to conventional ones. The benefits of a larger bandgap are twofold [4, 5]. First, the increasing gap between the conduction band, filled with holes, and the valence band, filled with electrons, allows emission of photons with higher energy. Thus, blue, green, and even ultra-violet (UV) light sources (LEDs and laser diodes LDs) could be demonstrated [6, 7, 8, 9, 10, 11, 12]. Second, wide band semiconductors provide high electric strength as their bandgap is comparable to insulators [13, 14]. Hence, smaller devices with higher power density can be realized enabling higher frequencies and reducing losses compared to conventional semiconductors.

Latter case, which will be discussed further in chapter 2, has triggered a lot of efforts

to design highly efficient power devices for low and high frequency applications. One of the promising radio frequency (RF) applications for GaN-based devices will be in base stations for wireless communication [15, 16, 17, 18, 19, 20]. Achieving higher efficiency in combination with thermally robust devices should permit the reduction of cooling efforts and thus reduce energy consumption and costs twofold. Frequency performance above 100 GHz has been demonstrated for applications in radar systems mainly designed for military purposes [21, 22]. The main target application for lower frequency classes is the conversion of electrical power. New energy concepts as smart grid systems [23] require frequent transformation between energy distribution systems, energy storage systems and consumers. Even though conversion efficiencies above 96% are already standard, multiply transformations required for alternative energy sources as off shore wind generators reduce the overall performance. Therefore, gallium nitride based devices capable of high efficient and high temperature stable power electronics are needed as part of an efficient energy solution.

Nitride-based materials include indium nitride (InN), gallium nitride (GaN), aluminum nitride (AlN), and their ternary and quaternary compounds [24]. Sequential two-dimensional growth of those materials allows a great freedom in the design of semiconductor devices. Similar to other III-V material systems based on arsenides, phosphides, and antimonide, two-dimensional electron gases can be achieved in III-N heterostructures. This allows the implementation of high electron mobility transistors (HEMTs) with enhanced mobilities and improved device characteristic by quantum confinement of the electrons compared to bulk structures.

While most results were shown on AlGaN/GaN barrier devices, InAlN/GaN based HEMTs have demonstrated high power and high temperature performance recently, constituting a new class of devices with even higher electron densities. However, high performance has been demonstrated only for normally-on transistors, which are not suitable for switching applications. In case of a failure, normally-on transistors open the channel providing a minimum resistance between source and drain which causes a short circuit. Therefore, normally-off or enhancement-mode (E-mode) devices are required to provide fail-safe operation.

The main part of this work is dedicated to the demonstration of a novel enhancement-mode device structure using an ultra-thin barrier layer. Scaling the device barrier down to only 2 nm revealed new insight into the technology and physics of such devices. In addition, the design includes a new concept to reduce RF dispersion, which is still an important technological challenge in InAlN-barrier devices, by applying a surface cap on top of the barrier. The design is therefore suitable for RF and switching power applications. The impact of this cap on the device has been modeled and investigated.

Furthermore, a novel measurement technique analyzing the effective Schottky barrier height in a heterostructure Schottky gate was developed. Thus, detailed investigations

of the electric potential at the gate are possible which is crucial for the design of normally-off devices. In cooperation with Prof. Kohn's group from Ulm University, an earlier proposed device technique was used to characterize the charge injection into surface passivation layers under long-time stress conditions leading to time delayed degradation and breakdown of the device.

Outline of the Thesis

After a brief motivation in the introduction, chapter 2 summarizes the key aspects of wide bandgap semiconductors with a few more details on III-nitride based materials including a discussion on the novel InAlN. This material has been investigated primarily as alternative barrier layer replacing the conventional AlGaN. Chapter 3 reviews the basic device physics and technological background necessary to understand the experimental chapters of this work. The presented content is seen as an impulse to the interested reader rather than a complete review. In addition, this part shows some general contributions from this work in the technology and characterization of GaN HEMT devices at the Vienna University of Technology. The main results of this work are summed up in the chapters 4 to 8. All experimental results include references to the fabricated substrate material listed in appendix A.

Chapter 4 presents two individual characterization methods which have been developed within the frame of this work and are closely related to the investigated device topics. In 4.1 an alternative Schottky barrier height method by capacitive measurement is shown. 4.2 reviews dual gated HEMT devices applied for device reliability measurements related to the surface passivation. Chapter 5 is dedicated to dry etching techniques on InAlN surfaces and focuses mainly on the recess technology of the ultra-thin barrier device. The electrical results, physical models and simulation as well as application based variations of this novel normally-off design are presented in chapter 6. Furthermore, chapter 7 explains a gate sinking effect which was discovered on the same device due to the large capacitance of the ultra-thin barrier layer. Finally, a few project ideas which have been discussed and partially investigated within the frame of this work are summarized in chapter 8.

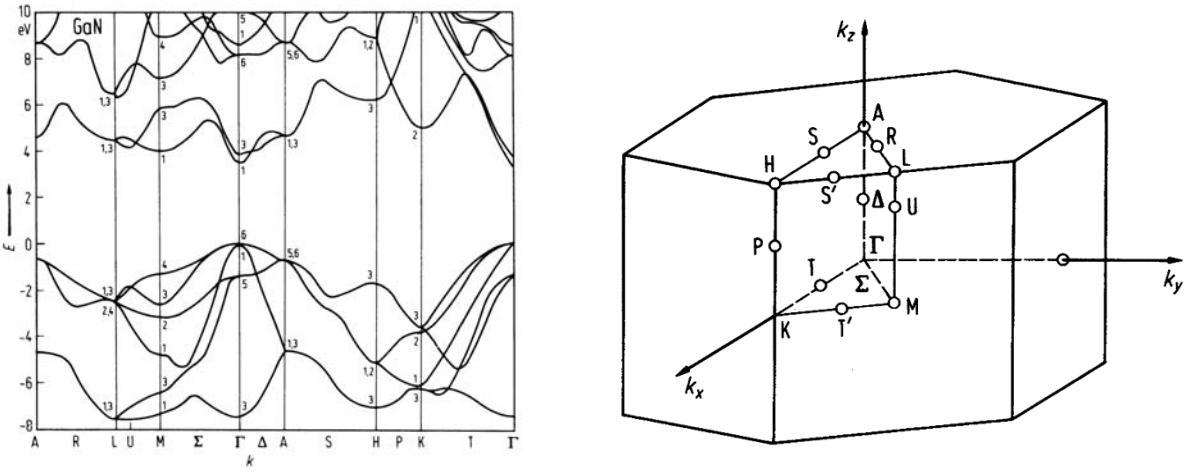
2 III-N Electron Devices

Some of the successful demonstrators of GaN devices have been already mentioned in the introduction. The following parts will briefly review the physical aspects of III-N materials in respect to other semiconductors with special focus on the recent developments in InAlN barrier devices. Further readings with supplemental information about wide bandgap semiconductors can be found in [25, 4, 26, 27, 5].

2.1 Wide Bandgap Electronics

In contrast to metals, the Fermi level in semiconductors lies within an energetic gap without electronic states. Charge transport is therefore only possible by electrons in the conduction band or holes in the valence band. This splitting of the bands originates from bonding and anti-bonding states of the semiconductor material [28]. Most semiconductors of interest consist of a wurzite, zinc blende (diamond), or rock salt crystal structure. Depending on the semiconductor lattice, the position and width of the bandgap differs. Therefore, different semiconductor materials provide fundamentally different electric properties for electrons and holes with regards to their lattice structure, atoms, binding mechanism, and other aspects. Figure 2.1 shows the fundamental bands of wurzite GaN in different lattice directions. The minimum gap between conduction band and valence band determines the relevant bandgap for electrons and holes including their transport properties [28]. The bandgap for GaN with zinc blende lattice structure is slightly smaller. Its symmetric structure causes a non-polar lattice, which is of interest in optical applications. However, due to the growth difficulties of this metastable phase most efforts have been done on the hexagonal configuration.

The potential of certain semiconductor materials can be judged by theoretical criteria combined in so called figure of merits. Johnson defined such a parameter (JFOM = Johnson's Figure of Merit) in respect to the power-frequency product [30] taking into account the bandgap energy E_G and saturation velocity v_{sat}. Another figure of merit (KFOM) was specified by Keyes et al. which includes the thermal limitation in addition to the switching performance of the transistors [31]. Therein, the thermal conductivity κ, the dielectric constant ε_r, and v_{sat} are considered. Table 2.1 summarizes



(a) (b)

Figure 2.1: Band structure (a) of conduction and valence band in wurzite GaN based on theoretical calulcations [29]. Fig. (b) shows the crystal directions of figure (a) based on the unit lattice cell.

some important electrical parameters of a few intensively investigated wide bandgap semiconductor materials in comparison to conventional ones as silicon or GaAs. It can be noted that diamond provides the largest bandgap and therefore also a high critical electric field for breakdown E_B in addition to an extremely good thermal conductivity κ. Gallium arsenide is the material with the highest mobility µ. However, the saturation velocity is slightly above the value for silicon. Further the low breakdown strength in GaAs makes it a less applicable candidate for high power applications. SiC and GaN (hcp, hexagonal close-packed) are the intermediate candidates between GaAs and diamond, providing a large bandgap >3 eV, higher mobilities and saturation velocities compared to silicon and better thermal conductivity than GaAs.

Applying the electrical parameters from table 2.1 in order to derive the figure of merits for high power applications reveals the comparison listed in table 2.2. As expected diamond exceeds others by far. The apparent advantage of GaN to SiC regarding JFOM almost vanishes if the drop of the velocity saturation at high field (shown in brackets in tab. 2.1) is taken into account. On the other hand the lower outcome of GaN from KFOM due to the reduced thermal conductivity κ is also less relevant as GaN is commonly grown on foreign substrates including SiC [34] and diamond [35]. The theoretical thermal conductivity was found to be comparable to SiC [33]. However, defects, doping and oxygen impurities reduces the heat transport in epitaxially grown layers below 2 W/cmK [36, 37]. Higher values were only shown for bulk GaN layers [38].

Even though, diamond has clear benefits from a material aspect, it has not yet achieved

	E_G [eV]	µ [cm^2/Vs]	κ[W/cmK]	E_B[MV/cm]	v_{sat} [10^7 cm/s]	ε_r
Si	1.12	1400	1.3	0.3	1	11.9
GaAs	1.4	8500	0.55	0.55	1.2	10.9
4H-SiC	3.3	900	4.9	3	2	9.7
6H-SiC	3	400	4.9	3	2	9.7
GaN (hcp)	3.4	2000	4.1 (1.3)	5	2.7 (1.3)	8.9
Diamond	5.5	2200	20	5.6	2.7	5.7

Table 2.1: Electrical parameters of several important semiconductor materials at room temperature (300K). Values in bracket correspond to measured results deviating from theoretically predicted values. [32, 33].

	JFOM	KFOM
Si	1	1
GaAs	5	0.5
4H-SiC	400	5.3
6H-SiC	400	5.3
GaN (hcp)	1736	1.6
Diamond	2540	25.3

Table 2.2: Comparison of semiconductor materials after Johnson's and Keyes' figures of merits [30, 31].

comparable device results [39]. One of the causes of wide bandgaps in semiconductors is the increased binding energy caused by decreasing atomic radius, leading to advanced challenges in the technologies of such materials. Consequently, higher bandgaps often involve increasing complexity in growth of the bulk material and the understanding of atomic surface behavior [40]. Therefore, the maturity of the technologies for such materials needs to be taken into account in addition to the results in table 2.2. The development of silicon technology has been strongly pushed by the early success of semiconductors and the fact that the native oxide on silicon provides an excellent controllable and stable interface. While diamond has been intensively studied in the early 90's, it was soon surpassed by activities on GaN with high expectations of new efficient lighting sources based on III-N LEDs. This rapid start on nitride activities has caused a wide understanding of this material which also benefited the development of electric devices. Today's activities are concentrated in cost effective solutions to be competitive with conventional devices in silicon and silicon carbide.

2.2 Benefits and Challenges of III-N Materials

The group III-N semiconductor materials with wurzite lattice as shown in figure 2.2 consist of the binary materials GaN, AlN, and InN, the ternary alloys AlGaN, InGaN, and InAlN (blue lines), and the quaternary InAlGaN (grey area). Most electron devices based on III-N materials consist of a relaxed GaN buffer layer (chapter 3). Therefore, the lattice mismatch of any other layer needs to be considered in respect to GaN. Strongly non-relaxed layers can only be grown up to a certain thickness - the critical thickness. Even though stress in AlN on GaN produces a very inhomogeneous layer for thicknesses >1 nm [41], recently thicker layers without cracking have been demonstrated using in-situ SiN passivation [42]. Reducing the aluminum content to around 20% in AlGaN layers allows growing crack-free layers on GaN exceeding 30 nm. InAlN with an indium ratio of 17% can be grown lattice-matched to GaN [43]. Therefore, the vertical red line in figure 2.2 indicates all quaternary compounds with the same lattice constant as GaN.

The ideal wurzite structure consists of symmetrical tetrahedrons of equal side length and equal angles. However, the wurzite configuration of III-N is distorted due to the strong ionic bonding caused by the metal-nitrogen bond [24]. Nitrogen has a small atomic radius and a high electron negativity causing a shift of the charge center away from the metal. Among III-N materials, this shift is highest for AlN and smallest for InN. The crystal structure for the two possible orientations can be found in figure 2.3.

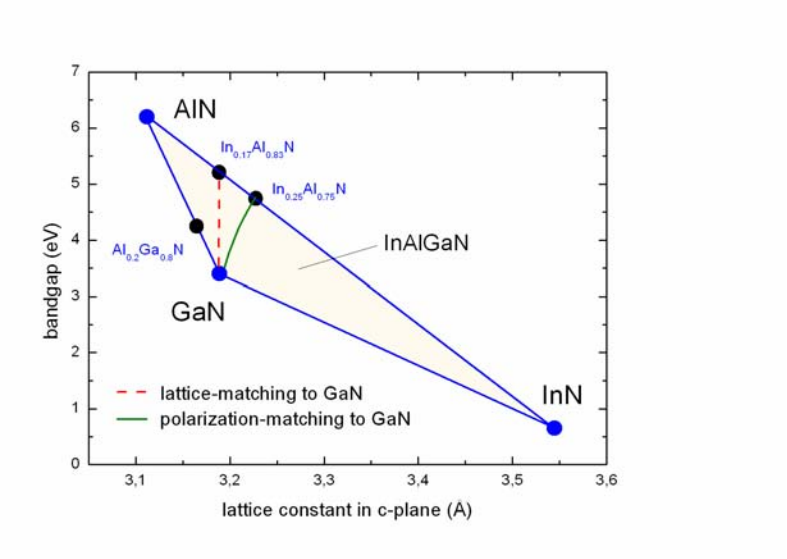


Figure 2.2: Bandgap versus lattice constant of III-N semiconductors. The lines regarding ternary compounds do not consider the bowing factor. [44, 45, 24].

The main orientation that is used is along the [0001] direction, which corresponds to the vertical axis in figure 2.1b. The corresponding [0001] plane perpendicular to its direction is also referred to as c-plane following the notation of the lattice constants. The distorted wurzite lattice modifies the triple bonding structure of the tetrahedron in the horizontal c-plane (Fig. 2.3) in contrast to the vertical direction. Therefore the rotational symmetry in the [0001] plane sustains, causing zero net polarization. However, the distortion in [0001] direction results in a dipole moment throughout the whole lattice. This effect occurs without any external impact. Hence, it is called spontaneous polarization. It was found, that the dipole moments in III-N materials are up to ten times larger than in conventional III-V and II-IV compound semiconductors, except ZnO, where comparable values have been reported [46]. Due to the lattice orientation, the polarization in Ga-face and N-face lattices is reversed (Fig. 2.3) [24].

When external mechanical stress is applied, the polarization effect can be increased or decreased depending on the direction of the stress. This effect is called piezoelectric polarization, and is found when heterostructures with different lattice constants are grown subsequently without stress relaxation. In electronic devices, this effect can be utilized to increase the total polarization, consisting of the spontaneous and the piezoelectric polarization, in order to achieve higher electron densities (chapter 3) as in AlGaN/GaN heterostructures. Alternatively, the total polarization can be reduced, by reversing the stress. Growing heterostructures of materials with compositions along

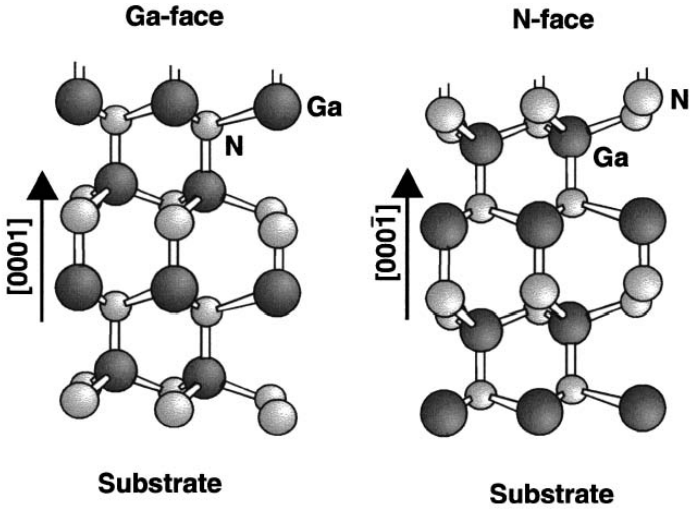


Figure 2.3: Wurzite structure of GaN in Ga-face and N-face polarity. [47, 48].

the green line in figure 2.2, results in polarization-matched layers. The lattice stress therein caused by increasing indium content compensates the spontaneous polarization. Recently, it has been demonstrated, that such structures can be used to achieve normally-off devices [44]. However, the quality of indium-rich layers is strongly reduced as high stress is required to balance out the spontaneous polarization.

Growing heterostructures with materials of different bandgaps allows a lot of freedom in the design of complex electronic and optoelectronic devices, enabling i.e. terahertz emission in quantum cascade lasers [49] far below the bandgap energy. However, the strong electric polarization causes a distortion of the wells and barriers by the induced electric field. This field originates from interface charges induced by the terminated polarization at any boundary of a material layer. The induced electric field separates the charges within quantum wells and can lead to a significant reduction in the efficiency of optoelectronic structures. The polarization effects can be eliminated by growing on non-polar orientations of hexagonal III-nitride crystals [50, 51]. In electron devices, however, the two-dimensional charge layer formed by the polarization induced field is utilized to create strong confined channels with high electron mobilities.

2.3 InAlN - an alternative Barrier Material

The first experiments on lattice-matched InAlN (referring to GaN) have been performed by Kubato et al. in 1989 revealing a smaller bandgap than GaN [43]. Combining lattice-matched heterostructures allows growing thick layers without introducing stress. The high aluminum content (83%) in lattice-matched (LM) InAlN causes a higher polarization compared to conventional AlGaN barriers with typical <30% aluminum

[45, 52]. Consequently, the lattice-matched InAlN/GaN heterostructure offers a few advantages. Any described InAlN in this thesis is therefore lattice-matched with an indium/aluminum ratio of about 17/83.

Early experiments have shown that the critical thickness to form a two-dimensional electron gas (2DEG) in InAlN/GaN heterostructures is around 10 nm [45, 41, 53]. Thinning down the barrier compared to conventional AlGaN HEMTs with a typical barrier thickness above 20 nm allows shortening the gate to channel distance (chapter 3). This is very important in short-channel devices, where it has been shown that short-channel effects become dominant for gate lengths shorter than 15 times the gate-to-channel distance [54]. Hence, reducing the barrier thickness by more than a half compared to AlGaN device enables shorter gate lengths. The maximum frequency of a device is limited by the carrier transit time across the gate [55]. Therefore, shorter gate lengths allows higher frequency performances.

In frequency ranges up to 10 GHz, the gate length is not as much of an issue as for frequencies above. Therefore, the question arises whether a thinner barrier would actually lead to a better performance. So far reasonable InAlN/GaN devices have been demonstrated with current densities between 1 and 2 A/mm and corresponding breakdown voltages of 100 to 50 V, respectively [56, 57, 58, 59, 60]. These devices demonstrated a maximum output power above 10 W/mm at 4 GHz and prove a first technological step but still do not equalize or exceed the performance achievements shown on AlGaN barrier HEMTs [61]. There, breakdown voltages above 1000 V have been demonstrated on RF devices using electric field plates on the drain side of the gate [62, 63, 64, 65]. But even without field plates, breakdown voltages of 400 V have been demonstrated. In order to achieve such performance with InAlN devices, a surface passivation with sufficient high critical electric field is required, which also allows reliable large signal operation at radio frequencies.

The biggest advantage of InAlN that could clearly be demonstrated so far is the extreme robustness against harsh environments. In 2006, it was shown that devices with InAlN barriers are feasible to operate at 1000°C in vacuum [66]. Later on, Maier et al. found out that the damage in devices operated for many hours at 700 and 800°C was caused only by the degradation of the metals while the heterostructure did not reveal any damage [67, 68]. New metal schemes have been proposed [69] allowing overgrowth of fully fabricated devices with nano-crystalline diamond [70, 71]. Thus, even higher robustness against corrosion can be achieved. In addition, the excellent heat conductivity of diamond allows spreading the heat created in the device directly from its surface to a larger heat sink.

The first enhancement-mode device on InAlN barrier HEMTs was demonstrated by implantation of fluorine into the barrier [72]. Authors argued that negative charges in the barrier were the cause of the increase of the threshold voltage, similarly as it has

been shown on AlGaN devices [73]. However, the electric characteristic of such devices was proven to be not very reliable. In 2010, a high performing recess HEMT has been demonstrated achieving 2.4 A/mm with a barrier layer of 3 to 4 nm [74]. The device achieved a record transconductance but exhibited a slightly negative threshold voltage. Recently, thermal oxidation of a 6 nm AlN barrier produced a positive threshold voltage even though the current density decreased drastically compared to its original value before oxidation [42].

In 2006 a new mechanism of device degradation was proposed by Joh et al. [75, 76, 77]. Authors reported on a field induced, non-recoverable damage caused by reversed gate bias. Further studies revealed that this effect seemed to correlate with the preexisting mechanical stress in the barrier. Reverse biasing of the gate increases the stress due to inverse-piezoelectric forces until the mechanical stress creates defects and electrical traps responsible for increasing gate leakage [77, 78]. However, it remains controversial, whether this effect applies only to highly stressed barriers as i.e. in high aluminum content AlGaN [79]. A comparative study on lattice-matched InAlN has demonstrated the absence of piezo-inverse degradation for such devices.[80].

3 Device Physics and Basic Technology

The provided topics presented in this chapter should offer the knowledge foundation for the following experimental chapters. As there exists already a large number of excellent books [81, 82, 83] on those issues, the topics are only briefly introduced.

3.1 Basic Model of GaN HEMTs

The general model of a field-effect transistor (FET) consists of a capacitively coupled gate electrode which controls the carriers in the channel flowing from source to drain (Fig. 3.1). Therefore it is important to insulate the gate in order to minimize parasitic current through the gate. In metal-oxide-semiconductor (MOS) FETs the gate is isolated by an oxide layer. Alternatively, the gate electrode can be implemented with a Schottky barrier providing a metal-semiconductor structure which is called MESFET. The Schottky barrier provides a good insulation in reverse direction but needs to be operated carefully under forward bias. While MOSFETs build up the basis for silicon devices due to the high quality oxide interface achievable with silicon oxide, different approaches are often chosen for compound semiconductor devices. Using a higher bandgap material as barrier in combination with a lower bandgap material for the channel is the basic idea of heterojunction FETs (HFETs). The gate contact can be realized either by a Schottky contact similar to MESFETs or with an additional oxide layer (MOS-HFET). Since the barrier in a HFETs is a semiconductor itself, it can be doped. The bandgap discontinuity between the higher conduction band in the barrier and the lower one in the channel causes a depletion of the barrier layer and provides free carriers in the channel. These carriers form a high density layer at the interface, which is called the two-dimensional electron or hole gas (2DEG/2DHG). The latter refers to the analog case in the valence band. As the realization of hole channels is feasible but requires more technological challenges, most devices in GaN include an electron channel. The separation of dopants and free carriers in addition to the high carrier density reducing the Debye length [55] minimizes the scattering of electrons and allows higher mobilities above typical conduction band mobilities in bulk layers. Such devices

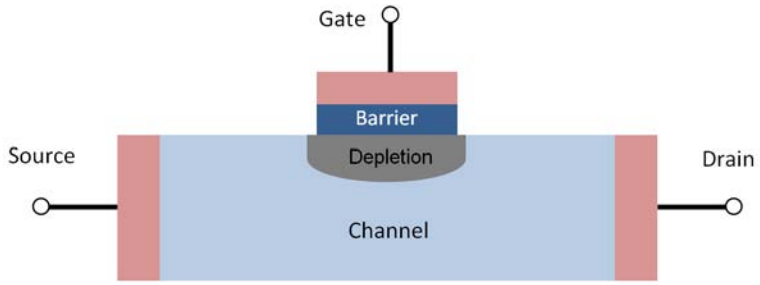
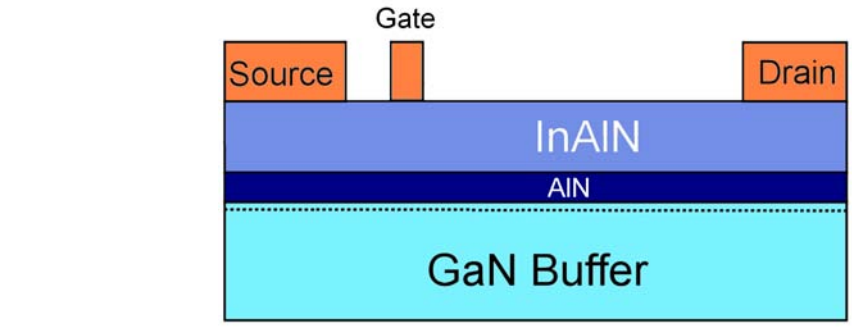


Figure 3.1: Basic structure of a field-effect transistor with source, drain and gate electrode.

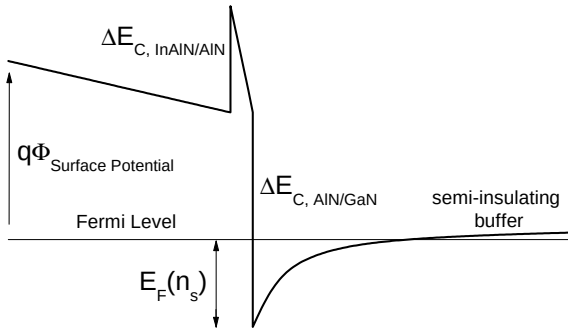
are therefore also named high electron mobility transistors (HEMTs), even though in the most relevant high electric field applications for GaN-based devices, the electron velocity is limited by the saturation velocity ν_s. In GaAs or InP devices the doping in the barrier can be increased until a separate channel in the barrier is formed. Thus the electron density is limited by the bandgap discontinuity [83].

A typical GaN-based HEMT with corresponding conduction band structure and charge distribution diagram is shown in figure 3.2. In contrast to the schematic FET in figure 3.1, the channel in the heterostructure FET is confined below the barrier while the buffer itself is not conducting. The barrier consists of an InAlN/AlN heterostructure. Even though the source and drain contacts are placed on top of the barrier, reasonable ohmic contacts to the channel layer can be achieved.

FETs based on wurzite-type GaN in [0001] direction (c-plane) exhibit a polarization which causes a large potential drop over the barrier (Fig. 3.2b). This potential drop allows achieving higher electron concentrations in the channel compared to conventional doping of the barrier layer. Enlarging the barrier thickness increases the potential at the free surface. It was found that surface donors are responsible for pinning the surface at a fixed surface potential [84]. The ionized donors create a positive surface charge density $n_{Surface}$ which counters the free carriers in the channel n_s. Consequently, no channel would form considering an ideal surface without ionized surface donors until the potential drop across the barrier causes a 2DHG at the surface. The charge diagram in figure 3.2c shows the negative fixed charge density $n_{pol,Surface} = \sigma_{pol,Surface}/q$ at the surface formed by the spontaneous and piezoelectric polarization P of the barrier. The positive fixed interface charge density at the 2DEG $n_{pol,Interface} = \sigma_{pol,Interface}/q = -[\![P]\!]/q$ depends on the difference in spontaneous polarization between the barrier and the buffer and the piezoelectric polarization of the barrier. The latter component



(a)



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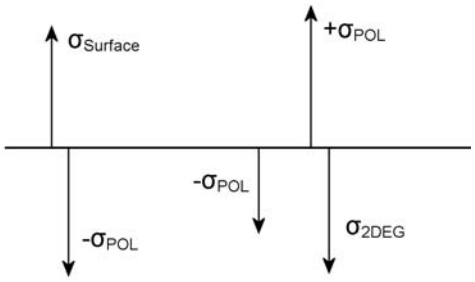


(c)

Figure 3.2: Schematic of epitaxial structure (a) of a typical GaN-based HEMT with an InAlN barrier and an AlN spacer including gate, source and drain metal electrodes. Band structure (b) and charge diagram (c) refer to a vertical cut through the device stack with a free surface.

depends on the stress in the barrier given by the difference in the lattice constant between the buffer and the barrier layer [48, 47, 85]. The charge balance across the barrier without the additional AlN interlayer can be written as

$$n_{Surface} + n_{pol,Surface} = n_{pol,Interface} - n_s, \tag{3.1}$$

Considering such a pinned surface allows defining the 2DEG density n_s by [86]

$$n_s = n_{pol,Interface} - \frac{\varepsilon_{Barrier}}{d_{Barrier} \cdot q} \left(\Phi_{SP} + \frac{E_F(n_s)}{q} - \frac{\Delta E_{C,Barrier/GaN}}{q} \right), \tag{3.2}$$

where $\varepsilon_{Barrier}$ and $d_{Barrier}$ is the dielectric contant and thickness of the barrier, Φ_{SP} is the surface potential of the free surface being equal to the Schottky barrier height (SBH) Φ_{SB} at the gate contact, $E_F(n_s)$ is the energy difference between the conduction band at the bottom of the 2DEG and the Fermi level, $\triangle E_C$ is the bandgap discontinuity between barrier and channel, and q is the elementary charge of an electron (Fig. 3.2). For simplicity, equation 3.2 corresponds to the homogenous barrier without AlN spacer in contrast to figure 3.2.

The threshold voltage, defined for the case of zero charge in the 2DEG below the gate ($n_s = 0$), can be calculated setting equation 3.2 zero and considering the gate electrode using $\Phi_{SP} = \Phi_{SB} - V_{Gate}$:

$$V_{Th} = V_{Gate}\,(n_s = 0) = \Phi_{SB} - \frac{\Delta E_C}{q} - \frac{q \cdot n_{pol,Interface}}{C_{Barrier}} = V_{bi} - \frac{q \cdot n_{pol,Interface}}{C_{Barrier}}, \tag{3.3}$$

where $C_{Barrier}$ is the barrier capacitance and $E_F(n_s) = 0$ for $n_s = 0$. The build-in voltage V_{bi} of the total gate contact is defined by material parameters. The threshold voltage depends therefore mainly on the 2DEG charge and the barrier capacitance. Taking into account the high polarization charge in GaN devices, a surface potential of around 1 eV, and typical barrier thicknesses >10 nm, reveals a threshold voltage $V_{Th} < 0$. From a technological point of view either the surface potential $\Phi_{SP} = \Phi_{SB}$ or the barrier capacitance can be modified. Therefore, for a given surface potential, the gate capacitance needs to fulfill the following condition in order to achieve a normally-off (enhancement-mode, E-mode) device with $V_{Th} > 0$:

$$C_{Barrier} > \frac{q \cdot n_{pol,Interface}}{\Phi_{SB} - \frac{\Delta E_C}{q}}. \tag{3.4}$$

Applying the described charge model, one can specify the source-drain current in the

transistor using the gradual channel approximation by the Schottky model [55]

$$I_{DS} = \mu C_{Gate} \frac{W_G}{L_G} \times \left(V_{DS} \left(V_G - V_{Th} \right) - \frac{V_{DS}^2}{2} \right), \tag{3.5}$$

which leads to a quadratic tendency on the gate bias in drain current saturation

$$I_{DS} = \mu C_{Gate} \frac{W_G}{L_G} \times \frac{\left(V_G - V_{Th} \right)^2}{2}. \tag{3.6}$$

Therein, I_{DS} is the source-drain current, V_{DS} the corresponding voltage, C_{Gate} the gate capacitance (basically equal to $C_{Barrier}$ in case of a HEMT), μ the electron mobility, and W_G and L_G are the gate width and length, respectively. However, this equation is only valid for electron velocities $\nu < \nu_s = \mu E_c$, where ν_s is the saturation velocity and E_c the corresponding critical field in the channel. E_c can be estimated macroscopically by the critical voltage $V_c = E_c L_G$. The mobility in GaN-based HEMT devices is usually above $1000 Vs/cm^2$ and hence the electron velocity reaches saturation for even small biases. In examples, electrons in a 1 µm long gate channel reach the saturation velocity at about 1.3 V. A first approximation of the velocity saturation can be achieved by a two-piece model [81], assuming a linear increase of the electron velocity until the electric field in the channel reaches E_c. Using this approach, the following expression was found [81]

$$I_{DS} = \mu C_{Gate} \frac{W_G}{L_G} \times V_c^2 \left[\sqrt{1 + \frac{(V_G - V_{Th})^2}{V_c^2}} - 1 \right]. \tag{3.7}$$

This equation be simplified using the approximation $V_G - V_{Th} > V_c$

$$I_{DS} \approx C_{Gate} W_G \times \left(V_G - V_{Th} - V_c \right) \nu_s. \tag{3.8}$$

It shows that the transfer characteristic is linearly dependend on V_G due to the velocity saturation in contrast to long-channel transistors. This is also indicated by current-voltage (IV) measurements of typical devices showing a linear transfer characteristic above 1 V.

3.2 Device Targets for Power HEMTs

The material parameters from chapter 2 already suggest a strong focus on power applications for GaN-based devices. Therefore two major branches exist: high frequency

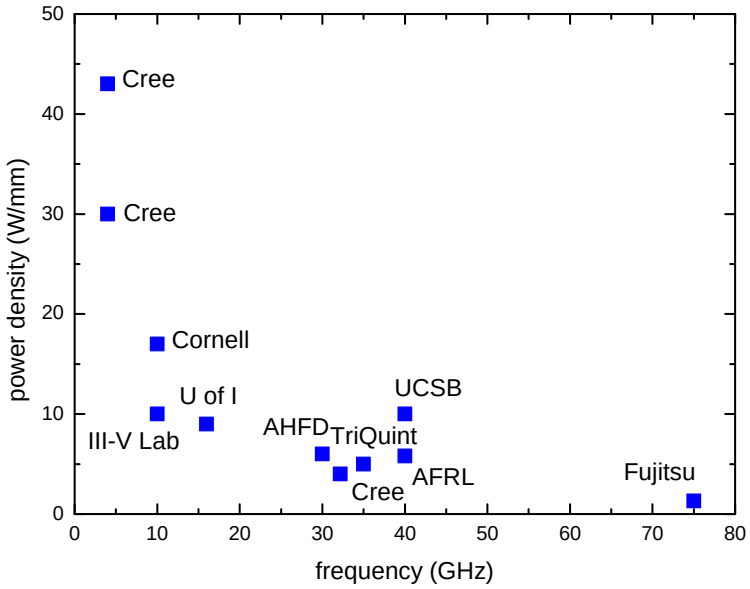


Figure 3.3: Summary of state-of-the-art RF power HEMTs [87, 88, 61, 57].

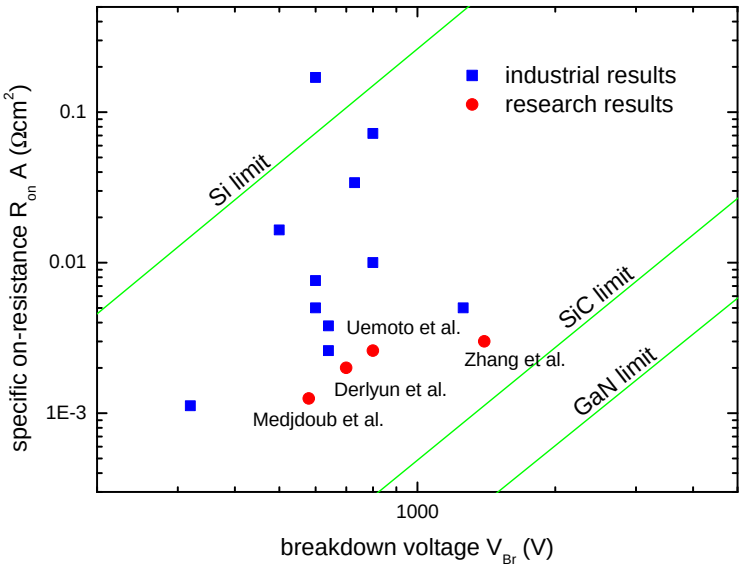


Figure 3.4: Comparison between on-resistance and breakdown voltage for recent results on GaN-based power switches [89, 90, 91, 42, 92].

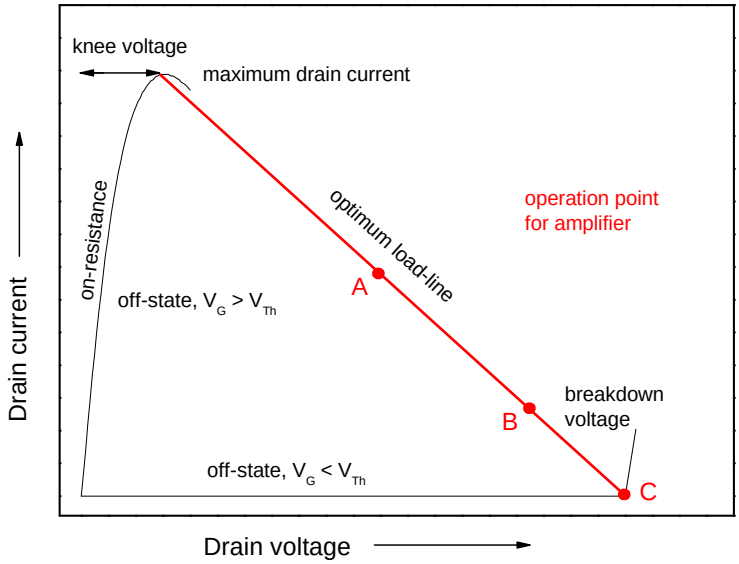


Figure 3.5: Important parameters in the output characteristic of a power transistor with load-line for class A, B, and C amplifiers [93].

and high voltage power operation. High frequency power amplifiers typically start from around 1 GHz concerning wireless communication up to above 100 GHz covering all kinds of radar bands. A comparison between frequency and RF power for state-of-the-art GaN-based devices [87, 88, 61, 57] is shown in figure 3.3. High voltage switches for power supply applications are settled at frequencies up to 1 MHz with switching voltages ranging from 100 V to 2 kV. A few recent results on power switching devices [89, 90, 91, 42, 92] are summarized in figure 3.4 showing that the physical limit of SiC (Tab. 2.1) has been almost reached by gallium nitride transistors. Even though several differences exist in the design and concept of power amplifiers and power switches, both are aiming for better efficiencies and higher thermal robustness using GaN in order to achieve higher output power.

Figure 3.5 summarizes fundamental aspects of a power transistor. It should provide a large drain voltage and current swing in order to provide a maximum output power across the load line. Thus a low knee voltage V_{Knee}, a high breakdown voltage $V_{Breakdown}$, and a high maximum drain current $I_{D,max}$ are desired. In order to maximize the drain current, the sheet carrier density in the 2DEG and the electron saturation velocity needs to be increased. Therefore, high total polarization in the barrier and

low surface potentials are preferred. Increasing of the polarization can be achieved by increasing the tensile strain in the barrier until the channel mobility degrades by increasing interface roughness. The knee voltage is linked directly to the on-resistance in the linear part of the output characteristics. It depends therefore on the contact metal resistance, the ohmic contact resistance and the resistance in the source and drain access region. Achieving high breakdown voltages includes aspects of the buffer, the substrate, and the surface passivation [64, 94, 91, 95, 96]. For a class A amplifier the maximum output power is

$$P_{out} = \frac{V_{Breakdown} - V_{Knee}}{8} I_{D,max}, \tag{3.9}$$

with an maximum efficiency P_{out}/P_{DC} of 50%. Low efficiencies caused by high electric losses require therefore large efforts on the thermal management for such devices. Modifications on the load-line in order to achieve class B or C amplifiers [93] (Fig. 3.5) for higher efficiencies involve a decline of the linearity of the amplification. Higher harmonics degrade the spectral bandwidth of a communication channel and therefore must be limited. An improved result can be achieved with a switch-mode amplifier (class S) [93]. This amplifier uses a pulse width modulation conversion of the analog signal which is than amplified by a switch-mode amplifier not requiring linearity. The analog signal can be recovered by a low-pass filter. While the efficiency of the power amplification is achieving a maximum in this configuration, the overall circuit reaches about 70% efficiency, due to the losses to higher spectral components [97].

3.3 Dispersion Effects

Dispersion of the drain current between RF and DC operation has been one of the major issues since the start of the development of GaN FETs. The dispersion causes an increase (walkout) of the knee voltage and a reduction of the maximum drain current. According to chapter 3.2, those effects reduce the maximum output power twofold. Therefore dispersion needs to be limited in the frequency range of the target application.

The origin of the RF dispersion was found to be donor-like traps at the surface [84]. It was described, in part 3.1, that the 2DEG in thin barrier structures originates from the surface donors. Without ionized surface donors the channel would not contain any free carriers due to charge neutrality of the polarization charges. The surface donors donate electrons to the structure, which are accumulated in the channel. The compensation charge at the surface is therefore required in order to have a 2DEG. During device operation electrons with sufficient thermal or electrical energy can be injected into traps in the buffer, barrier, surface or at any interface. If the device is operating in

off-state ($V_G < V_{th}$, Fig. 3.5), a high electric field builds up at the drain-side of the gate electrode. This electric field can lower the potential barrier between gate and surface causing electron injection into donor states at the surface [84]. The neutralized donors reduce the electron density in the channel. In on-state ($V_G > V_{th}$, Fig. 3.5), the applied bias causes much lower or even reversed electric field at the surface reducing the number of trapped electrons. However, if the time constant of this trap emission mechanism is too low in comparison to the modulation frequency, the electrons cannot be fully removed from their trapped state. Thus, the trapped electrons are causing a virtual gate, which is acting as a current limiter comparable to the regular gate electrode. If the trapped charge density is small enough the effect can be seen only from an increase of the device on-resistance (Fig. 3.6). Once the density of trapped electrons exceeds the charge density at the gate at maximum forward bias, the dispersion effect reduces the maximum output drain current. The combination of the virtual gate and the actual gate electrode can simply be described as two transistors acting as two serial current sources. The current source with the lower output current dominates. Figure 3.6 shows an analytical calculation [98] of such a dual gated transistor, demonstrating gate and virtual gate, using a two-piece [81] approximation for the electron velocity. The grey lines correspond to the output characteristic of the regular gate without any limitation from the second electrode (virtual gate). The additional red curves represent the maximum drain current at maximum bias at the regular gate with decreasing bias on the virtual gate causing the apparent drop of the drain current and increase of the on-resistance.

Several concepts of surface passivation have shown excellent results for the suppression of drain current dispersion. Deposition of dielectrics can passivate the surface bonds which are causing electrical states within the surface bandgap. However, since the surface charges are needed in order to establish the 2DEG, an ideal passivation of the surface would lead to an increase of the surface potential and a depletion of the channel. Therefore, counter charges are needed in the passivation layer or on top of it to sustain the 2DEG. A thick passivation layer can increase the barrier for injected electrons and hence reduce the accessibility for electrons to be trapped. Further ideas on how to measure the electron injection can be found in chapter 4.2.

As stated before, RF dispersion needs to be suppressed in the frequency range of the specific application. A power amplifier working for wireless communication should operate in the range of 1 to 3 GHz. Hence, traps much faster than this can be neglected. An absolute verification, if the device is able to work at the required frequency can be done by load pull measurements. This method alters the output impedance in order to test the large signal response of a device for a certain load line (Fig. 3.5). The

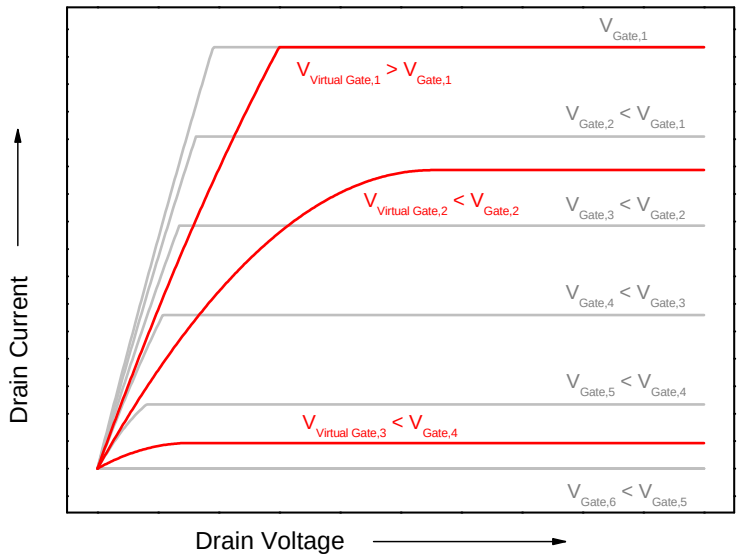


Figure 3.6: Simulation of drain current in dependency of gate voltage and virtual gate potential. The qualitative potential value of the gate and the virtual gate correspond to comparable gate geometries. If the bias V is replaced by the surface potential Φ, the figure becomes generally valid for all kinds of device structures. The grey curves represent the case without virtual gate. The red curves show the maximum drain current for the highest gate bias and decreasing virtual gate potential. The simulation was performed using an analytical dual gate model [98].

sweep across the load line includes biasing of the devices in off-state and on-state. The resulting output power is therefore a direct measure of the device performance. In addition, the actual dynamic load line can be measured, giving a clear indication whether the device is capable of reaching the maximum drain current from DC measurements [59]. Any current limitation by a virtual gate is therefore easy to detect. An alternative and faster way is to measure the output characteristic in pulsed mode. Such method is typically used to separate the self-induced heating effects in devices. Pulsing the gate with 100 ns long pulses from off-state to on-state allows investigating traps in frequency ranges up to 10 MHz. Since most relevant traps are known to be in this spectral range a quite good estimation can be achieved. However, if only the gate is pulsed, the device does not operate along the load-line with a lower drain bias in off-state. The measurement can simply be improved by increasing the drain voltage or pulsing gate and drain simultaneously. First one is however limited by the on-state breakdown which is typically lower compared to the off-state in compound semiconductors [99]. Another method to investigate surface traps is done by large signal load line measurements at frequencies in the MHz range. Increasing the drain bias for a fixed load allows sweeping through the output characteristic and investigate the time constant for electron trapping [84]. Due to electron injection, the decrease of the drain current at higher drain voltage is expected be faster. Alternatively, any of the above measurements can be included in long time stress tests in order to see a degradation of the passivation scheme. An approach that combines long time stress tests with detection of injected charges in the passivation layer is presented in chapter 4.2.

Finally, also capacitive-voltage (CV) measurements should be discussed in this context. They have been proven to be very effective in order to gain in-depth understanding of the oxide-semiconductor interface in silicon technology [100]. However, the adaptability of CV methods for wide bandgap semiconductors is limited due to larger time constants for deep traps. Additionally, electrons trapped at the barrier-insulator interface cannot be modulated by the gate potential and are therefore invisible in most characterization techniques. Furthermore, capture and emission time from the 2-terminal CV characterization does not correspond to the injection of electrons by the horizontal electric field under 3-terminal measurements.

3.4 Device Technology

The following part reviews some important aspects of the technology of InAlN barrier devices. General information as well as personal experience from this work is presented. However, due to the wide range of this topic, the focus is primarily set on new developments rather than basics, which can be found elsewhere [101, 102].

	available size (dev.)	lattice mismatch	thermal mismatch	dislocation density $[cm^{-2}]$	thermal cond. [W/cmK]
Si (111)	12" (18")	-16.9%	60%	10^{11}	1.3
Sapphire	4" (6")	16.1%	-34.4%	10^{9}	0.41
6H-SiC	4" (6")	3.3%	25%	10^{9}	4.9
Bulk-GaN	2"	-	-	$10^{4} - 10^{6}$	2.5
Diamond (s.c.)	<1"	11.8%	-21.6%	n.a.	20

Table 3.1: Comparison between typical used substrates for epitaxial growth of GaN at room temperature [103, 104, 38, 99, 89].

Epitaxial structures based on GaN are typically grown on different kinds of substrates by metal-organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE) due to the absence of bulk GaN substrates with reasonable prize and size. Commonly used substrates are sapphire, silicon, silicon carbide and recently diamond or composite substrates with diamond interlayer. Table 3.1 compares some important parameters including lattice mismatch and thermal mismatch to GaN, and available size for substrates used for GaN epitaxy. Silicon is the cheapest among all substrates but involves the highest lattice mismatch. This requires a transition layer to GaN in order to grow relaxed layers and reduce the defect density. SiC would be the most preferred substrate in terms of lattice constant and offers also a good thermal conductivity. However, to be considered in mass market production requires lower prices and availability of larger wafers. The best candidate in thermal robustness is diamond. Recently, Alomari et al. have demonstrated a HEMT device grown by MBE on single-crystalline (s.c.) diamond [35]. However, the high lattice mismatch and small wafer size makes it only applicable for special market segments. Sapphire has been the ultimate candidate for research activities with its acceptable lattice mismatch and hence controllable growth complexity and lower prize compared to SiC.

Epitaxial growth by MOCVD and MBE are non-equilibrium processes. In an MBE system Ga, Al, In and N are offered by a vapor beam towards a heated substrate in ultra-high vacuum. Nitrogen can be included by NH_3 or from a plasma source cracking N_2. Under suitable conditions, a layer-by-layer deposition is possible, achieving very sharp interfaces between neighboring layers. The growth temperature needs to be balanced between increasing defect density at lower temperatures due to reduced atom mobility at the surface and decomposition of GaN at higher temperatures. In contrast to MBE, MOCVD growth is performed at relatively higher pressures and higher tem-

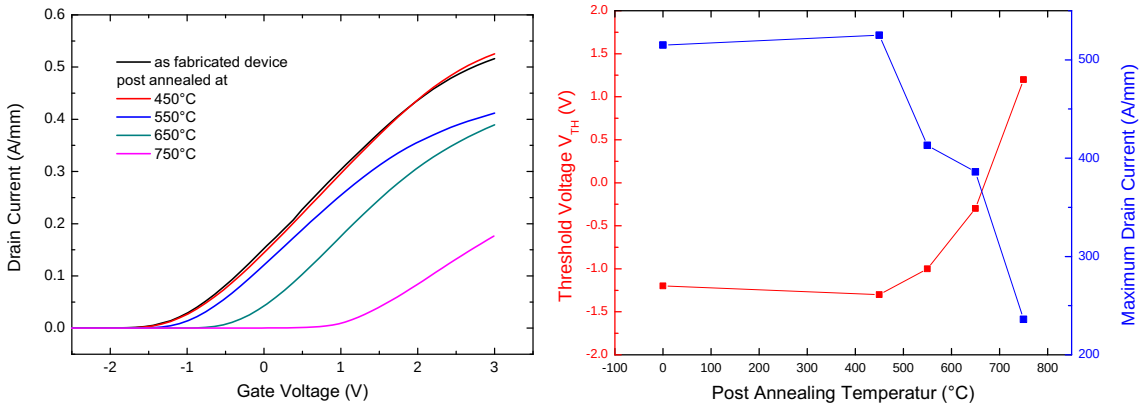
peratures. The metal-organic precursor for GaN is typically trimethylgallium (TMG, $Ga(CH_3)_3$). The challenge in the CVD process is the temperature uniformity across the wafer and the uniform distribution of reactants. The latter is defined by the design of the chamber. Improved performance and higher output capacity made MOCVD currently the method of choice for mass production of GaN epitaxy.

The growth of GaN-based HEMTs starts with a nucleation layer in order to achieve two-dimensional growth. A GaN buffer of about 2 µm is typically used to achieve a reasonable crystal quality for the channel. The buffer needs to be sufficiently insulating, otherwise it causes a parallel channel to the 2DEG. The ideal buffer would be a layer with the Fermi level around mid gap. Such a buffer can be achieved by Fe or C doping [105, 106, 107, 108, 109, 110, 111, 112]. While iron needs to be included into the growth by a separate precursor, carbon is already part of the metal-organic precursors. It has been demonstrated that the incorporation of carbon can be adjusted simply by the growth parameters and is therefore easy to switch on and off. In contrast, Fe doping is more difficult to control due to segregation on the growth surface and therefore requires thick Fe-free GaN layers below the channel [106].

Finally the top heterostructure can be grown. Switching the growth from the GaN buffer to the InAlN barrier requires no remnant gallium on the walls of the MOCVD reactor. This can be achieved by purging it for a few minutes with ammonia without insertion of other precursors. Before the barrier layer is grown, a thin AlN interlayer needs to be inserted which drastically improves the channel interface and hence the mobility [41].

Device isolation is done either by mesa-type recessing of the inter-device area leading to sidewalls which may affect the gate leakage and the device reliability [113]. Therefore industrial manufacturing uses preferred implantation of i.e. Ar to destroy the crystal lattice and create defects [114, 115]. Alternatively, local oxidation has been demonstrated to be very efficient even though only parts of the barrier layer were oxidized. However the induced stress in the neighboring devices may cause additional challenges for device reliability.

Ohmic contacts were formed by electron-beam evaporation of Ti/Al/Ni/Au layers with thicknesses of 30/180/40/50 nm, respectively [116]. The metal stack is annealed at 800°C for 30s. Maier et al. found that long time annealing improved the contact resistance slightly due to enhanced alloying of the metal stack [67]. Therefore the annealing time can be increased. Directly before metal deposition the samples with the ohmic mask layer are put into $HCl:H_2O$ with a ratio of 1:1 to 1:2 at 70°C to 80°C for at least 10 min in order to remove the native surface oxide. Alternatively, an Au-free metal scheme was tested for high temperature stability suggested by Alomari et al. [69]. Au was replaced by 100 nm thick Cu capped with a 20 nm of Ta to prevent oxidation of Cu. The Ta layer, which oxidizes during processing, needs to



(a) (b)

Figure 3.7: Shift of the transfer characteristic (a) influencing the drain current and threshold voltage (b) after post-fabrication annealing of unpassivated HEMTs (wafer AEC 1802, see App. A).

be removed by sputtering after final device processing. The ohmic contact resistance was extracted by the transfer line method (TLM) [55] using a 4 point measurement in order to deduce the variable tip-to-pad resistance. For simple 2 point measurements, the typical measurement error is between 1 to 2 Ω, causing random results as the tip pressure varies for each measurement.

As mentioned in chapter 2, InAlN was found to be stable up to 1000°C in vacuum. However, if the annealing chamber is contaminated with small traces of oxygen or water, the aluminum surface can react to form aluminum oxide. This thin layer can cause a loss of 2DEG electrons in the access region as well as below the Schottky diode. Figure 3.7a shows a series of measurements done on the same device after annealing for 2 min at different temperatures up to 750°C under nitrogen gas after device processing without surface passivation. The summary of the maximum drain current and threshold voltage is shown in figure 3.7b. Above 500°C annealing temperature, the increase of the threshold voltage indicates an increase of the surface potential due to surface oxidation. This thinning by oxidation reduces the potential drop induced by polarization charges across the barrier. However, this explanation was found to be not sufficient to explain the increase of the gate and channel resistance. Consequently, it was found that aluminum oxide thermally grown from InAlN or AlGaN causes an increase of the surface potential Φ_{SP} (chapter 3.1) [117]. Finally, gate metallization is done by Ni/Au, Ir/Au, Pt/Au or Cu/Ta metal stacks.

The complexity of the Schottky/heterostructure gate contact has caused several different models to describe the gate leakage current. Typically, a combination of tunneling and thermal emission is used to model the leakage current. In addition, it was shown

that fixed charges in the passivation beside the drain-side edge of the gate electrode modify the electric field at the gate and therefore strongly influence the device behavior [118]. However, still a lack of understanding exists about the dominating mechanisms and in several reports basic gate leakage current models are applied using a large number of input parameters and allowing non-physical fitting of the electrical behavior [119].

Depending on the device design, samples can be passivated after gate process or before ohmic contact in order to insulate the gate electrode. Oxide deposition before ohmic metallization includes several advantages. First, without any metallization harsh cleaning procedures which attack the metal layers can be applied. Second, if metals are brought into the dielectric deposition chamber, the chamber can be contaminated especially at higher deposition temperatures. Surface passivation was achieved by silicon nitride deposition in a plasma-enhanced chemical vapor deposition (PECVD) at 300°C or with an atomic layer deposition depositing various high-k dielectrics in the temperature range from 100°C to 300°C. The thermal stability of SiN deposited by PECVD is limited due to the mismatch of the thermal expansion coefficient to sapphire. Therefore, only thin layers <100 nm could be deposited if high temperature treatments above 800°C were applied afterwards. Otherwise the SiN layer would crack and partially peel off the surface.

Another process that is commonly applied in microelectronics is plasma ashing. It is a very useful process to remove remnant organics from photo resist mask layers and clean the surface for the next process step. Since surface oxidation is harming the device performance as described above, plasma oxidation could do the same. However, it was found out that plasma ashing using a Faraday cage around the sample does almost not modify the sheet resistance as depicted in figure 3.8. The Faraday cage is usually applied on samples with metallic surface parts in order to prevent sparks. The cage reduces the energy of the ions and hence prevents damage of the surface.

3.5 Characterization Techniques

Evaluation of individual process steps was done by optical and electron microscopy as well as electrical measurements. Final devices were characterized by current-voltage (IV) measurements in DC and pulsed mode. A programmable semiconductor parameter analyzer (Keithley 4200 SCS) was utilized in order to perform long-term stress tests and repeated measurements.

Additionally, capacitive analysis was applied using a standard LCR meter. Capacitance-voltage (CV) measurements [100] provide one of the most powerful tools for electrical device investigations. In contrast to IV measurements, where the figure under investiga-

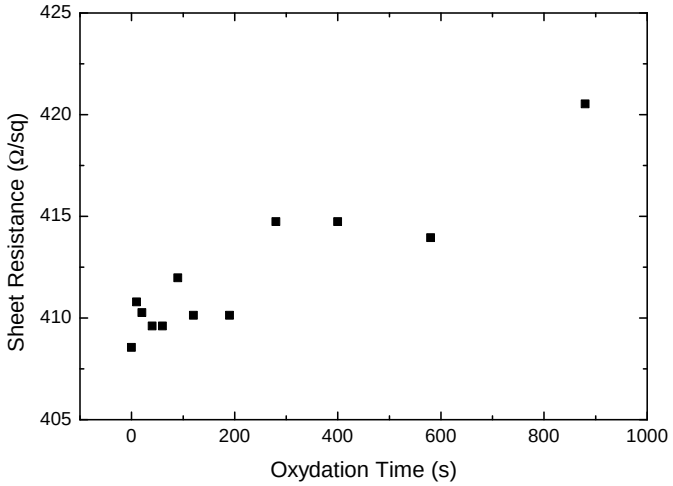


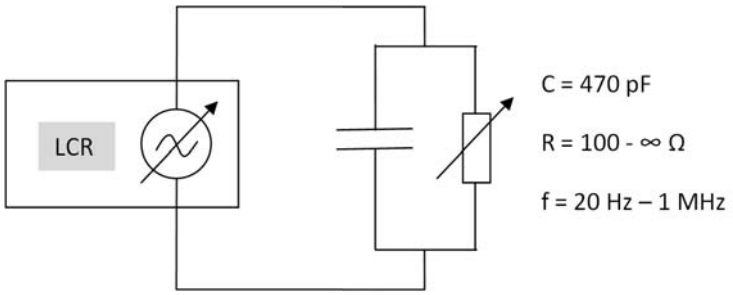
Figure 3.8: Impact of plasma asher with Faraday cage on the sheet resistance of a free InAlN surface (wafer AEC 1802, see App. A).

tion, mostly the drain current, depends on the carrier density times the carrier velocity, CV measurements reveal details on the carrier profile only. Thus it can be used to determine charge concentrations in any part of the structure. A very frequently applied method is therefore the characterization of interface charges at the semiconductor-oxide interface of MOS structures. Those charges can be extracted by comparing measurements with different parameters. Varying the frequency of the measurement allows to investigate traps of different time constant and hence energy position. Comparing measurements with and without above-bandgap light illumination allows measuring the CV with filled or empty interface states. The basic CV curve of the InAlN HEMT is shown in figure 4.3 in addition to the apparent total free carrier density N. The latter can be calculated by the depletion approximation using [55]

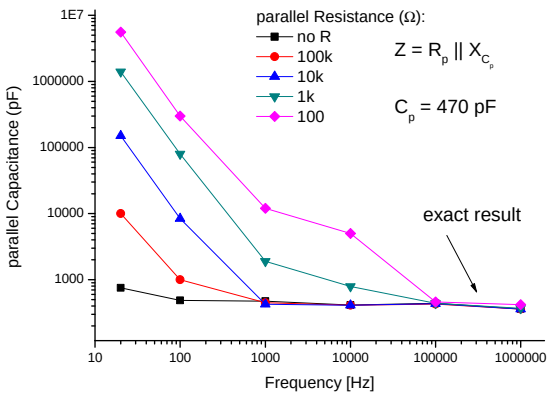
$$N\left(x=\frac{\varepsilon}{C'}\right)=\frac{2}{q\frac{\partial\frac{1}{C'^2}}{\partial V}\varepsilon}. \tag{3.10}$$

C' is the capacitance per area, ε the dielectric constant, V the applied gate voltage, and x the structural depth of the capacitance. Integrating the charge density over the gate voltage or the structure depth and assuming zero charges in the channel for $V_{Gate} < V_{Th}$, allows to calculate the 2DEG density (Fig. 4.3) in the channel.

If the charge density is known, one can also determine the carrier drift mobility. The drain current in the linear regions is determined by the number of charges, depending on the gate voltage, the mobility, and the electric field given by the drain voltage divided



(a)



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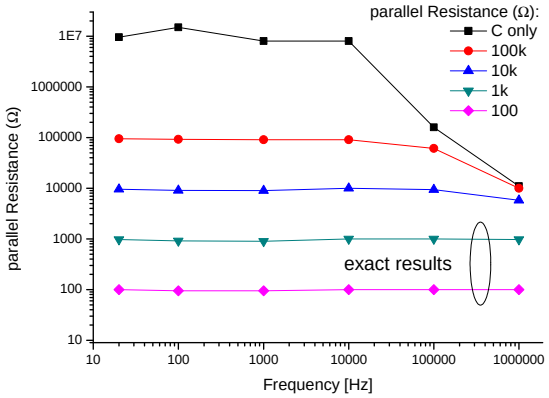


(c)

Figure 3.9: Measurement of given parallel capacitor (470 pF) and resistor (100Ω to 100kΩ) (a) at various frequencies (20 Hz to 1 MHz) investigating the accuracy of the LCR bridge for the parallel capacitance (b) and parallel resistance (c).

by the gate length. Inserting the already known charge density allows to extract the drift mobility at very low drain bias (i.e. V_D= 0.1 V) for different gate biases. An example of such measurements is shown in chapter 5.

The capacitive measurement is usually performed in a bridge circuit to calculate the complex impedance of the connected circuit. Semiconductor devices mostly offer very small dimensions and therefore the measurable capacitance is typically within the pico-Farad range requiring femto-Farad accuracy. Hence, CV meters are usually built up as a 4-point measurement system and require open and short calibration to minimize parasitic effects. The measured impedance can be then transferred into a parallel or serial circuit of a capacitance and resistance. Since the serial resistance can be usually omitted, the parallel model is preferred for most analyses. However, if the measured impedance is comparably small to the serial resistance, one needs to consider a three part model. Since the complex result allows only the extraction of two real components,

one part needs to be determined elsewhere. This can be done by either calculating the serial resistance by its geometrical dimensions and the sheet resistance, or by extracting the constant value of the serial resistance above threshold where the parallel resistance can be neglected. This assumption can only be made if the leakage through the capacitance is not significant. Further, measuring capacitances with parallel leakage requires additional attention towards the accuracy of the results. If one of the two components of a parallel circuit is sufficiently smaller than the other one, the larger part cannot be extracted accurately. It is evident that the error gets larger if the angle α of the complex impedance is close to 0° or 90°. In most cases the capacitance is of interest and therefore the parallel resistance must not be lower than a certain value. Additional adjustments can be done if the correct frequency range is chosen in order to increase or decrease the imaginary part X_C of the impedance. Figure 3.9 summarizes the measurement results of a fixed capacitor of 470 pF parallel to a variable resistor over frequency. The capacitance values become incorrect at low frequency when X_C, the capacitive reactance, is much smaller than the parallel resistance (Fig. 3.9b). In contrast, measuring a large parallel resistance gets an incorrect result for high frequencies when X_C decreases much below its resistive counterpart (Fig. 3.9c). Therefore if measuring capacitances with high parallel leakage, the CV measurement needs to be done at sufficient high frequencies and attention has to be taken to the validity of the result of the parallel resistance.

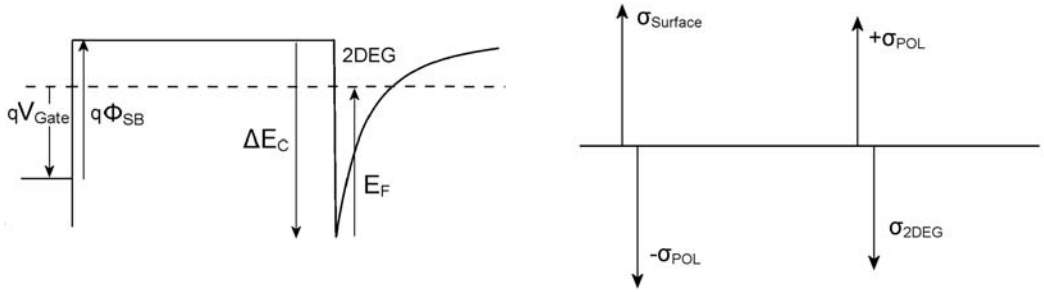
4 Novel Characterization Methods for HEMTs

4.1 Schottky Barrier Height Analysis by CV Method

The gate diode used in standard HEMT devices is generally refered to as Schottky contact, as it consists of a metal gate directly on a semiconductor. Therefore it is common to use the current-voltage model [55] based on thermal emission developed for the Schottky diode in order to describe the gate contact. However, a typical HEMT device (chapter 3.1) consists of a heterostructure barrier which forms a MOS-like bandstructure (Fig. 3.2). Considering i.e. a 10 nm thick InAlN barrier HEMT with an 1 nm thin AlN spacer, the actual Schottky barrier is formed by the depleted InAlN barrier. Hence, several questions raise if such a structure can be seen as a Schottky diode. The following list summarizes some of the important points that need to be considered:

- The thermal emission current is dominated by the highest barrier, which in case of reverse gate bias is the actual surface potential. However, in forward direction this assumption becomes invalid as the surface potential is lower than the barrier of the AlN interlayer.
- The depletion region depends on the barrier thickness and does not depend on the surface potential until electrons overshoot into the barrier.
- Tunneling causes a parallel current transport mechanism. The different barrier structure requires a new model for tunneling.
- The current in GaN HEMT Schottky diodes with passivation is pronounced at the edges due to field distortion by charges inside the passivation and surface state effects.
- Defects such as N vacancies in the barrier allow enhanced charge hopping and trapping inside the barrier. Hence other current mechansims than the Schottky model may dominate and a clear distinction is quite difficult.

Consequently, the current-voltage characteristic of the gate diode includes several parallel effects, which need to be seperated. Applying only the Schottky model for extraction of the Schottky barrier height (surface potential below the gate) may cause huge errors.



(a) (b)

Figure 4.1: Schematic bandstructure (a) and charge diagram (b) of a HEMT at flatband condition.

Alternatively, a different approach to analyze the effective physical Schottky barrier height between the semiconductor barrier and the gate metal is presented. As already described, the current through the barrier is a multi-component parameter and therefore it is difficult to distinguish a certain mechanism. Capacitive analysis can be applied as it neglects the DC current and considers only charges responding to an AC signal on the gate. Thus, a detailed analysis of the structure can be performed which is used for investigation of the barrier. As reference point for this measurement, the flatband voltage for HEMT devices will be defined, similarly to what is known from MOS analysis [55]. The following part will shortly describe the idea of this method, which is then demonstrated on experimental data.

4.1.1 The Flatband Voltage

The flatband voltage used in MOS structures is defined as the gate voltage leading to a flat conduction and flat valence band in the semiconductor, which further causes flat bands in the oxide layer without interface charges. In GaN-based heterostructures, the electric field in neigboring layers is strongly influenced by the polarization charges at the interfaces. Below threshold voltage, the conduction band in the channel layer is flat due to the absence of charges (electrons and dopants) and the electric field in the barrier reaches a maximum. For the descirbed investigation the flatband voltage is defined as gate bias, leading to a flat conduction band in the barrier. In this case, the electric field across the barrier layer is zero. Consequently, the total charges of the surface side and the channel side of the barrier must be both zero, following the charge neutrality from Maxwell's equation. The schematic band structure and charge diagram for a HEMT heterostructure under flatband condition at the barrier is shown in figure 4.1.

The seperated charge neutrality for the channel region allows to assume that the 2DEG density is equal to polarization charges at the interface ($n_s = n_{pol,Interface}$) (see eq. 3.1) as depicted by the charge diagram in figure 4.1b. Therefore the charge equation for a HEMT device including vertical polarization (eq. 3.2) can be reduced to

$$0 = q\Phi_{SB} - qV_{Gate} + E_F(n_s) - \Delta E_C, \tag{4.1}$$

where V_{Gate} becomes the flatband voltage under flatband condition. Therefore the flatband voltage can be written as

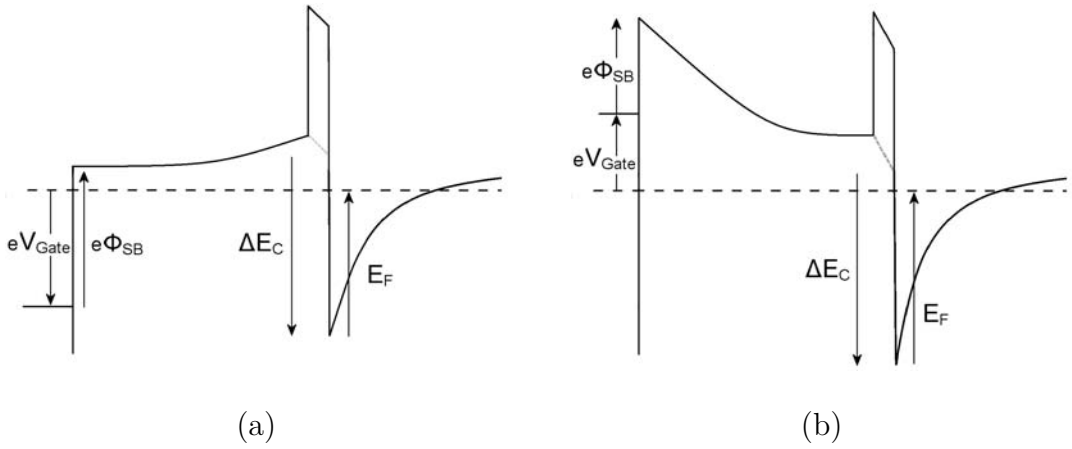
$$V_{Flatband} = \Phi_{SB} + \frac{E_F(n_s)}{q} - \frac{\Delta E_C}{q}. \tag{4.2}$$

This equation can be easily verified by the band diagram in figure 4.1a. Interestingly, it links the Schottky barrier height to the flatband voltage, and therefore allows an alternative method to determine the SBH.

However, the situation gets a little more complicated if the barrier consists of different materials and doping needs to be considered. Figure 4.2 shows two possible flatband conditions for a typical InAlN/AlN barrier. In addition, there exists one more flatband concerning the AlN layer at even lower surface potential. Regarding the flatband in 4.1a, one needs to consider also the potential drop within the InAlN layer. This drop originates from the ionized donors and free electrons in the barrier and can be taken into account by the simulation result. If the flatband voltage from figure 4.2b is used for analysing the SBH, this potential increase at the surface needs to be taken into account (eq. 4.2). For simplicity the following demonstration shows the flatband condition at the surface (Fig. 4.2a) even though the same result would be achieved using the flatband condition at the barrier.

The described flatband conditions suggest that the required surface potential needs to be lower than for the free InAlN surface ($V_{Flatband} \gg 0$). This causes “spill over” of electrons into the barrier and increases also the gate leakage current. However, capacitive measurements allow investigating the electric structure of the barrier even under parallel ohmic current. The results can be compared to a simple model from Poisson-Schrödinger calculations.

Lim et al. have shown a method to measure the Schottky barrier height by using CV measurements [120]. Thereby authors measured the CV characteristics from below threshold voltage until 0 V gate bias and integrated the total charges in the 2DEG. Applying the charge equation for GaN-based HEMTs (eq. 3.2) allows to extract the Schottky barrier height. However, this method assumes a very accurate measurement of the gate capacitance. In reality the characterization of the gate capacitance includes



(a) (b)

Figure 4.2: Flatband condition for a heterobarrier HEMT (Fig. 3.2) with influence of the doping. Flatband conditions can be found (a) at the surface or (b) at the interface to the AlN interlayer.

several challenges. Around the threshold voltage the capacitance cannot be properly detected until the 2DEG forms in order to lower the sheet resistance below the gate. This usually causes an underestimation of the gate capacitance around the device threshold. Further, it has be shown [121, 120] that the gate capacitance does not scale with the diode size proving an inhomogeneous distribution of the electric field which causes further uncertainties in the measurement result. In addition, chapter 7 of this work shows the impact of the serial capacitance at the gate interface, causing another measurement error. In contrast, the proposed method uses only the CV result in accumulation, where the high conductivity of the 2DEG removes the lateral influence of the measurement pattern. Furthermore, it compares only the qualitative shape of the CV curve and hence separates the influence of serial capacitances.

4.1.2 Modeling and Analysis

Diodes were fabricated on MOCVD-grown lattice-matched InAlN on a GaN buffer and sapphire substrate (wafer A 1730, see App. A). Circular patterns were formed by alloyed Ti/Al/Ni/Au contacts and gate contacts with a 15 nm Ir and a 150 nm Au deposition. Capacitance-voltage (CV) characterization was done with an HP4248 LCR meter at room temperature (RT) after short and open calibration measuring the parallel capacitance and resistance of the gate contact (Fig. 4.3a). From the threshold voltage at -5 V to around +1 V the value of the capacitance is dominated by the device barrier and the variable 2DEG capacitance (details can be found in chapter 7.3.2). For $V_{Gate} > 1V$ the capacitance increases due to increasing accumulation of carriers in the barrier layer, which can also be seen from the increase of the total charge extracted

from the CV measurement. The carrier profile is presented in figure 4.3b showing the peak concentration of electrons from the 2DEG between 10 and 13 nm below the surface. The additional peak at 5 nm corresponds to free carriers accumulated at forward bias $V_{Gate} > 1V$. The logarithmic plot of the parallel resistance in figure 4.3c proves a reasonable resistance for $V_{Gate} < 2V$ since it is above 100 Ω. However, beyond $V_{Gate} > 2.5V$ the resistance is too small and the capacitance value may become inaccurate (details can be found in chapter 3.5), which is also shown from the decreasing gradient of the capacitance (Fig. 4.3a).

The simulation was done by simple point by point calculation using a 1D Poisson-Schrödinger solver for different surface potentials. The result of the simulation is shown in comparison to the measured CV in a 1/C plot in figure 4.4. The simulation result is presented for several levels of barrier doping ranging from 1 to $8 \times 10^{19} cm^{-3}$. Any doping below $1 \times 10^{19} cm^{-3}$ reveals a comparable graph as for the lowest doping density and is therefore not shown. The artifacts around 0 V are related to the round off noise from simulations. Figure 4.5 summarizes the increase of the electron density in the barrier and the 2DEG for different doping densities. The total electron density increases steadily with lowered surface potential until a steep increase originating from the electron accumulation in the barrier, while the 2DEG density remains almost constant as the electric field is shielded. Lower doping in the barrier requires a reduced surface potential in order to achieve this electron spill over effect. This behavior can also be seen from the conduction band diagrams in figure 4.6. At the lowest doping level (Fig. 4.6a), it can be noted that the decrease of the surface potential still impacts the potential of the AlN barrier and hence the 2DEG density. This influence decreases for higher doping densities (Fig. 4.6b-d).

The measured CV was fitted to the simulation (Fig. 4.4) in two steps. First the inverse capacitance was shifted downwards as shown in the figure in order to consider any serial capacitive components. Then, the slope of the 1/C graph was fitted to the simulation results. At 0.5 eV the measurement diverges from the fitted simulation curve, which correlates to the increase of the gate leakage at $V_{Gate} > 2V$ in figure 4.3c. Therefore the capacitance becomes inaccurate and should not be considered. The extracted doping density of the barrier is found to be $2.5 \times 10^{19} cm^{-3}$ (Fig. 4.4). The related band diagram in figure 4.6b allows to extract the surface potential Φ_{SP} at the flatband voltage. The bold line marks the conduction band curve at a Φ_{SP} = -0.17 V.

As described before, the flatband voltage can be used to calculate the Schottky barrier height using equation 4.2. The conduction band discontinuity between GaN and InAlN was recently published to be 0.9 eV [123]. The energy gap between the 2DEG and the Fermi level $E_F(n_s)$ was simulated as shown in figure 4.7. For the ideal InAlN/GaN barrier n_s was estimated to be $3 \times 10^{13} cm^{-2}$ [52]. However, the measured CV (Fig.

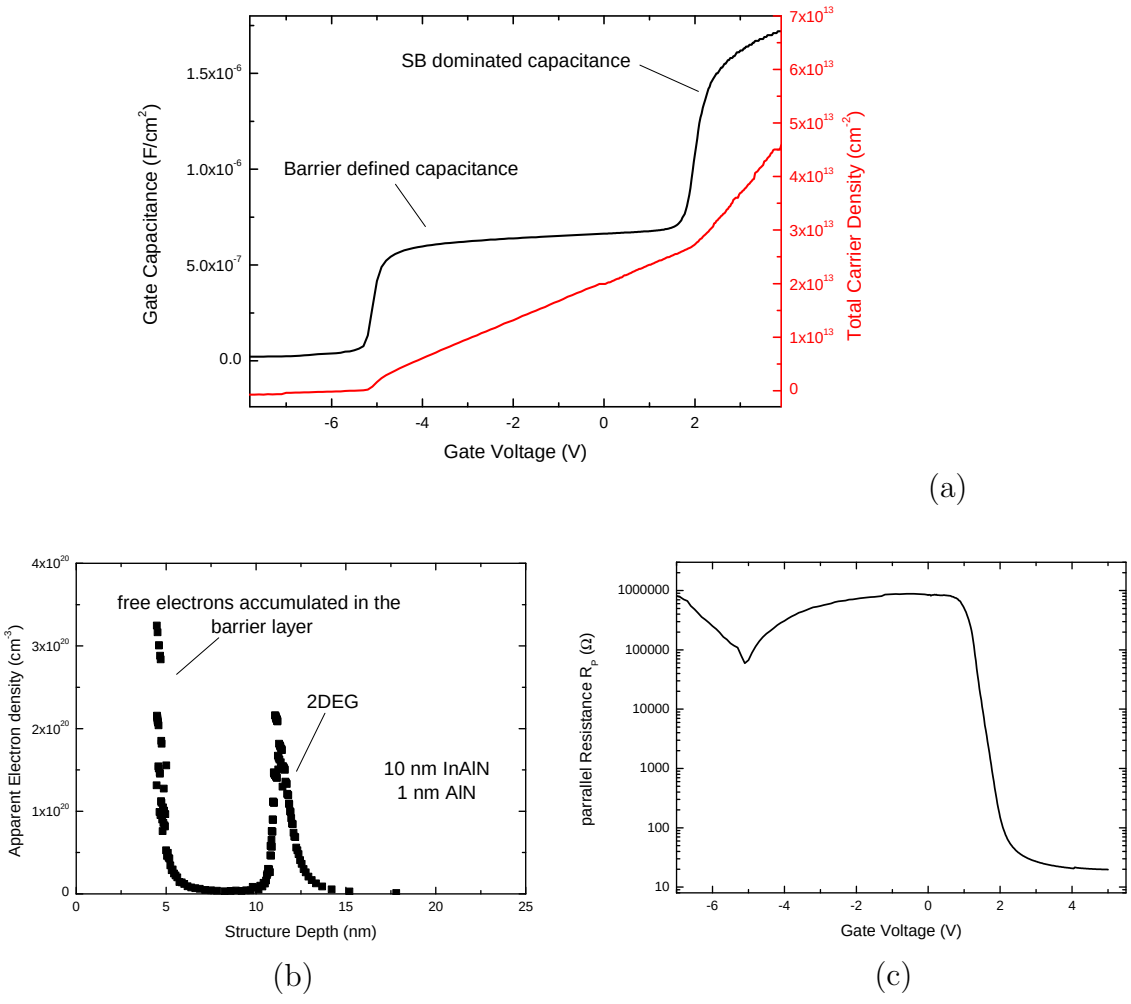


Figure 4.3: CV measurement (a) at RT with extracted total free charge. Fig. (b) shows the apparent free electron density within the heterostructure and (c) presents the parallel resistance of the CV measurement (wafer A 1730, see App. A) [122].

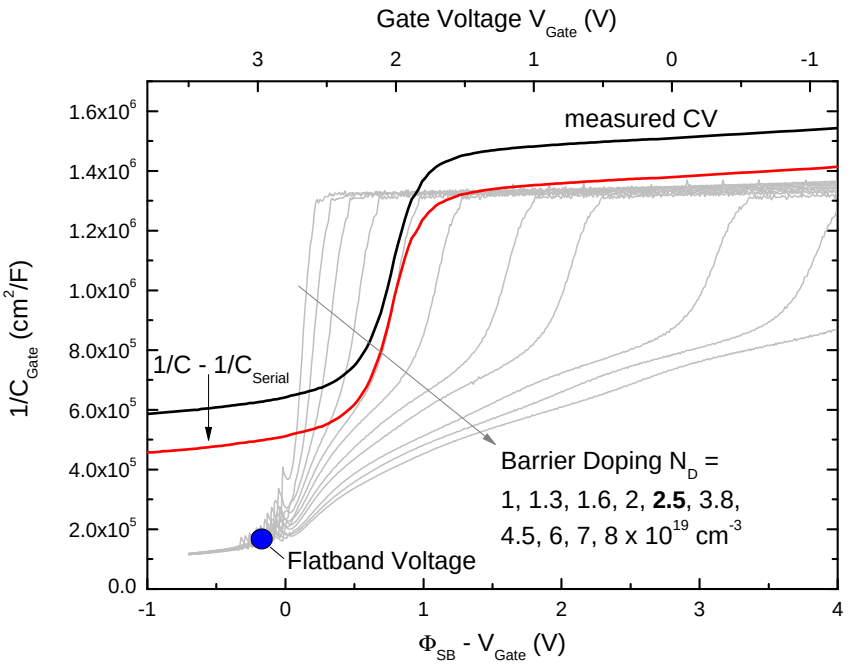


Figure 4.4: Comparison between measurement and simulation of 1/C. The simulated capacitances vary with the barrier doping density. The measured capacitance was fitted to the best matching curve ($N_D = 2.5 \times 10^{19} cm^{-2}$) substracting a serial capacitance. The flatband voltage was extracted from figure 4.6b [122].

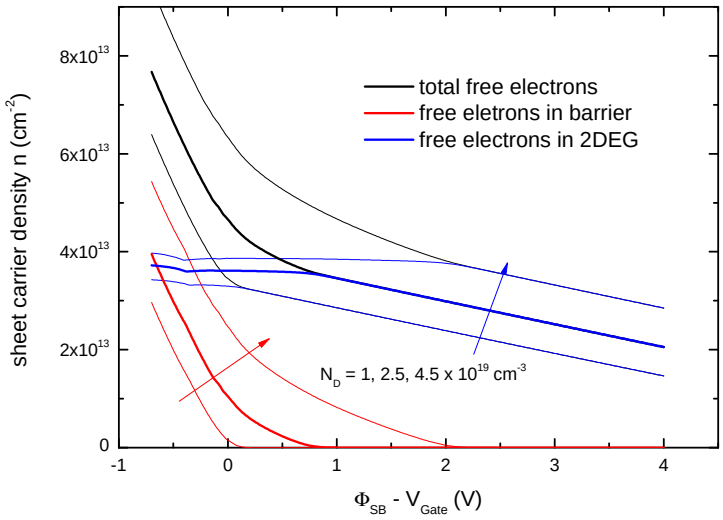


Figure 4.5: Summary of total free carriers and free carriers in the barrier and 2DEG for different barrier doping densities extracted from simulations.

4.3a) indicates that the actual 2DEG density appears to be slightly lower at around $2.6 \times 10^{13} cm^{-2}$. Hence, E_F was simulated to be 0.84 eV as seen in figure 4.7. Instead of simulation, E_F can also be calculated numerically [41, 45].

Inserting the flatband voltage and material parameters in equation 4.2, reveals a final Schottky barrier height of 2.3 eV. In this result, also the potential drop of the charges in the barrier was considered from simulations. In contrast, extracting the SBH from IV measurements using the Schottky model revealed a much lower barrier height of only 0.9 eV. As mentioned before, this value does not represent the physical Schottky barrier height.

In addition, this method has been repeated on several other devices with Ni/Au gates, indicating a SBH of around 1 eV. Therefore it is believed, that the InAlN surface in the presented device using Ir as gate metal was oxidized causing a thin native aluminum oxide layer [124]. This is known to increase the surface potential [117], and hence the apparent Schottky barrier height. Such a structure is called an oxide-assisted Schottky barrier providing reduced leakage current due to the increased barrier height. Therefore, the measured SBH of 2.3 eV does not only relate to the workfunction of the gate metal.

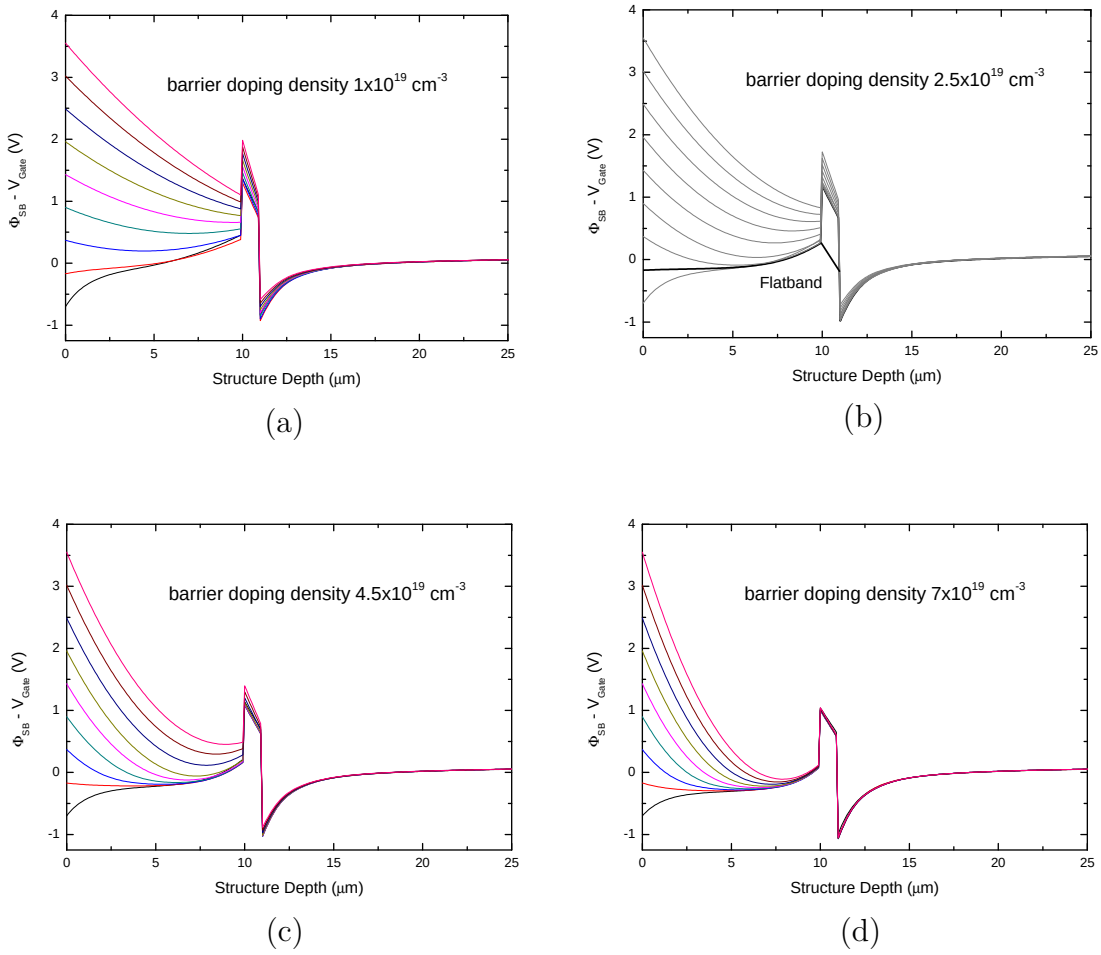


Figure 4.6: Simulation of the conduction band (a-d) in dependence of the surface potential $SP = \Phi_{SB} - V_{Gate}$ for different barrier doping densities [122].

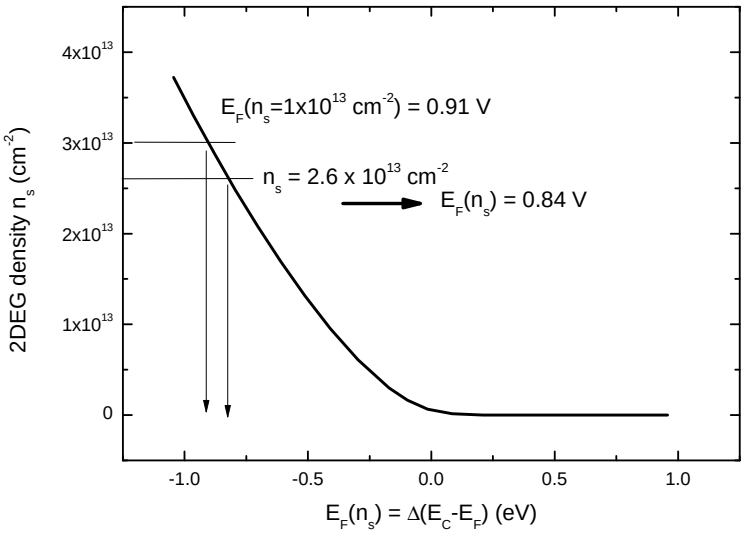


Figure 4.7: Simulated energy difference between the 2DEG conduction band minimum and the Fermi level for different 2DEG densities n_S.

4.1.3 Summary

A novel method has been presented to analyze the near surface behavior of the heterostructure barrier for GaN HEMTs. The gate capacitance was measured under high forward bias close to the flatband condition of the barrier. The accumulation of electrons in the InAlN layer allows to investigate the potential therein and was compared to Poisson-Schrödinger calculations of the band structure. The result indicates a higher SBH for oxide-assisted Ir/Au metal stack on 10 nm thick barrier devices compared to analysis using the standard thermal emission model applied on IV results. Therefore, this method is believed to provide higher accuracy but also more complexity for investigation of the actual SBH. As the SBH is an important factor for designing enhancement-mode devices, it could be an excellent method to investigate the physical SBH of the gate which determinds the threshold voltage of the device.

4.2 Characterization of Charge Injection Dual Gate Analysis

RF dispersion has been one of the major issues in research on GaN power devices during the last years. The measurement techniques presented in chapter 3 are frequently used to investigate drain current depression for different surface passivation. However, these

measurements do not state anything about the the trapping mechanism or the exact position at the surface. Neuburger et al. have proposed a different device structure which allows electrical probing of the passivation layer [125]. Therefore, a second gate was placed nearby the Schottky gate on top of the passivation in direction of the drain contact as shown in figure 4.8a. This dual gate transistor was operated in two relevant modes. First, if the standard Schottky gate (in the following referred as gate 1) was biased, the second gate (gate 2) was floating (not connected) (Fig. 4.8b). This mode allowed normal device operation and was used to stress the device in off-state (Fig. 4.8c). In the second mode, the transistor functioned as a MOS-gate device with gate 1 floating and gate 2 biasing the channel (Fig. 4.8d). The threshold voltage of gate 2 is lower compared to gate 1 due to the reduction of the gate capacitance by the passivation layer. In additon, charge injection into the passivation below gate 2 cause a shift of the threshold voltage. This shift is proportional to the amount of charges in the dielectric layer and can be used to characterize the passivation layer [125].

The stress conditions for GaN HEMTs are typically divided into on-state stress, off-state stress, and semi-on-state stress [80]. In on-stress the channel below the gate is open and $V_{Gate} > V_{Th}$. The maximum of the electric field under on-stress condition can be found in the pinched-off channel below the gate towards the drain side. Degradation is therefore mainly caused by hot electrons [126]. Stressing the device in off-state requires $V_{Gate} < V_{Th}$. The depleted channel hinders electrons to flow from source to drain. Hence, the electric field maximum is at the gate edge towards the drain. Considering the output characteristic for typical HEMT applications (Fig. 3.5) shows that the gate-drain voltage is a maximum in off-state condition. The gate electrode therefore can emit electrons into traps of the device. If V_{Gate} is only slightly above V_{Th}, the device is stressed in semi-on-state. It was found that this stress can cause the fastest degradation due $n_s > 0$ in combination with the high electric fields in the channel [80]. All stress tests were done by constantly biasing the device in either on-state or off-state (on gate 1 or 2) for a certain time. The shortest time occurred for single point measurements, whereas a maximum of 1 hour was applied for the longest stressing periods.

The model used to derive the injected charges is presented in figure 4.9. The charge density N in the passivation layer is assumed to be confined at one horizontal layer at the height t. Considering charge neutrality for the total configuration requires counter charges at gate 2 and the channel which establish a built-in voltage V_{G_2SD} between gate 2 and source and drain (Fig. 4.8e). If the charges are injected exactly in the middle (assuming $\varepsilon_{InAlN} = \varepsilon_{pass}$) between the 2DEG and gate 2, V_{G_2SD} is zero. Any deviation from the center can cause either a positive or negative potential at the contacts. Considering the partial capacitances of this gate stack (Figure 4.9), together

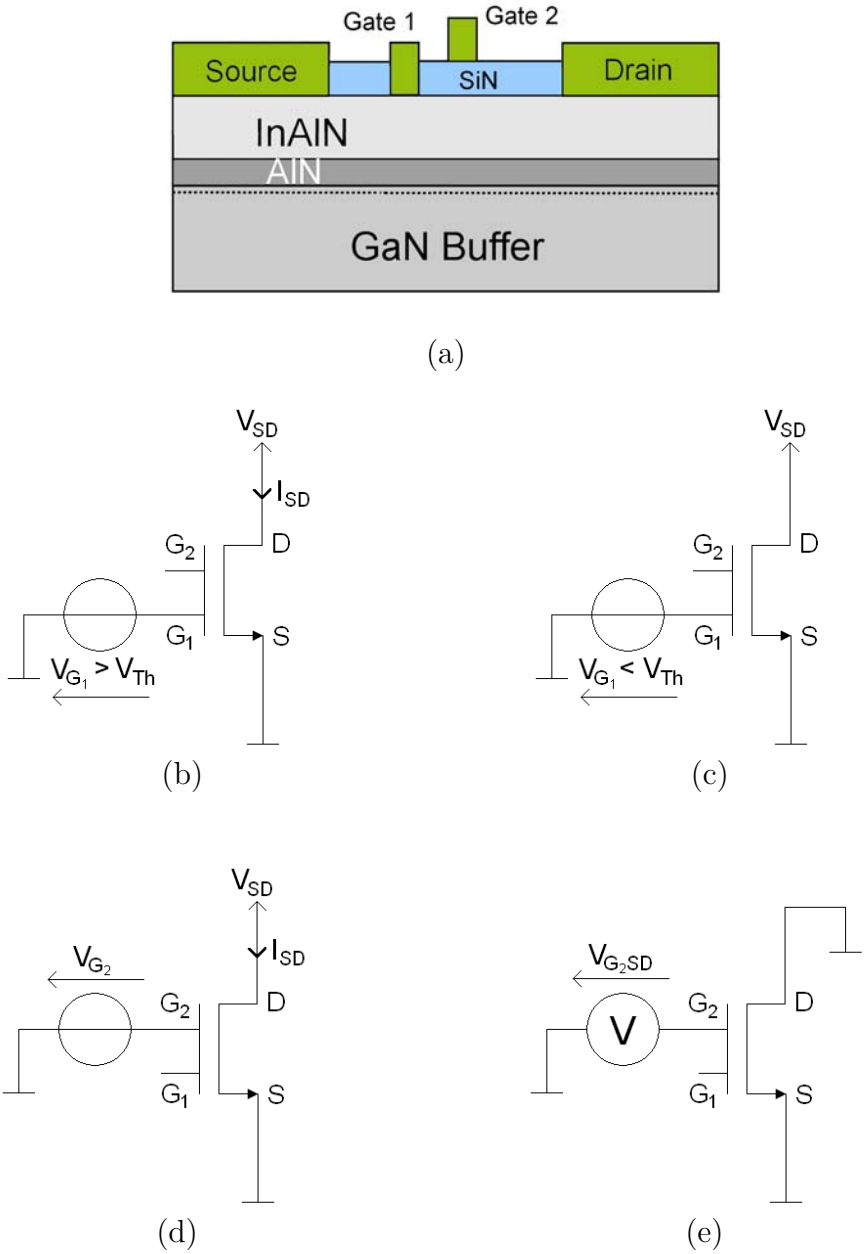


Figure 4.8: Schematic of a dual gate device (a) with a Schottky gate (gate 1) and a second gate on top of the passivation (gate 2) [127, 128]. The circuits indicate the different operation modes for this devices concerning the characterization of injected charges: (b) the device under normal operation using gate 1 (on-state), (c) off-state stress on gate 1, (d) operation of gate 2 with gate 1 floating (on-state), and (e) measurement of the voltage between gate 2 and the channel connected to source and drain. Both (b) and (d) denote on-stress in the device.

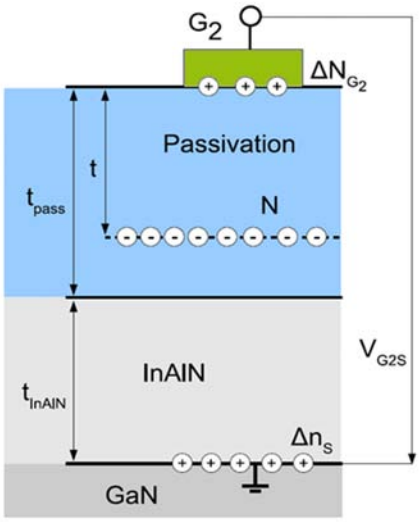


Figure 4.9: Model of dual gate analysis showing the charge centroid within the device passivation. $\bigtriangleup n_S$ represents the counter charges in the 2DEG causing the threshold shift. [128, 125]

with the threshold voltage shift $\triangle V_{th}$, allows to derive the position and sheet charge density N of this confined layer[125, 129, 130]

$$t = \frac{q\Delta n_s(V_{Th})\left(\frac{t_{pass}}{\varepsilon_{pass}} + \frac{t_{oxide}}{\varepsilon_{oxide}} + \frac{t_{barrier}}{\varepsilon_{barrier}}\right)^2 \varepsilon_{pass}}{V_{G_2SD}\varepsilon_0 + 2q\Delta n_s(V_{Th})\left(\frac{t_{pass}}{\varepsilon_{pass}} + \frac{t_{oxide}}{\varepsilon_{oxide}} + \frac{t_{barrier}}{\varepsilon_{barrier}}\right)} \tag{4.3}$$

$$N = \Delta n_s \left(1 + \frac{\frac{t_{pass}}{\varepsilon_{pass}} - \frac{t}{\varepsilon_{pass}} + \frac{t_{oxide}}{\varepsilon_{oxide}} + \frac{t_{barrier}}{\varepsilon_{barrier}}}{\frac{t}{\varepsilon_{pass}}}\right). \tag{4.4}$$

$\bigtriangleup n_s$ represents the counter charge in the 2DEG and is equal to $\Delta V_{th} \times C_{G_2}$. The result for the distance t needs to be corrected if $t > t_{pass}$ by the permittivity ratio between the InAlN and passivation layer. Instead of using the material parameters, the equations can be simplified to

$$\frac{1}{C_t} = \frac{t}{\varepsilon_0 \varepsilon_{pass}} = \frac{1}{C_{G_2}} \cdot \frac{\Delta V_{th}}{2\Delta V_{th} + V_{G_2SD}} \tag{4.5}$$

$$N = \frac{\Delta V_{th}}{q} \cdot \frac{C_{G_2}^2}{C_t} \tag{4.6}$$

if the gate 2 capacitance C_{G_2} is known.

Further details regarding this model can be found in the original publication of this model [128] as well as in other works applying the model on GaN based devices [98, 131] and passivated diamond devices [132, 133]. So far no study has been presented about

the dynamics of the traps being investigated in this model.

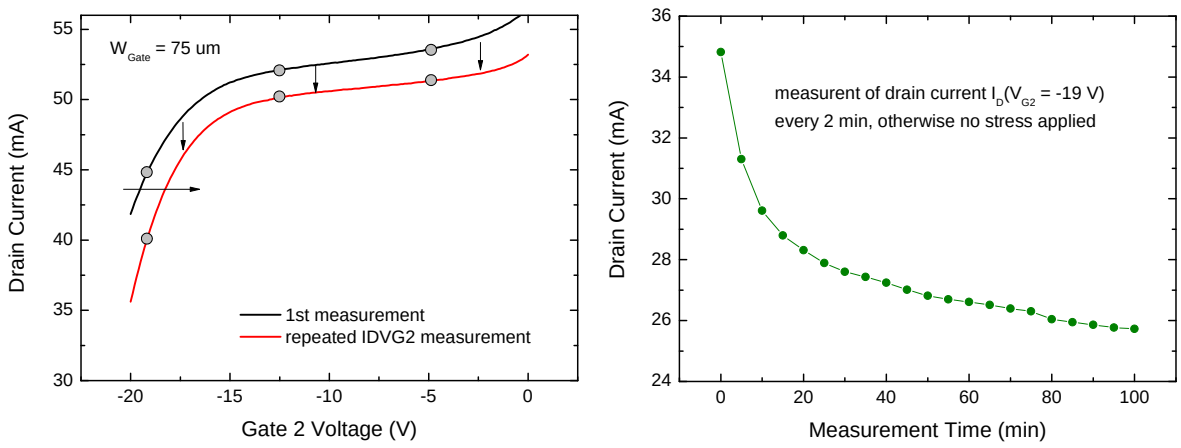
Devices used in this experiment were fabricated on heterostructures with a 11 nm thick InAlN barrier (wafer AEC 1802, see App. A) with thin layer (<4 nm) of thermally grown aluminum oxide below gate 1 and an additional device passivation on top of gate 1 using PECVD-SiN. Details on the device fabrication can be found elsewhere [124]. The second electrode (gate 2) was placed on the top of the 30 nm thick SiN layer. Both gates had a length of 200 nm and were placed around 200 nm apart from each other. The source-to-drain distance was 3 µm. All measurements were performed at room temperature in darkness with a Keithley 4200 Semiconductor Parameter Analyzer using automated measurements for all 4 probes in parallel. The probe which was not used during a certain part of the measurement sequence (gate 2 during the off-state stress on gate 1 and gate 1 during the charge sensing measurement on gate 2) was set floating by the measurement setup.

The basic measurement sequence started with an initial measurement of the transfer characteristic on gate 2 in order to estimate the threshold voltage, followed by stressing of the device in off-state and final characterization of the potential at gate 2 (V_{G_2SD}) and the shift of the threshold voltage. Alternatively, different experiments can be performed using a similar test sequence and applying on-state or semi-on-state stress.

4.2.1 Dynamics of Trap Injection

The dual gate measurement requires three measured components: the built-in voltage V_{G_2SD} and two comparative IV transfer measurements on gate 2 to determine the threshold voltage shift ΔV_{th}. In order to get a correct result, both measurements need to be done without modifying the position or amount of the injected charges in the passivation. The following part will discuss a few phenomena which have been discovered in repeated long-time measurements aiming to find a measurement sequence that allows a correct analysis.

Figure 4.10a shows a transfer characteristic from gate 2. After the first measurement, it was repeated again revealing a shift of the IV curve. This shift indicates fast charging or de-charging of traps within the passivation or at the interface during on-state. The effect was confirmed by measurements of the drain current I_D in on-state at a constant gate 2 bias $I_D(V_{G_2} = const)$ repeated every 2 min without applying any stress during the break (Fig. 4.10b). Analyzing a series of similar experiments revealed that the shift is proportional to the product of measurement time (integration time of a single measurement point) and drain current level, indicating hot carrier injection in the barrier, buffer, or passivation [134]. Furthermore, this induced shift during the on-state measurement was larger than the expected shift from the off-state stress test.



(a) (b)

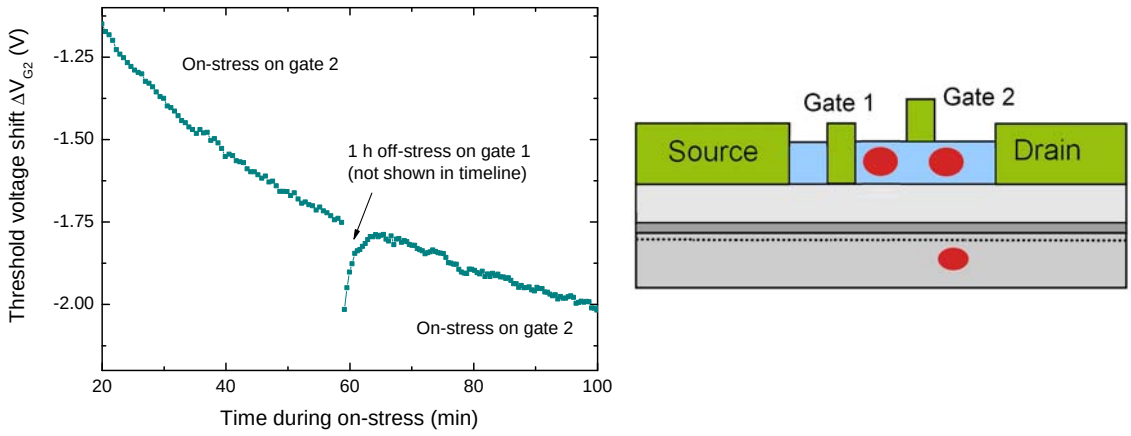
Figure 4.10: Repeated transfer characteristic measurement (a) on gate 2. The vertical and horizontal shift of the transfer characteristic is monitored at certain constant gate bias points. Fig. (b) shows the time dependent drain current for $V_{G_2} = -19V$ (wafer AEC 1802, see App. A).

Therefore, it was not possible to extract the shift of the gate 2 threshold voltage $\Delta V_{Th,G2}$ caused only by off-state stress.

Figure 4.11 shows a comparison between the charge trapping during on-state measurements and off-state stress. In order to reduce the impact of the threshold voltage measurement, the shift was extracted from single points measured at a constant gate 2 voltage in the linear region of the transfer characteristic by the assumption

$$\Delta V_{Th,G2} = \Delta I_D(V_{G_2} = const, \Delta t) \times \frac{\partial V_{G2}}{\partial I_D}, \tag{4.7}$$

where $\Delta I_D(V_{G_2} = const, \Delta t)$ is the change in drain current at a fixed V_{G_2} before and after the stress. At the beginning of the stress test the device was stressed only in on-state using gate 2 (Fig. 4.11). After one hour, the device was stressed in off-state using gate 1 for another hour without interruption. Then the previous stress sequence in on-state was continued. During the off-state stress, the drain current could not be monitored. The result in figure 4.11 indicates the effect of two independent virtual gates. It is assumed that the origin of those two virtual gates lies in different geometric positions of the two gates. Charges from gate 1 are most probably injected in its nearby region, while gate 2 can inject charges below and beside the second gate or even in the buffer (Fig. 4.11b). During the first part of the experiment, the virtual gate related to gate 2 reduces the drain current as described in chapter 3 by the electrostatic potential caused by the injected charges. During off-state stress on gate 1, carriers are



(a) (b)

Figure 4.11: Drain current (a) monitored at $V_{G_2} = -20$V during on-state stress on gate 2. At 60 min, the device is stressed for 1 hour in off-state on gate 1 without monitoring. Fig. (b) indicates some positions of trapped electrons by on-state stress at gate 2 or off-state stress at gate 1 as described in the text. The injected charges cause virtual gates in respect to gate 1 or gate 2.

injected around the vicinity of gate 1 causing the second virtual gate. Its impact on the drain current is noticed after the on-state stress is reapplied on the device. Continue stressing at gate 2 causes detrapping of injected charges at the virtual gate around gate 1. Therefore the drain current is able to recover slightly until the virtual gate caused by gate 2 dominates the drain current. Thus, it is proven that both, the actual stressing test as well as the sensing measurement, act on the passivation-related traps. As a consequence, the sensing measurements on gate 2 need to be as short as possible in order not to cover the results of the stress experiment.

Furthermore, the characteristic of the built-in voltage V_{G_2SD} was investigated. Several sequences listed in table 4.1 were performed subsequent to off-state stress on gate 1. The results in figure 4.12 indicate a strong correlation between the measurement sequence and measured built-in voltage. Using the results of V_{G_2SD} from sequence #1 and #2 in the presented model (eq. 4.5 and 4.6) produces complex numbers indicating a mismatch between the measurement and the model. Therefore it can be seen that the drain current measurement has strong influence on the injected charges and modifies the potential V_{G_2SD}. Consequently, the built-in voltage should be measured at directly after the stress test before any bias is forced onto gate 2.

Additionally, it should be noted that the transfer characteristic does not only shift in positive and negative voltage direction as indicated by the measurement in figure 4.10a.

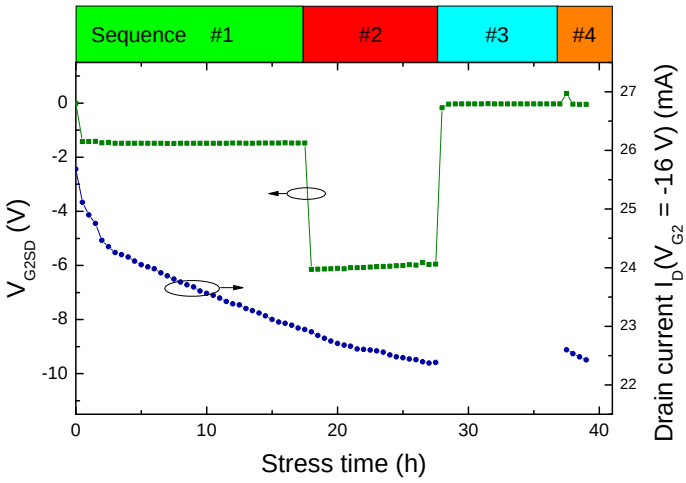


Figure 4.12: Monitoring of the built-in voltage V_{G_2SD} and drain current in different measurement sequences (Tab. 4.1) with 30 min off-state stress on gate 1 between two sequences.

Sequence	$1^{st}measurement$	$2^{nd}measurement$	$3^{rd}measurement$
1	$I_D(V_{G_2})$	$I_D(V_{G_1})$	V_{G_2SD}
2	$I_D(V_{G_2})$	V_{G_2SD}	-
3	V_{G_2SD}	-	-
4	V_{G_2SD}	$I_D(V_{G_2})$	-

Table 4.1: Measurement sequences following 30 min of off-state stress on gate 1.

repeated sequence	probe configuration	special note
V_{G_2SD}	G_1 floating	high resistive
$I_D(V_{G_2[1,2...N]})$, $I_{G_2}(V_{G_2[1,2...N]})$	G_1 floating	short integration time
$I_D(V_{G_1})$, $I_{G_1}(V_{G_1})$	G_2 floating	short integration time
Off-state stress G_1	G_2 floating	

Table 4.2: Final measurement sequence used monitor the injected charges into the passivation layer under long-time stress.

In order to extract the threshold voltage shift correctly from the transfer characteristic several gate 2 bias points should be monitored during the stress experiment as indicated by figure 4.10.

4.2.2 Long-time Stress Measurement

The final measurement sequence used for dual gate analysis is shown in table 4.2. Devices (wafer AEC 1802, see App. A) were analyzed using several bias points on the transfer characteristic as indicated in figure 4.10a.

The drain current characteristics in dependency of gate 2 show a common drop for all applied gate biases within the first measurement cycle (Figure 4.13). This behavior may be explained by electron trapping in the source-side of gate 2 or in the barrier. Those trapped electrons can cause an increase of the source resistance or a shift of the gate 1 threshold voltage (not monitored), respectively. Later cycles reveal no significant change until suddenly the drain current of the lowest bias point in the linear region starts to decrease. This delay can be explained by the 200 nm gap between the two gates. Electrons are injected from gate 1 into the passivation and travel through the dielectric. An alternative explanation is the sudden injection of electrons after defect-assisted barrier lowering of the potential between gate and passivation [135]. The number of injected charges increases with ongoing stress time, indicated by a further decrease of the drain current, until the gate 2 leakage current increases (Fig. 4.13c). It is assumed that the injected electrons below gate 2 assist the sudden increase of the gate current. This soft breakdown of the passivation reduces the number of injected carriers in the passivation and hence prevents the chance for another subsequent breakdown. Eventually, the degradation of the passivation becomes permanent seen by constant high gate leakage current. Without the gate 2 electrode, the device could have been tested until the injected charges reach the drain electrode. Interestingly, the actual HEMT device (gate 1) did not change significantly as seen in figure 4.13d.

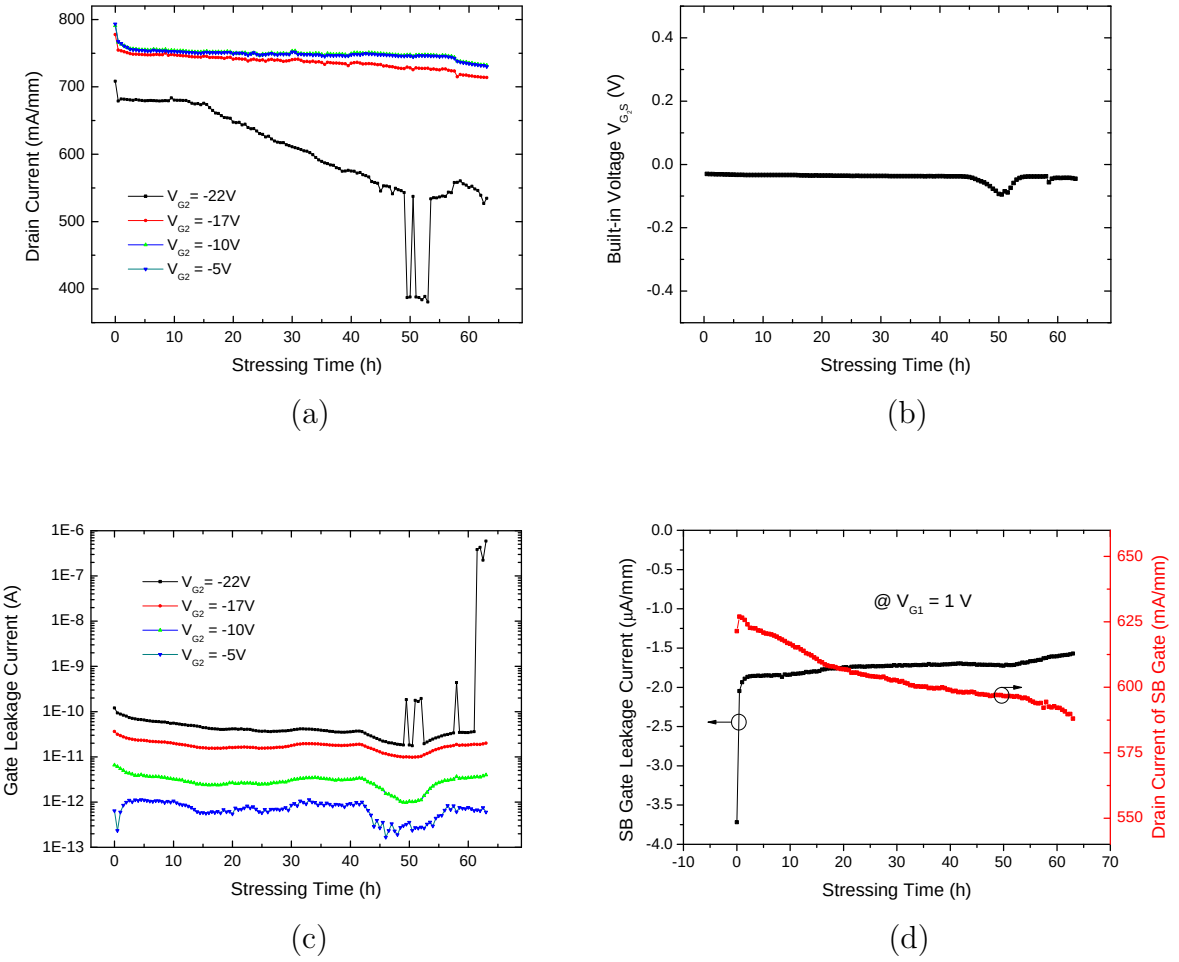
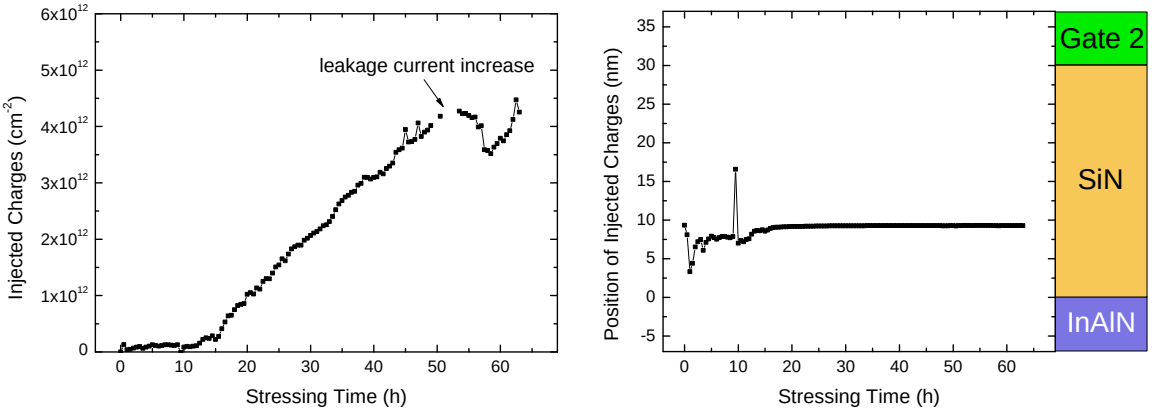


Figure 4.13: Off-state stress test for more than 60 hours with dual-gate measurement (wafer AEC 1802, see App. A) every 30 min. Fig. (a) shows the drain current at four individual gate 2 bias points and figure (c) depicts the corresponding gate 2 leakage current. Figure (b) summarizes the built-in potential measured between gate 2 and source and drain (no bias applied). In (d) the drain current and gate leakage current characteristics of gate 1 are presented [122].



(a) (b)

Figure 4.14: Analyzed results of the injected charge density below gate 2 (a). Graph (b) summarizes the position of the charge centroide within the total gate stack (gate 2 metal, SiN passivation, InAlN barrier). (wafer AEC 1802, see App. A) [122]

Analyzing the results of figure 4.13 with the equations 4.5 and 4.6 reveals the injected charge density and the trap position summarized in figure 4.14. The charge centroid is placed at the lower third of the passivation layer (Fig. 4.14b). This confirms the results of the pulsed IV measurements where no RF dispersion was detected. The maximum injected charge density was $4.5 \times 10^{12}/cm^2$ which is about 20 to 30% of the 2DEG density.

4.2.3 Summary

Dual gate measurements after Neuburger et al. [128, 125] were analyzed for long-term stress tests revealing charge injection under different stress conditions. The time constant of the injection during on-state stress was much shorter than during off-state stress. Subsequent stressing in on- and off-state indicates the formation of two independent virtual gates. Shortening the measurement time by sensing only a few gate 2 bias points with very short integration time could reduce the impact of these injected charges in on-stress. Eventually, the actual gate 2 threshold voltage shift due to charge injection could be extracted revealing a delayed charge injection at gate 2 after 15 h off-state stress. This delay can be explained by the 200 nm gap between the two gates. Electrons are injected from gate 1 into the passivation and move through the dielectric. Alternatively, the potential barrier may be lowered by injection nearby the gate causing a sudden injection of electrons into the passivation after 15 hours of

stress. The method proves to be an efficient way to analyze the mechanisms leading to RF dispersion.

5 Plasma-based Recessing of InAlN HEMTs

Etching of III-N compound semiconductors for electron devices involves many challenges due to the hardness of the materials and the creation of defects. AlN has a binding energy of 11.5 eV, for GaN it is 8.9 eV, and in case of InN 7.7 eV [136]. As a result wet etching without additional electrochemical or photoelectrochemical assistance nearly always yields to extremely low etch rates [137, 138], and most efforts have been put into developing dry etching processes for faster etch rates [139, 140, 141, 142]. These are required in deep mesa structures of optical devices and gate recessing in transistors with low defect generation [143, 144]. In addition, dry-etching is needed for exact pattern transfer for ohmic and gate contacts of passivated device structures. This chapter discusses dry etching of dielectrics and recessing of GaN on InAlN barrier devices. The required etching depths are within a few tens of nanometers and therefore a large variety of recipies exists with reasonable etch rates and selectivity to the subjacent structure. In the past, several gas mixtures have been reported including CH_4/H_2, BCl_3/Ar, Cl_2/H_2, $Cl_2/CH_4/H_2/Ar$, Ar, and $SiCl_4/SF_6/Ar$ [145, 146, 147, 148, 149, 150, 151, 142, 152] in similar procedures as known from GaAs and InP but with much lower etch rates [153].

In this work, mainly fluorine-based recipes for dielectric recess and chlorine-based mixtures for etching of III-N materials were used. The chlorine recipes contained also small fractions of fluorine in order to make the process selective. The chemical role of chlorine and fluorine containing gases has been investigated intensively on GaN and AlGaN/GaN heterostructures [144, 154]. Several authors have reported on the etch-rate increase on GaN by adding up to 30% of fluorine to chlorine gas mixtures [144, 155, 156, 157]. Additionally, the formation of the chemically stable AlF_3 (sublimation point 1260°C) plays a crucial role in controlling the etch selectivity of materials with different aluminum content [144, 157]. However, up to date almost no report is shown on the novel InAlN material [52, 45].

Damage caused by dry etching includes ion implantation [158, 159, 160], creation of traps at the surface and in the barrier, change of surface conductivity [161, 153, 162, 163], increase of gate leakage current, decrease of the Schottky barrier height [164, 165, 166, 167] and impact on the ohmic contact. The challenge of etching com-

pound semiconductors includes different etch rates for each element causing a non-stoichiometric surface condition. This surface reconstruction is one of the main reasons for the creation of traps near the surface. Injection of negatively charged ions into the barrier can cause an increase of the barrier potential and hence reduce the gate leakage current. However, the thermal stability of the injected ions determines the device reliability [168].

5.1 Inductively-Coupled Plasma RIE

Dry etching was performed in an Oxford Plasmalab System 100 inductively coupled plasma reactive ion etcher (ICP-RIE). In contrast to a normal RIE system with two electrodes and capacitively coupled RF power, this system includes a second RF source connected to a coil around a vacuum tube replacing the upper electrode, causing an additional inductively coupled plasma (Fig. 5.1) [101]. Both chamber elements are fed by an RF power generator at 13.56 MHz and connected by coaxial transmission lines. The impedance of these terminated inductor and capacitor are depending on the chamber geometry, the chamber pressure and gas mixture used in the process. In order to match the chamber to the power generators an automated matching network is used which contains variable capacitors and inductors. Depending on the gases and process parameters, it is sometimes required to increase the pressure for ignition. Once the glow discharge is stable, the pressure can be lowered to the desired process parameters. The electrons in the glow discharge are lighter than the ions and can diffuse to the electrodes. Therefore, the glow discharge is positively charged by the remaining ions. As a consequence, a layer forms around the electrodes, which is called „ion sheath". There the bias of the glow discharge drops and the ions are accelerated towards the surface or the top electrode. This DC bias depends mainly on the RF power. Increasing the RF power in order to increase the plasma density and the etch rate, also increases the level of ion bombardment and possible damage or ion implantation in the device. Using an ICP remote high-density plasma source allows to decrease the capacitively coupled plasma (CCP) power and, hence, the incident ion energy.

The etching process is always a combination of physical and chemical etching [101]. Recessing the mesa structure is done by Ar sputtering which basically does not involve any chemical reactions. However, any other recipe described in this chapter involves both mechanisms. Purely physical etching generally starts from a certain threshold of kinetic energy for the incident ions, which is sufficient enough to remove the surface atoms from the crystal. As the energy distribution of the impinging ions is not monoenergetic, this threshold is quite soft. Purely chemical etching can be done if practically no CCP power is used. Reactive ions are generated by the remote plasma

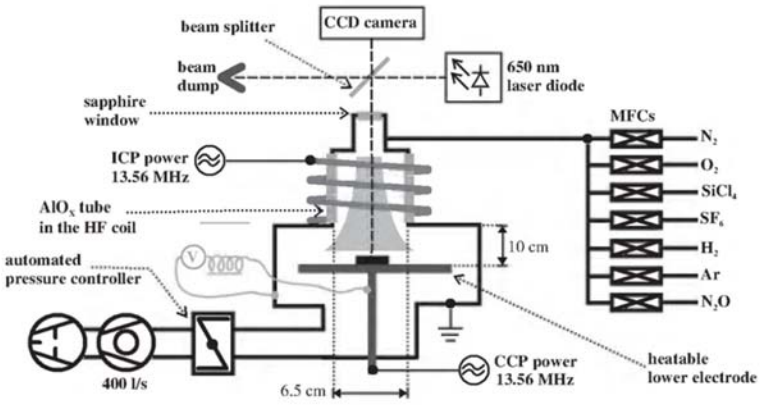


Figure 5.1: Schematic of inductively-coupled plasma reactive ion etcher (ICP-RIE) used for this work [169].

source and diffuse to the sample surface, where they react with surface atoms and produce volatile neutral products which then are removed by the vacuum pump. Using more physical etching components reduces the selectivity between different materials but increases the anistropy of the etching result. In case of compound semiconductor materials and dielectrics, similar etching rates for all involved elements are required. Otherwise the rate is limited by the slowest one and the surface will become heavily non-stoichiometric.

Our RIE system shown in figure 5.1 included various gases for a wide range of materials. Starting a new process always requires a minimum of 30 min of preconditioning of the chamber. Within this period the etch rate can drastically change as shown for a GaN etching process in figure 5.2. The signal was traced from an interferometer placed on top of the chamber. The optical signal originates from the surface of the sample and a second reflection below the surface. As GaN and most used substrates are transparent for visible light, this reflection occurs often from the carrier wafer or even the wafer holder. Therefore the signal usually contains more noise compared to GaAs samples but is enough sufficient to investigate the stability of the etch rate.

5.2 Recessing of Dielectrics on InAlN-Barrier Devices

Recessing of dielectrics can be needed if the device structure is passivated before ohmic contact or Schottky barrier gate formation. Some dielectrics can be deposited after metallization at temperatures that do not harm the metal layers. This typically requires an energy source in addition to the thermal energy of the processes, as in a plasma enhanced chemical vapor deposition (PECVD). Further reasons can be a harsh surface cleaning procedure prior to the deposition of the metal layers. Several deposi-

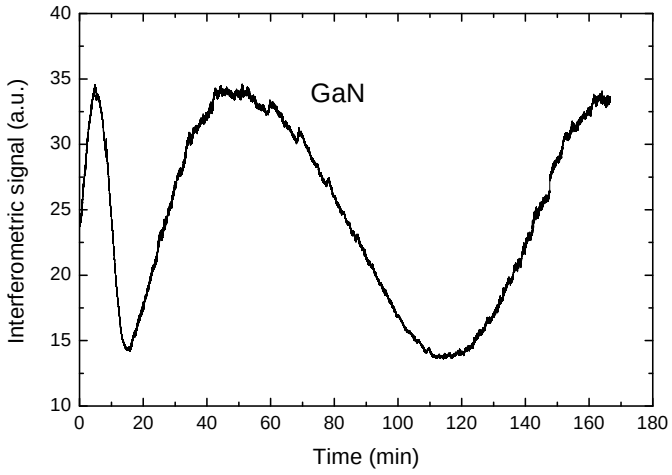


Figure 5.2: Interferometric signal of initialization of chlorine-based GaN etching process.

tion techniques require cleaning of surface in order not to contaminate the deposition chamber with metallic compounds. The passivation scheme which will be discussed in this chapter is in-situ grown silicon nitride (wafer AIX 3415, see App. A). This layer is grown directly after the heterostructure in the MOCVD chamber without breaking the vacuum. Hence absolutely no native oxide can form on the InAlN surface, which secures the electric behavior of the epitaxial stack throughout device fabrication.

The interferometric signals of different etch recipes are presented in figure 5.3. All processes include fluorine which is very common for etching dielectric material as it produces fast etch rates. The drawback is that it is quit hard to achieve anisotropic etching behavior, which is necessary to achieve vertical side walls for a well defined shape of the gate. In our case SF_6 was used as a fluorine containing gas, which is very rich in atomic fluorine causing dominant chemical etching. However, it was reported that using a high content of nitrogen and only very small amount of fluorine can increase the anisotropy for high bias [170]. The addition of N_2 in SF_6 plasma for SiN etching plays two important roles [170]. First, the presence of nitrogen limits the function of active fluorine species as N_2 slightly increases the recombination rate of the fluorine radicals [171]. Therefore, reducing the fluorine flux decreases the lateral etch rate which occurs mainly due to spontaneous mechanism [172]. A second reason could be that using the same atomic components as in SiN increases the partial pressure and hence may reduce decomposition and improve the quality of the sidewall protection [170]. The CCP power was set to 100 W which resulted in a DC bias of around 260 V. The resulting etch rate was 33 nm/min with obviously high selectivity to InAlN as

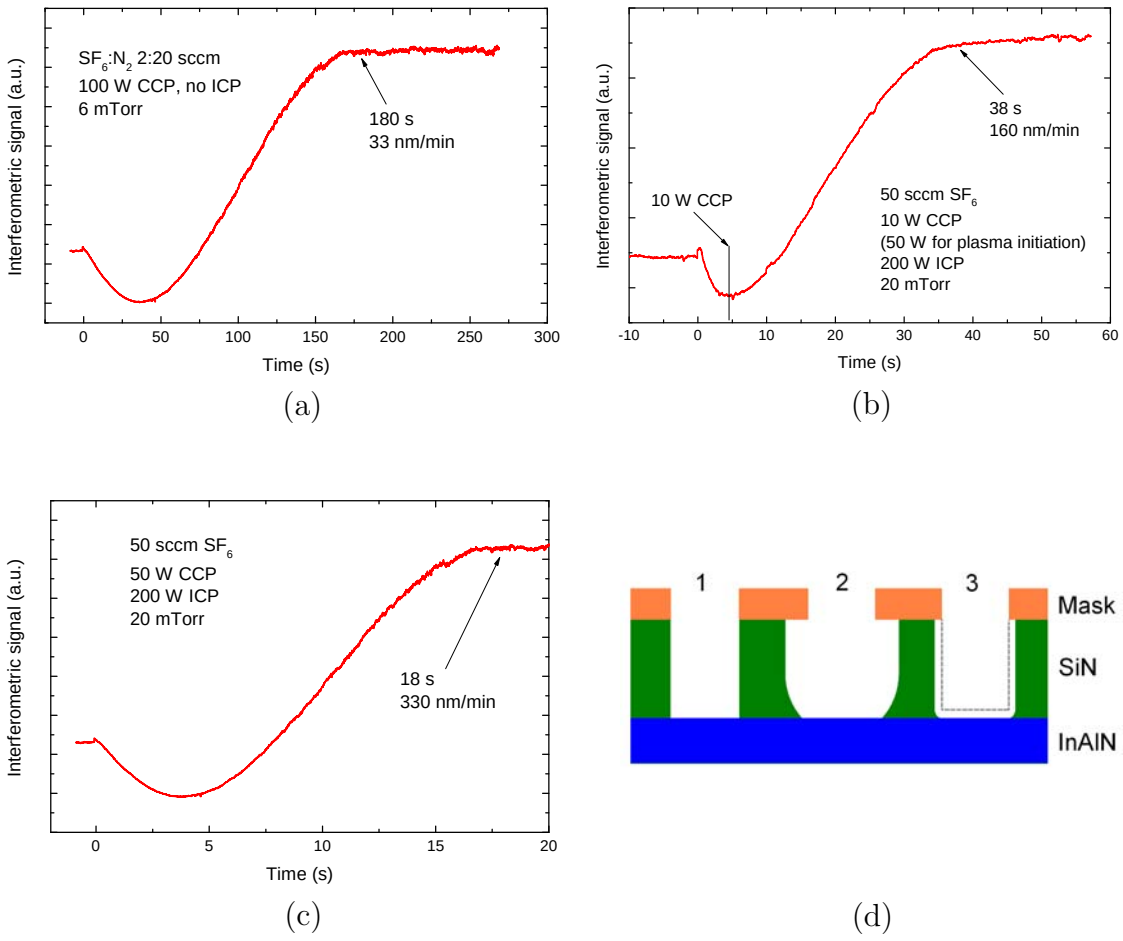


Figure 5.3: Interferometric signal (a-c) for three different recipes and (d) schematic crossections of an anisotropic (1) and isotropic (2) etching process and a combination of both (3) (wafer AIX 3415, see App. A).

can be noted from the constant trace in figure 5.3a. Ohmic contacts fabricated with this method exhibited a slightly increased contact resistance of 0.7 Ωmm compared to 0.5 Ωmm without prior recess, which were done on the same heterostructure without SiN (wafer AIX 3416, see App. A). Some of the recessed contacts showed a non-linear current-voltage behavior as indicated in figure 5.4. The increase of the contact resistance can be explained by fluorine implantation which causes an increase of the barrier potential and hence reduced tunneling. The non-linear behavior was noticed for samples which were slightly overetched and therefore it is believed that a small area on one side of the contact was depleted by heavy implantation (right side of inset of figure 5.4). Even though the etching process is anisotropic, some incident ions can reach the surface from a flat angle causing sidewards implantation. Using the same process at the gate as for the SiN recess, also revealed a strong depletion of the device and hence normally-off operation. It was often reported that this could be recovered if the sample would be annealed at temperatures above 700°C [72]. However, only 70% of the original current level before implantation of fluorine could be achieved, which is not a satisfying result.

Alternatively, the DC bias was reduced as much as possible in order to prevent fluorine from being implanted into the heterostructure. Using 200 W of ICP power allowed to reduce the CCP power to 10 W for an etch rate of 160 nm/min. The self-induced bias was below 50 V. The pressure of 20 mTorr was not sufficient to ignite the plasma. Therefore the CCP power had to be increased to 50 W for ignition. Directly after the plasma was established in the chamber, which can be indicated by the measured bias, the CCP was reduced again to 10 W. The etch rate at 50 W would be almost twice as fast as for the 10 W of CCP power. Obviously this process is quite isotropic, which was also confirmed by samples annealed after the ohmic contact deposition. Comparing samples with anisotropic recess and isotropic recess after annealing in our RTA with slight traces of water caused partial oxidation of the surface. The consequent current reduction produces a similar non-linearity as for the samples with fluorine implantation (Fig. 5.4). The reason is the extended free surface area beside the contact. This surface can oxidize causing an increase of the surface potential [117] and therefore again a partial depletion of the channel. Small asymmetry of the mask layer profile or sample tilt causes different sizes of the open surface areas at different directions of the sample and explains the asymmetric behavior.

Figure 5.3d summarizes the schematic etching profiles for (1) anisotropic and (2) isotropic behavior, while (3) shows an etching process which is neither perfectly isotropic nor anisotropic. In the case of SiN, no damage free recipe with sufficient anisotropic etching characteristic was found. Consequently, a sequent mixture of both has been chosen, starting with anistropic etching of about 90% of the total recess depth. Then the second recipe without nitrogen was used for less than half of the time which is suf-

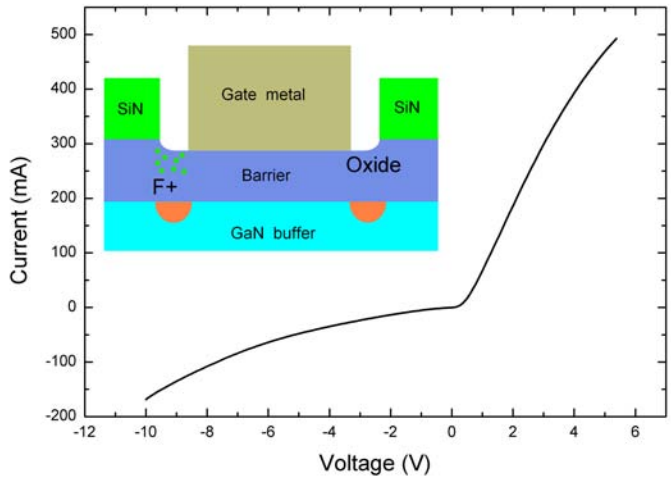


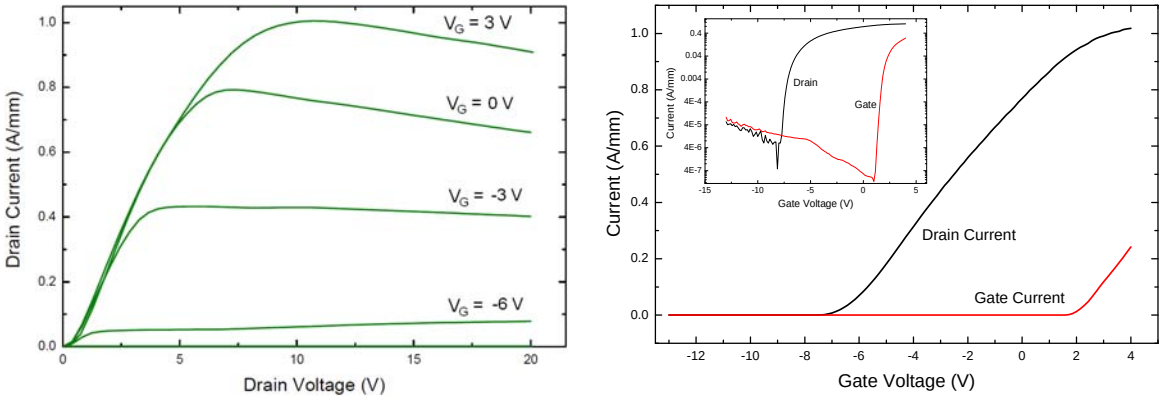
Figure 5.4: IV characteristic of ohmic contacts after dielectric recess. The non-symmetric and non-linear behavior is explained by either fluorine implantation or partial surface oxidation after isotropic etching as depicted in the inset.

ficient to remove the rest of the thickness. Thus, ohmic contacts below 0.5 Ωmm and gate leakage current below $10\mu A/mm$ at a gate voltage of -10 V were achieved. Final device characteristics of in-situ SiN passivated InAlN/AlN/GaN structures (wafer AIX 3415, see App. A) with 1 A/mm maximum drain current are shown in figure 5.5. Pulse measurements on devices with gate lengths of 2 µm and 200 nm revealed an increase of the knee-voltage up to 8 V. It is assumed that the unpassivated surface beside the gate metal after the recess causes the dispersion. Therefore the whole opening of the dielectric needs to be covered sufficiently by a metal layer.

5.3 Selective Recessing of GaN over InAlN

In contrast to dielectrics, etching of GaN on InAlN includes the challenge to achieve sufficient selectivity of the etch rate, as GaN and InAlN have more similarities in material properties. Investigations were started by testing the etch rate behavior as a function of the gas mixture and the capacitively coupled RF power in order to establish the maximum etch selectivity. Therefore at least 100 nm thick layers of GaN and lattice-matched $In_{0.17}Al_{0.83}N$ were partially etched and profiled by an atomic force microscope (AFM).

Transistor processing of 10 nm thick InAlN barrier HEMT structures (wafer A1730, see App. A) involved standard mesa isolation and ohmic contact formation (see chapter



(a) (b)

Figure 5.5: Output characteristic (a) and transfer characteristic (b) of SiN in-situ passivated InAlN/AlN/GaN HEMT devices. The inset in (b) shows the transfer characteristic in logarithmic scale. (wafer AIX 3415, see App. A) [122].

3). In order to investigate the electrical effects at the InAlN barrier caused by plasma damage from the etching process, plasma-treatment before gate metal deposition on a bare 10 nm thick InAlN HEMT for different etching times were applied and compared to a reference device without etching. Fabricated devices allowed us to investigate the influence of plasma-induced damage on the drain current and the gate leakage current. Directly before performing an etching process, the samples were cleaned with 1:2 diluted HCl to guarantee a comparable initial surface [173]. In addition to IV and CV measurements, the carrier drift mobility from long-channel devices with a gate length >40 µm was extracted. The channel charge density was analyzed from capacitance-voltage measurements and the drain current in the linear region at a drain voltage of $V_D = 0.1$V (chapter 3.5) [174].

5.3.1 GaN Recess using CH_4:H_2

Hydrogen plays an important role in several material aspects of III-V materials. Mg doped GaN grown by MOCVD in typical H-rich atmosphere needs to be annealed afterwards to break up the neutral Mg-H complexes [175]. Accumulation of hydrogen at the Schottky barrier interface was found to change the work function of the metal gate and therefore the barrier height of the Schottky contact. This effect is used to implement hydrogen gas sensors and has been reported for a number of metals [176, 177, 178]. Due to its small size, atomic hydrogen is able to diffuse fast and deep into the epitaxial layer but can be also be removed by annealing above 700°C [179]. Hydrogen can decrease the conductivity by neutralizing donors and creation of deep acceptor states, trapping electrons and removing them from the conduction process

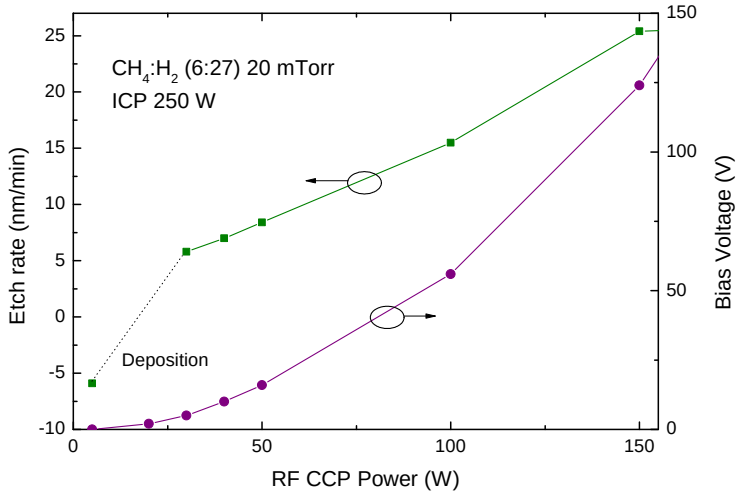


Figure 5.6: GaN etch rate and self-induced bias of methan:hydrogen process for different CCP power levels.

[179, 180].

Experiments started without ICP using a CH_4:H_2 flow ratio of 6:27 sccm with 20 mTorr chamber pressure. The self-induced bias reached above 310 V. Process runs for 30 min exhibited an etch rate for GaN of 8.6 nm/min for large areas. AlGaN layers with 27% aluminum content were recessed by 0.67 nm/min. In contrast, no measureable step could be detected on the InAlN sample containing 83% aluminum. Therefore the etch selectivity between GaN and InAlN should be above 100 which would be excellent for our final device structure with 6 nm GaN cap on 2 nm InAlN/AlN barrier (Chapter 6). The recipe was tested on normal TLM structures with gate mask and compared to samples without plasma treatment. The drain current after 2 min treatment reduced to less than 1% compared to the non-treated device. The gate current characteristic showed no rectifying behavior indicating hydrogen at the Schottky interface. In order to remove H from the epitaxy, the devices were annealed at different temperatures up to 750°C resulting a slight recovery of the drain current and the Schottky barrier height. However, the maximum recovery was still below 1% of the non-treated drain current. Further, accumulative annealing above 450°C increased the threshold voltage due to surface oxidation. It is expected that even though hydrogen could be removed from the device, the surface damage due to the ion bombardment caused non-recoverable damage.

Consequently, the kinetic energy of the incident ions was reduced by lowering the power in order to minimize the surface damage. Figure 5.6 summarizes the GaN etch rate at different CCP and constant ICP power of 250 W for the same gas mixture and chamber pressure as used in the first experiment. At very low CCP power of 5 to

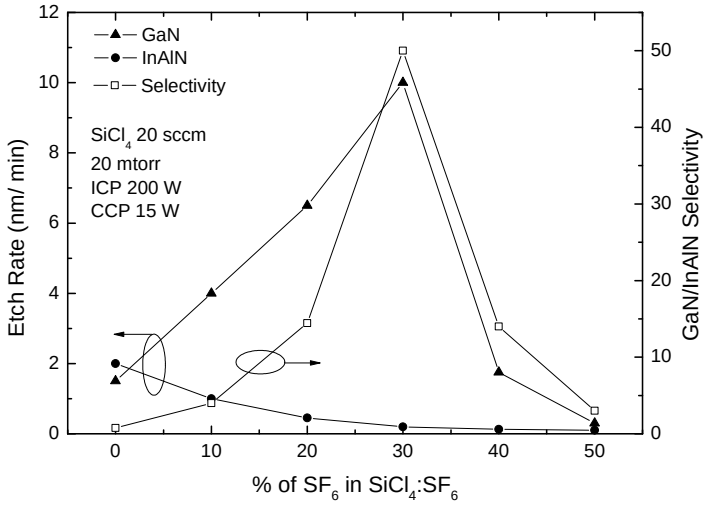


Figure 5.7: Etch rate comparison and selectivity between GaN and InAlN for different ratios of $SiCl_4$ and SF_6 [182].

10 W deposition of organic material was found. A minimum of around 30 W CCP power was required to achieve reasonable etch rates. For CCP power below that the self-induced bias was less than 2 V, and deposition and etching might compensate each other resulting in no noticeable etching behavior. Choosing a CCP power of 80 W for electrical investigations exhibited similar results as previously discussed with almost 99% current reduction and almost no recovery after annealing. Since the time of the annealing process was limited by surface oxidation causing also drain current reduction, one might not be able to remove the hydrogen sufficiently from the devices. Alternatively, different gas mixture without hydrogen were tested.

5.3.2 Etching with $SiCl_4$ and SF_6

Chlorine and fluorine gas mixtures have been extensively used in fabrication of III-N-based devices. Chlorine is very effective in etching Ga, In and Al [150] whereas the incorporation of fluorine leads to less volatile etch products (AlF_3 [181], GaF_3, InF_3), which can be used as etch-resistant barrier. Among them, AlF_3 has the strongest ionic bonding with a difference in electronegativity between Al and F of 2.39. In the samples with LM-InAlN barrier (42% of aluminum at surface) a dominant role of aluminum regarding the etch rate is expected. The combination of chemically-dominated etching by chlorine and sputtering of strongly bound fluorine layers can lead to effective differences in the etch rates of various III-N compounds resulting in a good etch selectivity.

The etch rate of GaN and InAlN as a function of the gas mixture and capacitively coupled power (CCP) is summarized in figure 5.7 and 5.8. Without fluorine, InAlN can be etched as fast as GaN. Adding fluorine by SF_6 up to 30% of the total gas mixture increases the dissociation of chlorine [157] and consequently increases the etch rate of GaN. On the other hand, the additional fluorine enhances the formation of AlF_3 [181] on the InAlN surface (with 83% of aluminum) and results in a chemically strong etch-resistant layer, which reduces the etch rate down to the sputter yield of the incident ions. The fluorine interlayer was confirmed by secondary ion mass spectroscopy (SIMS) of the whole device stack after 2 min recessing (inset of Fig. 5.8) and gate metallization (not shown). The decrease of the GaN etch rate with high concentration of SF_6 ($\geq$40%) is due to increasing formation of GaF_3 and the reduction of chlorine radicals by formation of sulfur-chlorine compounds [157, 183]. The etch rate of InAlN decreases further with increasing amount of SF_6 resulting in the highest selectivity at 30% of SF_6 in the total gas mixture. However, at this gas mixture an increase of the surface roughness of GaN and also InAlN compared to any other gas mixture was observed. Therefore a ratio of 20% SF_6 was chosen for further experiments with a selectivity $\geq$ 10. Varying the CCP (Fig. 5.8) does not change the selectivity between GaN and InAlN but increases the etch rate in accordance to the increase of the self-induced bias. This shows that the etch rate of both layers is triggered by physical ion bombardment. For further recessing of our devices, a CCP power of 15 W was chosen which resulted in a suitable etch rate of GaN of about 6 nm/min. No dependence of the etch rate on the structure size from 100 µm down to 0.3 µm has been noticed for aspect ratios <2.

5.3.3 Electrical Characterization

As in practical applications, the etching process nearly always leads to a slight over-exposure [184, 153], the effect of the etching time on the device properties was investigated. Therefore the same recipe as selected above was used on a 10 nm InAlN HEMT (wafer A 1730, see App. A) prior to the gate metallization with etching times ranging from 30s to 14 min, where the investigations for longer durations were done in order to understand whether an electrical degradation depends on the initialization phase or on the total etching time. Any dry etching process causes damage on the exposed area due to radiation damage and incident ion bombardment leading to possible defect creation in the lattice and implantation of ions into the barrier. Both mechanisms can affect the channel mobility as well as the electron density. The etch depth of these samples was measured by AFM and plotted over the etching time in figure 5.9. The differential etch rate, after an initialization of less than 2 min, is consistent with the

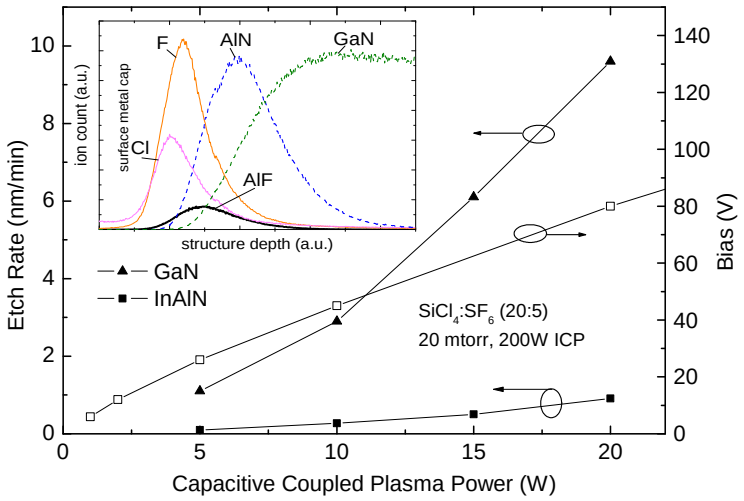


Figure 5.8: Dependency of the etch rate of GaN and InAlN and behavior of the self-induced bias on the capacitively coupled RF power. The inset shows the SIMS profile of a recessed heterostructure with 2 nm remaining InAlN/AlN barrier [182].

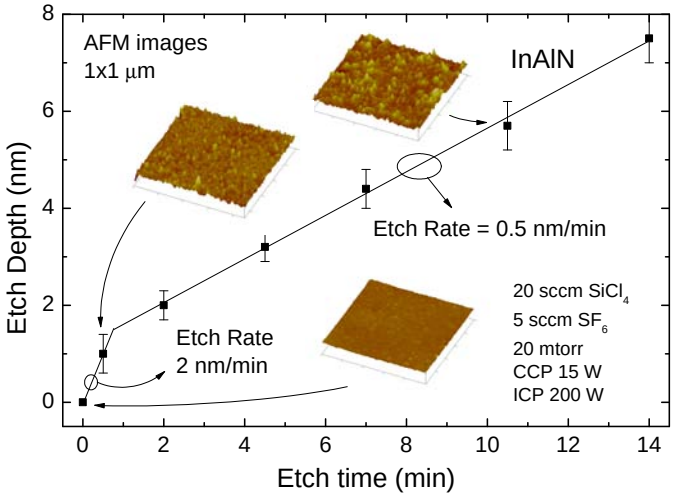
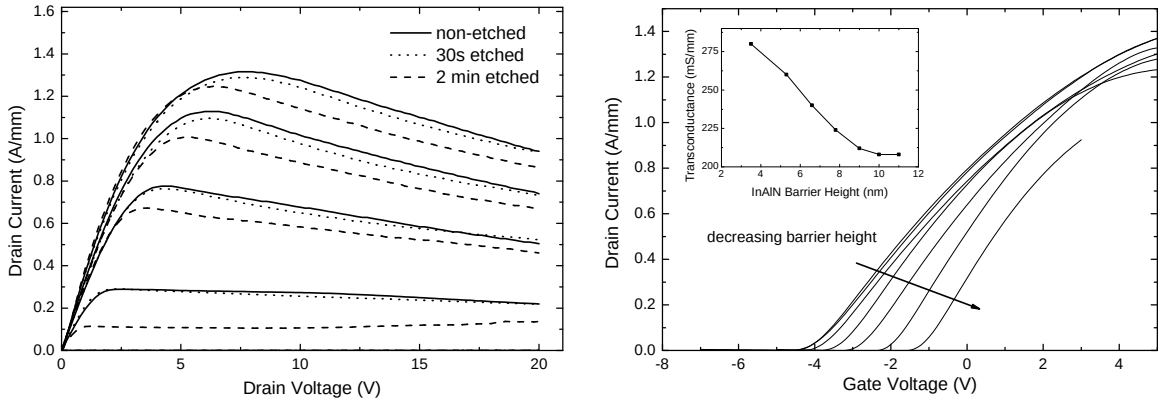


Figure 5.9: Etch depth dependency over time for recessed InAlN. The two lines indicate the approximate etch rate during the etch-resistant initialization (0-1 min) and the later etching process (>1 min). The AFM images refer to the InAlN surface after 0, 0.5, and 10.5 min recess etching, respectively (wafer A 1730, see App. A) [182].



(a) (b)

Figure 5.10: Output characteristic (a) and transfer characteristic (b) of 10 nm thick recessed InAlN barrier HEMTs. The inset in (b) underlines the increase of the maximum transconductance for decreasing barrier height. The gate length of the devices was 2 µm (wafer A 1730, see App. A) [182].

previous one measured from thick InAlN layers (Fig. 5.8). It should be noted that the etch rate is higher during the first minute of etching, which indicates a different etching mechanism for the initialization period. Regarding the effect of the fluorine concentration on the etch rate of InAlN (Fig. 5.7), it is assumed that the initial process (0-1 min) is dominated by chlorine chemistry while fluorine is only starting to form a stable AlF_3 etch-resistant. The initial etch rate of InAlN of about 2 nm/min is consistent with the etch rate measured without fluorine on the thick InAlN samples (Fig. 5.8). After approximately 1 min an AlF_3 barrier is formed which decreases the etch rate of the InAlN layer drastically. In addition, once the surface is dominated by fluorine-terminated aluminum the amount of nitrogen at the surface is expected to be reduced. Nitrogen is able to form volatile etching products [183] resulting in a non-stoichiometric surface [179]. This is in contrast to the initial etching behavior, where indium, aluminum and nitrogen are etched at nearly the same rate by chlorine resulting in an almost stoichiometric surface. Further, an increase of the surface roughness during the etch-resistant barrier initialization was observed (insets of Fig. 5.9). The as-grown root-mean-squared (RMS) value of the surface roughness of 0.28 nm increases to 0.85 nm after 30 s, while etching the sample for 10 min causes only a slightly further increase to 1.19 nm. Hence, the surface roughness seems not to change after the etch stop initialization, which follows the tendency discussed before.

The output and transfer characteristics of devices with 30 and 120 s plasma exposure time and without exposure are summarized in figure 5.10. The threshold voltage, determined from the transfer characteristics of the etched devices (Fig. 5.10a) can

be influenced by changes in the barrier thickness, the Schottky barrier height (SBH), variations in the sheet carrier density, and varying amounts of fixed charges in the barrier. After 30 s of exposure the threshold voltage is the same as for the non-treated device. Even though the barrier was slightly etched, no difference in the gate capacitance was found. Thus it is expected that no fluorine has been implanted into the barrier and the heterostructure has not been damaged by the process. Etching for 2 min or more shifts the threshold voltage towards more positive values, due to the reduction of the barrier thickness, which was confirmed by a proportional increase of the gate capacitance. It can be seen that the saturation drain current of 1.2 A/mm is comparable in all shown devices. The 30 s treated devices exhibit exactly the same transfer characteristics and maximum drain current as the non-treated ones (Fig. 5.10). However, after 2 min etching a slight reduction of the drain current appears which is consistent with a decrease of the channel drift mobility. The results of the long-channel devices show a mobility of $1250\,\mathrm{cm^2/Vs}$ for samples without plasma treatment, which starts to decrease down to $1050\,\mathrm{cm^2/Vs}$ after etching for 2 min or longer (Fig. 5.11). Therefore it is assumed that the sheet carrier density remains unchanged upon plasma exposure and hence conclude that our recipe does not damage the quantum well of the two-dimensional electron gas (2DEG). The decrease of the mobility may be accounted to nitrogen vacancies due to excessive over-etching and the formation of non-volatile AlF_3 and InF_3. Nitrogen vacancies are known to behave as donor-like traps in GaN [179], causing additional charges in the barrier and therefore enhance the scattering of electrons in the channel. No further decrease in drain current was observed for devices etched much longer until the barrier thickness reached about 3 nm causing additional limits due to tunneling. Therefore it can be concluded that the observed degradation is caused by the formation of the etch-resistant barrier.

Figure 5.12 summarizes the typical gate leakage current of plasma exposed and non-treated devices for different etching time durations. The apparent Schottky barrier height decreases significantly after 2 min of plasma exposure but remains practically unaffected for the 30 s etched device. Longer exposure time does not have significant impact on the SBH until the barrier thickness becomes considerably thinner. In a similar way, the reverse leakage current shows almost no difference between the non-treated device and the one etched for 30 s. The gate leakage for samples etched for longer time increased by 3 to 4 orders of magnitude. It is speculated that the non-stoichiometric surface after the AlF_3 formation causes the increased gate leakage due to nitrogen vacancies. It was already reported, that nitrogen vacancies are a source for enhanced tunneling through the barrier [185, 186]. The deterioration of the Schottky barrier gate correlates, therefore, also with the formation of the etch-resistant barrier formation. The results indicate a trade-off between device performance degradation due to the increase of the gate leakage and a safe level of over etching. Alternatively,

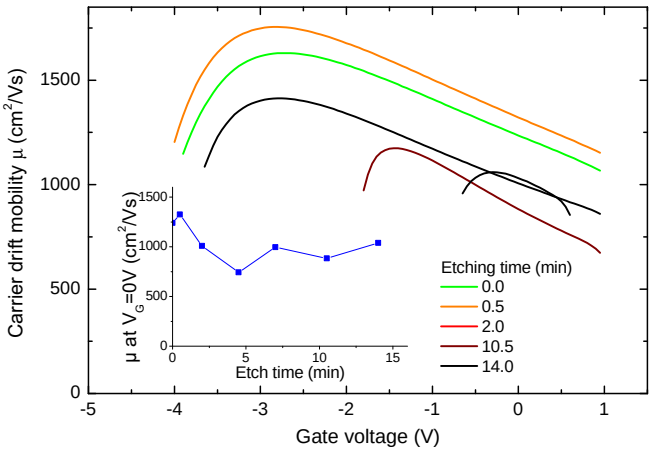


Figure 5.11: Carrier drift mobility for different etching times. The inset compares the mobility at gate voltage V_G=0V (wafer A 1730, see App. A).

one could oxidize the surface subsequently to the etching process by oxygen plasma or thermal method before gate fabrication. If sufficient energy is provided aluminum could form an aluminum oxide layer [124], possibly improving the surface properties.

5.4 InAlN Surface Oxidation by Oxygen Plasma

The previous chapters have all shown different challenges after gate recessing. Among them the gate leakage current is the most determining parameter for the device performance. If the gate cannot be insulated sufficiently from the channel, power gain, switching speed, and gate-drain breakdown are reduced. Hence the deterioration after recessing needs to be adressed and the Schottky gate requires a thin insulation layer which in the best case consumes surface damages. A very effective method of gate insulation was shown by M. Alomari et al., who annealed the InAlN at 800°C for 4 min in oxygen ambient and oxidized a very thin layer of less than 2 nm of the InAlN barrier, which reduced the gate leakage by 3 orders of magnitude [124]. However, for a recessed gate it is usually required to deposit the gate metal by using the same mask as for the recess. The resist layer does not sustain such high temperature and therefore thermally grown or deposited oxides are not an option. Even dielectrics deposited by PECVD cannot be used as their quality degrades very much for low temperature processes. Alternatively, oxygen plasma can be used to oxidize the open surface after recessing. In addition, thin layers of metals can be deposited thermally or by electron-beam evaporation before plasma oxidation. Repeating steps of metal deposition and

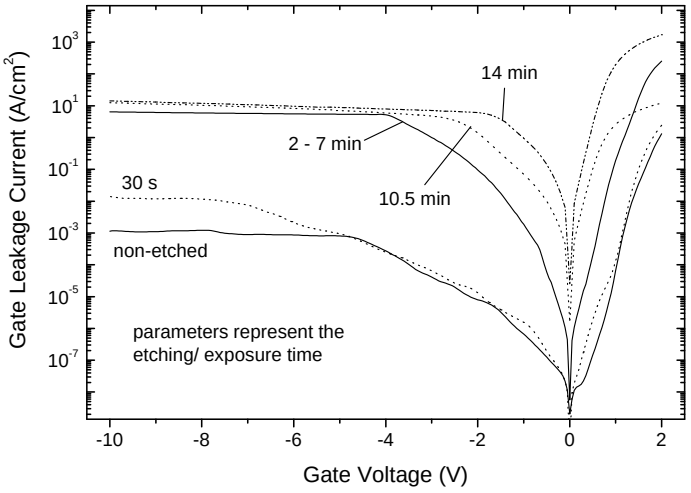


Figure 5.12: Gate leakage current of recessed devices with different recess etching time of 30 s, 2 min, 4.5 min, 7 min, 10.5 min, and 14 min in comparison to non-etched devices. No difference was noticed for devices etched between 2 and 7 min. Therefore only one representative graph is shown (wafer A 1730, see App. A) [182].

oxygen plasma can even produce thick layers of aluminum oxide, zirconium oxide, or other dielectrics. Addionally, dielectric layers can directly be sputtered, even though the quality of the film is reduced compared to thermally grown insulators.

The presented experiment has been performed in order understand the mechanism of surface plasma oxidation. According to Alomari et al. there should be a small processing window of surface oxidation where aluminum oxide can form allowing indium to outdiffuse to the surface [124]. Further oxidation would force indium to diffuse into the barrier causing stress and an increase of the surface potential which eventually leads to an increase of the sheet resistance. Hence, it is intersting to know if such window does also exist for plasma oxidation. It should be detected by a reduction of the gate leakage current without increase of the sheet resistance. The experiment was again carried out on TLM structures which were oxidized in the ICP-RIE at 300 W ICP power and 60 mTorr chamber pressure (wafer AIX3416, see App. A). The CCP power has been increased until a noticeable change of the sheet resistance could be measured. Finally, Ni/Au metal gates very fabricated to measure the gate leakage current. The non-treated sample exhibited a sheet resistance of around 200 Ω/□, which did not increase significantly for processes shorter than 5 min at 50 W. Oxidizing the samples at 100 W for 5 min doubled the resistance to 450 Ω/□. Pal et al. reported a stable saturation of the surface oxidation using plasma. Therefore, samples were oxized for 15 min at 80 W revealing a sheet resistance of 720 Ω/□. This indicates that the saturation

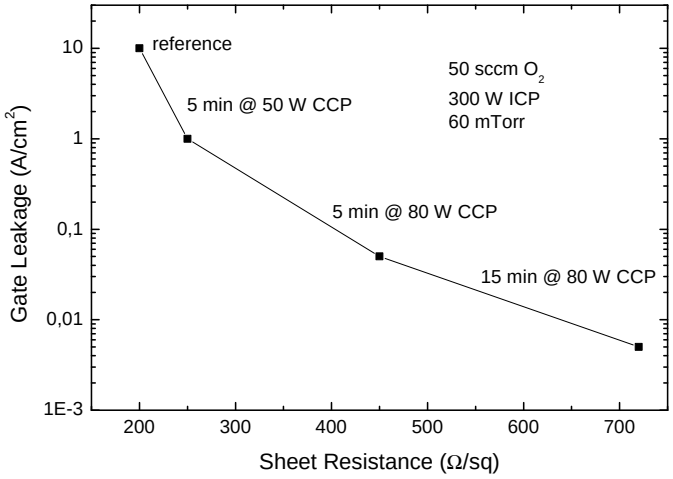


Figure 5.13: Schematic characteristics of E-mode devices with reduced barrier or increased potential in comparison to D-mode device (wafer AIX 3416, AEC 1802, see App. A).

requires more than 5 min. Figure 5.13 summarizes the gate leakage current versus the increase of the sheet resistance. It clearly indicates that an improvement of the gate leakage can only be achieved by a reduction of carriers in the channel using plasma oxidation. Since this concerns only the gate area, the reduction might be acceptable and this could be a useful method to improve the leakage and produce a positive threshold voltage shift in enhancement-mode devices.

5.5 Summary

Dry etching of 100 nm thick in-situ grown SiN and GaN on InAlN/GaN heterostructures has been achieved for reasonable etch rates and a minimum device impact. No degradation of the ohmic contacts was found after improving the recess process by a two-step recess. First, high bias is used to etch most of the SiN layer anisotropically. Second, a low-bias recipe provides the final removal of residual SiN areas. Devices exhibit 1 A/mm drain current and below 50 µA/mm gate leakage current at $V_G = -10\,\mathrm{V}$.

Another recipe was found to recess GaN on InAlN with a selectivity >10 for an inductively coupled plasma recipe with $SiCl_4$ and SF_6. The dependency of the etch rate on the gas mixture was consistent with the formation of an AlF_3 related etch-resistant barrier at the InAlN surface. The initial etch rate of InAlN of 2 nm/min was consistent with a chlorine-only etching process and decreased to 0.5 nm/min after around 1 min. This indicated that it takes around 1 min to form the etch-resistant layer. Electrical

measurements on a 10 nm thick InAlN barrier device after 30 s of plasma exposure revealed the same drain current level of 1.2 A/mm compared to non-treated devices. Only after 2 min of etching the channel drift mobility reduced slightly. Also the gate leakage current was unaffected by the etching process until the formation of the etch-resistant barrier. After this initialization the reverse gate leakage increased by 3 to 4 orders of magnitude probably due to nitrogen vacancies of the non-stoichiometric surface.

Oxidation of InAlN by oxygen plasma was found to produce a sufficient gate leakage reduction but increased the sheet resistance. However, the results are useful if only applied below the gate after recessing. The induced shift of the threshold voltage by surface oxidation can benefit the fabrication of enhancement-mode devices.

6 Enhancement-mode Device with Surface Passivation by GaN Cap

A positive device threshold voltage can be obtained by thinning the barrier below the gate. The presented design in the following chapter includes a barrier layer of only 1 nm InAlN with an additional 1 nm AlN spacer in order to achieve enhancement-mode operation. The first part focuses on the device idea and experimental results without targeting a specific application. Later, possible device implementations for target applications will be discussed. In addition to the excellent electrical results in E-mode operation the design allows to be combined with D-mode devices on the same epitaxial structure, enabling the implementation of digital circuits. Inserting additional gate insulation increases the gate voltage swing and hence opens up the possibility for switching applications.

6.1 Advantages and Challenges of E-mode Devices

Typical depletion-mode HEMT designs on GaN form a 2DEG channel below the barrier, requiring an increase of the surface potential in order to achieve depletion. In that sense the gate voltage is able to turn off the drain current in the channel. In enhancement-mode devices the 2DEG under the gate is already depleted even if no bias is applied and additional electric field is needed to generate electrons in the channel. This behavior offers great advantage in circuit designing, fail-safe operation for power applications and the possibility to integrate digital circuits. As D-mode circuits require a positive and negative power supply, designing circuits with E-mode devices allows a single source power supply and therefore cause a reduction of area of the electric circuit and costs. Further, D-mode transistors remain open in case of a broken connector to the gate, which requires additional consideration in circuit design. Hence fail-safe operation is an important issue concerning system integration. Digital circuits are still an exotic topic in the GaN community. However, considering improved handling of the material growth in the future, the larger bandgap and high electron saturation velocity makes GaN still a promising competitor in this field.

So far only n-type channels are common in GaN devices due to material reasons [187].

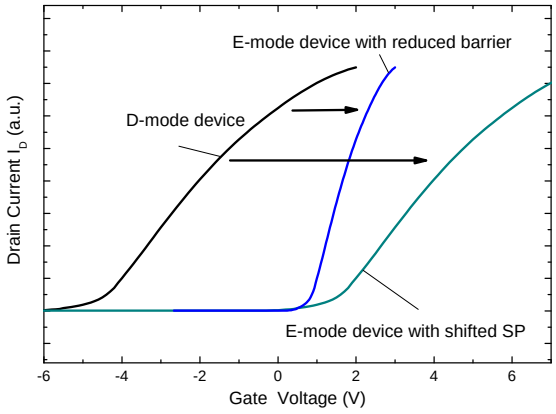
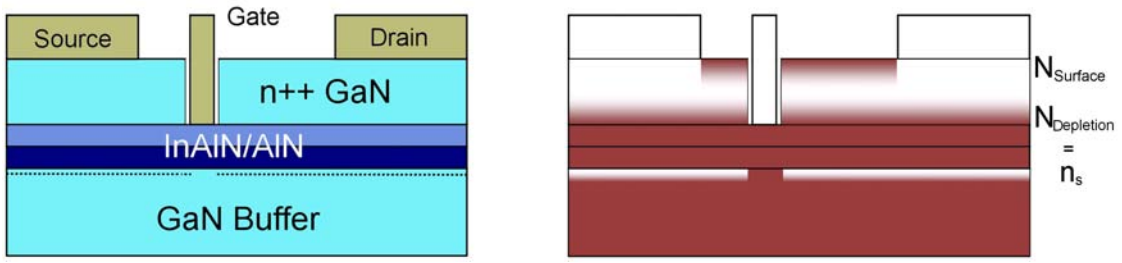


Figure 6.1: Transfer characteristics from a D-mode device in comparison to the schematic charcteristic of an E-mode device with reduced barrier and an E-mode device with same barrier but increased surface potential.

Therefore, both, D- and E-mode devices are biased in the positive bias direction. The important difference between them is however the build-in voltage, defined by the surface potential and the net polarization in the barrier. In the past, a lot of research has been carried out trying to increase the threshold voltage.

On the one hand, several approaches were developed to raise the conduction band below the gate. This increases the surface potential as well as the flatband voltage and causes a shift of the transfer characteristic towards positive bias. Hence, a higher forward gate bias is required to establish the 2DEG under the gate (Fig 6.1). The forward bias is however limited by the gate insulation of the Schottky contact or a dielectric. Using p-doped GaN [188] or InGaN [189] interlayers the transfer characteristic could be shifted to the normally-off regime but it reduces the device performance due to the limitation of acceptable forward bias. A similar approach was done using fluorine ion implantation in order to incorporate negative charges below the gate [73]. The increased barrier also reduces the gate leakage current allowing gate biasing up to 4 V [190]. However, such devices may not be thermally stable above 500°C [73, 72], which counters the desirable property of GaN-based devices to withstand harsh environments. Conclusively, all techniques targeting a shift of the device characteristics could not achieve as good results as it has been demonstrated for D-mode devices.

On the other hand there is a second approach to reduce the barrier thickness below the gate. Considering relation 3.3 explains the increase of the threshold voltage V_{Th} with decreasing barrier thickness. Figure 6.1 compares this approach to the previous one and shows that the flatband voltage remains unchanged. Hence, the device characteristic does not require a higher gate swing to reach comparable drain currents.



(a) (b)

Figure 6.2: Enhancement-mode device structure (a) [193] with schematic electron density (b) (white) versus depleted area (red).

High performing E-mode devices were produced reducing the barrier thickness below the gate [73, 191]. Nevertheless, the recess process used to achieve about 3 to 4 nm of barrier is hard to control and reproducibility is a challenge for such devices.

6.2 Device Idea and Structure

The device structure is based on a 1 nm lattice-matched InAlN barrier with an additional 1 nm AlN interlayer (Fig. 6.2a). The structure is capped with a highly doped n^{++} GaN layer providing free electrons in the 2DEG. In addition, the electrons in the cap shield the 2DEG from variations of the surface potential. Figure 6.2b shows the schematic electron concentration in the structure. The main advantage of this design is that processing will be easier due to the selectively recessable cap layer on top of the the thin barrier. Until now such thin barriers were only demonstrated for AlN/GaN heterostructure devices, which, however, include very high stress [192]. In contrast, our device has an only 1 nm AlN interlayer, which does not induce critical stress [41] while the rest of the heterostructure is lattice-matched to the substrate and hence does not cause any additional stress.

Using a one-dimensional Poisson-Schrödinger simulator [194] and experimentally extracted parameters for InAlN [45], conduction band structure and electron concentration were calculated as shown in figure 6.3a. The highly doped cap layer depletes on both sides which provides enough electrons to create a 2DEG at the AlN/GaN heterojunction, without the necessity of surface donors and even below the critical thickness for 2DEG formation of InAlN [45]. Surface depletion is caused by traps on the surface [84]. If sufficient electrons are provided in the cap, free electrons will remain in the n^{++} cap layer which lower the conduction band and shield the channel from variations of surface charges resulting in a reduction of the RF dispersion. The simulation in

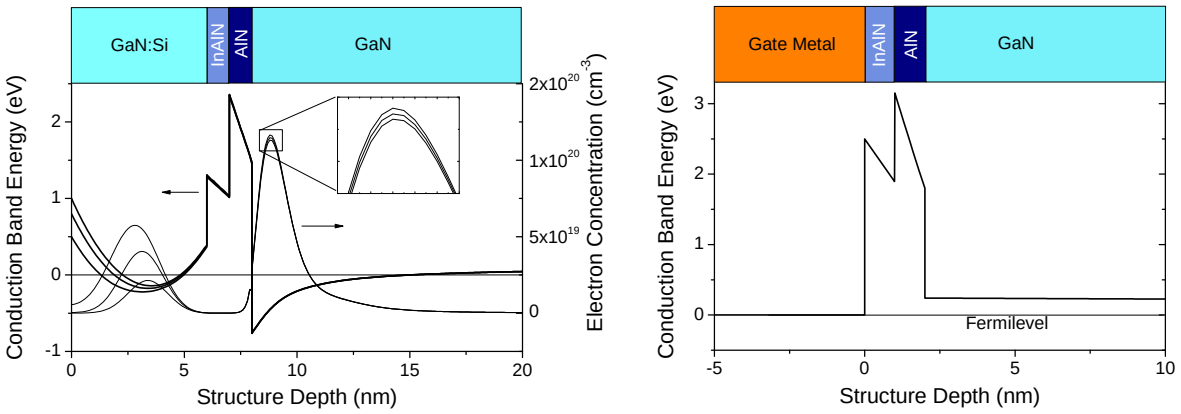


Figure 6.3: Schematic band structures of the E-mode device at (a) the access region [193] and (b) below gate. The variation of the surface potential Φ_{SP} in (a) shows a strong influence of the free electron concentration in the cap layer but only a minor effect in the channel.

figure 6.3a suggests that surface potential variations up to 1 eV result in nearly the same 2DEG densities, whereas for higher values the cap layer is fully depleted and hence does not shield the 2DEG. Figure 6.3b schematically shows the situation below the gate. The GaN cap layer is removed and therefore the channel is depleted. Earlier experiments have shown scaling behavior and critical thickness for forming a 2DEG for InAlN barriers[45, 195]. These results suggested a positive threshold voltage for a barrier thickness below 3 nm.

The simulation results explain that the highly doped GaN cap layer is the reason for the existence of the 2DEG and hence for prevention of RF dispersion. Both are directly linked to the total amount of available electrons equal to $N_D \times d_{cap}$, where N_D is the (volume) donor density in the GaN cap and d_{cap} is its thickness. The surface trap density was found to be around $2{\times}10^{13}$ cm^{-2} [196] and is equal to the sheet density of ionized donors in the cap at the free surface $N_{Surface}$. The total sheet density of free electrons in the cap layer can be written as

$$n_{cap} = N_D \times d_{cap} - N_{Surface} - n_s, \tag{6.1}$$

where n_s is equal to $N_{Depletion}$, the sheet density of ionized donors in the cap at the interface to the barrier (Fig. 6.2), if $n_{cap}{>}0$. The amount of free carriers in the cap layer determines how much the 2DEG is shielded from the surface. The more free electrons are provided the higher is the number of electrons that needs to be injected at the surface to start a depletion of the channel below. Since surface traps can almost

fully turn off the device, it is recommended to have at least as many free carriers in the cap as in the channel. Furthermore, the access resistance may decrease by having an additional channel parallel to the 2DEG beside the gate. Consequentially the parasitic capacitance would increase due to this parallel channel which is disadvantageous for RF application. This topic will be discussed in more detail after the electrical results of the cap layer in chapter 6.6. The final design contains $6{\times}10^{13}$ cm^{-2} donors in a 6 nm thick cap layer obtained by a doping density of $N_D{=}10^{20}$ cm^{-3}.

In addition to this basic calculation necessary for designing the structures, the dependence of the 2DEG density n_s on the cap doping density N_D should be discussed [197]. In order to be able to neglect any effects due to variation of the surface potential on the carrier density in the 2DEG, the GaN cap needs a sufficient thickness. Also, only a single barrier material is assumed in the calculation for simplicity. In this case the electric field $\overrightarrow{E_{cap}}$ and the potential ϕ_{cap} of the cap layer towards the barrier (Fig. 6.3a) can be described using the depletion approximation as

$$\overrightarrow{E_{cap}}(x) = \frac{qN_D}{\varepsilon_{GaN}} \cdot \overrightarrow{x}, \tag{6.2}$$

$$\phi_{cap} = \frac{qN_D}{\varepsilon_{GaN}} \cdot \frac{d^2_{depletion}}{2} + \frac{\Delta E_C}{q} + \phi_{N_D}, \tag{6.3}$$

where q is the charge of an electron, ε is the dielectric constant, x the vertical length, $d_{depletion}$ is the width of the depleted GaN cap, and ϕ_{N_D} is the potential difference of the conduction band without depletion in comparison to the Fermi level. ΔE_C is the conduction band discontinuity between the GaN buffer and the InAlN barrier. The electric field $\overrightarrow{E_{Barrier}}$ and the potential $\phi_{Barrier}$ of the barrier (Fig. 6.3a) can be described by

$$\overrightarrow{E_{Barrier}}(x) = \frac{q}{\varepsilon_{InAlN}} \cdot (n_{pol} - n_s) \times \overrightarrow{e_x}, \tag{6.4}$$

$$\phi_{Barrier} = \frac{q}{\varepsilon_{InAlN}}(n_{pol} - n_s) \cdot d_{Barrier} + \frac{\Delta E_C}{q} + \frac{E_f(n_s)}{q}, \tag{6.5}$$

where n_{pol} is the effective sheet charge density of the polarization between the barrier and the GaN buffer. $E_f(n_s)$ is the energy gap between the bottom of the quantum well and the Fermi level [48, 47, 45]. In case of an highly degenerated GaN cap layer it can be assumed that ϕ_{N_D} and $E_f(n_s)$ are equal. Taking further into account that $\varepsilon_{GaN} \sim \varepsilon_{InAlN}$, the equations 6.3 and 6.5 can be combined to a quadratic equation with the unknown parameter $d_{depletion}$. Solving this equation reveals the thickness of the depleted GaN cap layer, which can be inserted into the already known relationship

between n_s and the cap depletion, resulting in

$$n_s = N_D \cdot d_{Barrier} \cdot \left[\sqrt{1 + \frac{2n_{pol}}{N_D \cdot d_{Barrier}}} - 1 \right]. \tag{6.6}$$

The result indicates a higher 2DEG density with increasing cap doping density or larger barrier thickness. The dependency of the 2DEG density on the cap doping density is in contrast to the standard HEMT device (dependency on surface potential) introduced in chapter 3 (eq. 3.2). For simple processing it is desirable to achieve a thin cap, which requires a doping level close to the solubility of the dopant silicon in GaN is required.

6.3 Device Fabrication

The actual device structure was grown by metal organic chemical vapor deposition (MOCVD) on sapphire substrates (wafer A 1592, A 1589, A1732, see App. A). The epitaxial structure consists of 1 µm GaN buffer, 1 nm AlN interlayer, 1 nm lattice-matched $In_{0.17}Al_{0.83}N$ barrier layer and a 6 nm thick $10^{20}cm^{-3}$ Si-doped GaN cap. Directly after the growth electrochemical capacitive-voltage measurements were performed to extract the apparent electron density of the structure (Fig. 6.4). Therefore about three droplets of H_3PO_4 are diluted in 100 ml H_2O and brought in contract with the semiconductor. On the surface the solution causes a thin protective oxide without etching the semiconductor. The surface barrier caused by this method was extracted earlier to be around 1 eV. The free carriers in the cap layer can be clearly distinguished from the 2DEG (Fig. 6.4). Furthermore, it should be noted that the maximum free carrier concentration in the cap matches with the expected doping density. Hence, sufficient shielding of the 2DEG from surface potential variations can be expected. However, one needs to be careful when comparing the CV result measured on the surface directly after the growth with our device results, since the surface may oxidize causing an increase of the surface potential [117]. Figure 6.4 suggests a depletion width of around 3 nm which can be linked to a potential increase of 0.91 eV using (eq. 6.3). Hall measurements at room temperature exhibit a slightly lower electron sheet charge density than expected from the GaN cap depletion of $1.9 \times 10^{13} cm^{-2}$ and a mobility of $1180\,^{cm^2}/_{Vs}$. Both values do not differ much from expected values of typical 10 nm barrier InAlN/AlN/GaN 2DEG.

Device fabrication (wafer A 1592, A 1589, A1732, see App. A) starts with standard mesa isolation and ohmic contact formation. Measurements on linear TLM patterns exhibit a low contact resistance of 0.3 Ωmm and a sheet resistance of 290 Ω/□ for the as-grown heterostructure. Even without annealing, linear ohmic contacts were achieved with around 1 Ωmm. The electrical contact is formed with the GaN cap layer without

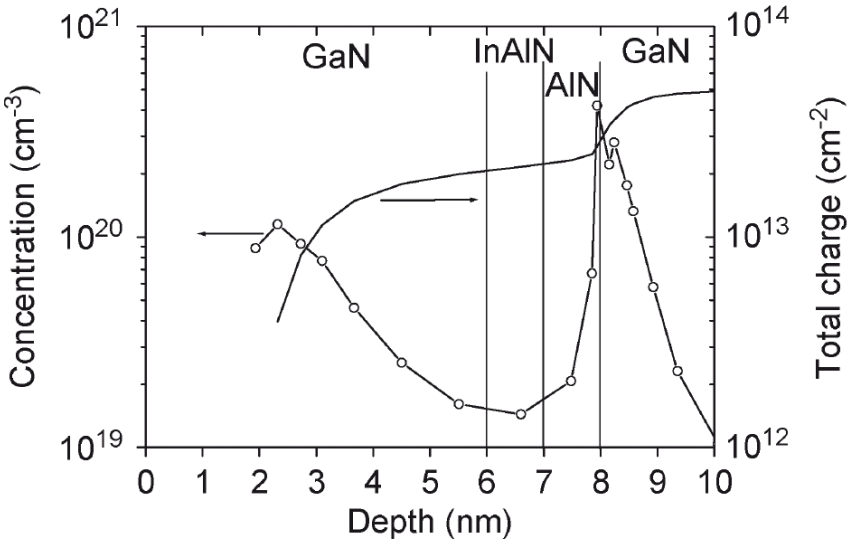


Figure 6.4: Apparent electron density of as-grown structure (wafer A 1592, see App. A) profiled by mercury probe [198].

recess. It is believed that the main transport mechanism between the cap and the 2DEG is tunneling [67, 68]. The highly doped layer together with the ohmic metal should cause sufficient decrease of the barrier potential to provide a good contact through the barrier. The GaN cap layer of E-mode devices patterned with a poly-methyl methacrylate (PMMA) gate mask is selectively etched in an inductively-coupled plasma (ICP) RIE system using a mixture of $SiCl_3$ and SF_6 gases as described in chapter 5.3. Using a selective etching process allows a reproducible and well controlled fabrication. The gate metallization directly follows the gate recess using the same mask, allowing simple device scaling which is required for high frequency performance. It was found out that if the recess is performed sufficiently long, no additional side wall insulation is required between the gate and the GaN cap. It is however a critical time window in which the recess process had to be performed. Figure 6.5 compares a few devices with different etching time. No absolute values of etching times are shown because the etching time strongly depends on the position of the sample on the wafer. All recess processes have been done at least as long as suggested by the etch rate found in 5.3. However, additional etching is required to underetch the sidewall layer. If the gate touches the remnant side wall the gate contact becomes ohmic (curve 1 in figure 6.5). Further etching improves the gate leakage current causing a Schottky-like IV characteristic. Therefore, the process requires a uniform wafer and a very stable etching environment in order to achieve reliable results.

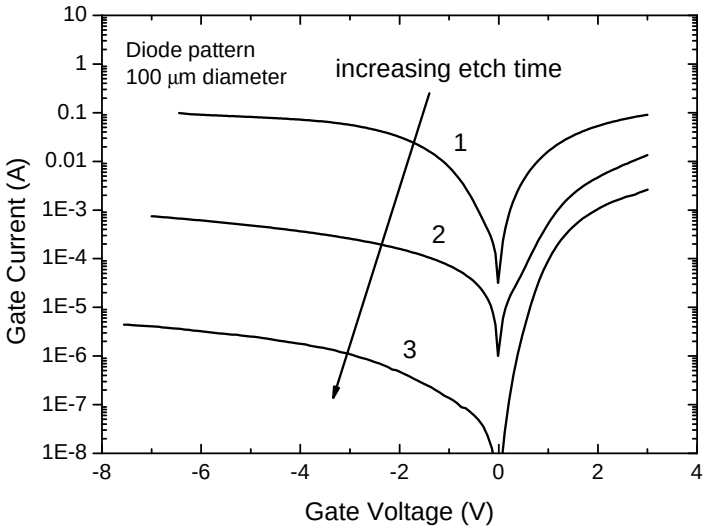
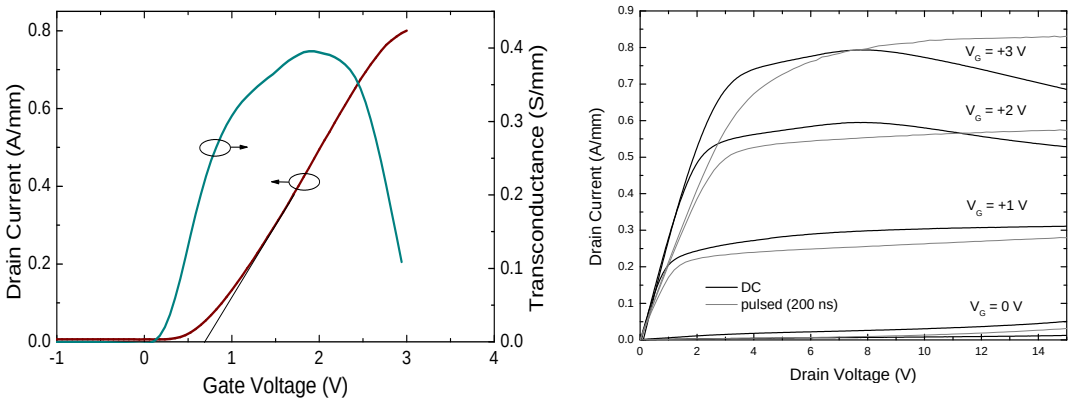


Figure 6.5: Gate current of recess gate E-mode device for samples with different etching time.

6.4 Experimental Results of E-mode Devices

The electrical characteristics (wafer A 1592, A 1589, A1732, see App. A) in figure 6.6 show a drain current I_{DS} of 0.8 A/mm for the E-mode device with 500 nm gate length and a threshold voltage of +0.3 V. The linearly extrapolated threshold voltage from the transfer characteristics (Fig. 6.6a) is +0.7 V. These results are in good agreement with [195], where authors analyzed the dependency between barrier thickness and threshold voltage. The maximum transconductance is 400 mS/mm which is one of the best results for enhancement-mode devices. However, the maximum device current is below typical InAlN HEMTs and therefore the transconductance is expected to be reduced in comparison to the actual barrier thickness of only 2 nm. Further experimental results and improvements of the transconductance are presented in the chapter 7. Pulsing the gate with 100 ns long pulses shows only a slight increase of the on-resistance for the unpassivated E-mode device. It is assumed that the apparent knee walk-out is related to variations of the surface potential resulting in slight current reduction as shown by the simulation. This could be improved using a thicker cap layer and shows that the 6 nm GaN cap might not be sufficient. However, no decrease of the drain current was found for any pulsed measurement up to 20 V drain bias on devices with source drain distance up to 16 μm.

The 3-terminal gate leakage current was 4 mA/mm at V_{GS}=2.5 V and V_{DS}=6 V. IV measurements on circular diodes at room temperature and liquid nitrogen temperature



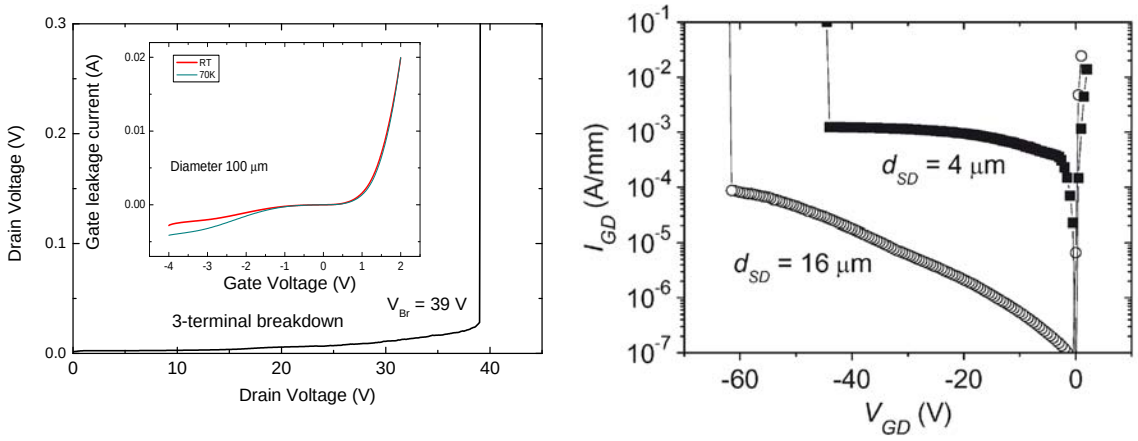
(a) (b)

Figure 6.6: Transfer characteristic (a) and output characteristic (b) of E-mode device in DC and pulsed operation [193].

(77 K) did not show any significant improvement for lower temperatures (inset of fig. 6.7a). Hence it can be argued that the gate current is dominanted by tunneling through the 2 nm barrier.

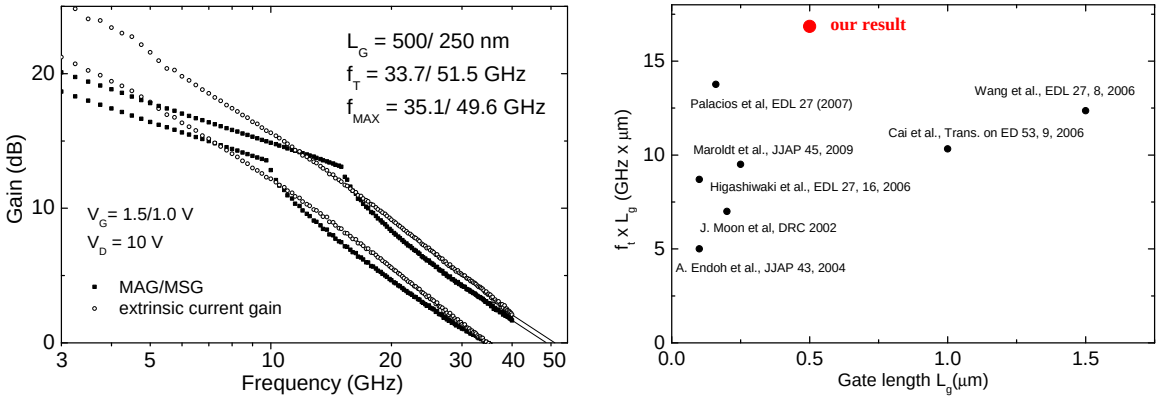
The abrupt 3-terminal breakdown measured in off-state at V_{GS}=-1 V occurs at about V_{DS}=40 V for a 4 µm source-drain distance design. However, the measurement in figure 6.7a shows significant buffer leakage which was already indicated by TLM measurements on the buffer. Hence breakdown occurs through the buffer and is not representative for the device. Higher breakdown voltages should be expected for an improved buffer quality. Additional measurements at devices with even larger source-drain distance but with higher buffer leakage resulted in lower breakdown voltages [198]. A better idea is to measure the 2-terminal breakdown between gate and drain. Figure 6.7 shows a breakdown voltage of V_{GD}=-45 V for d_{SD}=4 μm that scales with increasing gate-to-drain distance. This indicates that the breakdown is not initiated in the area around the gap between the gate and the GaN cap.

The small signal parameters were extracted from the extrinsic S-parameters in the microwave probes plane. The current-gain cut-off frequency f_T was 33.7 and 51.5 GHz for the 500 and 250 nm gate length device, respectively (Fig. 6.8a). The improvement can be explained by the reduced gate capacitance for shorter gate length and without significant increase of the transconductance for the shorter gate length. Comparing the figure-of-merit $L_g \times f_T$ of the 500 nm gate length device to previous results [191, 190, 199, 192] shows the high potential of the design to achieve even better performance. The access resistance with its large source-drain distance is probably the reason for



(a) (b)

Figure 6.7: 3-terminal breakdown measurements (a) and 2-terminal breakdown (b) between gate and drain [198] of the E-mode device. The inset in figure (a) shows the 2-terminal gate leakage measured at room temperature and cryogenic temperature (77 K).



(a) (b)

Figure 6.8: Comparison of small signal results (a) for devices with 250 and 500 nm gate length. Summary of figure-of-merit $L_g \times f_T$ (b) for state-of-the-art GaN enhancement-mode devices [193].

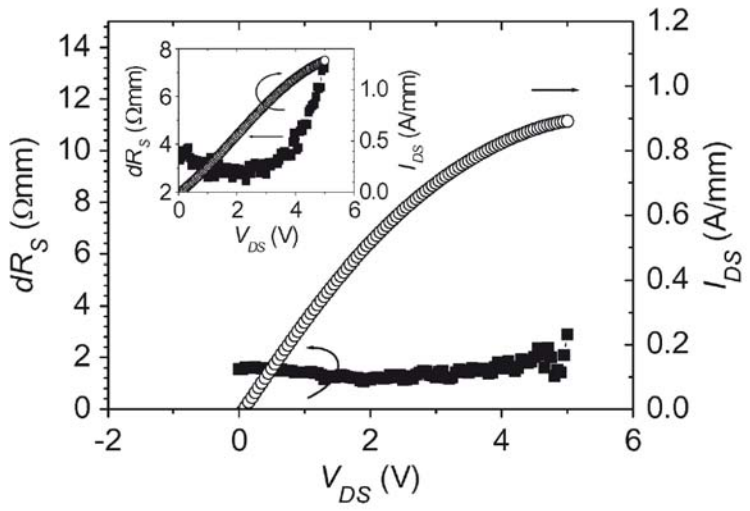


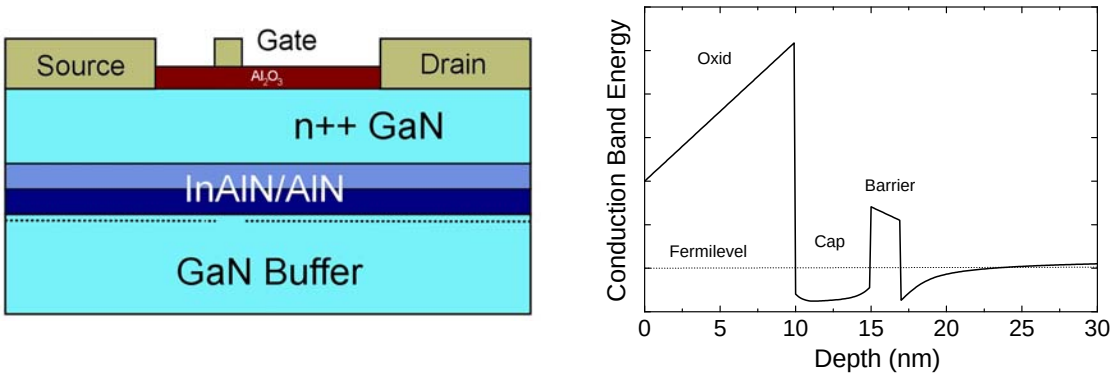
Figure 6.9: Differential source resistance dR_s determined from E-mode device with 6 µm source-drain distance. The inset shows the dR_s measured on a standard InAlN HEMT without n^{++} cap [198].

the worse scaling behavior of the 250 nm gate length device. The power gain cut-off frequency f_{max} was in the same range as f_T due to the non-optimized buffer.

In addition to the small signal analysis, the change of the differential source access resistances dR_s due to the drain current I_{DS} was estimated. This is relevant, as the usually noted increase of dR_s (inset of figure 6.9) causes a severe limitation of the large signal linearity of the gain [200]. So far a few authors suggested interface roughness or electron scattering [201] with hot phonons to be responsible for it. For measuring the dynamic source access resistance, the gate contact was forward biased with respect to the channel by introducing a gate current of 20 mA into the channel, while the source was grounded. The drain current was measured at different levels of drain bias. The source access resistance is defined as the derivative of the gate voltage with respect to the drain current [81]. The differential potential drop over the barrier can be neglected as the current through the gate is constant. The result in figure 6.9 shows a constant differential source resistance up to the maximum drain current. This, in addition to the fact that the only 2 nm thin barrier allows gate length scaling below 100 nm without introducing short-channel effects to the device, makes the device design very promising for high frequency applications.

6.5 Depletion-mode HEMTs

In addition to the E-mode device, D-mode HEMTs were fabricated on the same epitaxial design (wafer A 1592, A 1589, A1732, see App. A) using an additional layer of

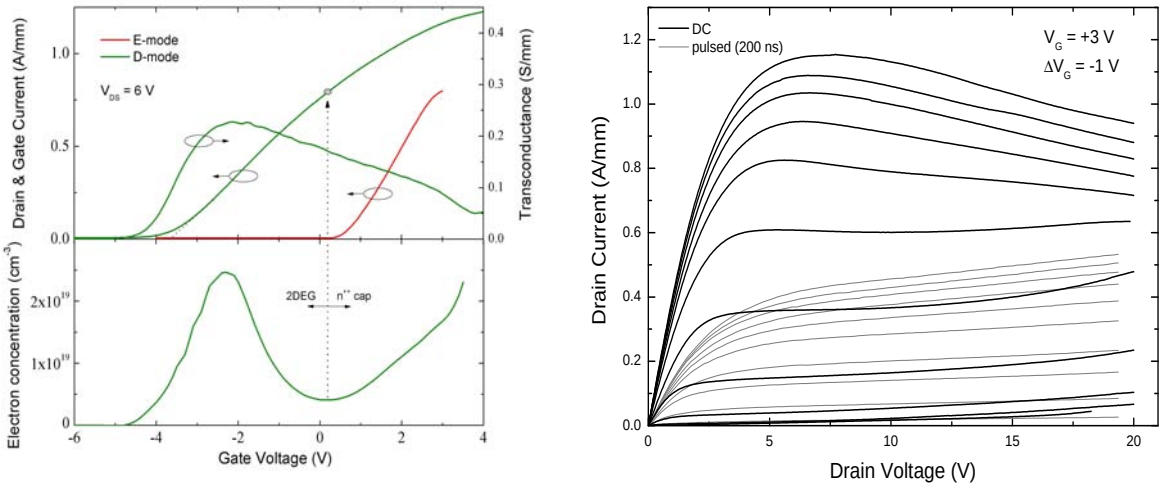


(a) (b)

Figure 6.10: Schematic structure (a) and conduction band (b) of depletion-mode devices [193].

Al_2O_3 for gate insulation on top of the n^{++} cap (Fig. 6.10a). The aluminum oxide layer was 10 nm thick and deposited by MOCVD at 600°C. The schematic conduction band diagram in figure 6.10b shows the whole structure below the gate. The D-mode device consists of two channels which are both vertically controlled by the gate. The carriers in the cap layer require additional gate bias to be depleted and hence lower the threshold voltage.

The linearly extrapolated threshold voltage from the transfer characteristics (upper graph in figure 6.11a) is -3.6 V for the D-mode device. The apparent free electron concentration profile (lower graph of figure 6.11a) obtained from CV measurements on the non-recessed MOS structure shows a clear distinction between the 2DEG and the cap layer, similarly to results obtained by electrochemical analysis. It was expected that these channels both contribute to the drain current if the cap layer is not depleted. For $V_{GS} \leq$0.2 V the cap layer is depleted and the drain current is essentially due to conduction through the 2DEG. Above V_{GS}=0.2 V additional free electrons in the cap layer start to contribute to I_{DS}, while the number of 2DEG electrons saturates. Therefore, a comparison between the maximum 2DEG related drain current of the non-recessed D-mode HEMT at $V_{GS} = 0.2$ V (marked by the gray circle in Fig. 6.11b) with the maximum drain current of the recessed E-mode HEMT at V_{GS}=3 V was possible. This shows no significant current reduction and indirectly proves that our process is damage free. The transconductance of the Al_2O_3 capped heterostructure appears quite flat due to the additional n^{++} layer with a maximum at 220 mS/mm. The output characteristic is shown in figure 6.11b for pulsed and DC operation. The maximum achieved drain current was 1.2 A/mm which however dropped by about 50% for pulsed measurements. This indicates a high surface potential after oxide deposition



(a) (b)

Figure 6.11: Transfer characteristic (a) of D-mode device in comparison to E-mode characteristic. The lower graph shows the apparent electron concentration extracted from CV measurements. Output characteristic (b) in DC and pulsed operation [193].

which has been known also from other reports [117]. It is assumed that a large number of free electrons from the cap layer are trapped at the oxide-semiconductor interface or inside the oxide layer. Hence, only a few free electrons are available to shield the channel from additional injected electrons from the gate into the oxide under negative gate-drain bias. Conclusively, it is expected that the drain current is dominated by electron flow through the 2DEG channel rather than parallel conduction through the cap layer.

6.6 Effect of n^{++} GaN Cap on Access Resistance

The electrostatic properties of the GaN surface cap have been discussed earlier in this chapter showing the possibility of free carriers therein. Further, the electrical results of the E-mode device have proven the shielding effect by free carriers in the cap. In contrast, no shielding was seen for aluminum oxide passivated structures on the D-mode device, possibly due to increase of the surface potential. However, so far the questions whether there is a parallel conduction through the GaN cap and if it contributes to the source-drain current could not be answered with certainty. The results in table 6.1 will therefore discuss TLM measurements on different epitaxial structures using different device structures .

The first structure refers to the E-mode device without any recess. The sheet resistance R_{sh} was measured from TLM measurements. The second one was extracted from the

#	TLM result	sheet resistance $R_{sh}(\Omega/\square)$	contact resistance $R_c(\Omega\text{mm})$
1	non-recessed 6 nm GaN cap structure (E-mode device)	(250) 289	0.3
2	access area (R_S+R_D) of reccessed 6 nm GaN cap (E-mode device)	475	0.85
3	non-recessed 6 nm cap passivated with Al_2O_3 (D-mode device)	460	0.95
4	non-recessed 10 nm cap passivated with ZrO_2	(230) 198	0.5

Table 6.1: Comparison of sheet and contact resistance for different GaN/InAlN/AlN/-GaN heterostructures. The values in the bracket refer to Hall measurements performed directly after the growth (#1-3: wafer A 1592, A 1589, A1732; #4: wafer A 1733, see App. A).

access region (R_S+R_D) of the regular E-mode device with recessed gate [198]. The access resistance was extracted using the method described in [81]. The third sample refers to regular TLM structures on the D-mode structure using Al_2O_3. The last result was measured on a different wafer using 10 nm of n^{++} GaN instead (wafer A 1733, see App. A) and passivated with ALD-deposited ZrO_2. The sheet resistance decreased after oxide deposition in contrast to the Al_2O_3 passivated device.

Comparing the first two results of the E-mode device shows a large increase of the sheet resistance if the GaN cap layer is partially recessed. Hence, one can conclude that the conduction through the cap builds a separate channel which plays only a role if it is fully connected from source to drain. The barrier resistance between the two channels is too high and the cap channel is irrelevant for drain current of the recessed E-mode device. This conclusion is not favorable for the access resistance of the device but explains the exclusion of the GaN cap from the device breakdown. Results mentioned above are confirmed by the increase of the contact resistance of #2 in contrast to #1 (Tab. 6.1). Including the conduction through the GaN cap (#1) reveals a lower contact resistance directly to the GaN cap. Without this channel, the electrons need to tunnel through the InAlN/AlN barrier and therefore the contact resistance increases. Sample #3 exhibits a comparable sheet resistance to sample #2 verifying the results from pulse measurements on the D-mode device which indicated the absence of free carriers in the cap layer. Hence the contact resistance is similar to the E-mode devices. The final structure exhibits the lowest sheet resistance with regard to the thicker GaN cap layer and the apparent surface potential decrease. The GaN cap channel in this

structure provides a better conduction than the quantum well channel, which should have a comparable 2DEG density as the other samples (#2, #3).

Considering this device for RF applications requires further investigations towards the parasitics of this potential parallel channel, even if they do not contribute to the total drain current. One reported solution has been a thicker, low-doped GaN layer without free carriers which simply reduces the influence of the surface by moving it far enough away from the channel [202]. Such idea however, involves new technological challenges.

6.7 Application-based Device Variation

Considering the presented devices for typical transistor applications (chapter 3) raises the question about particular benefits of the proposed device in certain fields. The high frequency performance together with the results of the pulsed-IV measurements presented earlier suggest already the great potential for RF power device. The following two sections give some insight into digital circuits realized by a combination of the D- and E-mode device and further device variations for switching applications.

6.7.1 Digital Applications combining E- and D-mode Devices

The fact that the presented devices can be implemented on the same substrate allows realizing combinations of both devices as integrated circuits for digital applications. In contrast to the well established and low-cost production of silicon-based CMOS technology, GaN offers a few exotic features as operation at extremely high temperatures or in harsh environment. Besides, GaN would solve several problems, summarized in table 6.2, which may become dominant device issues in the coming years.

However, complementary logic as it is standard in silicon-based technology is hard to achieve due to the lack of reasonable p-type doped GaN layers and less beneficial electrical parameters for hole-based devices. Therefore an option which allows building logic circuits is the combination of enhancement-mode and depletion-mode devices. Having E-mode devices available requires only a single voltage source and leads to two possible circuit indicated in figure 6.12. The voltage mode is based on a normal differential amplifier. A „high" input signal on one of the two inputs turns on the according transistor and reduces the output voltage to the open source-drain voltage of that device. If both inputs are „low", the source-drain current through the devices is zero and hence the output potential is close to V_{DD}. The upper D-mode device serves as an active load which operates either in linear or saturation mode [55]. The behavior of such a device is called a NOR gate. Alternatively, the devices can also be arranged

III-N properties	Benefit for digital circuits
Large E_g of GaN (3.4 eV)	Low drain to source and band to band tunneling
	High operation temperature with high power dissipation
High 2DEG density	High current density ~ 2 A/mm [184]
High effective mass	Enhanced channel confinement and gate control
Highly doped InN	Low source/drain resistances
Crystalline AlN cap layer with low interface state density	Low gate leakage
Large polarization	No dopant fluctuations [203, 113]
$v_e \sim 3 \times 10^7$cm/s, for $L_G < 10nm$ $v_{ballistic} \sim 7 \times 10^7$cm/s [204, 205]	High electron velocity and mobility

Table 6.2: Properties of III-N semiconductors and their benefits for digital devices [206].

in current-mode shown in 6.12b, which (in contrast to the voltage-mode) has a high fan-in but a low fan-out and allows optimization of the gain and circuit speed. Therein, the output transistors are „on" if the current into the input knot is zero. Otherwise the current from the input is mirrored to the second path and reduces the potential on the gate of the output transistors.

In order to demonstrate such device circuits, two E-mode devices were combined and connected to a single D-mode device, where all transistors had a gate width of 25 μm (Fig. 6.13). Hence, the β-factor ($= W_{G,E-mode}/W_{G,D-mode}$) was 2, causing a relatively high „low" leve, which is still sufficient to drive the next logic input. Designing a higher β-factor improves the switching characteristic but reduces the speed of the circuit. The electrical results further show a noticeable input current at the gate and a load current below 4 mA.

6.7.2 Enhanced E-mode Design for Switching Applications

The recessed GaN cap device with a 2 nm thin barrier proved to be working in enhancement mode (chapter 6.4). Additional thinning of the interface capacitor by post-fabrication annealing could further increase the threshold voltage from 0.3 to 1 V

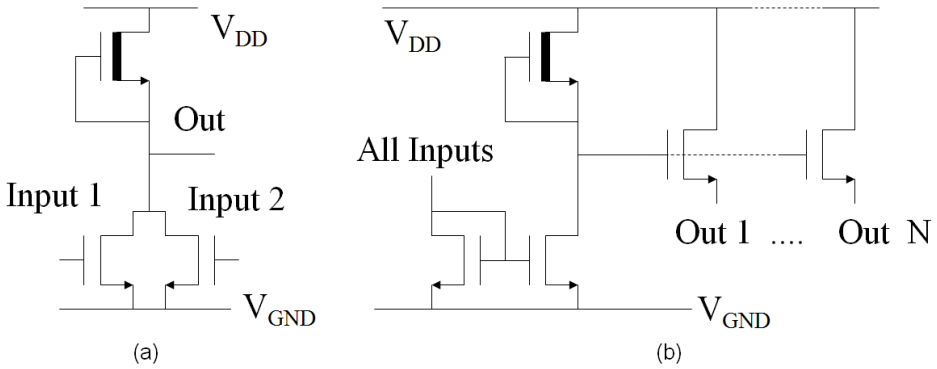


Figure 6.12: Logic circuits in (a) voltage-mode and (b) current-mode.

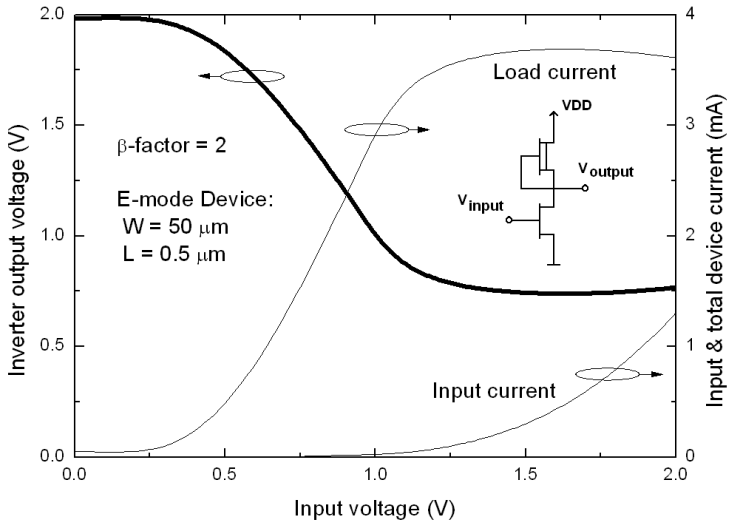
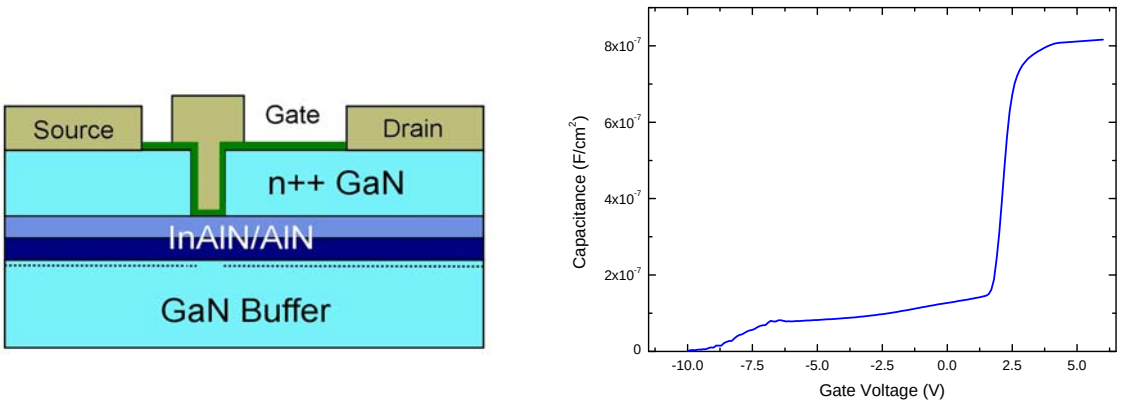


Figure 6.13: Electrical characteristic of logic inverter made of E- and D-mode device as shown in the inset.

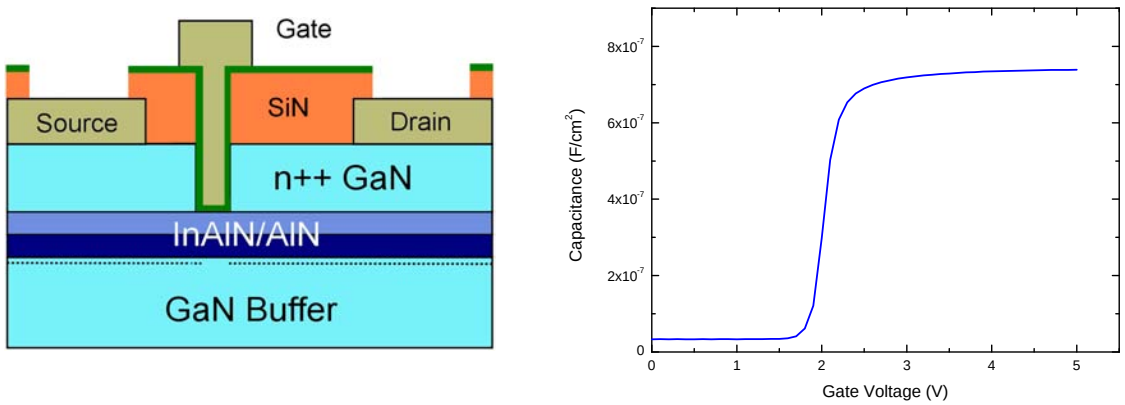


(a) (b)

Figure 6.14: Schematic of recessed E-mode device (a) with inseration of a thin oxide (green layer) after gate recess. The graph in fig. (b) shows the CV measurement using the design with an overlapping gate on top of the oxide, indicating the parasitic capacitance below the threshold voltage at around 2V [122].

(chapter 7), which is already an excellent result considering that no other mechanism as fluorine implantation or barrier doping has been implemented. However, if the device design should be considered for switching applications typically a threshold above 1 V with a reasonable voltage swing to at least 5-6 V needs to be achieved. This is certainly not achievable with the current design as the gate leakage of the Schottky barrier gate gets too high. Therefore the design needs to be altered by inserting an additional oxide below the gate.

Device processing was done equally to previous shown devices until the preparation of the gate mask. All samples were fabricated on the same epitaxial stack grown on silicon substrates (wafer A 1818, A 1819, A 1874, see App. A). The gate fabrication process so far was done in a self-aligned manner, using the same mask for recessing and metal deposition. If an additional oxide layer needs to be inserted between these two steps, two masks are required for the recess and the lift-off process. Alternatively, a thin metal layer could be deposited after recessing, which can be oxidized in oxygen ambient at low temperature or using soft oxygen plasma. However, the quality of such layer may be poor and the photolithographic mask of the gate should not be damaged during this process steps. The design, using two mask for the gate is shown in figure 6.14a. The gate metal mask needs to overlap with the recessed gate finger in order to get a functioning device. This overlap, however, causes parasitic capacitance as seen from the gate capacitance measurement (Fig. 6.14b). In fact it works as a parallel gate with a threshold voltage around -10 V similarly as the depletion-mode device presented earlier. Depending on the oxide layer, the overlapping gate causes an earlier



(a) (b)

Figure 6.15: Improved design (a) with additional SiN spacer to seperate the overlapping metal gate area from the highly doped GaN cap. The corresponding CV graph (b) shows no parasitic compontents after inseration of 100 nm SiN [122].

oxide breakdown and enhanced gate leakage.

In order to prevent both effects, a 100 nm SiN layer was inserted between the GaN cap layer and the overlapping part of the gate metal by being deposited before preparation of the gate recess mask (Fig. 6.15a). In that sense, both layers were subsequently recessed by different recipies. For etching SiN a higher self-induced bias could be used during the RIE process, as the damage would be caused only in the area of the GaN cap which would be removed afterwards. Therefore the layer was etch by N_2:SF_6 (20:2) at 100 W CCP power and 6 mTorr (see chapter 5.2). Another benefit of the additional SiN layer is that the whole device, except the recessed area, is covered and contamination of the chamber during oxide deposition can be limited. The deposition was done by atomic-layer deposition (ALD) which guarantees excellent isotropy and hence a good coverage of the side walls. The CV result of the design with SiN spacer shows no noticeable additional parasitics below threshold voltage (Fig. 6.15b).

The IV results of the same structure using 10 nm ZrO_2 are shown in figure 6.16. A maximum drain current of 400 mA/mm could be achieved at 6 V gate bias, where the sheet resistance of the hetereostructure measured by TLM was above 500 Ω/□. This increased resistance in comparison to previous results on sapphire substrates arises from the higher number of defects and reduced crystal quality of the GaN buffer as the silicon substrate provides a higher lattice mismatch to GaN. Fabricating such devices on the same wafer as the E-mode HEMT (chapter 6.2) should in fact exceed those results as the gate leakage is improved. The threshold voltage was above 2 V. The breakdown of the oxide in forward bias direction occurred between 8 to 10 V. The on/off ratio of the current is 4 orders of magnitude were the off-current is dominated by buffer

leakage. The gate leakage is 7 orders of magnitude lower than the drain current level in on-state, which is a significant improvement in contrast to the Schottky barrier device. The off-state breakdown was dominated by increasing buffer leakage and could therefore be only measured until 20 V.

Comparing these results to the one of the same structure but with Schottky barrier gate rises the question of the origin of the increase of the threshold voltage. The surface potential of the heterostructure may be increased by depositing an oxide on top of the structure, depending on the deposition method [117, 124]. In addition, interface charges influence the electric field of the oxide barrier which together with the metal work function has impact on the energy difference between the conduction band and the Fermi level (Fig. 6.17a). Therefore a series of devices has been fabricated using different thicknesses of ZrO_2 while the rest of the structure was not varied. The threshold voltage was mapped across the sample. The result can be seen in figure 6.17b, indicating a decrease of V_{Th} with increasing oxide thickness. The structure was further simulated using the 1D Poisson-Schrödinger solver using material parameters for ZrO_2 from [207, 208, 209]. Interestingly, the work function of Ni (5.1 eV) at the interface to ZrO_2 is reduced by surface pinning which results in an effective metal work function of 4.7 eV [209, 208]. The band offset of ZrO_2 to GaN was found to be 1.1 eV and -1.5 eV to AlN [209, 210]. The bandgap of InAlN is between AlN and GaN and therefore the band offset to ZrO_2 is expected to be around 0 eV.

Analyzing the band structure in figure 6.17a shows that the whole structure does not contain any free carriers. The highly resistive GaN layer is fully depleted as well as the barrier. Considering the device structure with micrometer distance (in contrast to the nanometer scale of the heterojunctions) allows assuming an infinite depleted GaN buffer. Hence, any potential change at the surface by varying the gate voltage will shift the whole conduction band up and down as if it would be floating. The potential drop from the barrier to the 2DEG is insignificant as the buffer is considered to be infinite (or at least much wider than the area around the heterojunction). Furthermore, trapped electrons (with trap energy smaller than thermal energy $E_T < 3kT$) in the barrier or semiconductor/oxide interface can be considered as fixed charges for $V_G < V_{Th}$ without the emission of holes.

The floating characteristic of the band structure (Fig. 6.17b) allows estimating the energy between the GaN conduction band and the Fermi level as the energy related to the threshold voltage (Fig. 6.17a). The linear trend in figure 6.17b is therefore a direct link to the electric field in the oxide layer causing the shift of the threshold voltage for different thicknesses of the oxide. Taking into account the voltage shift for a certain thickness variation reveals an interface charge density of $+7 \times 10^{12}\, cm^{-2}$.

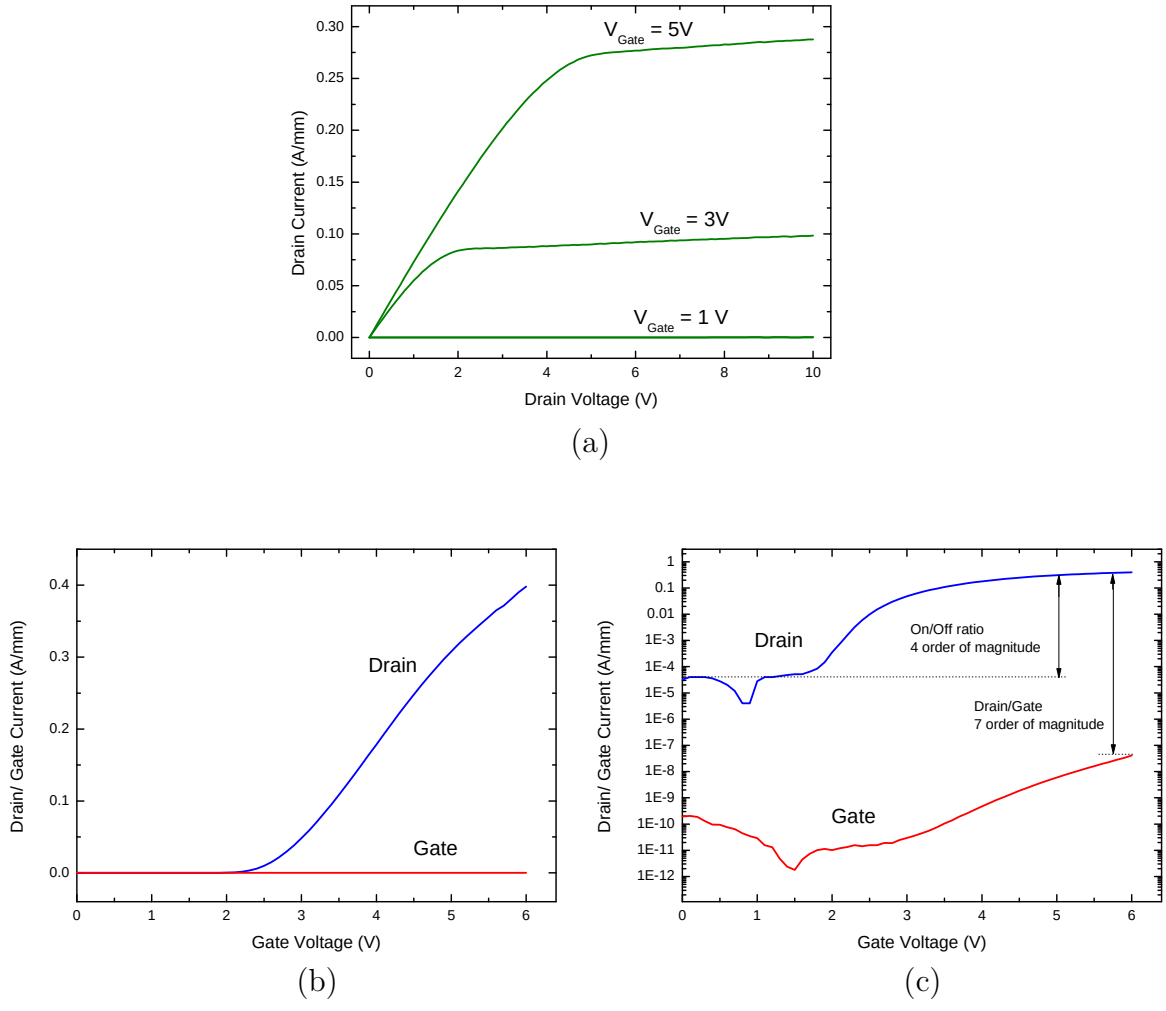


Figure 6.16: Electrical results of the device design using a 10 nm thin ZrO_2 and a 100 nm thick SiN spacer. The output characteristic (a) and transfer characteristic in linear (b) and logarithmic scale (c) prove the strong improvement by the advanced design (wafer A 1818, A 1819, A 1874, see App. A) [122].

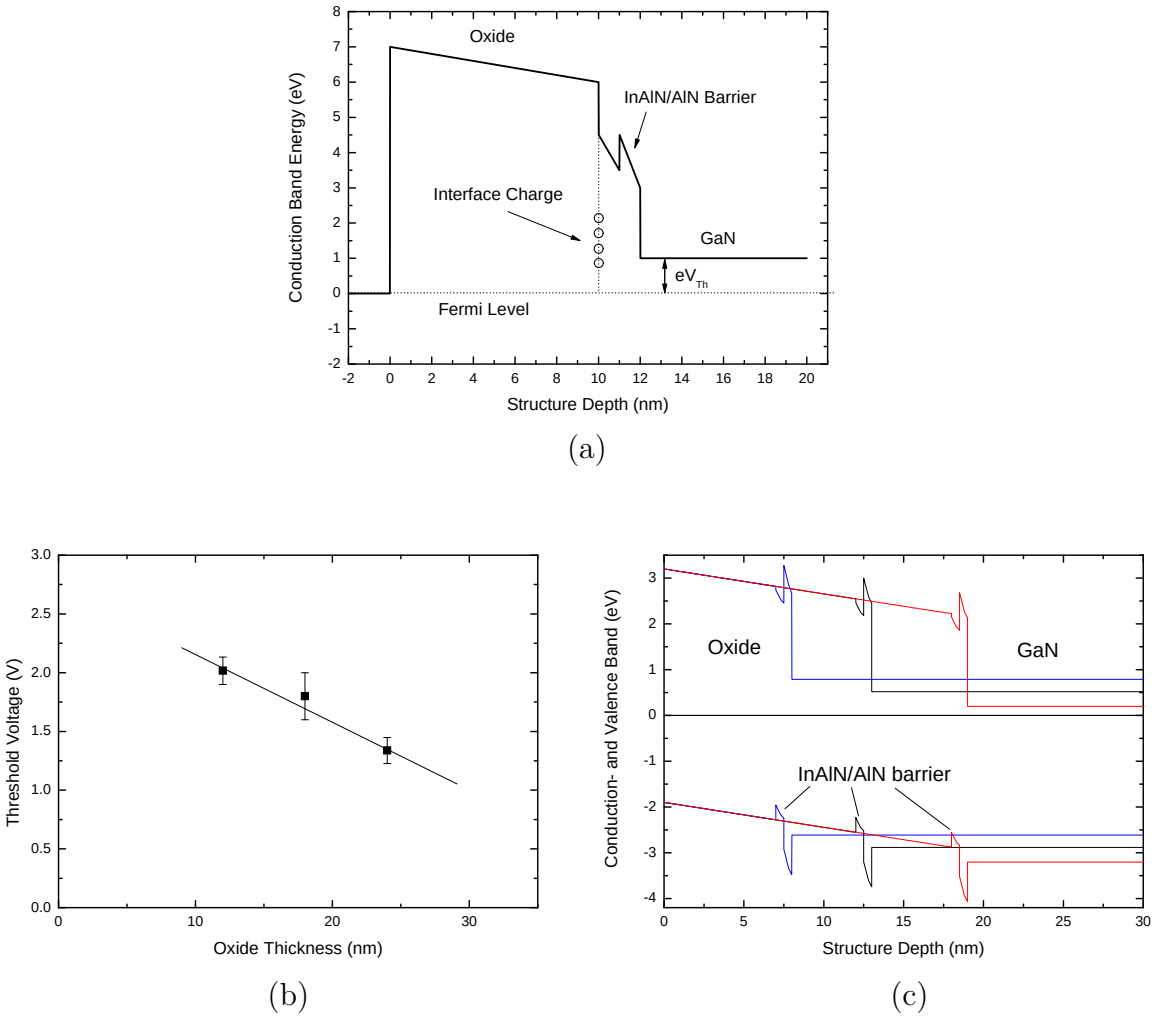


Figure 6.17: Schematic of the conduction band (a) with oxide and InAlN/AlN barrier. The interface charge is assumed to be positive, bending the band of the oxide downwards, according to the trend of the threshold voltage (b) with increasing oxide thickness [122]. Simulation results of the band structure (c) for different oxide thickness assuming material parameters of ZrO_2 from [207, 208, 209].

As the device structure is assumed to be free of mobile charges, the counter charges must be in the gate metal. It is assumed that the interface charges originate from unsaturated bonds causing donor-like traps as described by the virtual gate effect [84]. So the trend of the threshold voltage allows comparing the threshold voltage of the Schottky barrier device ($V_{Th} = 0.3$ V) and the projected threshold voltage $V_{Th} = 2.7$ V at an oxide thickness of t=0 nm (Fig. 6.17b). Considering the assumptions made above, it can be concluded that the deposition of the oxide causes a surface potential increase of the InAlN/AlN barrier of 2.4 eV. In this device design, we gain large benefits from this surface potential increase. If the same ZrO_2 layer is deposited directly on the surface of a HEMT structure without GaN cap layer, it will cause a depletion of carriers in the 2DEG and an increase of the sheet resistance. Similar observations have been made by the deposition of Al_2O_3 used in chapter 6.5. It can only be speculated why the surface potential is increased. Pietzka et al. have investigated the surface potential of electrochemically oxidized InAlN layers, showing an increase of 3 eV [117]. In our case, the ALD deposition process was started with a few water pulses without introduction precursors in order to establish a good coverage of OH bonds on the surface [211, 212, 213]. It can be speculated, that this may cause a thin surface oxidation considering the deposition temperature of 200°C.

The same qualitative trend for the threshold voltage was found in the simulation, using the extracted interface charges from the desribed analysis (Fig. 6.17c). However, in quantitative numbers the simulation does not fit the experimental results, achieving a too low conduction band at the GaN layer. This appears obvious by comparing the material parameters with the extracted values above. Hence, the reason of the surface potential increase needs to found elsewhere, which supports the idea of an additional thin layer of surface oxide at the InAlN/oxide interface.

6.8 Summary

A 2 nm thin barrier HEMT was shown based on a selective gate recess fabricated on an n^{++} GaN/InAlN/AlN/GaN heterostructure. The devices operate in E-mode with a threshold voltage of +0.3 V and exhibit excellent small signal performance of f_T =33.7 GHz at 0.5 µm gate length. The maximum drain current is 0.8 A/mm under pulsed and DC operations. By inserting an insulating layer on top of the same epitaxial stack a D-mode device was demonstrated, for potential monolithic integration of E- and D-mode devices in integrated circuits. Analyzing the two structures proves that no current reduction due to the recess process occurs in the E-mode device. Investigations of the differential source-drain resistance revealed no increase for drain voltage up to 5 V. This, in addition to the fact that the only 2 nm thin barrier allows gate length

scaling below 100 nm without introducing short-channel effects to the device, makes it a very promising candidate for high frequency applications. The highly doped GaN cap layer provides no parallel conduction to the 2DEG once it has been interrupted by the gate recess. Therefore, the breakdown voltage seems not to be limited by the cap layer.

Insulating the gate with an additional ALD-deposited oxide increases the threshold voltage above 2 V. The gate swing greatly improves, achieving a drain current of 400 mA/mm at $V_G = 6\,\mathrm{V}$ for the same structure grown on a silicon substrate. The overlapping metal gate was insulated by a thick SiN layer reducing the gate leakage by 4 orders of magnitude in contrast to the Schotty Barrier E-mode device. Scaling of the oxide thickness and modeling of the threshold voltage exhibited an interface charge density of $+7 \times 10^{12}\,cm^{-2}$. The increase of the threshold voltage could not be explained by the band offsets given in literature [208]. Therefore it is assumed, that an additional native oxide layer might be formed during ALD deposition.

7 Analysis of Gate Sinking in Ultra-Thin Barrier Devices

The benefit of having a device with only 2 nm thin barrier is not only the excellent channel control by the gate but also the large gate capacitance which provides a higher sensitivity for analyzing effects of the gate stack. The gate stack in a Schottky-type gate contact includes the barrier and gate metal as well as the interlayer between them. In state-of-the-art HEMT devices with 10 to 20 nm thick barriers, these interlayer can be usually neglected. However, the ultra-thin barrier devices described in chapter 6 allow further insight and investigations of the interfaces between metal and semiconductor. Chapter 7 describes annealing-induced changes of these interlayer which were observed by electrical measurements and confirmed by nanostructural TEM analysis.

7.1 History

The term "gate sinking" is not frequently used in GaN devices and was introduced on AlGaAs/GaAs HEMT devices back in 1986 [214, 215]. Authors referred to gate sinking when the gate metal diffused into the barrier layer and hence reduced its thickness with impact on the drain current and threshold voltage. III-N related barriers show much higher stability and therefore such diffusion behavior was basically not noticed under operation condition. However, during device fabrication, metal-barrier diffusion is known to be part of ohmic contact annealing in AlGaN/GaN HEMT devices [216, 217]. In contrast, InAlN is believed to be stable up to higher temperatures, even though Zhou et. al has reported on ohmic metal diffusion along defects [218]. Even though gate sinking, as it is known from GaAs devices is not an issue in GaN and even less in InAlN devices, several other mechanism mainly by degradation due to hot electrons [126] or electric field induced strain in the barrier by the inverse piezoelectric effect [77] have been reported on the reliability of devices. Applying high temperature treatments or electrical stress has shown changes in the Schottky barrier height due to reconstruction of the metal-semiconductor interface. Using different refractory metals directly at the interface [219] or as an interlayer [220] could preserve the metal structure during stress and improve the electrical and thermal stability. Singhal et al. have investigated the

commonly implemented Ni-based gate stacks on AlGaN barrier and found an improvement of the Schottky barrier height accompanied by a threshold voltage increase during long-time tests involving thermal stress, which was explained by a modified interfacial layer [221]. Annealing the devices could arrange the interface and hence reduce device instabilities. However, up to date no report has shown gate metal sinking [215] or inter-diffusion into the semiconductor barrier for III-N semiconductors.

7.2 High-Gain Devices through Gate Sinking

Starting with the same recess fabrication as used for GaN-cap recessed Schottky devices in chapter 6 (Fig. 6.2) different gate stacks were applied in order to test the high-temperature stability of the devices up to 800°C. The thermal treatment can lead to numerous effects on the transfer characteristic of the device:

- Reconstruction of the metal-semiconductor interface can influence the Schottky barrier height SBH, which has direct impact on the threshold voltage and the gate leakage.
- Mobile ions can diffuse inside the material. Regarding to the chemical stability of InAlN, this relates only to the outdiffusion of foreign atoms as defects of implanted ions. F^- ions can be implanted during a preceding plasma process.
- Gate metal can diffuse into the semiconductor barrier. Hence, the gate leakage increases because of the reduced barrier thickness.
- Increasing gate leakage enhances the impact of the gate resistance and reduces the effective potential on the gate.

In the described experiment, Ni/Au and Ir/Au gate stacks are compared. Iridium has a melting point of 2466°C and therefore acts as a diffusion barrier, while nickel gates may deteriorate for one of the reasons mentioned above. The samples were immediately annealed after gate metal evaporation in a rapid thermal annealing (RTA) process at 400°C to 700°C for 2 min. The typical transfer characteristics of devices with Ir and Ni gate metals as a function of annealing temperature T_A are compared in figure 7.1. The device characteristics of the non-annealed devices do not differ much and show a threshold voltage V_{Th} of around 0.3 V independent of the gate metal. After annealing, the threshold voltage for the Ir gate electrodes increases up to 1 V and the transconductance improves up to 50%. Interestingly, the drain current I_D of devices annealed at 500°C or higher succeeds the I_D of devices annealed at lower temperatures. Three major reasons can be responsible for this:

- The flatband voltage introduced in chapter 4.1 is lower than the applied gate bias.
- A reduction of the gate leakage reduces the potential drop by the gate resistance.

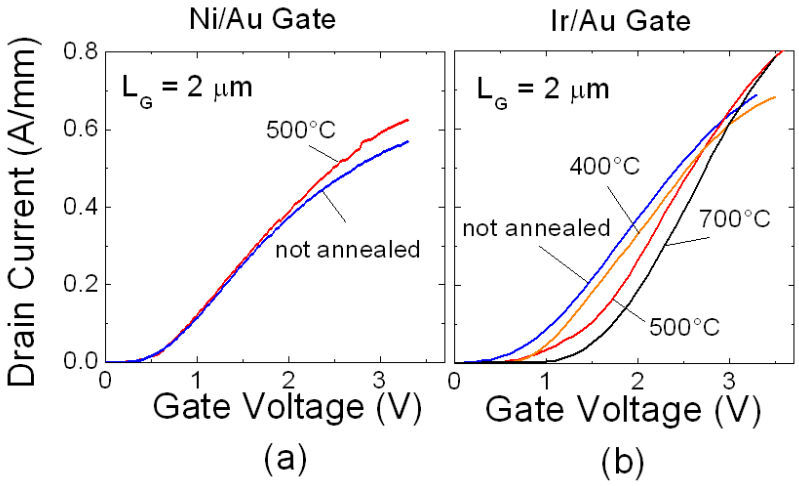


Figure 7.1: Transfer characteristics before and after annealing of (a) Ni/Au and (b) Ir/Au gate stacks [222].

- An increase of the channel mobility, which could be caused by a reduction of defects at the interface to the semiconductor barrier, in the barrier or at the heterojunction.

From a material aspect point of view, the last point is not believed to play a major role [67]. However, the first two aspects both contribute to an unknown degree. Further details on the dynamics of the thermal-induced device changes and the differences of annealing step at 400, 500 and 700°C will be discussed later (chapter 7.3.1), after introducing the capacitive measurement results. In contrast, devices with Ni gates show only a slight increase of the drain current after annealing together with a small improvement in gate leakage current; similar to what has been already observed in AlGaN/GaN devices [168]. The decreasing gate current may follow a reconstruction of the Schottky interface and reduces the influence of the gate resistance and, hence, causes an increase of the drain current.

In addition, it should be noted that the threshold voltage of both metals before annealing is about the same. This is a surprise as one would expect a higher Schottky barrier height of Ir by comparing the result of chapter 4.1 with SBH values of state of the art Ni diodes [120]. However, it is expected that after the recess process the semiconductor surface involves many surface states, leading to pinning of the surface potential Φ_{SP} and hence, reduce the effect of the metal[55].

The measurement was repeated on 500 nm gate length devices which were annealed at 500°C for 2 min. Annealing this device at 500°C for 2 min increased the transconductance from 400 mS/mm to 640 mS/mm (Fig. 7.2). This is one of the highest values for GaN-based HEMT devices and the highest for enhancement-mode transistors in all

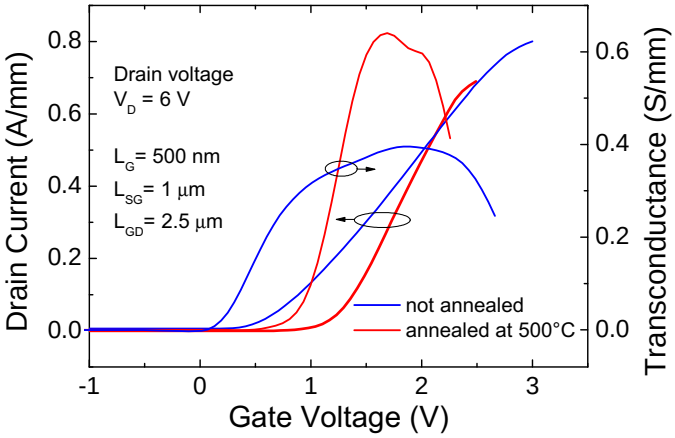


Figure 7.2: Drain current and transfer characteristic of a 500 nm long Ir/Au gate device before and after annealing [222].

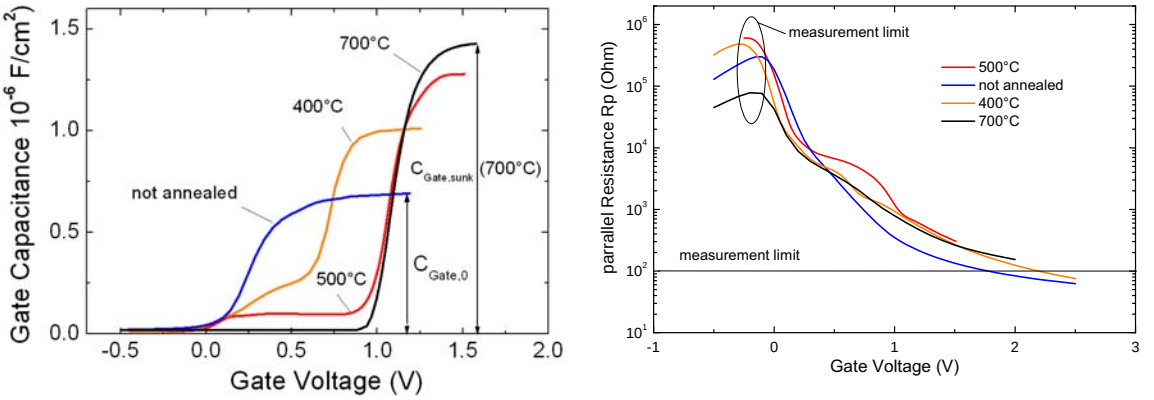
III-N material devices. The slight decrease of the maximum drain current originates from an increase of the sheet resistance due to surface oxidation during the annealing process. It was already shown that shielding of the 2DEG from surface potential variations is limited to a certain potential. In addition surface oxidation of GaN could thin down the cap layer thickness and hence further reduce the shielding effect.

The threshold voltage shift combined with the transconductance increase already suggests a reduction of the electric distance between the gate and the 2DEG channel, even though other reasons as mobility variations may play an additional role.

7.3 Capacitive Analysis of Sinking Process

While the IV analysis reveals the drain current in dependency of the gate action, the capacitive analysis is a much more direct approach in order to derive the electric behavior of the gate stack without influence of the channel mobility.

Before obtaining the CV results several parasitic effects of the measurement had to be taken into account. Most of all the gate leakage in forward direction could become too high for accurate measurements. Therefore the series resistant R_S was taken into account. R_S was calculated from the geometry of the diode design using the sheet resistance of the wafer, which was measured by TLM patterns. Furthermore, testing the LCR meter (chapter 3) revealed an accurate capacitance measurement for a parallel resistance >100 Ω.



(a) (b)

Figure 7.3: Gate capacitance measurement (a) and parallel resistance (b) of Ir/Au diodes without annealing and after annealing at 400°C, 500°C and 700°C, respectively. With increasing annealing temperature the original capacitance plateau decreases and the second plateau of the inhomogeneously sunk gate area at higher threshold voltage increases [222].

7.3.1 Dynamics of the Sinking Process

The typical gate capacitances of Ir/Au gate stacks before and after annealing measured on circular diodes are presented in figure 7.3a. The CV characteristics of Ni gate devices is not shown as it is comparable to the Ir-gate results and does not show a noticeable effect after annealing. Annealing at 700°C causes a shift of the onset voltage of the capacitance, which is consistent with the V_{Th} shift in Fig. 7.1b, and an increase of the maximum gate capacitance plateau. Interestingly, the curves of the gate capacitances annealed at 400 and 500°C suggests an intermediate state between the not annealed one and the one annealed at 700°C. The increase of the capacitance plateau confirms the assumption of an decrease of the electric distance between the gate metal electrode and the 2DEG channel.

7.3.2 Modeling and Analysis

CV characteristics of the non-annealed samples and those annealed at 700°C exhibit only a single capacitance component. In contrast, the samples annealed at intermediate T_A of 400°C and 500°C show CV characteristics composed of two capacitance components. This can be explained by considering that the gate sinking process into an interfacial layer occurs only at a fraction α of the total gate area (Fig. 7.4). The physical aspect behind this is indicated by an interlayer which is partially consumed by the iridium layer during the annealing process. Interestingly, this inhomogeneous

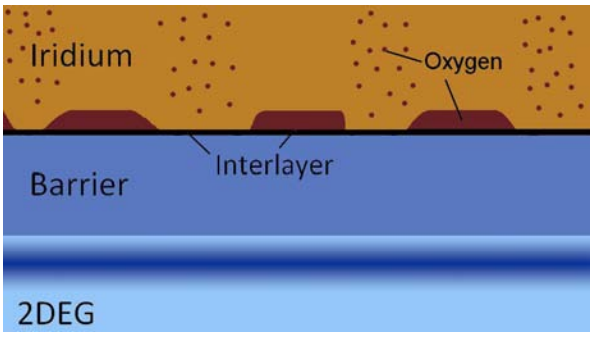


Figure 7.4: Schematic view of the oxygen diffusion and the gate sinking process for a fractional gate area α.

nature of the channel region is also observed in the IV results. While the non-annealed sample and the one annealed at 700°C exhibit an ideal quadratic $I_D(V_G)$ dependency near V_{Th}, those annealed at 400°C and 500°C show a weaker drain current increase until the second onset of the gate capacitance (Fig 7.1b).

All of the first components of the capacitance curves in figure 7.3a have the identical onset voltage as the non-annealed device. This onset also corresponds to the V_{Th}=0.3 V. Therefore, this first component corresponds to the non-sunken area with the capacitance $C_{Gate,0}$, where all capacitances are meant as capacitance per area. The second capacitive component with onset voltages between 0.5 and 1 V is related to the sunken gate area with the capacitance $C_{Gate,sunk}$. Using this terms, the gate capacitance at any particular temperature can be written as

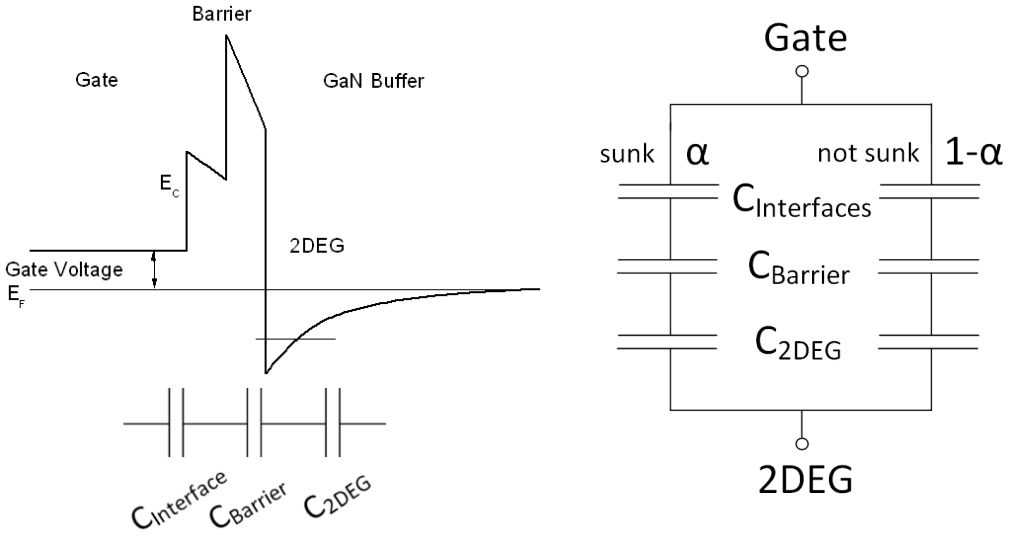
$$C_{Gate}\left(T_A\right) = \left[1 - \alpha\left(T_A\right)\right] \cdot C_{Gate,0}\left(T_A\right) + \alpha\left(T_A\right) \cdot C_{Gate,sunken}\left(T_A\right), \tag{7.1}$$

wherein α and $C_{Gate,sunk}$ are assumed to be not constant with the annealing temperature T_A. At T_A = 700°C, the CV shows only one plateau and thus the capacitance is homogeneously sunken. Hence, $\alpha = 1$ and leads to the maximum achieved gate capacitance $C_{Gate,sunk}$(700°C). As both capacitances, $C_{Gate,sunk}$ and $C_{Gate,0}$, consist extensively of the same gate stack shown in figure 7.5a, the capacitive gate stack can be quantified using

$$\frac{1}{C_{Gate}} = \frac{1}{C_{2DEG}} + \frac{d}{\varepsilon} + \frac{1}{C_{Interface}}, \tag{7.2}$$

where d = 1.9 nm, being the thickness of the barrier measured by TEM, and ε, its dielectric constant, represent the ideal barrier capacitance. $C_{Interface}$ is dedicated to the variable interlayer and C_{2DEG} consists of the finite quantum capacitance [223] and charge centroid capacitance [224]. The quantum capacitance is defined as

$$C_Q = \frac{g_\nu m^* q^2}{\pi \hbar^2} \tag{7.3}$$



(a) (b)

Figure 7.5: Schematic of band diagram (a) with related capative components. Circuit of gate stack (b) with partially sunken interface capacitance.

and quite large in GaN due to the relatively large effective electron mass m^* and therefore its influence can usually be neglected. g_ν in equation 7.3 represents the valley degeneration factor [223]. However, taking into account the charge centroid capacitance due to the 2DEG quantum well lowers the total 2DEG channel capacitance significantly. Using a 1-D Poisson-Schrödinger solver, the 2DEG related capacitance was calculated by simulating the ideal barrier capacitance of a quantum well and comparing it to the ideal barrier capacitance. Using equation 7.2 in order to derive the capacitance of the quantum well results in a C_{2DEG} of $5.0\times10^{-6}\mathrm{F/cm^2}$ at the threshold voltage, which is in the order of the ideal barrier capacitance $C_{Barrier}=\varepsilon/d=4.9\times10^{-6}\mathrm{F/cm^2}$.

The total gate stack using the sunken and non-sunken capacitive components is presented in figure 7.5b, with the area ratio α between the two branches. Applying (7.1) and (7.2) on the results from figure 7.3b reveals the dynamics of the sinking process for each temperatures (Fig. 7.6). The initial interlayer capacitance $C_{Interface}$ is $8.7\times10^{-7}\mathrm{F/cm^2}$ and increases after annealing at 700°C to $3.2\times10^{-6}\mathrm{F/cm^2}$. This final capacitance might correspond to a remaining interlayer of fluorine bound to the InAlN surface. Figure 7.6 suggests that not only the sunken area increases with temperature but also the sunken capacitance increases until annealing at 700°C. It should be noted again that this experiment was done for a 2 min annealing procedure only. Comparing the values of $C_{Barrier}$ and C_{2DEG}, one can immediately see the influence of the interlayer capacitance on the total gate capacitance. Figure 7.7 puts side by side the gate capacitance versus the gate-channel distance. While the ideal gate capacitance

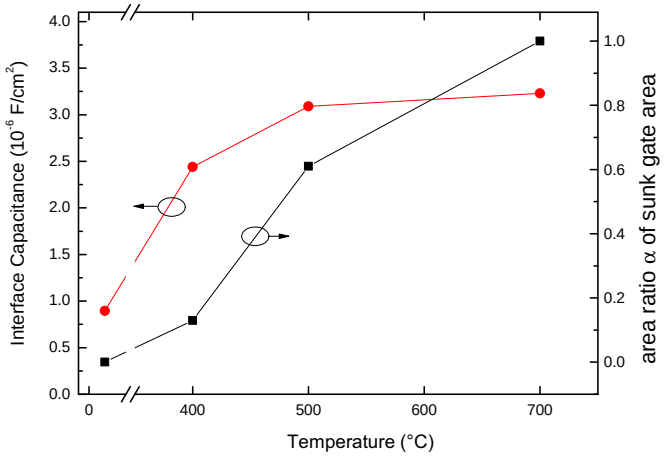


Figure 7.6: Interface Capacitance and area ratio α versus annealing temperatur after extraction.

increases, the non-annealed capacitance remains almost constant for barriers from 10 to 2 nm. Therefore no significant capacitance increase was noted for the original result. The impact of the interlayer as well as quantum well capacitance is therefore of great relevance for scaling of the barrier.

7.3.3 Flatband Voltage Estimation from CV

The flatband voltage was introduced in chapter 4.1 as voltage which causes a flat band at the barrier and allows extracting the Schottky barrier height. However, the method presented there, requires a relatively low gate leakage and an accurate capacitance measurement under forward gate bias. Since this is certainly not the case for the 2 nm thin barrier after recessing, this method cannot be applied. Instead, we can take advantage of having two comparable gate stacks of different thickness. Comparable in this respect means, that the potential differences as the SBH in the stack are assumed to be equal before and after annealing.

From the definition of the flatband voltage, one can note that it is independent of the thickness of the barrier. Therefore two comparable gate stacks of different thickness must have the same electron density in the 2DEG under flatband conditions. Figure 7.8 summarizes the 2DEG density of the non-annealed gate stack and the one annealed at 700°C. The linear result reflects the relation between charge and voltage in a constant capacitor. Extending the linear behavior beyond the measurement limit, let us find the intersection, which corresponds to the flatband voltage of 1.9 V. Using equation 4.2 we can calculate the SBH as 1.8 eV. This value is slightly lower than what was

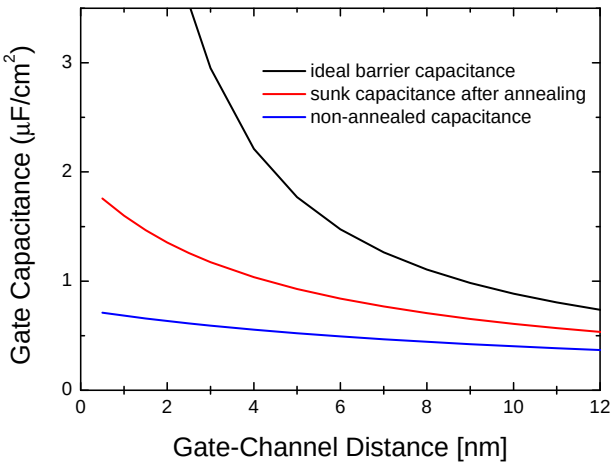


Figure 7.7: Variation of gate capacitance versus gate-channel distance in dependency of the interface capacitance.

found in chapter 4.1 from 10 nm barrier devices with oxide-assisted Schottky contact (chapter 4.1). It is obviouse that this analysis should be seen as a rough estimation, even though the capacitive data used for this calculation were taken after the series resistance correction (chapter 3.5). Without this correction the Q-V relation becomes non-linear for these particular devices. However, the role of oxygen which will be discussed in detail in the next part may have also affect the barrier surface similar as for the device in chapter 4.1.

Finally, the flatband voltage should be discussed in comparison to the intersection of the corresponding IVs in figure 7.1b. First of all, the current voltage relation follows a quadratic behavior around threshold until the electron velocity saturates, which linearizes the relation [81]. At high forward bias the transconductance decreases as the impact of the gate resistance increases. Therefore a comparison between the IVs cannot be done without having a complete model of all this three sections and its parameters.

7.4 Nanostructural Analysis

The previous derived model was verified by investigating the structures before and after annealing by high-resolution transmission electron microscopy (HR-TEM) with additional mapping of oxygen and iridium detected by electron energy loss spectroscopy (EELS) in figure 7.9. None of the HR-TEM shows evidence of an distinct interlayer between Ir and InAlN, but the bright appearance at the Ir/InAlN interface indicates a low concentration of materials with medium or high Z (atomic number). As oxide

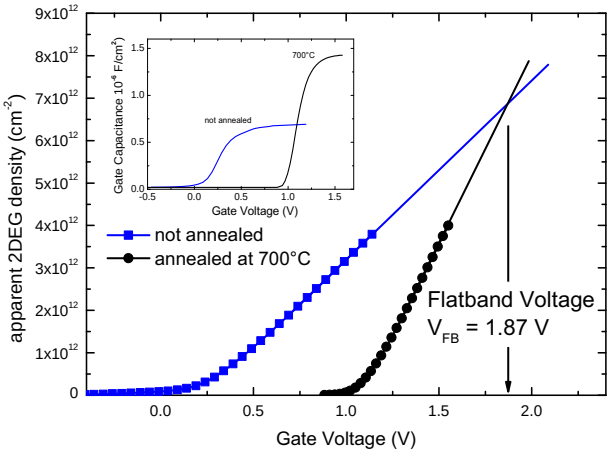


Figure 7.8: Extraction of flatband voltage using CV with different barrier thicknesses.

should exhibit a similar contrast to the surrounding semiconductor material, we expect that no interfacial oxide has been formed [222]. However, a high concentration of oxygen confined at the Ir/InAlN interface is detected by EELS. We believe that oxygen is not able to form an aluminum or indium oxide layer since both are terminated with fluorine from the recess process [222]. During annealing, no stable iridium oxide forms due to its low formation energy (H_f = -249 kJ/mol for IrO_2 [225]); instead oxygen is able to diffuse into the Ir layer as seen from EELS images after annealing at 500°C (Fig. 7.9). Diffusion of oxygen thus reduces the oxygen-rich interlayer, as depicted in the model presented in the figure 7.4. In addition, the diffusion length of oxygen in evaporated iridium is only in the order of 1 nm for 2 min annealing at 500°C [226]. Therefore, oxygen cannot diffuse efficiently in dense iridium at that temperature. We assume that oxygen diffusion is enhanced by crystal defects and grain boundaries, which is a direct explanation for the inhomogeneous O concentration in the Ir layer and the electrically observed inhomogeneities [222]. Annealing at 700°C increases the diffusion length to about 100 nm [226] and allows for a homogeneous diffusion of oxygen into iridium, leading to the most complete removal of the oxygen interlayer, as seen from the CV measurements. In contrast, Ni is known to form a thermally stable interlayer [221] and therefore electric devices variations are mainly due to changes in the Schottky barrier height. In addition, the TEM analysis proves that the thickness of the InAlN/AlN barrier does not change after annealing and metal does not diffuse into the barrier. This confirms the already proven robustness of InAlN [68].

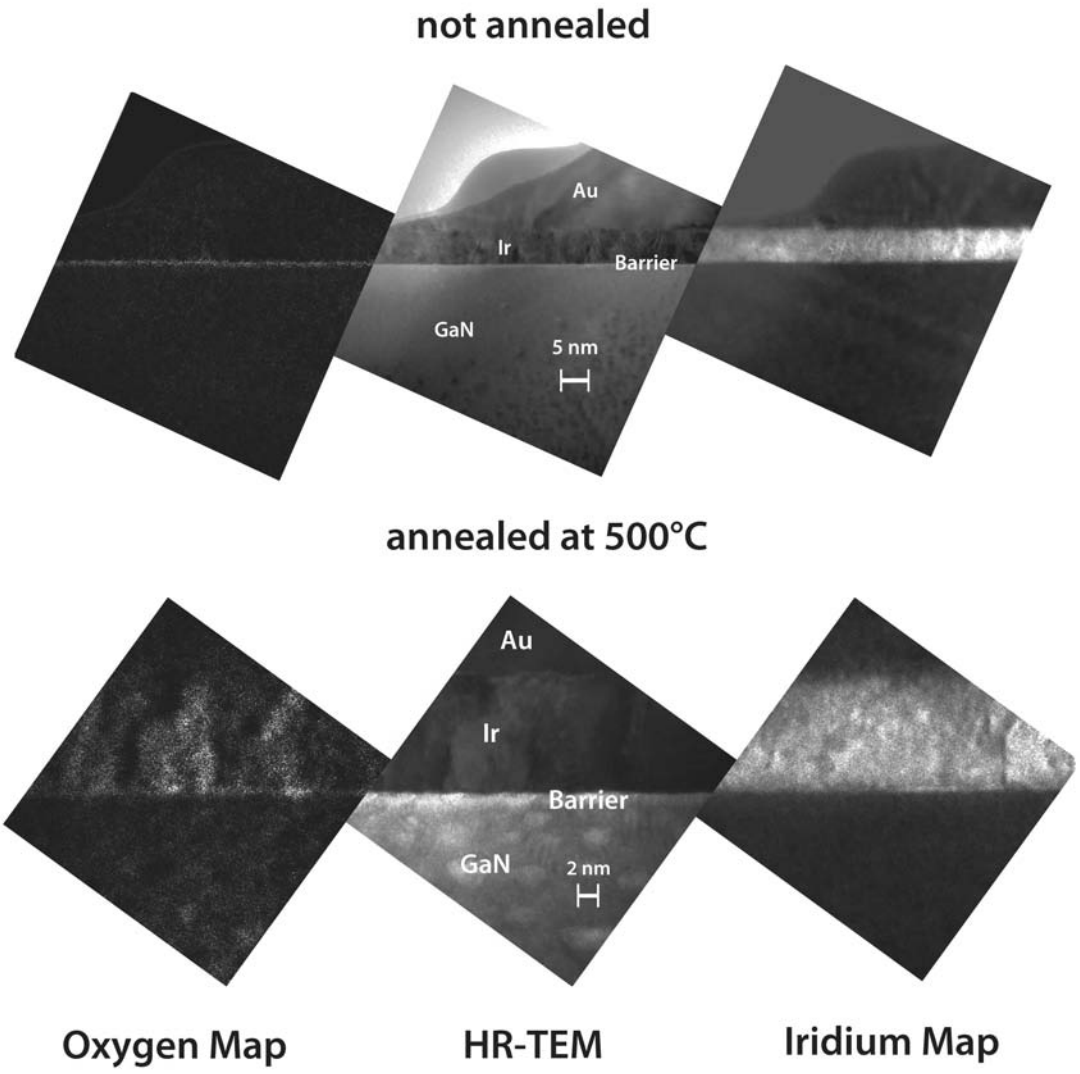


Figure 7.9: TEM image and corresponding EELS oxygen and iridium map of the 2 nm barrier with Ir/Au metallization before and after annealing at 500°C. Bright areas in the EELS images correspond to the mapped element [222].

7.5 Summary

In conclusion, we observed an increase of the gate capacitance by a factor of 2 after annealing at 700°C of Ir-gate HEMTs with a 2 nm thin $In_{0.17}Al_{0.83}N$/AlN barrier [222]. Diffusion of oxygen from an interfacial layer into iridium seems to be responsible for this sinking effect, which was not detected for Ni based gates. Below 700°C, localized diffusion only at grain boundaries occurs, causing an inhomogeneous nature of the gate channel. This partial diffusion was detected by IV and CV measurements and was modeled by a parallel circuit of series capacitances. The interlayer capacitance before annealing was 8.7×10^{-7} F/cm^2 and increased to a maximum of 3.2×10^{-6} F/cm^2 after annealing at 700°C. Devices exhibited a 50% increase of the transconductance reaching 640 mS/mm for 500 nm gate length and a threshold voltage of +1 V.

8 Outlook and Future Ideas

Within the scope of this work several important achievements regarding technology and physics of high electron mobility tranistors with focus on enhancement-mode devices could be accomplished:

- A new method investigating the effective Schottky barrier height was proposed proving the impact of oxide-assisted Schottky barriers.
- Dual-gate measurements were utilized to monitor the charge injection into the surface passivation allowing in-depth analysis of the trapping mechanism and the device degradation.
- The impact on gate leakage current, 2DEG density, and channel drift mobility of the etch-stop layer from fluorine-based dry etching of dielectrics and GaN layers on InAlN was investigated indicating a process initialization window where surface damage can be minimized.
- A 2 nm thin barrier HEMT with $V_{Th} = +0.3\,V$ and $I_{DSS} = 0.8$ A/mm was demonstrated exibiting excellent small signal performance with $f_T = 33.7\,GHz$ at 0.5 µm gate length.
- RF dispersion-free device passivation using a highly doped GaN cap layer, together with a selective recess process at the gate, demonstrated a surface independent device scheme.
- Seperation of the gate electrode from the ultra-thin barrier device by a SiN cap and additional gate insulation by ALD-oxide resulted in a high potential power-switch device with threshold voltages up to 3 V and maximum gate bias up to 10 V.
- A model for MOS-HFET was found, explaining the threshold voltage based on the oxide-semiconductor interface charge and the band offset.
- Annealing induced "sinking" of the gate capacitance was discovered and could be explained by diffusion of oxygen into the Ir metal gate. Devices with optimized gate capacitance exhibited a transconductance of 640 mS/mm.

The following ideas have been partially investigated and developed and are believed to have high potential for successful integration. Most of the ideas follow the device structure and results of chapter 6.

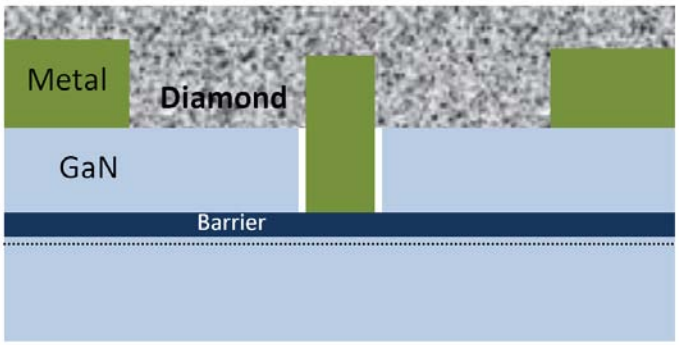


Figure 8.1: Schematics of recessed HEMT with GaN cap and diamond overgrowth.

8.1 GaN Cap Surface Passivation for direct Diamond Overgrowth

Diamond as heat spreader has been discussed during recent years [227, 228, 229]. Its high thermal conductivity should enable heat removal from the active area to a large scale heat sink. The use of diamond substrate causes not only difficulties for the growth due to the large mismatch of the lattice constants but also include a thermal boundary resistance between the substrate and the heat source. This boundary can hardly be improved unless the diamond is used on top of the device directly. However, this requires a post device fabrication deposition at several hundred degrees Celsius for hours. Alomari et al. have developed a metal scheme consisting of Ta and Cu instead of Au which survives such thermal budget without out-diffusion [69]. Applying this metallization, long-time high temperature operation above 800°C was proven under AC stress [67]. Devices also survived deposition of several micrometers of diamond without degradation of the electrical properties [70]. However, the deposition of the diamond film requires a about 100 nm thick SiN interlayer and a 50 to 100 nm Si layer which is used to nucleate the diamond film. Thereby most of the Si layer is consumed forming a thin layer of SiC below the diamond clusters. In respect of the device, the SiN layer serves also as a passivation layer to suppress RF dispersion[84]. This total interlayer stack between the device and high thermally conducting diamond layer is forming an boundary resistance for the heat, which reduces the heat spreader functionality of the diamond layer. Therefore it is the goal to reduce this layer to a minimum thickness. Alternatively, diamond clusters can be seeded directly on an passivation layer, which can be used to grow a thicker diamond layer [230]. The two methods however differ in the quality of the thermal characterization by cluster size and density of clusters.

The device design presented in chapter 6 uses an highly doped GaN cap layer to passivate the device structure below and electrically shields the devices from any surface

variations (up to the level of free carriers available in the barrier). Therefore a more direct approach can be used as for a standard barrier device with dielectric passivation. In the dielectric passivated device the suppression of the RF dispersion is also a function of the thickness of the passivation. Is trade-off can be avoid by the proposed idea were not additional dielectric passivation layer is required. Therefore the diamond layer can be seeded directly on the device as shown in figure 8.1, assuming that the diamond layer does not provide a leakage path between the contacts of the device. Otherwise a thin insulating layer needs to placed in between. Furthermore, the carbon-containing diamond layer may form alloys with the exposed metal layers, which could cause material clusters with lower melting point and hence reduced thermal stability. Therefore a thin passivation layer would serve as a protection barrier to the diamond layer. The thermal boundary resistance in such a device could be reduced to a minimum and therefore should provide optimum thermal properties.

8.2 In-situ SiN Passivation

Even though not mentioned in this work, a lot of efforts has been put into passivation studies on standard 10 nm thick InAlN barrier HEMTs. Conclusively, none of the tested oxides (ZrO_2, Al_2O_3, Si_3N_4) has shown a reliable and reproducible suppression of RF dispersion to be applied in RF power HEMTs. Dual gate investigations (chapter 4.2) have further proven that even dispersion-free dielectric layers may degrade after a few days of stress until the breakdown of the passivation. Consequently, new ways of passivation are needed. Recently Behmenburg et al. have presented the in-situ growth of SiN directly after finishing the epitaxial growth of InAlN HEMTs at 800°C, producing up to 100 nm of relaxed SiN [231]. Since the surface of InAlN has never been exposed to oxygen, a better interface with lower surface potential should be expected. First attempts of device fabrication have been started and the recess process of the SiN layer is shown in chapter 5. Final device fabrication showed excellent electrical characterization with drain currents above 1 A/mm and sheet resistance below 200 Ω/□. However, pulsed IV measurements revealed a slight dispersion in comparison to DC measurements, which is most probably caused by the open area beside the metal gate after the recessing of the SiN layer. Hence, an improved gate structure similar to a T-gate needs to be tested in order to provide a solid result on the electrical properties of the in-situ grown SiN layer.

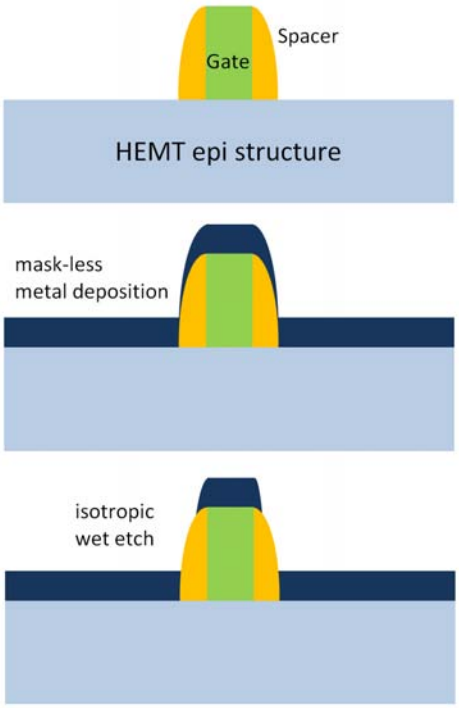
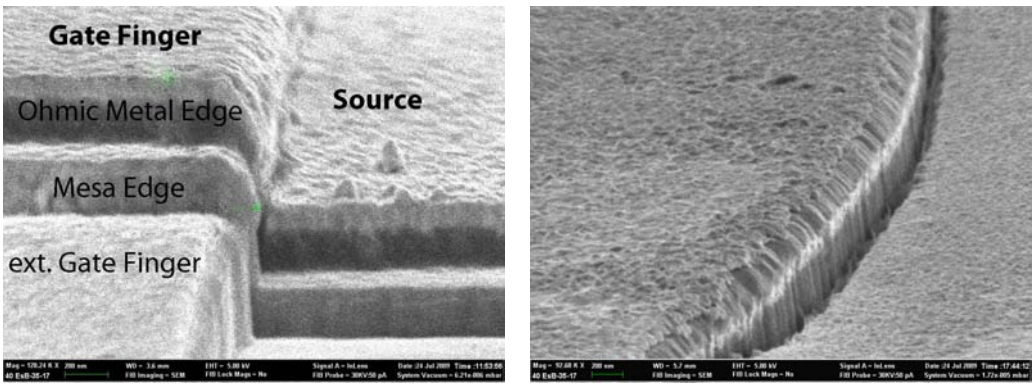


Figure 8.2: Schematics of HEMT crossecions demonstrating the self-aligned ohmic process (from top to down). After gate deposition, the dielectric spacer is formed by isotropic deposition and anisotropic etching. Then, metal is deposited anisotropically by thermal or electron-beam evaporation. Finally, a short isotropic wet etch removes the metal at the thinnest part and separates the gate from the source and drain electrode.

8.3 Self-aligned sub-nm Devices

A clear advantage of silicon technology is the simple formation of ohmic contacts by self-aligned implantation for the source and drain region. Even though Si implantation can be applied in order to create high doped regions, activation temperatures above 1000°C prevent prior formation of the gate [232]. In order to achieve very short source-to-drain distances electron-beam lithography can be used which has its limit at a few 100 nanometers. A few authors have proposed a self-aligned ohmic contact formation for T-gates where the head of the T-gate is used as mask for the ohmic contact [233, 234]. If thermally stable gate metals as wolfram are applied, the ohmic contacts can be annealed even after gate deposition [235]. However, none of these methods allows source-to-drain distances below 100 nm as it is used in state-of-the-art silicon technologies.

The fabrication process of the proposed idea is outlined schematically in figure 8.2. Device fabrication starts with gate metal deposition and a spacer formation similar to standard silicon gate stacks. The spacer is produced by deposition of any dielectric layer without mask in an isotropic process. The isotropy helps to deposit relatively more



(a) (b)

Figure 8.3: SEM cross-sections of (a) gate after spacer formation and metallization and (b) after additional wet etching. The short wet etching process opens up a gap between the lower and upper metal layer. Fig. (a) shows a source and gate contact comparable to the second schematic in figure 8.2. Figure (b) was taken from a circular diode with a top gate contact and a bottom ground contact, similar to the last schematic in figure 8.2.

material at any corner of the sample structure. Subsequently, the sample is etched in an anisotropic dry etch process, which removes the whole dielectric layer at horizontal structures and leaves only a thin spacer at any vertical slope. In contrast the ohmic metal should be deposited only at horizontal structures without leaving any trace on vertical ones in order not to shorten the gate with source or drain (schematic in the middle of figure 8.2). As a consequence, the reverse process to the spacer formation can be applied. Starting with an anisotropic metal deposition as it is used by thermal or electron-beam evaporation, the metal is mostly deposited on horizontal structures and with reduced thickness at vertical slopes. A perfectly vertical wall would almost be free of metal, as has been already demonstrated for GaAs devices [170]. Finally, an isotropic etching process is needed to remove the thin layer of metal which still causes an electrical path between the electrodes. Even though, this removes partially metal everywhere on the samples, less time is required for the thin deposits on vertical structures, leaving sufficient thick metal layers for the actual ohmic contacts (bottom figure in 8.2). Finally, it should be noted that both process steps again do not require any masking step and the ohmic deposition is fully self-aligned by the prior deposited gate metal. However in order to separate different devices a rough mask layer for the metal deposition should be used, which however does not relate to the individual gate.

A brief proof-of-concept has been provided by applying the above described process on the device structure from chapter 6 (Fig. 6.2). Scanning electron microscopy images

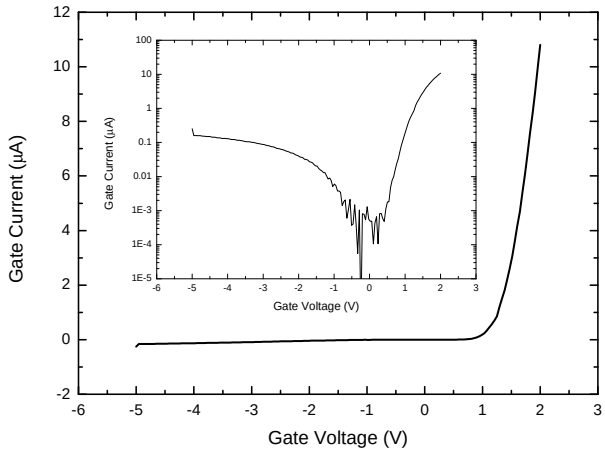


Figure 8.4: Current-voltage characteristic of self-aligned diode. The inset shows the same curve in logarithmic scale. The asymmetric characteristic proves a sufficient separation between ohmic and gate metal (wafer A 1730, see App. A).

are provided of the devices after metal deposition (Fig. 8.3a) and the subsequent wet etching process (Fig. 8.3b). The gate metal stack was chosen to be around 500 nm high, in order to be sufficiently higher than the total ohmic metal stack (around 250 nm). The SEM image proves the thinning of the metal layers around the vertical structure which could be totally removed after metal etching. Etching was provided in a short dip into HNO_3 and HCl (1:3) to remove the top gold metal layer at the thinner area and an additional wet etch in diluted HCl to remove the remaining ohmic stack metals, which did not affect the areas with thicker gold layer.

Electrical proof of the fabricated devices is shown in figure 8.4 of an self-aligned diode (SEM image in figure 8.3b). The top layer of the semiconductor at the ohmic contacts consisted of the highly GaN cap, which provided a rectified ohmic contact with 1 Ωmm contact resistance without annealing.

A successful integration of this method requires further investigation of the wet chemical process and an optimization of the metal layers required for ohmic contact deposition. Considering the small signal results from the enhancement-mode device with recessed gate, extremely high frequency operation close to the terahertz regime may be enabled by achieving short channel devices with very short source-to-drain distance.

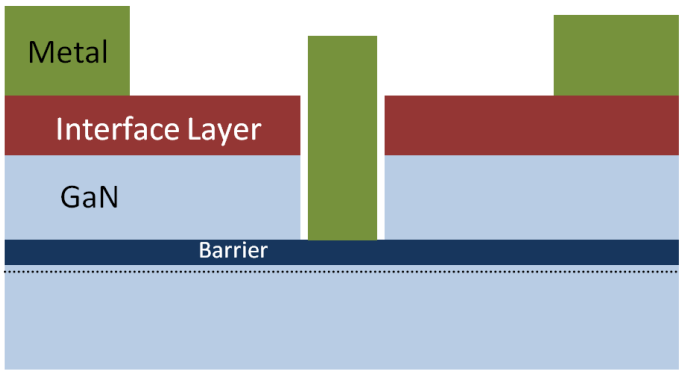


Figure 8.5: Schematic of HEMT structure with recess gate and interface layer for improved ohmic contacts.

8.4 Improved Ohmic Contacts by Gradual InN Interlayer

The concept in chapter 8.1 utilized already the fact of the device design from chapter 6, that the surface does not affect the 2DEG. This instance allows us to make any additional changes to the surface that may benefit the device characteristics. Figure 8.5 proposes a design with an interlayer between the GaN cap layer and the metal to reduce the ohmic contact. Such layer could consist of a graded InGaN layer to minimize the tunneling barrier for the ohmic contact. Dasgupta et al. have presented a similar idea on an N-face grown HEMT structure achieving an ohmic contact of 27Ωµm [236]. Such contact scheme does not require annealing of the metal contacts and is therefore the ideal choice in combination with self-aligned source/drain metallization presented in chapter 8.3.

As the layer needs to be removed around the gate region, it fits perfectly into the recess design of the gate. It needs to be assured that this top interface layer can be removed selectively in order to have a well controlled etching process without introducing to much degradation of the masking layer which is also required for metal lift-off.

8.5 GaN Power Switches

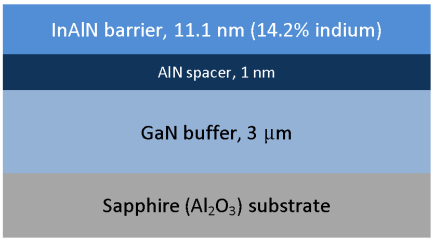
The power switch results from chapter 6.7.2 suggest a high band offset of ZrO_2 which allows to increase the barrier thickness and hence reduce the gate leakage as well as the complexity of the recess process. Barrier scaling of InAlN HEMTs revealed a threshold voltage decrease of 0.7 V per nm of barrier thickness [53]. Hence, a total barrier of 1 nm AlN and 2 to 3 nm InAlN may still provide an enhancement-mode device if ZrO_2

is applied as a gate oxide. Further, the doping density of the GaN cap layer can be reduced as power switch devices are not operated in the radio frequency range and relatively fast traps in the ns range do no degrade the device operation. A reduced doping level in the barrier may further improve the breakdown voltage, if it is provided through the cap layer. In all wafers with highly doped cap layers, it was found that the buffer was less insulating as in comparable structures. Even though this phenomenon has not been clearly solved, a reduction of the doping level could improve also the buffer leakage, if the cause of the problem is related to the Si doping in the cap layer.

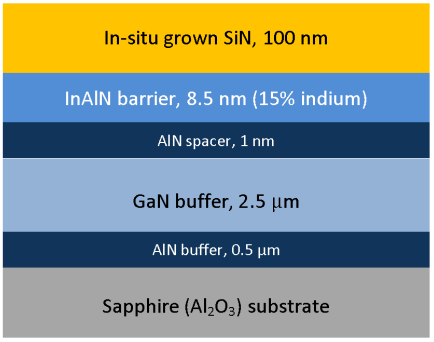
8.6 Charge Injection Mechanism into Passivation Layer

The concept of the charge injection experiment presented in chapter 4.2 could be used as a starting point to investigate the electron injection mechanism into the passivation layer. In contrast to vertical MOS structure it is assumed that the electrons need to overcome a barrier until they can be injected into the passivation. Injected electrons could then move forward to the drain direction by hopping mechanism. Therefore the whole system can be modeled as serial circuit including a diode, representing the barrier, a resistance and a capacitance to the 2DEG. Clarification whether this model is capable to describe the injection mechanism can be achieved by repeating the measurement at different temperatures and variation of the drain voltage under off-stress. Higher temperature influences the impact of the barrier and increased drain voltage can cause a reduction of the barrier potential as well as enhanced hopping in the passivation. Furthermore, new device designs should be prepared with varying distances between the two gates in order to investigate the dimensions of the injection.

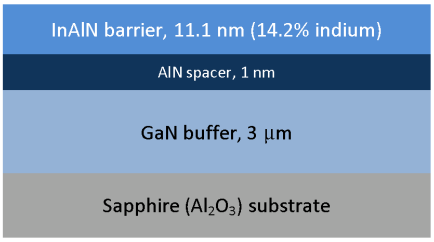
Appendix A: Wafer Data Sheet



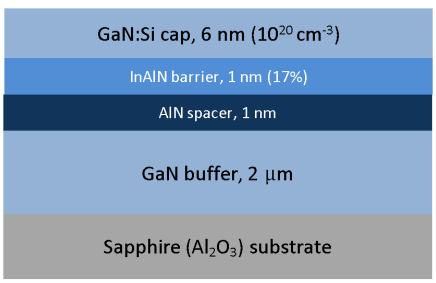
AEC 1802 (III-V Lab Alcatel-Thales, Paris)
sheet carrier density $n_s = 1.74 \times 10^{13} cm^{-2}$,
sheet resistance $R_{sh} = 366^{\Omega}/\square$



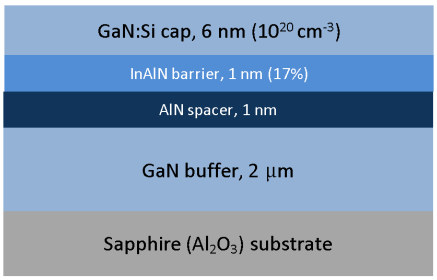
AIX 3415 (Aixtron, Aachen)
mobility $\mu = 1260\ ^{\mathrm{cm}^2}/_{\mathrm{Vs}}$,
sheet carrier density $n_s = 2.1 \times 10^{13} cm^{-2}$,
sheet resistance $R_{sh} = 181^{\Omega}/\square$



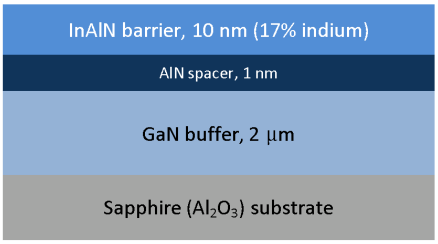
AIX 3416 (Aixtron, Aachen)
mobility $\mu = 1800\ ^{\mathrm{cm}^2}/_{\mathrm{Vs}}$,
sheet carrier density $n_s = 1.82 \times 10^{13} cm^{-2}$,
sheet resistance $R_{sh} = 191^{\Omega}/\square$



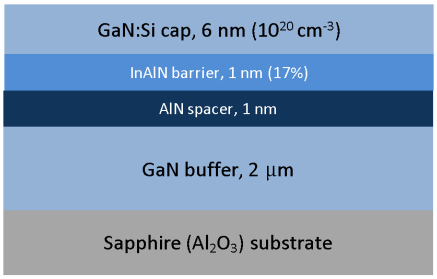
A 1592 (EPFL, Lausanne)
mobility $\mu = 1180\ ^{\mathrm{cm}^2}/_{\mathrm{Vs}}$,
sheet carrier density $n_s = 1.82 \times 10^{13} cm^{-2}$,
sheet resistance $R_{sh} = 289^{\Omega}/\square$



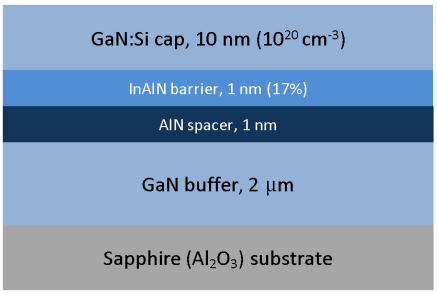
A 1589 (EPFL, Lausanne)
mobility $\mu = 1190$ $^{cm^2}/_{Vs}$,
sheet carrier density $n_s = 1.97 \times 10^{13} cm^{-2}$,
sheet resistance $R_{sh} = 266^{\Omega}/_{\square}$



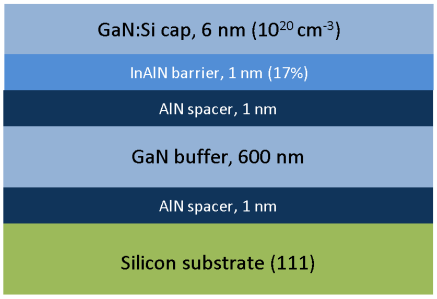
A 1730 (EPFL, Lausanne)
mobility $\mu = 1220$ $^{cm^2}/_{Vs}$,
sheet carrier density $n_s = 2.32 \times 10^{13} cm^{-2}$,
sheet resistance $R_{sh} = 221^{\Omega}/_{\square}$



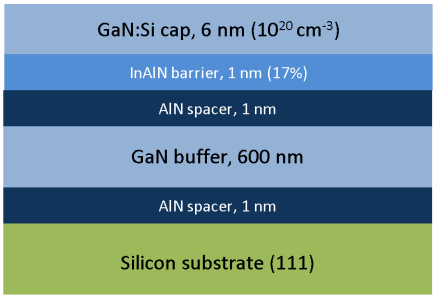
A 1732 (EPFL, Lausanne)
mobility $\mu = 1280$ $^{cm^2}/_{Vs}$,
sheet carrier density $n_s = 1.93 \times 10^{13} cm^{-2}$,
sheet resistance $R_{sh} = 252^{\Omega}/_{\square}$



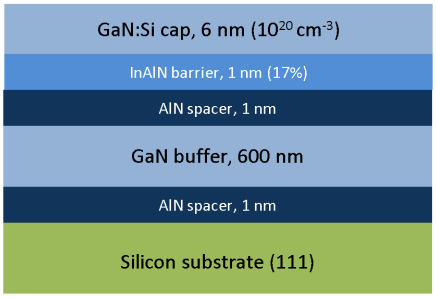
A 1733 (EPFL, Lausanne)
mobility $\mu = 1030$ $^{cm^2}/_{Vs}$,
sheet carrier density $n_s = 2.6 \times 10^{13} cm^{-2}$,
sheet resistance $R_{sh} = 232^{\Omega}/_{\square}$



A 1818 (EPFL, Lausanne)
mobility $\mu = 796$ $^{cm^2}/_{Vs}$,
sheet carrier density $n_s = 1.97 \times 10^{13} cm^{-2}$,
sheet resistance $R_{sh} = 397^{\Omega}/_{\square}$



A 1819 (EPFL, Lausanne)
mobility $\mu = 823$ $^{\mathrm{cm}^2}/_{\mathrm{Vs}}$,
sheet carrier density $n_s = 2.01 \times 10^{13} cm^{-2}$,
sheet resistance $R_{sh} = 378^{\Omega}/_{\square}$



A 1874 (EPFL, Lausanne)
data not available

Appendix B: MATLAB Code for CV Simulation

The following code was used in Mathlab under Linux to simulate a series of points with the Poisson-Schrödinger solver from Greg Snider [194]. The solver was embedded into the program allowing a fast and easy calculation for different surface potential which were used to derive the total charge in the structure, barrier and 2DEG. The derivative of the charges led to the gate capacitance:

```
%variable definition
barrier = 100;              %define position of barrier layer

neg = -0.7:0.01:-0.01;
pos = 0.01:0.01:4.0;
ext = 1.5:0.2:5;
SurfacePotential = [neg pos];
Nd = 1e19;                  %Nd could be a vector

Simulation=zeros(length(SurfacePotential),6);
Simulation(:,1)=SurfacePotential;

%repeat simulation for different surface potential
for a=1:length(Simulation);

    %define text file for simulator
    simfile=fopen('hemt.txt','wt');
    fprintf(simfile,'surface Schottky=%f v1\n',Simulation(a,1));
    fprintf(simfile,'InAlN t=100  Nd=%f   x=0 dy=1\n',Nd);
    fprintf(simfile,'AlGaN t=10   Nd=1e19 x=1 dy=1\n');
    fprintf(simfile,'GaN   t=1000 Nd=1e16     dy=1\n');
    fprintf(simfile,'substrate\n\n');
    fprintf(simfile,'fullyionized\n');
    fprintf(simfile,'v1 0.0\n');
    fprintf(simfile,'schrodingerstart=0\n');
    fprintf(simfile,'schrodingerstop=1000\n');
    fprintf(simfile,'temp=300\n');
    fclose(simfile);
```

```
%start Poisson-Schrödinger Simulator
!1dpoi < /home/clemenso/Simulation/command > /dev/null

data=importdata('hemt_Out.txt');      %read in simulation file
i=1;                                  %set counter to first line
nbarrier=0;                           %reset charges in barrier
n2DEG=0;                              %reset charges in 2DEG
ymax=length(data.data(:,1));

%add up the charges from simulation result
while i<=barrier+1 && i<=ymax         %surface to barrier
    nbarrier=nbarrier+data.data(i,6)*(data.data(i+1,1)-data.data(i,1)
        )*1e-8;
    i=i+1;
end
while i<=ymax-2                       %barrier to buffer
    n2DEG=n2DEG+data.data(i,6)*(data.data(i+1,1)-data.data(i,1))*1e
        -8;
    i=i+1;
end

Simulation(a,2)= n2DEG+nbarrier;      %save data
Simulation(a,3)= nbarrier;
Simulation(a,4)= n2DEG;               %finish single run end

for a=1:length(Simulation)-1          %calculate CV
    Simulation(a,5)=(Simulation(a+1,2)-Simulation(a,2))/(Simulation(a
        +1,1)-Simulation(a,1))*-1.6022e-19;
end

Simulation(:,6)=1./Simulation(:,5); %calculate 1/C
```

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Abbreviations

2DEG	two-dimensional electron gas
2DHG	two-dimensional hole gas
AFM	atomic force microscopy
Al	aluminum
AlN	aluminum nitride
Au	aluminum nitride
CCP	capacitively coupled plasma
CTLM	circular transfer line measurement
CV	capacitive-voltage
CW	continuous wave
dev.	development
DH	double heterostructure
DI	deionized
D-mode	depletion-mode
EELS	electron energy loss spectroscopy
E-mode	enhancement-mode
fcc	face-centered cubic
FET	field-effect transistor
f_{max}	maximum frequency of oscillation
f_T	current gain cut-off frequency
Ga	gallium
GaN	gallium nitride
g_m	transconductance
H_2	hydrogen
HCl	hydrochloric acid
hcp	hexagonal close packed
HEMT	high electron mobility transistors
H_f	formation energy
HFET	heterostructure field-effect transistor
HR-TEM	high resolution transmission electron microscopy
HT	high-temperature
HVPE	hydride vapor phase epitaxy

ICP	inductively coupled plasma
In	indium
InN	indium nitride
IV	current-voltage
JFOM	Johnson's figure of merit
KFOM	Keyes' figure of merit
LD	laser diode
LED	light-emitting diode
LM	lattice-matched
LT	low-temperature
μ	mobility
MBE	molecular beam epitaxy
MIS	metal-insulator-semiconductor
MOS	metal-oxide-semiconductor
MOCVD	metal-organic chemical vapor deposition
MOVPE	metal-organic vapor phase epitaxy
n	carrier concentration
N_2	nitrogen
NH_3	ammonia
Ni	nickel
n_s	sheet charge concentration
P	total polarization
PAE	power added efficiency
PECVD	plasma-enhanced chemical vapor deposition
P_{pz}	piezoelectric polarization
P_{sp}	spontaneous polarization
RF	radio-frequency
RIE	reactive ion etching
rms	root mean square
RT	room temperature
R_{sh}	sheet resistance
SBH	Schottky barrier height
s.c.	single crystaline
sccm	standard cubic centimeter per minute
SEM	scanning electron microscope
Si	silicon
SiC	silicon carbide
SiH_4	silane

SiN	silicon nitride
SIMS	secondary ion mass spectroscopy
Φ_{SP}	surface potential
T_0	characteristic temperature
TEM	transmission electron microscopy
Ti	titanium
TLM	transfer line measurement
TMAl	trimethylaluminum
TMGa	trimethylgallium
TMIn	trimethylindium
UV	ultra-violet
XRD	x-ray diffraction

List of Publications

Journals

J1 S. Kalchmair, H. Detz, G.D. Cole, A.M. Andrews, P. Klang, M. Nobile, R. Gansch, C. Ostermaier, W. Schrenk, G. Strasser, *Photonic Crystal Slab Quantum Well Infrared Photodetector*, accepted, to be published in Applied Physics Letters 1/2011.

J2 C. Ostermaier, M. Alomari, D. Pogany, G. Strasser, E. Kohn et al., *Investigations of Injected Charges into Surface Passivation by Dual Gate Stress Measurements*, to be submitted to IEEE Electron Device Letters.

J3 C. Ostermaier, M. Alomari, D. Pogany, G. Strasser, E. Kohn et al., *Barrier Height of Oxide-Assisted Schottky/Heterostructure Gate Contacts by CV Measurement*, to be submitted to IEEE Electron Device Letters.

J4 C. Ostermaier, G. Pozzovivo, B. Basnar, W. Schrenk, J.-F. Carlin, M. Gonschorek, N. Grandjean, A. Vincze, L. Tóth, B. Pécz, G. Strasser, D. Pogany, and J. Kuzmik, *Characterization of Plasma-Induced Damage of Selectively Recessed GaN/InAlN/AlN/GaN Heterostructures Using SiCl4 and SF6*, Japanese Journal of Applied Physics 49, pp. 116506 (2010).

J5 J. Kuzmik, C. Ostermaier, G. Pozzovivo, B. Basnar, W. Schrenk, J.-F. Carlin, M. Gonschorek, E. Feltin, N. Grandjean, Y. Douvry, C. Gaquiere, J.C De Jaeger, K. Cico, K. Froehlich, J. Skriniarova, J. Kavoc, G. Strasser, D. Pogany, and E. Gornik, *Proposal and performance analysis of normally off n++ GaN/InAlN/AlN/GaN HEMTs with 1-nm-thick InAlN barrier*, IEEE Transactions on Electron Devices 57, pp 2144 (2010).

J6 C. Ostermaier, G. Pozzovivo, J.-F. Carlin, B. Basnar, W. Schrenk, A.M. Andrews, Y. Douvry, C. Gaquiere, J.-C. De Jaeger, L. Tóth, B. Pecz, M. Gonschorek, E. Feltin, N. Grandjean, G. Strasser, D. Pogany, and J. Kuzmik, *Improvements of High Performance 2-thin InAlN/AlN Barrier Devices by Interface Engineering*, Proceedings of the 30th International Conference on the Physics of Semiconductors 2010, accepted for publication.

J7 C. Ostermaier, G. Pozzovivo, B. Basnar, W. Schrenk, M. Schmid, L. Tóth, B. Pecz, J.-F. Carlin, M. Gonschorek, N. Grandjean, G. Strasser, D. Pogany, and

J. Kuzmik, *Metal-related Gate Sinking due to Interfacial Oxygen Layer in Ir/InAlN High Electron Mobility Transistors*, Applied Physics Letters 96, pp. 263515 (2010).

J8 C. Ostermaier, S.I. Ahn, K. Potzger, M. Helm, J. Kuzmik, D. Pogany, G. Strasser, J.-H. Lee, S.-H. Hahm, J.-H. Lee, *Study of Si implantation into Mg-doped GaN for MOSFETs*, Physica Status Solidi c 7, pp. 1964 (2010).

J9 S. Abermann, C. Ostermaier, G. Pozzovivo, J. Kuzmik, O. Bethge, C. Henkel, G. Strasser, D. Pogany, C. Giesen, M. Heuken, M. Alomari, E. Kohn, E. Bertagnolli, *Atomic Layer Deposition of High-k Oxides on InAlN/GaN-Based Materials*, ECS Transactions 25, pp. 123 (2009).

J10 J. Kuzmik, G. Pozzovivo, C. Ostermaier, G. Strasser, D. Pogany, E. Gornik, J. Carlin, M. Gonschorek, E. Feltin, and N. Grandjean, *Analysis of degradation mechanisms in lattice-matched InAlN/GaN high-electron-mobility transistors*, Journal of Applied Physics, 106, pp. 1245031 (2009).

J11 S. Abermann, G. Pozzovivo, J. Kuzmik, C. Ostermaier, C. Henkel, O. Bethge, G. Strasser, D. Pogany, J. Carlin, N. Grandjean, E. Bertagnolli, *Current collapse reduction in InAlN/GaN MOS HEMTs by in situ surface pre-treatment and atomic layer deposition of ZrO2 high-k gate dielectrics*, Electronics Letters 45, pp. 570 (2009).

J12 C. Ostermaier, G. Pozzovivo, J. Carlin, B. Basnar, W. Schrenk, Y. Douvry, C. Gaquière, J. DeJaeger, K. Cico, K. Fröhlich, M. Gonschorek, N. Grandjean, G. Strasser, D. Pogany, J. Kuzmik, *Ultrathin InAIN/A1N Barrier HEMT With High Performancien Normally-Off Operation*, IEEE Electron Device Letters, 30, pp. 1030 (2009)

J13 C. Ostermaier, H.C. Lee, S.Y. Hyun, S.I. Ahn, K.W. Kim, H.I. Cho, J.B. Ha and J.H. Lee, *Interface Characterization of ALD deposited Al2O3 on GaN by CV Method*, Physica Status Solidi c, 5, pp. 1992 (2008).

J14 H.C. Lee, S.Y. Hyun, H.I. Cho, C. Ostermaier, K.W. Kim, S.I. Ahn, K.I. Na, J.B. Ha, D.H. Kwon, C.K. Hahn, S.H. Hahm, H.C. Choi and J.H. Lee, *Enhanced Electrical Characteristics of AlGaN/GaN Heterostructure Field Effect Transistor with p-GaN Back-Barriers and Si-delta Doped Layer* Japanese Journal of Applied Physics, 47, pp. 2824 (2008).

J15 H. D. Wanzenböck, C. Ostermaier, A Gruen, B. Eichinger, M. Karner, E. Bertagnolli, *Dot-array implantation for patterned doping of semiconductors*, Nuclear Instruments & Methods B, 242, pp. 257 (2006).

Book Contributions

B1 C. Ostermaier, *Design of a Two-Input NAND Gate using CMOS 0.35um Technology* in: *MOSFET Circuits and Electronic Applications*, edited by Sung-Ho Hahm, Kyungpook National University Press, Daegu, 2007, ISBN 978-89-92688-04-8-93560 (2007)

Oral presentations

O1 C. Ostermaier, A. Alexewicz, C. Henkel, O. Bethge, J.-F. Carlin, M. Gonschorek, N. Grandjean, D. Pogany, Emmerich Bertagnolli, and G. Strasser, *Ultra-thin barrier Enhancement-mode device with High-k Gate Insulation*, WOCSDEMMAD, Savannah, Geoarge, U.S., February 20-23, 2011.

O2 J. Kuzmik, C. Ostermaier, G. Pozzovivo, B. Basnar, W. Schrenk, J.-F. Carlin, M. Gonschorek, E. Feltin, N. Grandjean, Y. Douvry, C. Gaquière, J.-C. De Jaeger, G. Strasser, D. Pogany, E. Gornik, *Role of the gate-to-drain distance in the performance of the normally-off InAlN/GaN HEMTs*, 8th International Conference on Advanced Semiconductor Devices and Microsystems 2010, Smolenice, Slovakia, October 25-27, 2010.

O3 S. Valdueza-Felip, L. Monteagudo-Lerma, F. B. Naranjo, M. Gonzalez-Herraez, E. Monroy, C. Ostermaier, G. Strasser, J. Viegas, and P. Marques, *Optimization of GaN/AlN-based Waveguides for All-optical Switching at 1.5 um*, International Workshop on Nitride Semiconductors 2010, Tampa, Florida, U.S.A., September 19-24, 2010.

O4 J.C. De Jaeger, C. Gaquiere, Y. Douvry, N. Defrance, V. Hoel, S. Delage, M.A. di Forte-Poisson, N. Sarazin, E. Morvan, M. Alomari, E. Kohn, A. Dussaigne, J.F. Carlin, J. Kuzmik, C. Ostermaier, D. Pogany, *Microwave power capabilities of InAlN/GaN HEMTs*, 4th Microwave and Radar Week - 18th International Conference on Microwaves, Radar and Wireless Communications, MIKON 2010, Vilnius, Lithuania, June 14-16 2010.

O5 C. Ostermaier, G. Pozzovivo, J.-F. Carlin, B. Basnar, W. Schrenk, S. Ahn, H. Detz, P. Klang, A.M. Andrews, Y. Douvry, C. Gaquiere, J.-C. De Jaeger, L. Tóth, B. Pecz, M. Gonschorek, E. Feltin, N. Grandjean, G. Strasser, D. Pogany, and J. Kuzmik, *Improvements of High Performance 2-nm-thin InAlN/AlN Barrier Devices by Interface Engineering*, International Conference on the Physics of Semiconductors 2010, Seoul, Republic of Korea, July 25-30, 2010.

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Poster presentations

P1 A. Alexewicz, C. Ostermaier, G. Pozzovivo, W. Schrenk, M. Schmid, L. Tóth, B. Pecz, J.-F. Carlin, M. Gonschorek, N. Grandjean, J. Kuzmik, D. Pogany, G. Strasser, *Microstructural and Electrical Analyses of Oxygen Diffusion into Iridium Metal Gates*, Jahrestagung der "Oterreichischen Physikalischen Gesellschaft, Salzburg, Austria, September 6-10, 2010.

P2 C. Ostermaier, G. Pozzovivo, J.-F. Carlin, B. Basnar, W. Schrenk, Y. Douvry, C. Gaquiere, J.-C. De Jaeger, M. Gonschorek, E. Feltin, N. Grandjean, G. Strasser, D. Pogany, E. Gornik, J. Kuzmik, *A Novel Concept of High Performance FETs for Harsh Environment*, Microelectronics Conference 2010, Vienna, Austria, April 7-8, 2010.

P3 C. Ostermaier, G. Pozzovivo, J.-F. Carlin, B. Basnar, W. Schrenk, Y. Douvry, C. Gaquiere, J.-C. De Jaeger, M. Gonschorek, E. Feltin, N. Grandjean, G. Strasser, D. Pogany, E. Gornik, J. Kuzmik, *Ultrathin 2 nm Barrier HEMT for state-of-the-art fT x LG product of 16.9 GHz.um*, 16th International Winterschool on New Developments in Solid State Physics, Mauterndorf, Austria, February 22-26, 2010.

P4 C. Ostermaier, S. Ahn, K. Potzger, M. Helm, J. Kuzmik, D. Pogany, G. Strasser, J. Lee, S. Hahm, J. Lee, *Study of Si implantation in to Mg-doped GaN for MOS-*

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P6 C. Ostermaier, S. Ahn, K. Potzger, M. Helm, S. Kalchmair, D. Pogany, J. Lee, S. Hahm, J. Lee, *Realization of Inversion-type GaN MOSFETs with Ar Implantation for Device Isolation*, Junior Scientist Conference 2008, Vienna, Austria, November 16-18, 2008.

P7 G. Pozzovivo, J. Kuzmik, S. Abermann, C. Ostermaier, J. Carlin, M. Gonschorek, E. Feltin, J. Liday, N. Grandjean, E. Bertagnolli, G. Strasser, D. Pogany, *Recent Improvements on InAlN/GaN MOS-HEMTs*, Forum der Gesellschaft für Mikroelektronik 2008, Vienna, Austria, November 13-14, 2008.

P8 C. Ostermaier, H.C. Lee, S.Y. Hyun, S.-I. Ahn, K.W. Kim, H.I. Cho, J.B. Ha and J.H Lee, *Interface Characterization of ALD deposited Al2O3 on GaN by CV Method*, International Conference on Nitride Semiconductor (ICNS), Las Vegas, Nevada, U.S.A., September 16-21, 2007.

P9 S.Y Hyun, K.W. Kim, H.I. Cho, H.C. Lee, C. Ostermaier, S.I. An, J.B. Ha, S.H. Hahm, C.K. Hahn, H.C. Choi and J.H. Lee, *Effectiveness of Si delta-doping on AlGaN/GaN HFET with p-GaN backbarrier* International Conference on Nitride Semicondutors (ICNS), Las Vegas, Nevada, U.S.A., September 16-21, 2007.

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Curriculum Vitae

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