

DISSERTATION

Topography Simulation of Deposition and Etching Processes

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ALIREZA SHEIKHOLESAMI

Neilreichgasse 23/14-15
A-1100 Wien

Matrikelnummer 9825631
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Zusammenfassung

Heutzutage ist es üblich die Simulation der Herstellungsprozesse als ein Mittel für die Entwicklung neuer Produkte oder Prozesse zu nutzen. Das Ziel dieser Technik ist, die Optimierung der Prozesse und infolgedessen der Produkte, bevor sie in die Produktionslinie kommen. Dies ist vorteilhaft, da experimentelles Optimieren sehr teuer ist. Die Simulation der Herstellungsprozesse hilft, die bestmögliche Konfiguration des Produktionsprozesses, auch wenn das bestehende Gerät noch nicht vorhanden ist, zu finden. Die Erweiterung und Konfiguration der existierenden Prozesse können noch vor der Investition getestet und evaluiert werden.

Die Abscheidung und das Ätzen sind zwei wichtige Herstellungsprozesse, deren Simulation einen gemeinsamen Teil besitzt, nämlich die Beschreibung der sich bewegenden Grenzoberflächen. Grob gesagt gibt es drei verschiedene Kategorien der Algorithmen für die Oberflächenevolution: Die Methode der Polygone, die der Zellen, und die Level Set Methode. Die Level Set Methode leidet nicht unter den Problemen der beiden anderen Methoden.

Diese Arbeit konzentriert sich auf die Entwicklung und Implementierung eines auf der Level Set Methode basierten mehrzweckigen Topographiesimulators in zwei und drei Dimensionen. Fortgeschrittene Algorithmen und Techniken wie Narrow Banding und Fast Marching Methoden sind für die Implementierung eines effizienten und schnellen Simulators unumgänglich. Der Simulator ist fähig, verschiedene physikalische Modelle für die Abscheidung und das Ätzen zu behandeln. Diese Modelle können in einem separaten Modul verwendet werden. Die Parameter dieser Modelle wurden mittels Messungen und mit Hilfe von Inverse Modelings kalibriert und optimiert.

Der große Teil der in dieser Arbeit präsentierten Applikationen ist von unseren Industriepartnern angefordert oder inspiriert. Die Applikationen, die sich auf Entwurf von Interconnect-Linien beziehen, entstanden in Zusammenarbeit mit Cypress Semiconductor Corporation (San Jose, CA, USA). Die Profile der abgeschiedenen Schichten und Voids in zwei und drei Dimensionen wurden simuliert. Zweidimensionale Simulationen geben Auskunft über die zwischen den verschiedenen Metallschichten entstehenden Kapazitäten, die Schaltverzögerungen stark beeinflussen. Zusätzlich sind dreidimensionale Void Charakteristika simuliert worden, um einen Einblick in möglichen Layout-Entwurf-Regeln zur Vermeidung der Cracking-Effekte zu geben.

Weiters wurden aussagekräftige Simulationen der Abscheidung von Siliziumdioxid in Gräben mit verschiedenen Seitenverhältnissen für power MOSFETs von Infineon Technologies (Villach, Austria) ausgeführt.

Schließlich wurde Plasmaätzen für das Toshiba R&D Zentrum (Kawasaki, Tokyo) simuliert, wobei ein unerwünschtes Abrunden der Kanten minimiert wurde.

Abstract

Nowadays, it is common to use the simulation of semiconductor manufacturing processes as a mean to support the development of new products or processes. The aim of this technique is to rationalize these processes and, consequently the products, before they actually enter the production line, since experimental optimization is very expensive. Simulation of manufacturing processes helps to find the best possible configuration of the production process even if the production equipment can not be used yet. Extension or reconfiguration of the existing processes can be tested and evaluated before investment takes place.

Deposition and etching are two of the most important semiconductor manufacturing processes. The common aspect regarding the simulation of the deposition and etching processes is tracking moving boundaries. Roughly speaking, there are three categories of algorithms for surface evolution. The first one is the string-based method, the second one is the cell-based method, and finally the most recent is the level set method. This method avoids many problems inherent in the first two methods.

This work focuses on the development and implementation of a general purpose topography simulator in two and three dimensions using the level set method. Sophisticated algorithms and techniques such as narrow banding and fast marching methods for implementation of an efficient and fast simulator have been used. The simulator is capable of handling different physical models for deposition and etching. These models can be implemented in a completely separated module in the simulator. The parameters of different models are calibrated and optimized using measurements based on inverse modeling.

The great part of applications presented in this work was requested or inspired by our industrial partners. The applications regarding the design of interconnect lines were needed by Cypress Semiconductor Corporation (San Jose, CA, USA). The profiles of deposited layers and voids in two and three dimensions are simulated. The two-dimensional simulations predict the capacitances formed between the different metal layers that significantly determine the timing delays. In addition, three-dimensional void characteristics are simulated for gaining insight into possible layout design rules for avoiding cracking effects.

A predictive simulation of the deposition of silicon dioxide into trenches with different aspect ratios is performed for power MOSFETS from Infineon Technologies (Villach, Austria).

Finally, plasma etching for obtaining the etching profiles with minimum corner rounding is simulated for Toshiba R&D Center (Kawasaki, Tokyo).

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List of Acronyms

BTRM	Ballistic Transport and Reaction Model
CBCM	Charge Based Capacitance Measurement
CD	Critical Dimensions
CFL	Courant–Friedrichs–Levy
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Planarization
CPU	Central Process Unit
CVD	Chemical Vapor Deposition
ECAD	Electronic Computer Aided design
ELSA	Enhanced Level Set Applications
IADF	Ion Angular Distribution Function
IC	Integrated Circuit
ILD	Interlevel Dielectric
IPD	Input Deck Library
LDMOS	Laterally Diffused MOS
LPCVD	Low Pressure Chemical Vapor Deposition
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PDE	Partial Differential Equation
PECVD	Plasma Enhanced Chemical Vapor Deposition
PIF	Profile Interchange Format
PSLG	Planar Straight Line Graph
PVD	Physical Vapor Deposition
RCX	Resistance and Capacitance Extraction
RESURF	Reduced Surface Field
RF	Radio Frequency
RIE	Reactive Ion Etching
SEM	Scanning Electron Microscope
SOI	Silicon-On-Insulator
SIESTA	Simulation Environment for Semiconductor Technology Analysis
SPICE	Simulation Program with Integrated Circuit Emphasis
TCAD	Technology Computer Aided Design
TMOSFET	Trench MOSFET
TCO	Total Cost of Ownership
TEOS	Tetraethoxysilane, $\text{Si}(\text{OC}_2\text{H}_5)_4$
ULSI	Ultra Large Scale Integration
UV	Ultraviolet
WSS	Wafer State Server

List of Symbols

β, β_0	sticking coefficients
D_{ijk}^{+x}	forward difference in x direction
D_{ijk}^{-x}	backward difference in x direction
D_{ijk}^{+y}	forward difference in y direction
D_{ijk}^{-y}	backward difference in y direction
D_{ijk}^{+z}	forward difference in z direction
D_{ijk}^{-z}	backward difference in z direction
F_c	neutral flux on the surface
F_d	inhibitor flux on the surface
F_i	ion flux on the surface
S_c^0	clean sticking coefficient for neutral
S_d^0	clean sticking coefficient for inhibitor
$F(t, \mathbf{x})$	speed function
F_{ext}	extended speed function
F_{ijk}	grid values of the speed function
I_N	total flux after N reflection
I_R	vector of fluxes from reflections
$I_{R,k}$	vector of fluxes from k th reflection
I_S	vector of fluxes coming from the sources
$I_{S,k}$	vector of fluxes stucked at the k th bounce
J_n	electron current density
J_p	hole current density
Ω	radiosity matrix
φ_{ijk}^n	grid values of the level set function at time n
V	electric potential
$\varphi(t, \mathbf{x})$	level set function
φ_{temp}	temporary signed distance function
R_E	etching rate
θ_c	surface coverage for neutral
θ_d	surface coverage for inhibitor
Y	etching yield

**Alles wissen nur alle, aber alle
sind noch nicht geboren.**

Bozorgmehr

1 Introduction

This introductory chapter gives an overview of both the history and importance of the semiconductor technology. The motivation for TCAD (technology computer aided design) and the importance of simulations are discussed. The different process steps used in the manufacturing of semiconductors are briefly presented. The importance of topography simulation is also discussed. Finally, this chapter concludes with an outline of this thesis.

1.1 History and Importance of Semiconductor Technology

During the human history, scientific and technological inventions have progressed considerably the type and the whole standard of living. In the last century the atom has been split into its components and the micro- and nano-technologies have been developed. Furthermore, machines have been invented that perform millions of computations per second. The most important common themes of the above mentioned advances are the electronic properties of materials, which show a richness of physical interactions dominating the modern life from household applications to global industries.

1947 Shockley, Bardeen, and Brattain invented the silicon-based transistor. This invention was the beginning of the semiconductor industry. Semiconductors provide a very good electronic control and thus they are the foundation stone of computer revolution. Soon after the transistor invention, many transistors were fabricated on a single chip. Since the production of the first IC (integrated circuit) in the late 1950s the number of components had been doubled yearly. This tendency was first predicted in 1964 by Gordon Moore who was a semiconductor engineer and a co-founder of Intel in 1968. His law was valid till the late 1970s as the doubling period was extended to 18 months and has remained up to now.

Although there are many problems to improve the integration factor per chip and to manufacture faster and smaller electronic devices, the demand is still increasing. The miniaturization and integration enable to use batch processing techniques that lead to cost reduction. For example, the computer revolution is the father of Internet which is continuously demanding an increase of information capacity and data bandwidth required for tele- and data-communication applications.

1.2 Technology Computer Aided Design

TCAD is widely used in the semiconductor industry to design and optimize transistors. With the increasing complexity of device structures and the assault of sophisticated diffusion mechanisms, separate process simulation investigations were developed independently to model the complete process flow from the silicon substrate to the passivation of the surface. It is the ultimate goal of TCAD to replace the experimental trial and error process with simulations to reduce capital outlay as well as to shorten the development cycle.

Process modeling and simulation have historically begun from stand-alone programs for single process steps, such as oxidation, lithography, ion implantation, diffusion, etching, deposition, and metalization. The goal of all of these simulators is to predict the different effects of each single process and to quantify the influence of the process parameters. Not already enough, these different simulators are combined to an integrated process simulation flow to follow the process steps applied in semiconductor manufacturing as closely as possible. The output of an integrated process simulator ideally results in a device representation which exactly mirrors the fabricated chip. This device representation can not only be used for device simulators but also for resistance, capacitance, and parameter extraction of interconnect lines. Therefore, the final simulation results also give insight into device characteristics which are hardly accessible to measurements.

Topography simulation plays the most important role in linking TCAD to the design and layout of ICs, which is realized with ECAD (electronic computer aided design) [59,64]. ECAD provides the tools necessary for the generation of a physical representation of the circuit diagram which is a symbolic description guaranteeing the complex functionality of the circuit required by the operational specifications of the customer.

Although costs have played an important role for the development of TCAD, it is wrong to see the costs exclusively as its reason. TCAD is also serving scientific interests in process and device physics by modeling and simulation.

Classical TCAD simulation tools solve PDEs (partial differential equations) within a specific macroscopic simulation domain. Common semiconductor manufacturing steps are simulated and modeled by continuum equations and numerical algorithms. The application of these TCAD simulation tools for reactor-scale simulation domains is limited by the number of required discretization points and subsequently by the speed as well as the available memory of computers nowadays. In order to link the reactor-scale simulations with the feature-scale simulation certain approximations have to be taken into account. Since the wafer size is increasing and the feature sizes are decreasing, the gap between reactor-scale and feature-scale simulations is growing with every new generation. This leads to the conclusion that reactor-scale simulations will play only a minor role for feature-scale simulations (cf. Chapter 4). Therefore, we limit ourselves to feature-scale simulations in this thesis.

1.3 Semiconductor Process Technology

This section provides an overview of the processing steps used to manufacture advanced electron devices.

1.3.1 Etching

Etching processes are used to partly remove material in order to create patterns to obtain the desired device or interconnect geometry. Particles in the etching component (a liquid or gas) remove material by attacking the exposed surface. The material may be removed isotropically, as often encountered in chemical or wet etching, or anisotropically for which dry or a plasma etching is used. In the case of a dry-etching process, the total etch rate consists of an ion-assisted rate and a purely chemical etch rate due to etching by neutral radicals which may still have a directional component. The total etch rate can depend on shadowing within the reactor and by the structures on the substrate itself,

the angle-dependent flux distribution of particles from the reactor volume, the angle of incidence of the particles relative to the surface normal direction, reflection/re-emission of etching particles, and surface diffusion effects. RIE (reactive ion etching) provides high anisotropy which is achieved via different mechanisms by ions impinging onto the surface. The main advantage of RIE is its enhanced directionality compared to chemical etching. RIE becomes increasingly important as device sizes decrease substantially and etching must proceed even deeper in vertical direction without negatively affecting adjacent features.

1.3.2 Deposition

A wide range of different techniques is used for the deposition of conducting and insulating materials in semiconductor processing. CVD (chemical vapor deposition) and PVD (physical vapor deposition) are most important among them. Materials in semiconductor manufacturing that can be deposited by CVD are, e.g., silicon dioxide, silicon nitride, poly-silicon, tungsten, copper, titanium nitride, and aluminum. Materials in semiconductor manufacturing that can be deposited using PVD are, e.g., aluminum, titanium, titanium nitride, tantalum, and copper. One of the most important factors during the deposition of materials is the conformality, i.e., for all positions at the device surface the same layer thickness is deposited. Because of the better conformality of CVD compared to PVD, CVD is usually preferred.

1.3.3 Oxidation

Today's ULSI (ultra large scale integration) technology is to a large extent based on the excellent properties of thermally grown silicon dioxide layers. SiO_2 is used as gate dielectric in MOS (metal oxide semiconductor) devices, as implantation or doping mask, and for device isolation purposes.

It has been proven by a number of experiments that thermal oxidation of silicon proceeds by diffusion of the oxidant through the growing oxide. The oxidation reaction itself takes place at the oxide-silicon interface. During oxidation, the oxide-silicon interface moves into the silicon material as the silicon is oxidized. Considering the densities of silicon and of SiO_2 , it can be shown that a part of the oxide layer grows into the silicon substrate. The remaining part grows on top of the silicon, resulting in a non-planar surface if oxidation is local.

1.3.4 CMP (Chemical Mechanical Planarization)

CMP is an enabling technology used for manufacturing integrated circuits with interconnect geometries of less than $0.18\mu\text{m}$. As line widths continue to shrink below $0.18\mu\text{m}$, and as circuits become more complex, the need for planarity becomes critical. Topological imperfections adversely affect the lithographic process that is used to etch the circuit patterns on the wafer (cf. Section 1.3.5). As the number of layers increases, the difficulty in maintaining the focus in the lithography processes increases. The multiple metalization layers in today's devices require extreme planarity to maintain high manufacturing yields. The CMP process enables the manufacture of these complex devices by polishing the surface of the wafer after each layer of the circuit is added. The resultant

CMP waste stream contains suspended particles, dissolved metals, chemicals and other contaminants from the wafer and CMP slurry.

1.3.5 Lithography

Lithography is the process of transferring geometric shapes on a mask to the surface of a silicon wafer. These shapes make up the parts of the circuit, such as gate electrodes, contact windows, metal interconnections, etc. The final IC is made by sequentially transferring the features from each mask, level by level, to the surface of the silicon wafer. An ion implant, oxidation, or metalization operation may take place between the successive image transfers.

In the IC lithographic process, a photosensitive polymer film is applied to the silicon wafer, dried, and then exposed to UV (ultraviolet) or other radiation with the proper geometrical patterns provided by a photo-mask. After exposure, the wafer is brought into contact, e.g., by dipping or spraying, with a solution that develops the images in the photosensitive material. Depending on the type of polymer used, either exposed (in the case of positive resists) or non-exposed (for negative resists) areas of the film are removed during the developed process. After development the resist acts as a mask to etch patterns into the underlying layers, for instance.

1.3.6 Ion Implantation

Ion implantation is used to introduce dopants into the silicon crystals in a very controlled way. In order to do this, atoms or molecules are ionized, accelerated in an electric field and implanted into the target material. The range of the implanted ions in the substrate depends on the mass of the implanted ions, their energy, the mass of the substrate atoms, the structure of the crystal, and the angle of incidence.

The electrical activation of ion-implanted species is carried out by annealing. This causes a redistribution of the impurity atoms which should be kept as low as possible. In order to optimize the electrical behavior of the device, it is important to know how the impurities redistribute during the anneal. The development of appropriate models and simulation programs to predict the diffusion is a major topic in semiconductor technology research.

Main advantages of ion implantation compared to diffusion for the doping of semiconductors are:

- Short process times, good homogeneity and reproducibility of the profiles.
- Exact control of the amount of implanted ions by measuring the current. This is of particular importance for low concentrations, e.g., to adjust the threshold voltage of MOS transistors.
- Relatively low temperatures during the process.
- Various materials can be used for masking, e.g., oxide, nitride, metals, and resist.
- Implantation through thin layers, e.g., SiO₂ is possible.
- Low penetration depth of the implanted ions. This allows modification of thin areas near the surface with high concentration gradients.

- Sequences of implantation steps with different energies and doses allow optimization of the dopant profiles.

There are also some disadvantages, such as:

- The implanted ions cause damage in the substrate.
- The change of material properties is restricted to the substrate domains close to the surface.
- Additional effects during or after implantation, e.g., channeling or diffusion, make it difficult to achieve very shallow profiles and to theoretically predict the exact profile shapes.

1.3.7 Diffusion

Diffusion of impurity atoms in silicon during processing is important for the electrical characteristics of silicon devices. Various ways of introducing dopants into silicon by diffusion are used and have been studied with the goal of controlling dopant distribution, total dopant concentration, uniformity, and reproducibility.

Diffusion is used to form base, emitter, and collector regions in bipolar device processing, to form source, drain and channel regions, and to dope poly-silicon in MOS processing. Dopant atoms that span a wide range of concentrations can be introduced into silicon in many ways. The most commonly used methods are:

- diffusion from a chemical source in a vapor form at high temperatures,
- diffusion from a doped-oxide source, and
- diffusion and annealing from an ion-implanted layer.

1.4 Importance of Topography Simulation in Semiconductor Manufacturing

Inhomogeneities of the results of a manufacturing process step caused during the fabrication characterize the manufacturability and yield of a technology. This refers especially to inhomogeneities across the wafer or between different wafers. Processes where these effects are especially important are deposition and plasma etching. Therefore, although topography simulation in fact crosses almost all manufacturing processes mentioned in the previous sections, it is used especially in this work for deposition and etching processes. In addition, as the importance of the three-dimensional effects in shrinking devices and interconnects increases, more accurate methods to track the motion of the interface have to be developed.

Generally, predictive simulation of etching and deposition processes using topography simulators is still limited by lack of knowledge of the physical properties of the material and chemical processes involved. The development of accurate models for reaction paths, the extraction of reliable values for the required parameters and also the development of reduced chemistry models which include only the primary mechanisms needed

for practical applications is an important challenge as is reported by ITRS (international technology roadmap for semiconductors)¹.

There exists a considerable number of commercial and academic tools for topography simulation. They are based on different surface tracking techniques which can be roughly grouped into three different categories. The string-based method, the cell-based method, and finally the level set based method. These different techniques are discussed in Section 2.2 and Section 2.2.3 in detail. This section only introduces the tools based on these techniques and neglects their detailed description.

The string-based techniques have the advantage of a high level of accuracy for moving surfaces, but they need techniques to avoid the formation of non-physical loops and self-intersection of the evolving surfaces. Whereas these disadvantages impact the efficiency of the simulator in two dimensions as can be seen in the ESPRIT [60, 103], the three-dimensional implementation of this method is much more expensive in time and memory. Nevertheless, three-dimensional topography simulators based on string techniques such as SPEEDIE [9, 10, 73, 98] exist.

In addition, several implementations based on the cellular method such as an early implementation of the cell-removal algorithm can be found in [29]. The other topography simulator is called MASTER [54]. At our institute Dr. Pyka also implemented a topography simulator based on the cellular method in two and three dimensions for lithography, etching, and deposition processes [64, 66].

The third category of methods is the level set method which is, for instance, used by the commercial packages such as SENTTAURUS². SENTTAURUS is an advanced one-, two-, and three-dimensional process simulator for the development and optimization of silicon and compound semiconductor process technologies. After joining ISE to SYNOPSIS their best features have been combined that has led to a great range of capabilities. This new generation of process simulator addresses the important challenges of process technologies. The simulator contains a set of models including calibrated parameters obtained from measurements. Therefore, it enables to simulate a broad range of processes.

Among all techniques, as we will discuss in Chapter 2, the level set method has been known as the best method for tracking the evolution of the surface. Therefore, we have developed and implemented a level set based general purpose topography simulator in two and three dimensions named ELSA (enhanced level set applications). The first version of a two-dimensional topography simulator based on the level set method at our institute was developed and implemented by Dr. Heitzinger. The code was written in Lisp. According to his experiences related to the problems emerging in implementation of two-dimensional topography simulator a second version in two dimensions and a first version in three dimensions capable of handling the more complicated physical models are written. The two- and three-dimensional codes are written in C and C++, respectively.

1.5 Outline of the Thesis

In Chapter 2 we introduce different well-known techniques used for tracking moving boundaries. These techniques are used in conventional topography simulators.

¹<http://public.itrs.net/HomeStart.htm>

²<http://www.synopsis.com>

In Chapter 3 fundamental physical mechanisms of deposition and etching responsible for the creation of both desired and undesired topographic features and a base to understand and model these effects within topography simulation are presented.

In Chapter 4 we describe some physical models for the deposition of SiO_2 layers from TEOS in a CVD process. The parameters of these models are calibrated by comparing simulation results to SEM images in order to obtain optimal agreement of measurements and simulation results.

Chapter 5 deals with describing the level set technique and related techniques used for an efficient implementation of our two- and three-dimensional topography simulator.

In Chapter 6 simulation results for the backend of a 100nm CMOS process, where the influence of void formation between metal lines profoundly impacts the performance of the whole interconnect stack, are presented. The results from output of our topography simulator serve as input to the subsequent capacitance extraction.

In Chapter 7 we present the application of the simulator for the simulation of plasma etching processes. The surface kinetics is modeled based on the Langmuir adsorption model. Etching profiles with minimal corner rounding are simulated.

In Chapter 8 the application of the general purpose three-dimensional topography simulator for obtaining the void characteristics in interconnect lines is presented. These characteristics are used to avoid crack formation.

In Chapter 9 we present the application of the simulator to generate structurally aligned grids. The generated grids are used for device simulation with MINIMOS-NT [15].

Finally, Chapter 10 provides an insight into the efficiency and CPU time consumption of three-dimensional topography simulator.

2 Mathematical Description of the Motion of Interfaces

In this chapter we present PDEs which describe moving interfaces. From one point of view this leads to a boundary value problem for a PDE and from another point of view to a time-dependent initial value problem for a PDE. We also lay out the theoretical and computational advantages of these two formulations.

2.1 Formulation of the Motion of Interfaces

In order to describe a moving boundary in direction normal to the boundary (we neglect the tangential component of the speed, because the addition of a tangential component has the effect of just changing the parameterization of the boundary [71]) one has to know the value of the normal speed function which we denote as F . The speed function F generally depends on many parameters and can be written as $F(L, G, I)$, where L , G , and I stand for local, global, and independent parameters described as follows:

- Local parameters are determined by geometric informations, e.g., normal vector and curvature.
- Global parameters are determined by shape and position of the interface.
- Independent parameters are independent of the shape of the interfaces, such as an underlying fluid velocity that passively transports the front.

For the moment we assume that F is known and our goal is to track and describe the motion of interface.

2.1.1 The Boundary Value Formulation

Assuming $F > 0$, the interface will always move outward. One way to detect the position of the interface is to find the time $T(x, y)$ at which the interface crosses a point with coordinates (x, y) . Considering the fact that in one dimension distance is equal to speed multiplied by time, the equation of motion of the interface can be formulated as follows:

$$dx = F \cdot dT.$$

In multiple dimensions ∇T is orthogonal to level sets of T and analogous to one dimension it is inversely proportional to F . Therefore, we can write

$$|\nabla T|F = 1 \quad T = 0 \text{ on } \mathbf{x} \tag{2.1}$$

where \mathbf{x} is the initial position of the interface. Hence, this formulation of motion of an interface leads to a boundary value problem.

2.1.2 The Initial Value Formulation

In contrast to the requirement of $F > 0$, the speed is not strictly positive but it can be arbitrarily positive or negative. This leads to a motion of the interface backward and forwards. Therefore, the interface can pass a certain point more than one time. Therefore, $T(x, y)$ is no unique value to detect the position of the interface. In order to solve this problem we embed the initial position of the interface as the zero level set of a function φ in a higher dimension. Linking the position of the interface to the evolution of φ leads to a time-dependent initial value problem. At each time step the interface is given by the zero level set of the time-dependent level set function φ .

To derive the equation of motion, we define the interface $\mathbf{x}(t)$ which must always guarantee the following equation

$$\varphi(\mathbf{x}(t)) = 0.$$

Using the chain rule the above equation results in

$$\varphi_t + \nabla\varphi \cdot \frac{d\mathbf{x}}{dt} = 0.$$

Since the normal vector $\mathbf{n} = \nabla\varphi/|\nabla\varphi|$, and $\mathbf{n} \cdot d\mathbf{x}/dt = F$, we get the level set equation in the following form [80]:

$$\varphi_t + F|\nabla\varphi| = 0. \tag{2.2}$$

2.1.3 The Beneficial Properties and Comparison of These Formulations

Some common advantages of the boundary and initial value problem are listed [80] here:

- The topological changes of the interface are handled very well. Since the position of interface is given either by the zero level set of the level set function or by the level set $T(x, y) = t$ in each time, which are single-value functions, the interface need not be a single boundary and it can break and merge as t proceeds.
- The geometrical quantities such as normal vector and curvature can be determined easily.
- They are very efficient because of the possibility to use fast marching and narrow banding methods which will be discussed in Section 5.5 and in Section 5.6, respectively.

At the same time there are important differences between these two formulations [80]:

- Because of the ability of the initial value formulation to accept positive and negative speeds, models with complex speed functions, e.g., curvature dependent speed, are handled with initial value formulation and not with the boundary value formulation.
- In contrast to the initial value formulation, the boundary value formulation requires no time stepping and does therefore not depend on a CFL (Courant-Friedrichs-Levy) condition which will be discussed in Section 5.13.

- The boundary value formulation enables to use a fast marching method which is very efficient¹.

2.2 An Overview of the Techniques for Tracking the Motion of a Surface

Various surface representation algorithms beside the level set method have been used to develop topography simulators. Roughly speaking, these algorithms fall into two categories [53], namely, string-based and cell-based methods. In the next sections we briefly present these three methods.

2.2.1 String-Based Methods

This approach has also been known under different names such as marker particle, nodal, and string method [72, 97]. The interface is represented as a series of lines in two dimensions (cf. Figure 2.1) or triangle segments in three dimensions. The position of nodes forming a line or triangle segment is advanced in each time step using interface information about the normals and curvatures of the surface facets. Several techniques have to be used for an accurate advancement of the interface, while at the same time

¹Fast marching method is principally used by the boundary value formulation, but it can be used for the calculation of the distance function when using the initial value formulation.

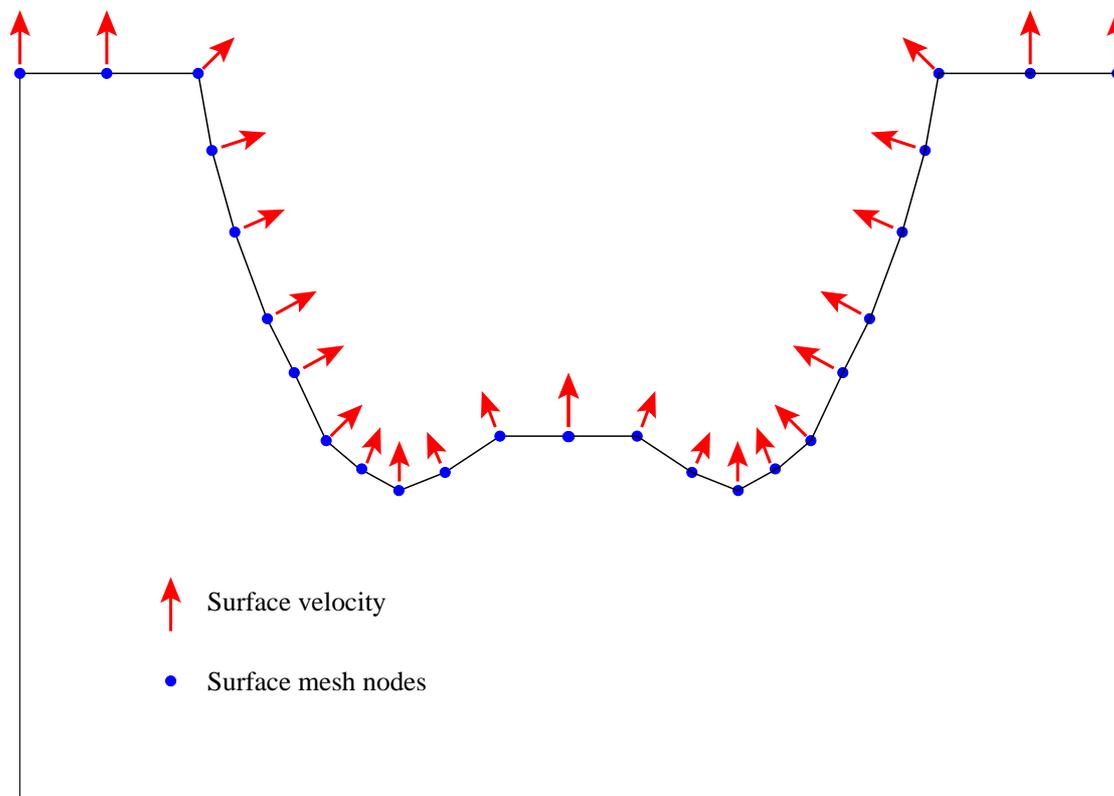


Figure 2.1: Illustration of the representation of a boundary by string-based method.

keeping the CPU time at a minimum. For this purpose the number of nodes needs to be kept at a minimum. In order to do this the nodes have to be distributed as a function of the curvature. Thus the flat part of the interface only requires one line segment independent of its length. While this can be easily achieved, during the advance of neighboring surface facets along their normals, interstices or duplications occur and thus area-readjustment procedures for de-looping are needed. However, these procedures induce significant computational error into the simulation result in proportion to the complexity of the process geometry. Furthermore, these methods are very time and memory consuming in three dimensions and strongly limit the applicability of these methods in three dimensions.

2.2.2 Cell-Based Methods

This method has also been introduced under different names such as partial fraction or cell method [64, 65]. Considering a grid within a computational domain, a basic idea of this method is to assign values to each grid cell depending on the fractional part of the cell containing the interface. Therefore, grid cells which are totally lying within or outside the interface get 1 or 0, respectively. The grid cells containing a part of interface get a value between 0 and 1. These grid cells are called surface cells as shown in Figure 2.2. After advancing the interface, the fractional values are updated where the interface is detected. The main advantages of this approach are its robustness and good handling of critical structures such as high aspect ratio trenches used in simulations.

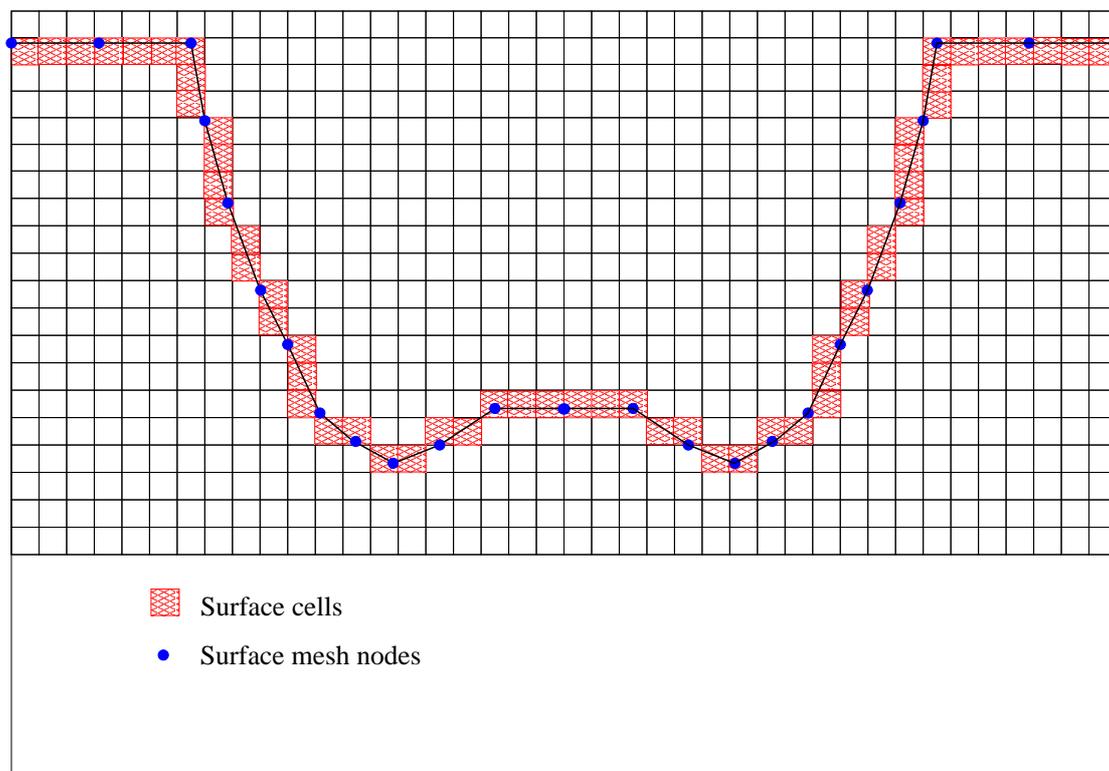


Figure 2.2: Illustration of the representation of a boundary by cell-based method.

There are some disadvantages, however:

- Calculation of geometrical quantities such as surface normals and curvatures is inaccurate.
- Since the accuracy of the localization of the interface based on fractional values strongly depends on the grid resolution, a high grid resolution is needed to extract the interface reliably.

At our institute Dr. Pyka has implemented a topography simulator based on the method described above. The simulator has been used to rigorously treat different etching and deposition models. Furthermore, it has been used to generate accurate input geometries to guarantee reliable interconnect or device analysis [64].

2.2.3 Level-Set-Based Methods

The level set method [80] is an interesting alternative method that solves the previously mentioned problems emerging with the other methods. It provides means to describe boundaries, i.e., curves, surfaces or hyper-surfaces in arbitrary dimensions, and their evolution in time which is caused by forces or fluxes normal to the surface. The basic idea is to view the curve or surface in question at a certain time t as the zero level set (with respect to the space variables) of a certain function $\varphi(t, \mathbf{x})$, the so called level set function as shown in Figure 2.3. Thus the initial surface is the set $\{\mathbf{x} \mid \varphi(0, \mathbf{x}) = 0\}$.

Each point on the surface is moved with a certain speed normal to the surface and this determines the time evolution of the surface. The speed normal to the surface will be denoted by $F(t, \mathbf{x})$. For points on the zero level set it is usually determined by

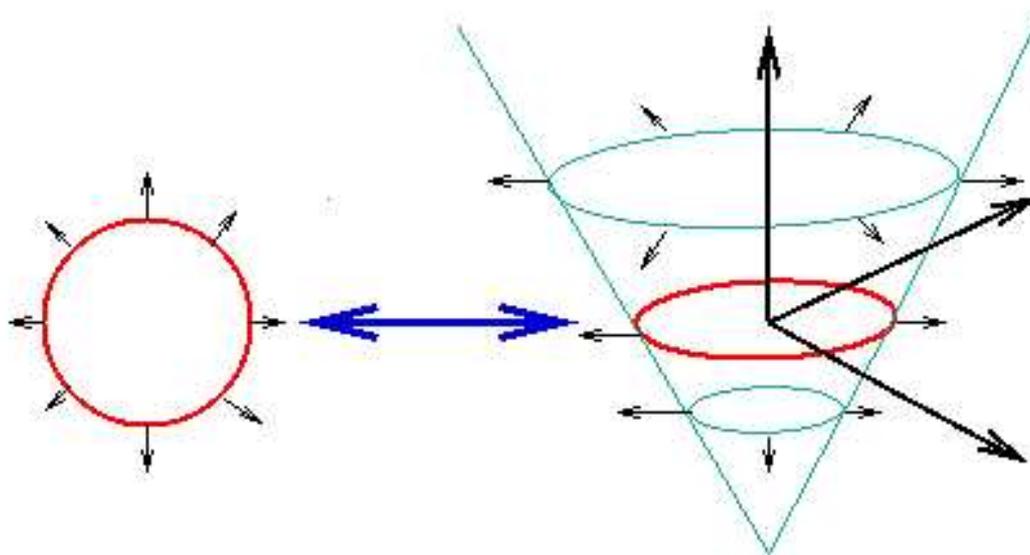


Figure 2.3: Illustration of the idea of the level set method. The curve on the left is the original curve in xy plane. This curve is built into a cone-shaped surface, namely, the level set function as shown on the right. The intersection of the level set function with xy plane in each time step gives the curve.

physical models, in our case by etching and deposition processes, or more precisely by the fluxes of certain gas species and subsequent surface reactions. The speed function $F(t, \mathbf{x})$ generally depends on the time and space variables and we assume, for now, that it is defined on the whole simulation domain and in the whole time interval considered.

The surface at a later time t_1 shall also be considered as the zero level set of the function $\varphi(t, \mathbf{x})$, namely $\{\mathbf{x} \mid \varphi(t_1, \mathbf{x}) = 0\}$. As we showed in (2.2) with some notational differences, this leads to the level set equation

$$\varphi_t + F(t, \mathbf{x})\|\nabla_{\mathbf{x}}\varphi\| = 0, \quad \varphi(0, \mathbf{x}) \text{ given}, \quad (2.3)$$

in the unknown function φ , where $\varphi(0, \mathbf{x})$ determines the initial surface. Having solved this equation, the zero level set of the solution is the sought curve or surface at all later times.

Although in the numerical application the level set function is eventually calculated on a grid, the resolution achieved is in fact much higher than the resolution of the grid, and hence higher than the resolution achieved using a cellular algorithm on a grid of the same resolution. This is due to the surface extraction step, where the curve or surface is reconstructed by lines or triangles using linear interpolation of the level set values on the grid. Of course the level set function must essentially remain a linear function near to the zero level set.

3 Topography Effects in Deposition and Etching

Fundamental physical mechanisms in deposition and etching processes generate both desired and undesired topographic features. In this chapter we provide a basis for understanding and modeling these effects on topography. A common framework for modeling etching and deposition is given, including the terminology used for describing the various physical phenomena and effects.

3.1 Common Aspects of Deposition and Etching

While deposition and etching are nearly opposites and there is great diversity of processing equipment used to perform them, from a topographical point of view they have a lot in common.

The starting point for both is the nature of flux which arrives from a source above the wafer. The second commonality is how the self-shadowing of an existing profile affects the visibility of the source and how the re-emission from the profile or radiosity affects other points of the profile. The third common aspect is that mechanical and chemical reactions at the surface determine the local advancement rate and are one of the most challenging aspects of deposition and etching. The final common characteristic of deposition and etching is the time-advance of the surface profile. In this chapter we focus on this final common aspect.

3.1.1 Flux Nature

In the case of deposition a broad angular distribution of small particles of target material is introduced from an upper electrode. In the case of etching there may be one or more positively charged species bombarding the wafer with a nearly vertical Gaussian distribution of incident angles.

3.1.2 Effects of Topography on the Visibility

The topography profile on the wafer affects the visibility of local points on the profile. Certain parts of the profile may cast shadows on other parts of the profile (cf. Figure 3.1) and thus reduce the visibility to various flux components. In deposition this plays a very important role in filling contacts with metal, because, as the aspect ratio of the contacts increases, it becomes increasingly difficult to deposit enough metal on either the bottom or the side-walls due to this shadowing. More complex point to point interactions along the topography profile can also be important. In deposition and etching processes a particle might not stick where it first lands, but plays a small game of billiards before coming to a final rest. This is known as re-emission (cf. Figure 3.1) and the sticking coefficient between zero and one is the fraction of the particles that sticks. A sticking

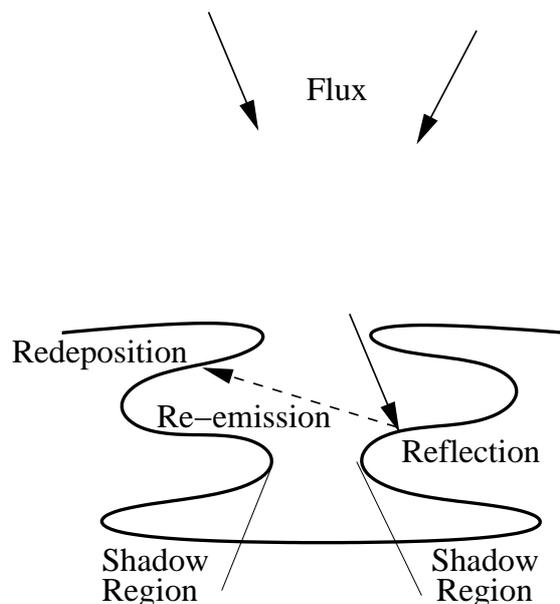


Figure 3.1: An illustration of the boundary interaction with the incident flux and re-emission.

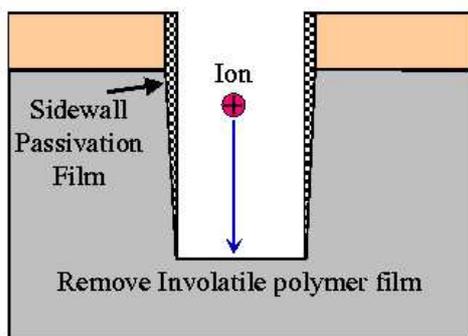


Figure 3.2: A schematic of forming the protective layer on the side-walls during an anisotropic etching process.

coefficient of unity means that the particle sticks. Conversely, a low sticking coefficient means that the particle may bounce many times. In plasma etching and more properly reactive ion etching it is the directed flux of species, which passes through the mask opening that enhances the etch rate. The selectivity of the etch rate of the substrate relative to the mask has to be considered. High energy bombardment is associated with mechanical etching effects which are less selective than chemical etching. On the other hand the anisotropy of the etching can be enhanced by providing a thin protective layer mostly polymer on the side-walls (cf. Figure 3.2) against the spontaneous etch reaction. Indeed, this layer prevents lateral etching and then leads to the vertical side-walls during an etching process.

3.1.3 Surface Reaction

The third common aspect stems from mechanical and chemical reactions at the surface determining the local advancement rate. These are one of the most interesting phenomena of deposition and etching. In deposition, columnar grain growth is possible and the column angle tilts with the angle of incidence according to the billiard player's rule. In deposition and etching processes there is evidence that a specific orientation of the initial boundary can affect the final profile, because the shadowing effects due to visibility between the boundary and source plane depend on the orientation of the boundary relative to the source plane, i.e., it makes a difference when the boundary is aligned parallel or perpendicular to the source plane. Furthermore, surface mobility can introduce diffusion of species along the surface in both deposition and etching. In plasma etching the ion bombardment can both accelerate reactions and remove by-products. During etching a protective layer (cf. Section 3.1.2) can be formed that even protects from energetic neutrals and leads to vertical etch profiles [62].

3.1.4 Time-Advance of the Surface Profile

The local fluxes and etch or deposition reactions provide sufficient information on how the surface is to be deformed for a short time step. The time evolution of the profile requires many time increments which allow the change of the profile shape to influence its future shape through shadowing, etc. As the surface evolves there may be major topological changes. For example, outgrows of the material from sides of a trench might collide and close off a void, or etch fronts from two trenches might move laterally, collide and form a tunnel or an air bridge.

To ease the presentation a simpler two-dimensional case will be used. In two dimensions the profile is sometimes said to be made of line segments and intersections points which may also be called nodes. Figure 3.3 shows the simulation result of an isotropic deposition of a material into a rectangular structure. It can be seen easily that the boundary is expanded radially outward for a time step $\Delta t = t_2 - t_1$. The top right convex outward corner point causes a fan (cf. Figure 3.3) of facets to be generated which creates a rounded section in the profile at time t_2 . At the concave outward corner the planar fronts from the horizontal and vertical facets intersect in a line which is the location of a new corner point. These collisions where overlapping fronts occur and some information about the initial profile is lost are said to be shocks (cf. Figure 3.3). Note that shocks and fans play a very important role in determining the changes of topography during processing. For isotropic etching the profile moves from the surface into the material as shown in Figure 3.4. As expected the convex outward corner now produces a shock and the concave corner point produces a fan.

3.1.5 Basic Facet Analysis

To understand faceting of the initial profile the advancement of two neighboring facets as shown in Figure 3.5 is considered. The direction and rate of advance of a vertex where two facets intersect is of key interest. The two facets have downward normals which form angles θ_1 and θ_2 with respect to the vertical downward direction. They advance a distance which is the product of the planar etch rate for their orientation $R_p(\theta)$ and time step δt as $R_p(\theta_1)\delta t$ and $R_p(\theta_2)\delta t$, respectively. The vertex moves at an angle θ_v

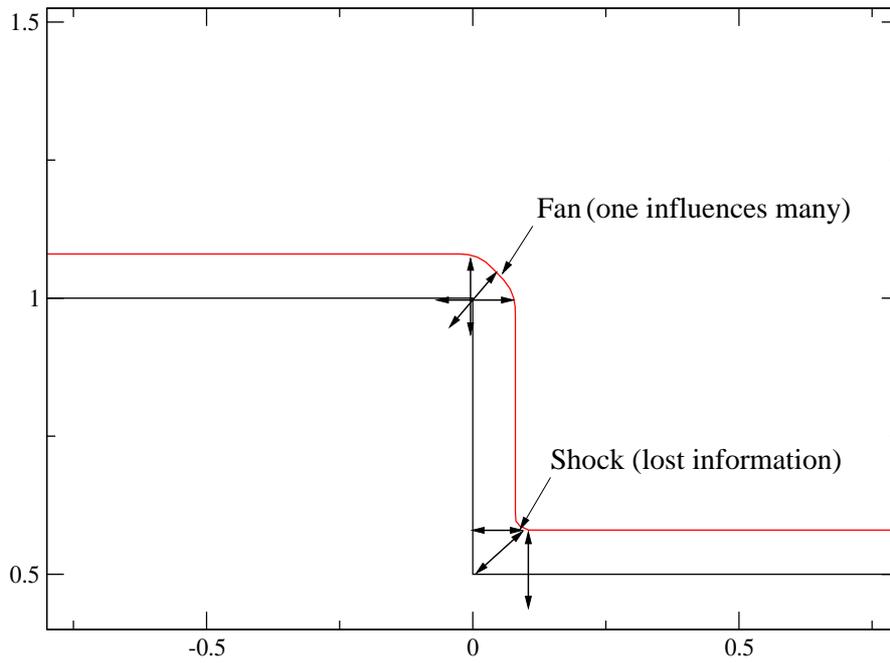


Figure 3.3: Isotropic deposition of a material into a rectangular structure.

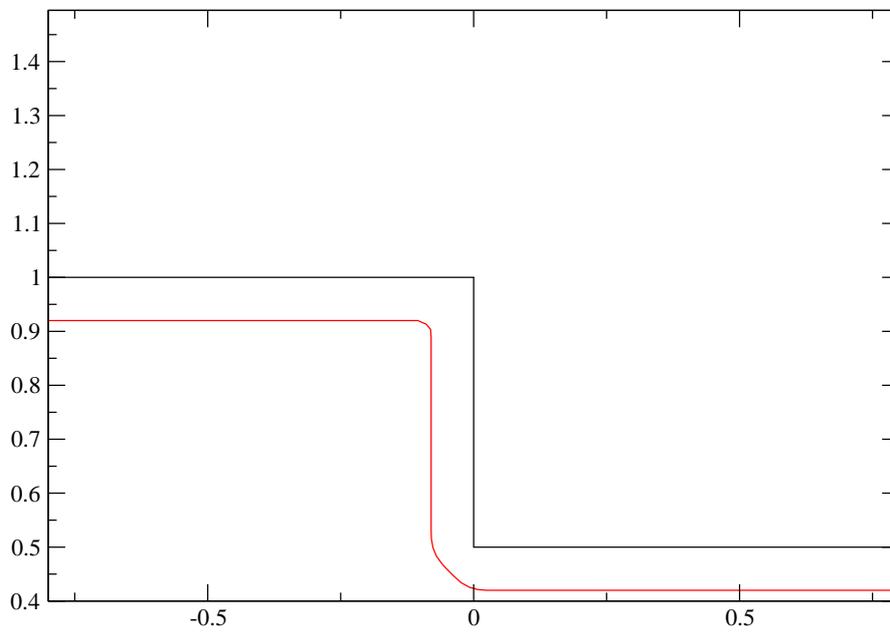


Figure 3.4: Isotropic etching of a material from a rectangular structure.

and a rate $R_v(\theta_v)$ and therefore a distance $R_v(\theta_v)\delta t$. The angles of the path of this vertex with respect to the normal of the two facets are α_1 and α_2 which are $\theta_v - \theta_1$ and $\theta_v - \theta_2$, respectively. Projecting the distance of movement of this vertex onto the distances advanced by the facets gives the two following equations:

$$R_v(\theta_v)\delta t \cos(\theta_v - \theta_1) = R_p(\theta_1)\delta t \quad (3.1)$$

$$R_v(\theta_v)\delta t \cos(\theta_v - \theta_2) = R_p(\theta_2)\delta t \quad (3.2)$$

Taking the ratio between (3.1) and (3.2) and eliminating $R_v(\theta_v)$ gives

$$\frac{\cos(\theta_2 - \theta_v)}{\cos(\theta_1 - \theta_v)} = \frac{R_p(\theta_2)}{R_p(\theta_1)}. \quad (3.3)$$

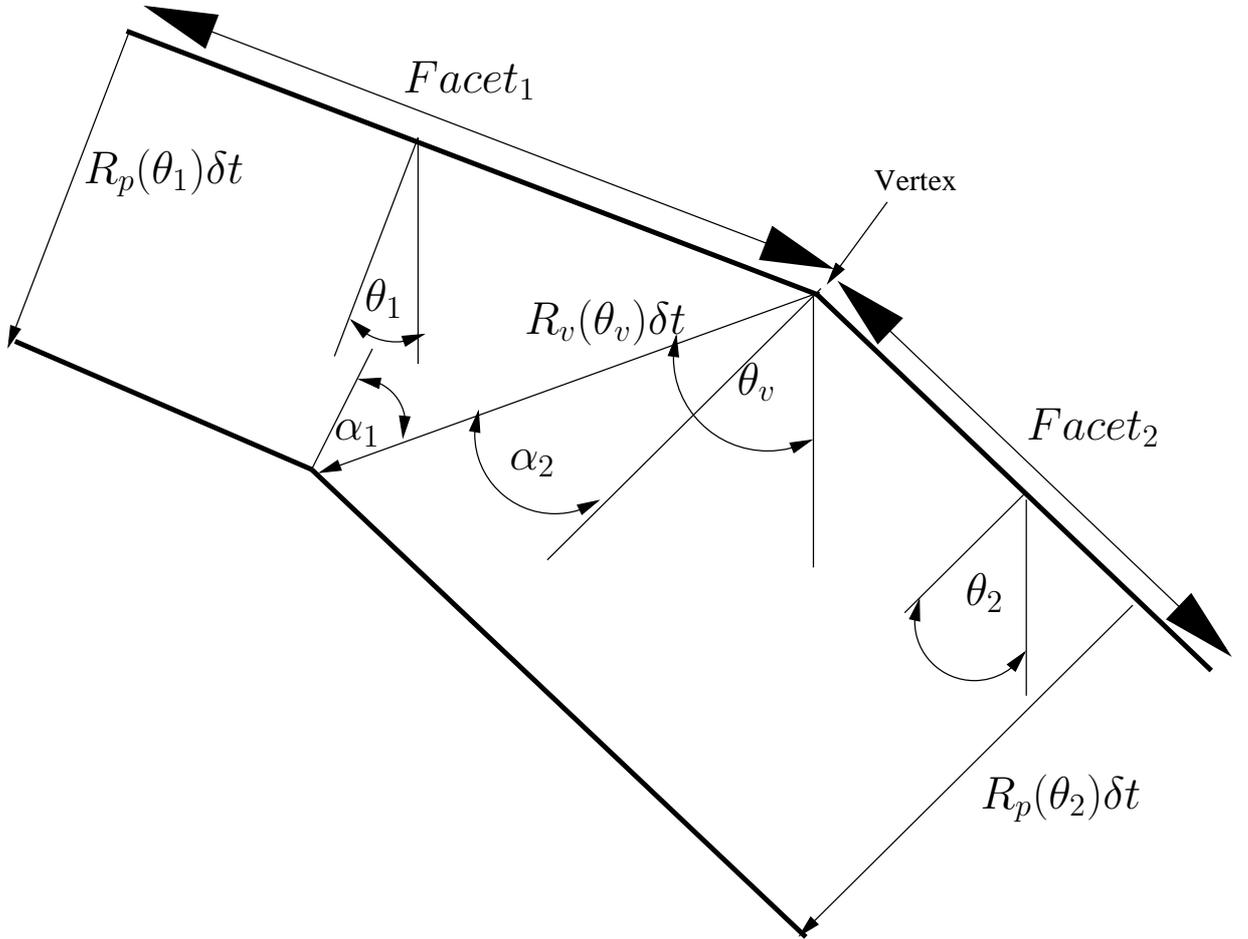


Figure 3.5: Geometry for the analysis of the advancement of the intersection between two adjacent facets.

Once θ_v is known the associated rate $R_v(\theta_v)$ can be found from (3.1) and (3.2) and is of course higher than $R_p(\theta_1)$ and $R_p(\theta_2)$.

(3.3) makes a number of interesting predictions about the physical nature of the motion of the vertex. Assuming that $\theta_1 < \theta_v < \theta_2$ and R_p is not a function of the facet angle θ , then the right hand side of (3.3) is unity, forcing $\theta_2 - \theta_v = \theta_v - \theta_1$ or $\theta_v = \theta_1 + \theta_2/2$ which means that the intersection vertex moves along the bisecting angle.

Another important case is that R_p increases with the angle θ . This makes the right hand side of (3.3) > 1 which leads to $\theta_2 - \theta_v < \theta_v - \theta_1$ or $\theta_v > \theta_1 + \theta_2/2$. This means that the faster moving facet will encroach into the region of the slower moving facet and likely expands in size.

To further explore how the movement of a facet depends on the shape of the rate function, the direction of travel of a facet at angle θ with rate function R_θ is now derived in a limiting case. Assuming that the angle between a facet pair is small enough, their intersection vertex will propagate in the direction of motion of the facet. This limiting case can be determined from (3.3) by taking the special case of $\theta_1 = \theta$ and $\theta_2 = \theta + \delta\theta$ and letting $\delta\theta$ go to zero. Substituting θ_1 and θ_2 in (3.3) and expanding R_p in a Taylor series gives

$$\cos(\delta\theta) - \frac{\sin(\theta - \theta_v) \sin(\delta\theta)}{\cos(\theta_v - \theta)} = 1 + \frac{dR_p(\theta)}{d\theta} \cdot \frac{\delta\theta}{R_p(\theta)}. \quad (3.4)$$

Letting $\delta\theta$ go to zero in (3.4) gives

$$\tan(\theta_v - \theta) = \frac{dR_p(\theta)}{d\theta} \cdot \frac{1}{R_p(\theta)}. \quad (3.5)$$

(3.5) indicates that a facet at angle θ moves laterally with a rate component proportional to the slope of the rate function $dR_p(\theta)/d\theta$ as well as normal to the surface at the usual rate $R_p(\theta)$.

3.1.6 Corner Rounding

Regarding the evolution of facets each facet has a plane associated with it. The plane moves with a given normal speed which may be different for different facets. The boundaries of the facets are determined by the intersection of the planes. The two-dimensional evolution near a corner is shown in Figure 3.6. If we use a level-set method where the normal speed is a simple interpolation between the two normal speeds, then the corners would be rounded, as shown in Figure 3.7 (in particular, an arc of a circle would arise, if the two speeds are the same). In order to keep flat facets and sharp corners, the following precautions must be made. The evolution of a smooth curve only depends on the normal speed, the addition of a tangential component only has the effect of changing the parameterization of the curve. With a velocity that has a proper tangential component to the facet and is directed towards a corner, the facets will evolve maintaining sharp corners as shown in Figure 3.6. For example, for $\mathbf{v}_1 = \mathbf{v}_2$ and a square corner, the necessary tangential velocity component which has to be added on both sides of the corner is \mathbf{v}_1 . Note that this is a lower bound for the tangential velocity. In fact, if we move the points with a tangential velocity larger than this value, the evolution of the interface will still be the same. The addition of the tangential velocity causes the characteristics to collide; the solution does not become multivalued, because standard techniques are

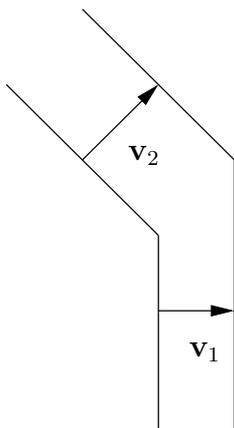


Figure 3.6: Facet evolution near a corner.

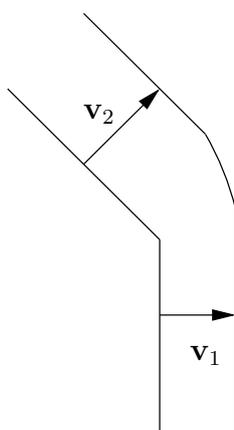


Figure 3.7: Evolution near a corner when the normal speed at the corner is a linear interpolation of the normal speeds of the two facets.

used for viscosity solutions of the Hamilton-Jacobi equation [71]. This causes a shock to form and maintains a sharp corner. Note that the velocity that we add is tangential to the facet, not to the interface. This has the effect of modifying the normal component of the interface, if the latter is not aligned with the facet. In this respect the method can be viewed as a technique to construct a proper normal velocity law, given the speeds of the facets.

3.2 Minimizing the Corner Rounding

In order to minimize the corner rounding during the movement of a boundary the approach introduced by Russo and Smereka [71] can be used where the speed of each facet must be specified. Consider an interface consisting of M facets, with normals \mathbf{v}_m and absolute value of normal speeds ω_m for $m = 1, \dots, M$. Let \mathbf{n} be the normal at a given point of the interface.

In order to compute the proper velocity of the surface at a given point, first the facet

is selected which is closest in direction to \mathbf{n} , i.e., for which $n \cdot \mathbf{v}_m$ is a maximum,

$$k = \arg \max_m (\mathbf{n} \cdot \mathbf{v}_m). \quad (3.6)$$

Next the following velocity is defined

$$\mathbf{c} = \omega_k \mathbf{n} + u \mathbf{a} \quad (3.7)$$

where

$$\mathbf{a} = \frac{\mathbf{n} - (\mathbf{n} \cdot \mathbf{v}_k) \mathbf{v}_k}{[|\mathbf{n} - (\mathbf{n} \cdot \mathbf{v}_k) \mathbf{v}_k|^2 + \varepsilon^2]^{\frac{1}{2}}} \quad (3.8)$$

and u is the tangential speed which will be specified below. The parameter ε in the denominator is a numerical parameter which ensures that \mathbf{a} vanishes smoothly when the numerator vanishes.

Some simple geometric considerations as shown in Figure 3.8 and the following equations help us to find the tangential speed that must be added to keep a sharp corner.

$$(\omega_1 + u_{12}^\perp \tan \alpha)^2 + \omega_2^2 - 2\omega_2(\omega_1 + u_{12}^\perp \tan \alpha) \cos \alpha = d^2 \quad (3.9)$$

where $d = l \cos \alpha$ and $l = (\omega_1 + u_{12}^\perp \tan \alpha) \tan \alpha$. Substituting l and d in (3.9) gives

$$[(\omega_1 + u_{12}^\perp \tan \alpha) \cos \alpha - \omega_2]^2 = 0 \quad (3.10)$$

and finally the equation for the tangential speed is as follows:

$$u_{12}^\perp = \frac{\omega_2 - \omega_1 \cos \alpha}{\sin \alpha} \quad (3.11)$$

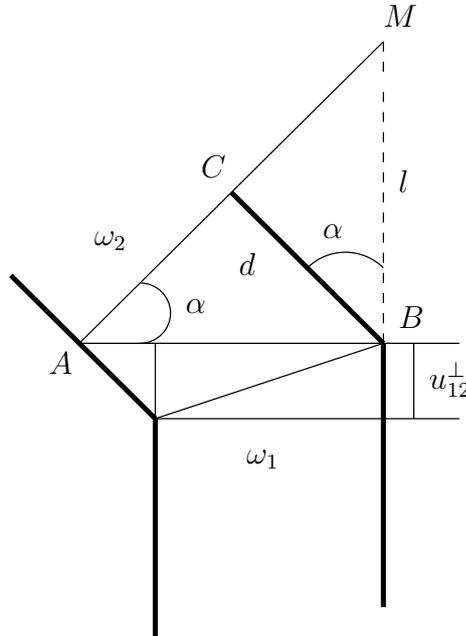


Figure 3.8: Geometry to analyze the advancement of the intersection between two adjacent facets.

The quantity u can then be chosen equal to u^* , where

$$u^* = \max_{ij} u_{ij}^\perp \quad (3.12)$$

where facet i is a neighbor of facet j and $\omega_j \geq \omega_i$.

For a faceted interface $\mathbf{a} = 0$, because $\mathbf{n} = \mathbf{v}_k$ and the facet will evolve with the standard normal speed. On the other hand, if we evolve the whole interface with the velocity $\mathbf{v} = \omega_k \mathbf{n}$, then the corners get rounded as shown in Figure 3.7. When the corners become slightly rounded, then \mathbf{a} becomes directed towards the corners and the surface will move with a velocity that will try to keep the corners sharp.

Choosing a small value for ε , the vector \mathbf{a} is basically a unit vector whenever \mathbf{n} is not aligned with the facets. Neglecting ε , the normal speed \mathbf{c} can be calculated from (3.7) with the following equation

$$\mathbf{c}^\perp = \omega_k \mathbf{n} + u \mathbf{a}^\perp \quad (3.13)$$

The normal part of \mathbf{a} can be calculated from (3.8) as follows:

$$\mathbf{a}^\perp = \frac{\mathbf{n} - (\mathbf{n} \cdot \mathbf{v}_k) \mathbf{v}_k (\mathbf{v}_k \cdot \mathbf{n})}{|\mathbf{v}_k| \cdot |\mathbf{n}| \cdot |\mathbf{n} - (\mathbf{n} \cdot \mathbf{v}_k) \mathbf{v}_k|} \quad (3.14)$$

and therefore

$$|\mathbf{a}^\perp| = \frac{1 - (\mathbf{n} \cdot \mathbf{v}_k)^2}{\sqrt{1 + (\mathbf{n} \cdot \mathbf{v}_k)^2 - 2(\mathbf{n} \cdot \mathbf{v}_k)^2}}. \quad (3.15)$$

Substituting (3.15) in (3.13) gives the normal speed of our model for the level set function

$$F = \omega_k + u \sqrt{1 - (\mathbf{n} \cdot \mathbf{v}_k)^2}. \quad (3.16)$$

In Chapter 7 we will present the application of this method to get the trenches with a minimal corner rounding during the simulation of an etching process.

4 Simulation Models for Deposition of Silicon Dioxide Layers from TEOS

During the fabrication of an IC a wafer has to undergo many processes. Each process accomplishes a specific change in the state of the wafer. Some of these processes can be described using relatively simple models. However, many processes require more complex models to be described reliably. Process modeling and simulations have been used to provide a general understanding and not for quantitative prediction of processes [17,18]. Therefore, for more general prediction and analysis, a general topography simulator must use detailed descriptions of chemical reactions with chemical reaction rates and thermodynamic properties of the species obtained by experiment and/or by calculation. In addition, topography simulations should be done in conjunction with reactor-scale simulations in order to compute gas transport to and from the reactive surface in a self-consistent manner.

One standard way to accurately perform a feature-scale simulation of CVD processes is to use a system of reversible elementary chemical reactions which are implemented in the general topography simulator using CHEMKIN or SURFACE CHEMKIN [26,49].

In order to quantitatively understand and optimize the reaction conditions in a CVD or plasma process, complex chemical reaction flows have to be simulated. Although reaction conditions and geometries are very variable among the applications of chemically reaction flows, all of them need accurate and detailed descriptions of the chemical kinetics occurring in the gas-phase or on reactive surfaces. Chemical reaction mechanisms containing hundreds of reactions and involving fifty or more chemical species are not uncommon in such models. The CHEMKIN suite of codes broadly consists of three packages for dealing with gas-phase reaction kinetics, heterogeneous reaction kinetics, and species transport properties [50].

The CHEMKIN software package has been developed for incorporating the complex mechanisms of gas phase chemical reactions into numerical simulations [49]. Thereafter, different codes based on CHEMKIN have been implemented that solve chemical reacting flows. In order to easily enable the user to specify the necessary input information, the CHEMKIN interface uses a high-level symbolic interpreter. This interpreter parses the information and passes it to a CHEMKIN application code. The user writes an input file declaring the chemical elements in the problem, the name of each chemical species, thermochemical information about each chemical species, the rate constant information, and a list of chemical reactions which is written in the same manner that a chemist would write them, i.e., a list of reactants converted to products [50]. The thermochemical information is entered as a series of polynomial coefficients describing the species entropy, enthalpy, and heat capacity as a function of temperature. Because the information about the reaction mechanisms is parsed and summarized by the CHEMKIN interpreter, if the user desires to modify the reaction mechanisms by adding species or deleting a reaction, for instance, only the interpreter input file has to be changed, while the

CHEMKIN application code (for example, a rotating-disk reactor simulation code) does not have to be altered. The modular approach of separating the description of the chemistry from the set-up and solution of the reacting flow problem gives the software designer great flexibility in writing chemical-mechanism-independent code. In addition, the same mechanism can be used in different chemically reacting flow codes without changes.

The SURFACE CHEMKIN package has been developed for specifying the mechanistic and kinetic rates of heterogeneous chemical reactions [50]. SURFACE CHEMKIN is run in connection with CHEMKIN and the execution of the CHEMKIN interpreter is required before the SURFACE CHEMKIN interpreter can be run. The user interface for SURFACE CHEMKIN is very similar to that of CHEMKIN, but is extended to account for the richer nomenclature and formalism required to specify heterogeneous reaction mechanisms.

The transport software package provides the gas-phase transport properties. It also includes the effects of such phenomena as thermal diffusion and provides the calculation of the pure species viscosity, pure species thermal conductivity, and binary diffusion coefficients for every gas-phase species in the mechanism, as a function of the temperature.

A number of high-level CHEMKIN applications for chemically reacting flow simulation has been produced during the last years. Many researchers around the world are using these codes and while the challenge for the researcher at the beginning was the software development, this is nowadays developing a realistic reaction mechanism for an accurate description of the system of interest.

These software packages have to describe chemical kinetic reactions in a reactor and on the surface. They consist of a thermodynamic database, interpreters to transform user-defined, human-readable chemical reaction mechanisms into rate equations suitable for numerical calculation, and subroutine libraries to perform kinetics calculation within simulation codes. The link between CHEMKIN and a topography simulator has two major implications. First, a wide range of chemical reaction systems already expressed in the CHEMKIN formalism can be simulated immediately both at the reactor-scale, using several CHEMKIN-based reactor simulation codes, and at the feature-scale, using a topography simulator, without manual reinterpretation of the reactions into a different reaction format.

This allows feature-scale simulators to employ detailed reaction mechanisms previously developed for the reactor-scale. Second, computational analysis of processes can be made at one scale with immediate feedback to the other scales. For instance, a predicted film profile inside a submicron feature will not only be sensitive to transport in the reactor and in the submicron feature, but also to the choice of reaction mechanisms. Therefore, the individual models at different length scales must be coupled by feeding the results from higher order scales into the lower order scales and feeding back the lower orders to the higher order scales for forming a tightly coupled solution.

However, the basic difficulty of combining reactor- and feature-scale simulations has been the inherent disparity in length scales. These length scales can span more than six orders of magnitude, i.e., from about a meter at the reactor-scale to submicrometer at the feature-scale. Cale *et al.* [17] investigated a different approach which consists of using a reactor-scale simulator to predict the conditions near the wafer surface based on the operating conditions. These local conditions are then used in a feature-scale simulator to predict deposition profiles at different positions on the wafer surface. Holleman *et al.* [17] have attempted to determine the effect of feature-scale on the reactor-scale, of course,

with only focussing on the feature-scale. Thus, in both of the above approaches, there was no feedback of information of one scale to the other one.

Another approach used to link up reactor- and feature-scale simulations is the effective reactivity function formulation described by Rogers and Jensen [17]. In this approach the reactor- and feature-scale simulations are linked together using an effective reactivity ε , which includes effects of both surface variations as well as feature-scale transport. A Monte Carlo-based ballistic transport (cf. Section 4.1) scheme is used to calculate the effective reactivity of a single feature. The reactivity of each set of features is then linearly superimposed to obtain ε . To resolve the gradients in ε one has to guarantee that the source plane for the Monte Carlo simulation is at a sufficient distance from the wafer surface. Satisfying this requirement is an elementary step to use superimposition.

The effective reactivity is then fed into the reactor-scale simulation as an enhancement factor to the flux boundary condition over a blanket area. The reactor- and feature-scale simulations are then iterated to arrive at a consistent solution. This technique has been applied to the simulation of tungsten deposition. While this technique can be used to couple reactor- and feature-scale simulations, the prohibitive time requirements for each feature-scale simulation and calculation of ε , and the iterative nature of this process, make it difficult to efficiently use this approach.

The above mentioned two-scale approaches assume that the reactor-scale simulator, utilizing a mesh which is much coarser than typical for a feature-scale simulation, can compute appropriate conditions for a particular feature. Furthermore, the structure of the wafer surface representation in the two-scale approach is necessarily crude [30]. When using a feature-scale simulator at a particular boundary of the reactor-scale, the implicit assumption is that any single feature is a part of a cluster of identical features for which the single feature is a representative member. But in order to represent such a cluster appropriately in a numerical sense, several grid points across the cluster are needed. This limits the reactor-scale simulator to model unrealistically large feature clusters. However, the details of the surface structure of a realistic die with several much smaller clusters can not be represented. Thus, feedback from the feature-scale to the reactor-scale is indeed difficult.

Gobbert *et al.* [30] introduced a mesoscopic-scale model to simulate deposition processes at the scale of a few dies. It was used to provide an understanding of the deposition processes at a scale inaccessible by both reactor- and feature-scale models. This approach not only avoids the excessive grid resolution that is necessary for a single model, but also allows to capture the underlying physics by varying the model description according to the scale. The model regime changes from continuum transport (cf. Section 4.1) to ballistic transport at different length scales. This implemented model involves a transient reactor-scale simulator for continuum mechanics, which solves the governing equations of mass, momentum, heat, and species concentrations as a function of position and time. On the reactor-scale, the wafer topography is not explicitly taken into account, and the information from the other scales is only incorporated as a net flux boundary condition on all nodes of the final grids representing the wafer. At the next level which corresponds to the meso-scale, continuum equations are still valid and the same solver is used as for the reactor-scale problem. However, at the feature-scale the continuum equations are no longer valid and the transport of individual molecules has to be taken into account to accurately represent the underlying physics.

This three-scale simulation approach couples numerical meshes whose typical mesh

sizes are separated by fewer orders of magnitude than in the two-scale approach. Moreover, due to meaningful feedback from the smaller scales to the larger ones, reactor scale simulations may account for the depletion or accumulation of chemicals close to the surface [30]. However, it is important to note that even in the coarsest implementation of the mesoscopic model, which assumes all features inside one cluster to be identical, there can be variations from one cluster to the others both in geometry and in reactor conditions. Indeed, an implementation using a sufficient number of mesh points can even represent variations inside a cluster. Furthermore, this model has also limited predictive capability because of its dependence on input parameters from the two other scales. A truly predictive simulator must have the capability to couple phenomena occurring at the reactor-scale, meso-scale, as well as the feature-scale, where information from each scale is transferred correctly and coupled tightly to the other scales.

Generally, the proposed models for the deposition of SiO_2 from TEOS CVD process fall into two categories: first as mentioned above, those which use complex surface reaction models including the integration of reactor-, meso-, and feature-scale. Second, those which use the sticking coefficient model with one or more species.

In spite of the complexity of the models from the first category, their quantitative predictability is still very limited for processes of industrial interest. Therefore, the simpler calibrated sticking coefficient models provide good alternatives for process investigations and especially for time-consuming optimizations and inverse modeling tasks. The parameters of simulation are evaluated and optimized using SIESTA (simulation environment for semiconductor technology analysis) [16, 35].

The goal of this chapter is to identify simulation models for the deposition of silicon dioxide layers from TEOS in a CVD process and to calibrate the parameters of these models by comparing simulation results to SEM images of deposited layers in trenches with widely different aspect ratios. We describe the models which lead to the best results. We also draw conclusions regarding the usefulness of the models.

4.1 The Models

A transport model can be characterized by the ratio of the mean free path length of the species to the characteristic length scale (the largest dimension of the feature). This ratio is called K_n (Knudsen number) [18]. A high K_n ($\gg 1$) implies that the frequency of particle-particle collisions is negligible relative to particle-surface collisions, i.e., the process is in free molecular regime or BTRM (ballistic transport and reaction model). A small K_n ($\ll 1$) implies that collisions between particles occur much more frequently than collisions between particles and the feature surface. This is called continuum transport regime. A K_n about one implies the transition regime where the order of magnitude of the particle-particle and particle-surface collisions are approximately the same [18].

Because of the low pressure condition of the TEOS process, the mean free path length of the species is much higher than the feature dimensions and thus K_n is $\gg 1$. The process is in the free molecular regime and the radiosity model can be applied for the transport of the particles [80].

In the earliest attempts at our institute [37], a single trench was simulated successfully. The so called point-shape source model was used, where the source of species is assumed to be a single point or a very small number of points in the middle of the simulation

domain or along a line above the trench. The flux distribution around the vertical axis follows a cosine form (this distribution is also assumed for the models presented in the next sections) and the direct flux received at the surface elements was assumed to be proportional to the inverse of the distance between the source and the middle point of a surface element. However, the optimum sticking factors showed a strong dependence on the aspect ratio [37].

4.1.1 Line Source Model

As mentioned above, the previous model is not able to predictively simulate a set of trenches with widely different aspect ratios. There are additional problems as the model does not allow to simulate several trenches back to back (cf. Chapter 6). The first idea for overcoming this problem was to set many point-shaped sources along a source line above the wafer. However, one open question is at which distances the points must be placed, i.e., how many source points and how far do we have to extend the source line beyond the simulation domain to obtain a reliable number of sources? To avoid the problem of asymmetry which becomes apparent with this solution, if one half of the trench sees a source point more than the other half due to the discretization, the number of points has to be increased above a certain threshold value which is related to the chosen discretization. However, the simulation time is increased considerably, because the number of visibility tests between the surface elements and point-shaped sources increases significantly. The line source model presented in the following is a good alternative to overcome the mentioned problems.

In this model [9] the source consists of a line of continuous point-shaped sources above the trench as shown in Figure 4.1. Using this model, one of the expensive time consuming parts of the discrete set of point-shaped sources, namely, the visibility test is moderated and the computation time is therefore significantly reduced. In our experience, visibility

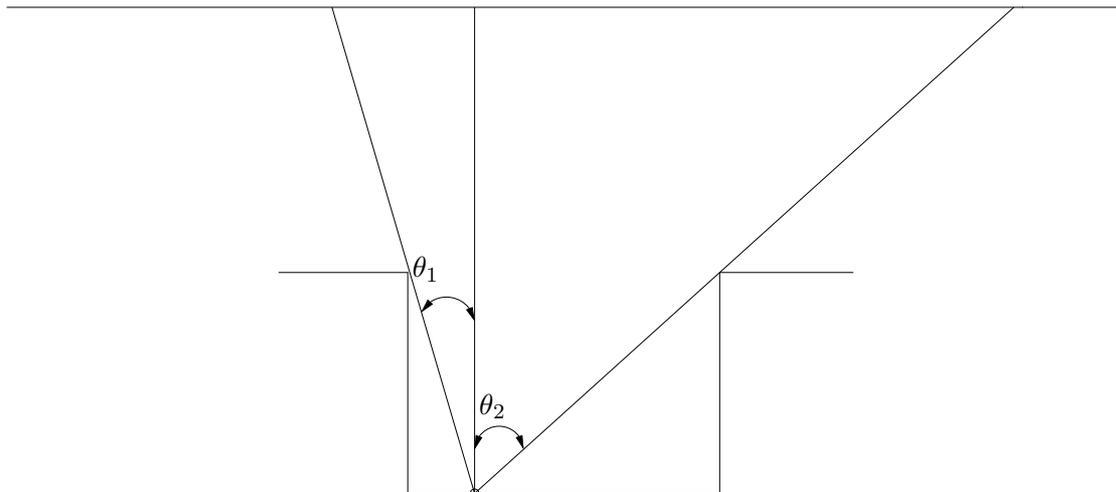


Figure 4.1: Illustration of the calculation of the incoming flux.

tests in steps of one degree give sufficient accuracy. Therefore, instead of separate visibility tests among a surface element and different sources, a complete visibility test is performed in a maximum 180 steps, which is the case if a surface segment is on the flat open part of the trench. After the calculation of the visibility angle between a surface element and the source line the incoming flux can be calculated. In this model the incoming flux has been assumed to depend only on the visibility angle between the surface elements and the source line as follows:

$$\text{Flux}_{\text{incoming}} \propto \int_{-\theta_1}^{\theta_2} \cos(\theta) = \sin(\theta_2) + \sin(\theta_1)$$

Two different sticking coefficients have been identified by calibration using SIESTA. The first coefficient denotes the sticking probability of the particles arriving directly from the source on the surface while the second coefficient describes the reflection probability of the particles from the surface elements. Although the outline of the trench for a low aspect ratio is reproduced predictively as shown in Figure 4.2, it is difficult to reproduce both the upper and lower part of the trenches at the same time for a higher aspect ratio as demonstrated in Figure 4.3.

4.1.2 Flux Dependent Sticking Coefficient Model

Although in the previous model the sticking coefficients have been assumed to be constant, the overall sticking coefficient for a species can be written as a function of the local fluxes of the reacting species on the surface [19]. Assuming that the deposition from TEOS is through heterogeneous decomposition of species with the rate depending on temperature and the flux of the species [19] the overall sticking coefficient can be written as

$$\beta(T, F(\mathbf{x})) = \frac{R(T)}{F(\mathbf{x})} \quad (4.1)$$

where R is the number of molecules per area and per time that become part of the film, and $F(\mathbf{x})$ denotes the position-dependent flux. If the heterogeneous deposition reaction follows m th order kinetics with respect to Arrhenius temperature dependence of the rate parameter $k(T)$, then

$$R(T) = k_0 \exp\left(\frac{-E_a}{k_B T}\right) F(\mathbf{x})^m = k(T) F(\mathbf{x})^m \quad (4.2)$$

where k_0 is the temperature independent pre-exponential factor and E_a is the activation energy for the reaction. (4.2) is a commonly used form for heterogeneous kinetic expressions which are usually determined by analyzing film growth rates on a flat substrate as a function of temperature and reactant concentrations. Substituting (4.2) into (4.1) results in

$$\beta(T, F(\mathbf{x})) = k(T) F(\mathbf{x})^{m-1}. \quad (4.3)$$

Based on (4.3) and two further assumptions we developed a flux dependent sticking coefficient model [9]. The first assumption is that the temperature T remains constant

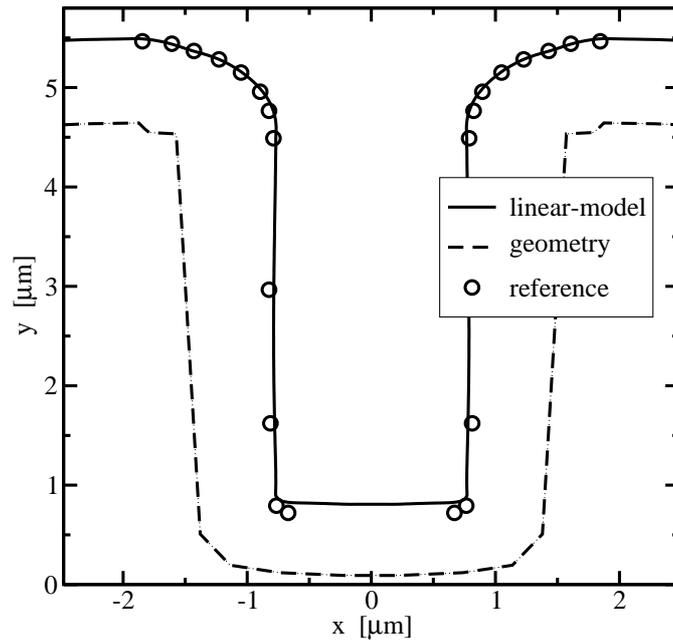


Figure 4.2: Comparison of simulation and measurement for the continuous line source model for a trench with a low aspect ratio.

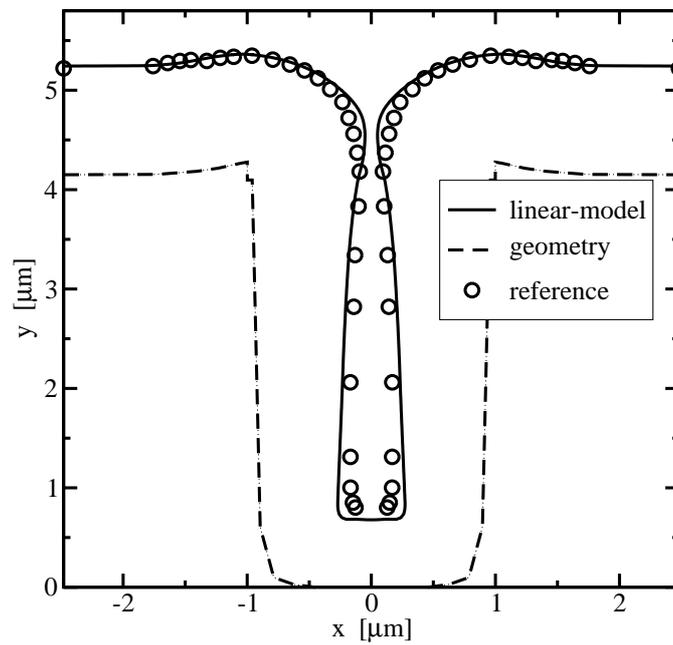


Figure 4.3: Comparison of simulation and measurement for the continuous line source model for a trench with a higher aspect ratio.

and the second is that the deposition of silicon dioxide from TEOS follows a half order reaction [19], i.e., $m = 1/2$. Therefore, the sticking coefficient is $\beta = \beta_0 F(\mathbf{x})^{-1/2}$, where β_0 is a constant scaling factor to guarantee that sticking coefficients are always equal to or less than one.

The simulation results are in good agreement with the measurements for trenches with low aspect ratio as shown in Figure 4.4. For higher aspect ratios, however, the amount of material deposited on the side-walls is overestimated as shown in Figure 4.5. This may result in spurious void formations.

4.1.3 Two Species Model

With the last two models we have reached the limits of models which assume a single species for the deposition of silicon dioxide from TEOS.

Generally there are two approaches to model the kinetics which control a LPCVD (low pressure CVD) process: surface kinetics dominated and transport dominated.

The surface kinetics dominated model has been pursued by many authors modeling deposition on flat surfaces [21, 24, 55]. Here, it is assumed that the source gases do not react until they reach the wafer surface and thus, the deposition is totally controlled by surface reactions. In this case, modeling proceeds by assuming different surface reaction paths, and comparing the resulting rate kinetics with the observed dependence of the growth rate on partial pressures calculated from the source gas flow rates. It is assumed that the reaction path model whose kinetics best matches the measurements is the correct model. While this approach has been successful for some deposition processes, it leads to models with too many parameters for topography simulations. In addition, the assumption that no pre-reaction takes place does not hold well when deposition shows poor conformality. Therefore, one has to assume a highly reactive species whose deposition rate is inconsistent with the source species concentrations [48].

With the second approach, as described in [48], the deposition is assumed to be controlled by the transport inside the device structure of one or two rate limiting species which contribute considerably for determining the growth rate. These species are not confined to the source gas species, but could be the result of gas phase reactions or reactions on surfaces of the reactor. The model does not deal with the details of the chemistry of growth, which is not completely understood in the case of deposition of silicon dioxide from TEOS. However, this model can be extended easily to take detailed growth chemistry into account if these details are known.

The incident species is adsorbed at the surface and depending on the reaction probability (reactive sticking coefficient) of the species with the surface, the incident species may be re-emitted from the surface, react at the point of incidence and become a part of the surface or diffuse along the surface to another surface site and then react or be re-emitted.

Studies have shown [12, 48, 56] that for LPCVD of silicon dioxide from TEOS, re-emission instead of surface diffusion is the most likely surface-species interaction mechanism. Therefore, we also neglect surface diffusion and only consider re-emission in our simulations.

An often debated issue related to the single sticking coefficient model for the LPCVD of silicon dioxide from TEOS is the mechanism which has been commonly suggested. This mechanism assumes that silicon dioxide is deposited by TEOS decomposition at the

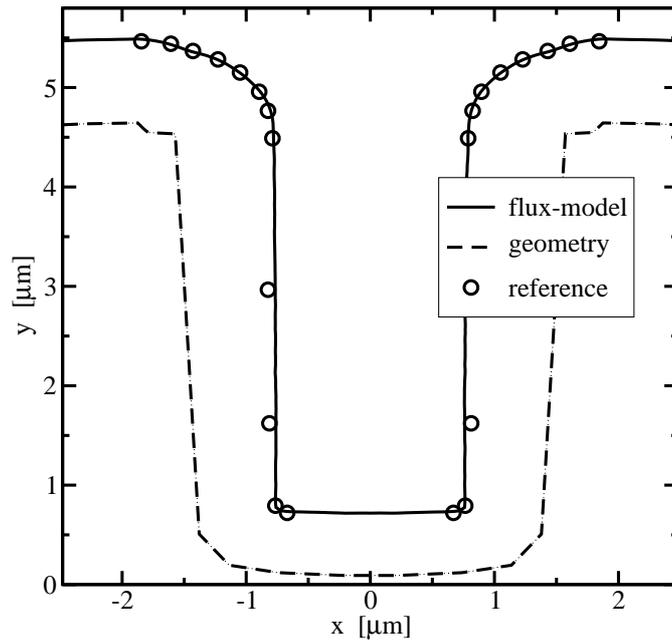


Figure 4.4: Comparison of simulation and measurement for the flux dependent sticking coefficient model for a trench with a low aspect ratio.

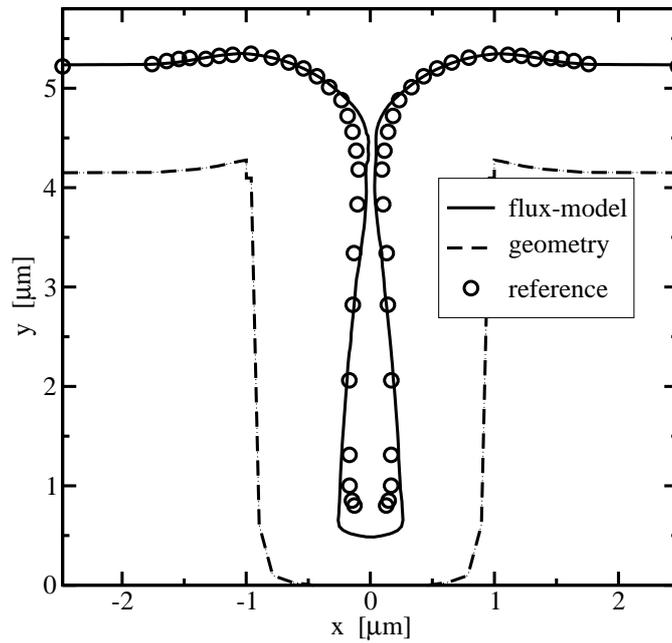


Figure 4.5: Comparison of simulation and measurement for the flux dependent sticking coefficient model for a trench with a higher aspect ratio.

surface. However, this does not describe the formation of intermediate reaction products in the gas phase or on the surface. It has been proposed in [48] that there may be a second reaction path in the LPCVD of silicon dioxide from TEOS. This leads to formation of a very reactive intermediate, due to gas phase reactions, which reacts with the surface to form silicon dioxide. The reactions used there, are merely a suggestion of one possible set of reactions but do not rule out any other reaction paths. The model considers two species but does not care how they are formed. Therefore, the model is independent of the reaction path for the formation of the species.

Based on the idea of this model we have developed our two species model [9], which not only considers the transport of a single gas species above the wafer and its sticking and reflection on the surface, but also producing a second species at the surface because of the chemical reaction happening in interaction between the first species and the surface. We assumed that the flux of the second species is proportional to the flux of the species coming directly from the source. In our model there are two possibilities to include the effects of the second species, either to consider increasing or decreasing the deposition rate.

The following equation has been used for the calculation of the total flux on the surface segments

$$F_{\text{total}} = F_A \cdot (1 \pm \alpha F_B) \quad (4.4)$$

where F_{total} is the total flux at the surface segment, F_A is the flux of the first species, α is a proportional factor, and F_B is a normed flux of the second species. It is important to note that F_A and F_B in this model and the flux in Section 4.1.2 can be calculated using an iterative solver. This iterative solver can be set to stop the calculation if the difference between the flux value at the new step and the last step is smaller than a user defined error term (cf. Section 5.10). This model shows excellent agreement with SEM images as shown in Figure 4.6 and Figure 4.7.

4.2 Summary

A multitude of deposition models for TEOS processes as well as means for the calibration of simulation results to measurements have been proposed. In summary we find that a two-species model yields the best results among the three different deposition models investigated, both for high and low aspect ratio trenches. More complex deposition models can be avoided with this model.

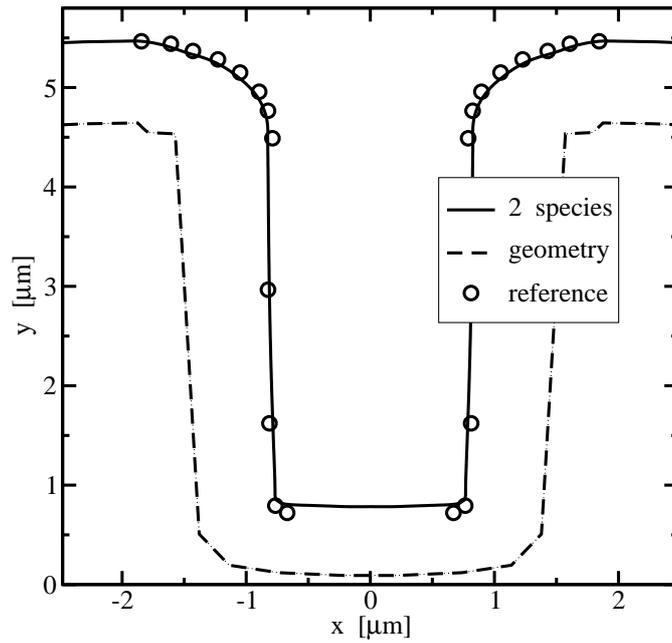


Figure 4.6: Comparison of simulation and measurement for the two species model for a trench with a low aspect ratio.

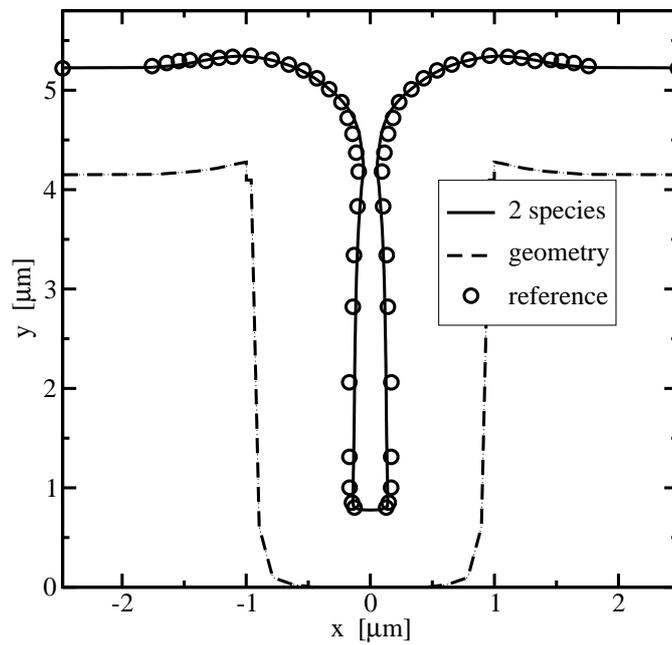


Figure 4.7: Comparison of simulation and measurement for the two species model for a trench with a higher aspect ratio.

5 The General Purpose Topography Simulator ELSA

In this chapter the application of the level set and fast marching methods for the development and implementation of the topography simulator ELSA in two and three dimensions is presented. ELSA rest on many techniques, including a narrow band level set method, fast marching for solving the Eikonal equation and extension of the speed function, transport models, visibility determination, and an iterative equation solver.

The development and implementation of a two-dimensional topography simulator based on the level set method have begun at our institute by Dr. Heitzinger [35]. It has been written in Lisp. However, its use was only limited to the simulation of the deposition of layers into single features.

5.1 Simulation Flow of ELSA

Every feature-scale topography simulation must take the following three main steps into account. First, the transport of particles above the wafer in the boundary layer must be simulated. This can happen in the radiosity regime as described in Section 5.3. Second, the fluxes of particles at the wafer surface found in the previous step determine the chemical reactions that take place at the wafer surface. Third, the surface of the substrate moves according to the fluxes found in the second step.

The simulation flow is shown in Figure 5.1. The simulation stops when a prescribed time is reached or when a layer of prescribed thickness has been deposited. In the next sections the different techniques used during the implementation of ELSA are explained and discussed.

5.2 Initialization

In order to apply the level set method a suitable initial function $\varphi(0, \mathbf{x})$ has to be determined first. There are two requirements: first it goes without saying that its zero level set has to be the surface given by the application, and second it should essentially be a linear function so that linear interpolation can be applied in the final surface extraction step.

The signed distance function of a point from the given surface has shown to be a good choice for the initial level set function. This function is the common distance function multiplied by minus or plus one depending on which side of the surface a grid point lies. The common distance function of a point x from a set S is then defined by $d(x, S) := \inf_{y \in S} d(x, y)$, where d is a metric, usually the Euclidean distance.

Consider a fixed orthogonal grid for a whole simulation domain. Because of the ease of two-dimensional illustration, we show a two-dimensional interface introduced as a series of points which form line segments. To construct the initial boundary, we try

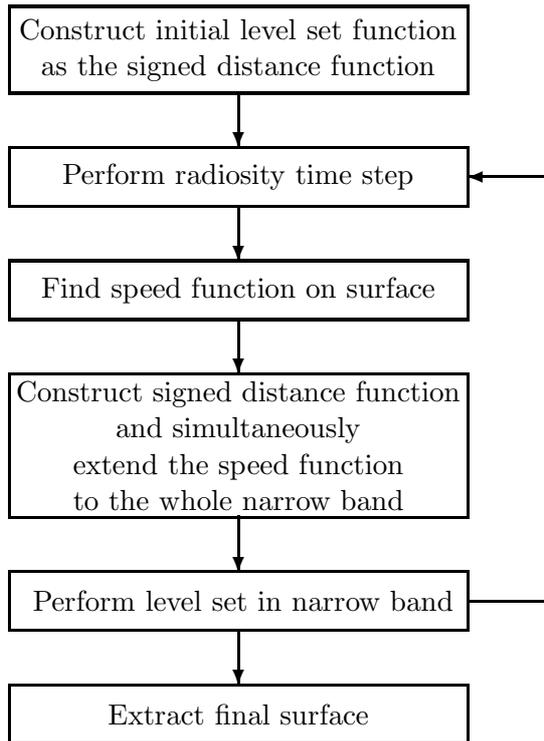


Figure 5.1: Overview of simulation flow as combination of a physical transport model and surface evolution using the level set method.

to keep the number of points representing the interface to a minimum to avoid long computational time during the calculation of the initial level set function. Figure 5.2 shows an example to illustrate the technique used for the calculation of a common distance function. Consider the grid point M whose distance from the boundary we want to calculate. We first calculate the distance of M from all segments which form the boundary. The line segments are AB , BC , CD , DE , and EF . From elementary mathematics we know that the distance of a point from a line is the length of the normal line drawn from point to the line, e.g., the distance of M from line segment CD is MG . However, there is not always an intersection point between the normal line and segment as it is the case for the line segment EF , where MH is outside EF . In such cases the distance is the minimum of ME and MF .

After the calculation of these different distances and getting the minimum value among them, we still need to assign a sign to this value depending on the position of the grid point relative to the boundary. In order to do this we choose a reference point R inside the boundary and at the bottom of the simulation domain. If the connection line between a grid point and the reference point intersects the boundary at an odd or even number of times, the grid point is outside or inside the boundary and the common distance function must be multiplied by plus or minus one, respectively. For example, the grid point N is outside the boundary since the line RN intersects the boundary once at I and the grid point O is inside the boundary, because the line RO intersects the boundary twice, at J and K .

Since the level set algorithm will later only work in a narrow band and the calcu-

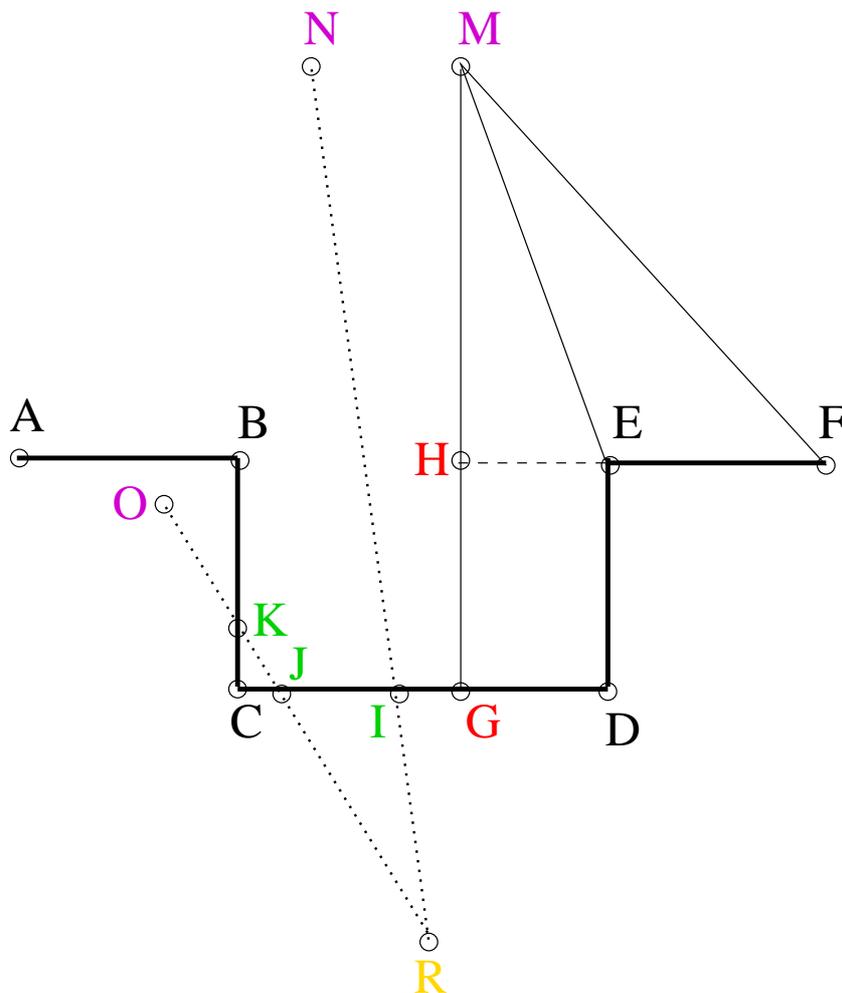


Figure 5.2: Illustration of the calculation of a common distance function of a grid point from a boundary.

lation of the distance function especially in three dimensions is very CPU expensive, it is sufficient to perform the distance calculations near the initial boundary. This can be achieved, e.g., by a recursive algorithm walking along the boundary. First, a point whose distance to the boundary is smaller than the width of the future narrow band is identified by walking along the boundary of the simulation domain in y -direction or z -direction for two or three dimensions, respectively. When such a point is found, it is used as the starting point for the recursion. In the recursion only points with a distance smaller than the narrow band width are considered for the next step. The maximum distance ever computed during this procedure is used to initialize the grid points above and below the boundary with a positive or negative sign, respectively. This method reduces the computational effort of initialization from $O(N^3)$ and $O(N^2)$ to $O(N^2)$ and $O(N)$ in three and two dimensions, respectively, where N is the number of grid points in each direction.

For three-dimensional initialization, in analogy to two dimensions one has to calculate the distance of the grid points to different triangles which represent the boundary. The

distance of a point from a triangle t is given by $d(P, t) = \min_{T \in t} \|P - T\|_2$ and the distance $d(P, b)$ of a point from the initial boundary $b = \{t_1, \dots, t_m\}$, consisting of a set of triangles, is given by $d(P, b) = \min_{t \in b} d(P, t)$.

The initial level set function for a rectangular trench is shown in Figure 5.3. As it can be seen in this figure the signed distance function is a linear function with a value of zero at the boundary.

5.3 Transport of Particles

Before we begin to describe the radiosity model used by transport of particles, we have to present the definition of the visibility of a point from another point. This plays an important role for the calculation of the flux at the surface elements as it can be seen later in this section.

Figure 5.4 is an illustrative example for the definition of visibility. There are different kinds of visibility which have to be defined. The first kind is the visibility among the points of a boundary such as (A, B) , (A, C) , and (B, C) . The second kind is the visibility between a boundary point and a source point which is assumed to be S in Figure 5.4.

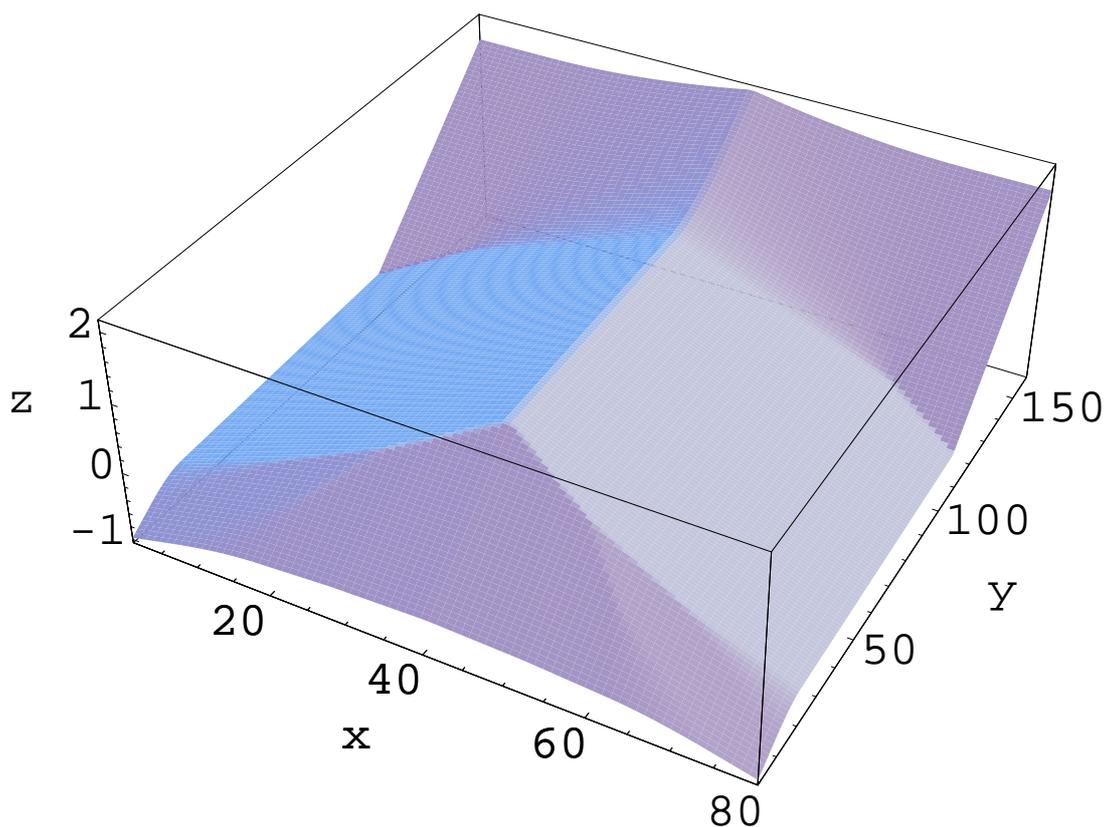


Figure 5.3: The signed distance function is used as the initial level set function which corresponds to the initialization of a rectangular trench. The grid resolution was 80×160 .

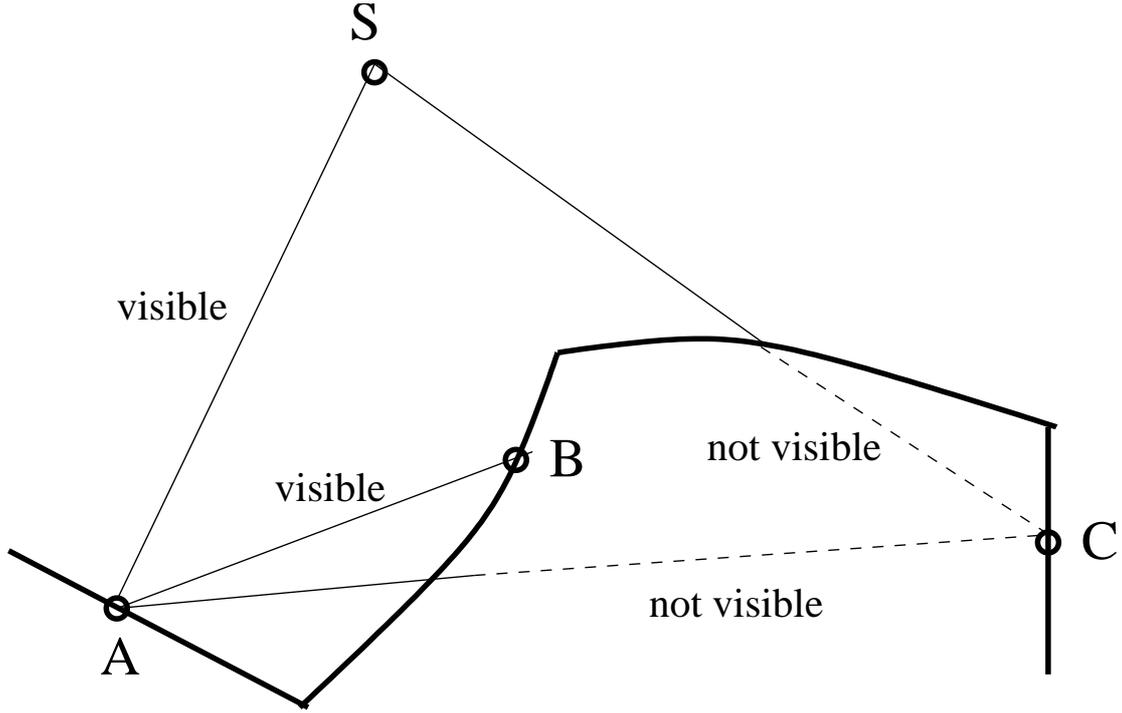


Figure 5.4: An illustrative example for the definition of the visibility between two points.

Whereas the pairs of points (A, S) , (A, B) , (B, S) , and (B, C) are visible from each other, there is no visibility between the pairs of points (A, C) and (S, C) .

A formulation of the radiosity model [80] for the case of luminescent reflection, pertaining to low energy particles (cf. Section 4.1), can be used in the deposition simulations.

To model deposition it is assumed that the distribution of the particles coming from the source obeys a cosine function around the normal vector of the plane in which the source lies [19]. This implies that the incoming flux at a surface element is proportional to the cosine of the angle between the connecting line between the center of mass of a surface element and the source, and the normal vector of the source plane.

The flux reaching the surface elements obtained by the surface extraction step may be written as a vector,

$$\begin{aligned} \text{Flux} &= \beta_0 I_S + \beta \Psi L I_R \\ &= \frac{\beta - \beta_0}{1 - \beta} I_S + \frac{\beta(1 - \beta_0)}{1 - \beta} \underbrace{L^{-1}(L^{-1} - (1 - \beta)\Psi)^{-1}}_{T:=} I_S. \end{aligned}$$

Here I_S is the vector of fluxes coming from the sources to the surface elements, I_R is the vector of fluxes that arrive because of reflections, β_0 the sticking coefficient for particles coming directly from the source, β the sticking coefficient for secondary bounces, L the diagonal matrix containing the lengths of the surface elements, and

$$\Psi_{ij} = \frac{n_i \cdot (t_j - t_i) n_j \cdot (t_i - t_j)}{\pi |t_j - t_i|^3} v_{ij}$$

where t_i are the centroids of the surface elements, n_i their unit normal vectors, and v_{ij} is 1 if the surface element j is visible from i or 0 if not.

The second line in the equation above is obtained from the first one and the relationship $I_R = (1 - \beta_0)I_S + (1 - \beta)\Psi LI_R$ results from straightforward algebraic manipulations. In the case of multiple, low energy species, the calculation of the visibility matrix and the inverse T only depends on topographic information and thus does not have to be repeated for each species.

Most of the computation time for the simulation of the transport of the particles above the wafer by the radiosity model is consumed by first determining the visibility between a surface element and the source, and secondly, between two different surface elements. The latter has an $O(n^2)$ operation complexity, where n is the number of surface elements growing approximately with $O(N^2)$. If the connecting line between the center of mass of two surface elements does not intersect the surface, i.e., the zero level set, those surface elements are visible from each other. In order to decrease the computational effort related to determining the visibility between the surface triangles, we have assumed that two triangles are visible from each other if the center point of the grid cells in which the triangles are located, are visible from each other. Since there are at least two triangles in each grid cell, considerable time is saved.

5.4 Extending the Speed Function

In most of applications the speed function is only given on the boundary. For example, in the simulation of etching and deposition processes, the speed function on the boundary depends on the visibility of the source of species from the boundary segments. However, this visibility can only be calculated between the boundary and source of species, since it does not have any physical meaning, when we want to calculate it between the other level sets and the source of species [2–4]. Therefore, we must extend the speed function.

After we have calculated the speed function on the boundary, where the models of calculation differ depending on the process conditions (in Chapter 4 we will introduce several different models which are used to calculate the speed function on the boundary), we can start with extending the speed function. An extended speed function must satisfy two basic requirements. First it has to match the speed function calculated from a physical model on the boundary, and second it has to guarantee that it moves the other level sets in such a way that the signed distance function is preserved.

Assume that $\varphi(\mathbf{x}, 0)$ is a signed distance function which satisfies $|\nabla\varphi(\mathbf{x}, 0)| = 1$. We will prove that $|\nabla\varphi(\mathbf{x}, t)|$ will be equal to one, i.e., the level set function remains a signed distance function, if we build the following equation to extend the speed function [104]

$$\nabla\varphi \cdot \nabla F_{ext} = 0. \quad (5.1)$$

In order to prove this we build the following equation

$$\frac{d|\nabla\varphi|^2}{dt} = \frac{d(\nabla\varphi \cdot \nabla\varphi)}{dt} = 2\nabla\varphi \cdot \frac{d\nabla\varphi}{dt}. \quad (5.2)$$

The derivation of the level set equation in space is

$$\nabla(\varphi_t) + \nabla F_{ext} \cdot |\nabla\varphi| + \nabla|\nabla\varphi| \cdot F_{ext} = 0$$

which is represented as follows:

$$\frac{d\nabla\varphi}{dt} = -\nabla F_{ext} \cdot |\nabla\varphi| - \nabla|\nabla\varphi| \cdot F_{ext}. \quad (5.3)$$

Substituting $d\nabla\varphi/dt$ from (5.3) in (5.2) gives

$$\frac{d|\nabla\varphi|^2}{dt} = -2\nabla\varphi \cdot (F_{ext} \cdot \nabla|\nabla\varphi| + |\nabla\varphi| \cdot \nabla F_{ext})$$

which can be rewritten to the following form

$$\frac{d|\nabla\varphi|^2}{dt} = -2\nabla\varphi \cdot \nabla F_{ext} \cdot |\nabla\varphi| - 2\nabla\varphi \cdot \nabla|\nabla\varphi| \cdot F_{ext}. \quad (5.4)$$

The first term at the right hand side of (5.4) is zero because of (5.1) and if $|\nabla\varphi(\mathbf{x}, t)|=1$, the second term on the right hand side vanishes simultaneously with the term on the left. Therefore, we have proven that the level set function remains a signed distance function for all time if we extract the speed function using (5.1).

Now the speed function can be extended. For a level set function φ_n , where n stands for the n th time step, we choose a signed distance function φ_{temp} whose zero level set is equal to the zero level set of φ_n . As mentioned above, we need to satisfy the following equation

$$\nabla\varphi_{temp} \cdot \nabla F_{ext} = 0.$$

Note that the temporary signed distance function φ_{temp} is only used to extend the speed function and to guarantee that the signed distance function is preserved. It plays no other role such as for re-initialization, etc. The calculation of φ_{temp} is done by solving the so called Eikonal equation

$$|\nabla\varphi_{temp}| = 1$$

which is solved very effectively using the fast marching method. In the next section we will describe this method shortly.

5.5 Fast Marching Method

The fast marching method [78] is a method for the efficient calculation of the signed distance function. As mentioned in Section 2.1.3, the fast marching method is used in the boundary value formulation where the speed function must have a unique sign. Therefore, it is necessary to calculate once the signed distance function above the boundary and once below the boundary. The goal is to solve the Eikonal equation $|\nabla T|F = 1$ using proper and efficient algorithms. The key idea is to build an approximation of the gradient term which correctly deals with the development of corners and cusps in the evolving solution. It is well-known that the Eikonal equation becomes non-differentiable, and an appropriate weak solution must be built which is related to the entropy condition of propagating interfaces introduced in [76]. One of the simplest entropy-satisfying approximation of the gradient is from Godunov, and was used, for example, by Rouy and Tourin [68] to solve the Eikonal equation as follows:

$$\sqrt{\max(D_{ijk}^{-x}T, -D_{ijk}^{+x}T, 0)^2 + \max(D_{ijk}^{-y}T, -D_{ijk}^{+y}T, 0)^2 + \max(D_{ijk}^{-z}T, -D_{ijk}^{+z}T, 0)^2} = \frac{1}{F_{ijk}} \quad (5.5)$$

where

$$D_{ijk}^{-x}T = \frac{T(i, j, k) - T(i - 1, j, k)}{\Delta x}$$

$$D_{ijk}^{+x}T = \frac{T(i + 1, j, k) - T(i, j, k)}{\Delta x}$$

and i , j , and k are the indices of a grid point on the x , y , and z axis, respectively. D^{-y} , D^{+y} , D^{-z} , and D^{+z} are defined in analogy to D^{-x} and D^{+x} . Additional schemes for solving Hamilton-Jacobi equations may be found in [11, 63].

The upwind scheme¹ of (5.5) enables the calculation of T from the grid points adjacent to the boundary which have the smallest values of T . The boundary is swept along considering points in a narrow band (cf. Section 5.6) around the boundary. Marching this narrow band forward and freezing the values of the existing points and bringing the new points into the narrow band results in a solution of the Eikonal equation within the narrow band. More details can be found in [78, 79].

5.6 Narrow Banding Technique

The straightforward method for solving the level set equation is to solve it in the entire computational domain where one has to update all the level sets and not only the zero level set. This approach has been called the full matrix method. The advantage of this simple method is the simplicity of data structures and operations. Furthermore, it is a good starting point for the construction of a level set code. There are even cases in which this type of implementation is necessary, such as if all the level sets are themselves important as is the case in problems encountered in image processing. However, there is the disadvantage that an increase in the resolution of the grid increases the calculation time and the complexity according to $O(N^2)$ and $O(N^3)$, in two and three dimensions, respectively.

One technique to reduce the calculation time is to use adaptive mesh refinement. This refinement may be required especially in two regions. The first region is where the curvature of the boundary is high and the second is where the speed function changes very rapidly. For example, if the zero level set identified with the boundary is the object of interest, as is normally the case, then one has to adaptively refine the mesh around the location. However, considerable care must be taken at the interfaces between the fine and coarse cells. In particular, a subtle update strategy for the level set function values is required at so called hanging nodes where the boundary between two levels of refinement does not have a full set of nearest neighbors. Whereas advection terms which do not depend on the curvature lead to hyperbolic equations and a straightforward interpolation of the level set values from the coarse grid points easily produces the level set values at hanging nodes, there are some complications for the curvature dependent

¹An upwind scheme correctly respects the upwind nature of the differential equation and sends information in the direction that correctly matches the differential equation. Furthermore, an associated issue is the stability of a scheme. Stability is examined by finding those values for the time step and space step such that the small errors in the solution do not grow uncontrollably. Typically, the stability of a scheme depends on a balance between the time step Δt , the space step $\Delta \mathbf{x}$, and the speed; this is known as the CFL (Courant-Friedrichs-Levy) condition. For a constant speed equal to one, stability of the upwind scheme will require that $\Delta t \leq \Delta \mathbf{x}$.

advection terms. The situation is not so straightforward, since this corresponds to a parabolic term that can not be approximated by simple interpolation [80].

The idea leading to fast level set algorithms stems from the observation that only the values of the level set function near its zero level set are essential, and thus only the values at the grid points in a narrow band around the zero level set have to be calculated. The advantages of this technique are as follows:

- **Efficiency:** when working only in a narrow band around the zero level set, the operation complexity reduces from $O(N^3)$ and $O(N^2)$ to $O(lN^2)$ and $O(lN)$, for three and two dimensions, respectively. Here, l is the number of grid points in the narrow band.
- **Extending the speed function:** as mentioned in Section 5.4, in applications linking to physical models the speed function is not known on the whole simulation domain, but only at the surface. In order to use the level set method it has to be suitably extended from the known values to the whole simulation domain. Therefore, the problem of obtaining a smooth speed function within the entire computational domain is avoided or reduced into the narrow band.
- **Stability:** one of the most important things which must be taken into account, is the stability problem during the update of the level set function using finite difference methods where the CFL (cf. Section 5.13) condition must be fulfilled. Whereas this condition can be satisfied more easily by the zero level set and adjacent level sets, it is difficult to fulfill it for all level sets.

Figure 5.5 shows the simulation results of different steps of a deposition process into a typical trench. Except for step 0 for which the level set function with and without narrow banding has been shown, other intermediate level set functions corresponding to Figure 5.5 have been shown only within the narrow band in Figure 5.6. The grid resolution is 80×160 . The zero level set can be seen easily in each intermediate step and the formation of a void in step 48, as well.

5.7 Combining Narrow Banding and Extension of the Speed Function

In this section we present the implementation of an algorithm which combines narrow banding and extension of the speed function. This algorithm works as follows: first the initial points near the zero level set, where the speed function is known, and the neighboring trial points are determined. It is checked in the main loop, if there still is a trial point to be considered in the narrow band. All trial points are stored on a heap ordered by their distance from the zero level set. If there is a point to be considered, its distance is approximated, its extended speed is calculated, and its neighbors are updated accordingly. Finally, after the main loop, the bookkeeping information for the narrow band points is updated using the distance information just computed.

The detailed steps using several auxiliary functions are as follows: concerning the data structures, the information about the level set grid, the distance function, the extended speed function, and the tags for the fast marching method are stored in arrays. The trial points are stored on a heap. The implementation flow is as follows:

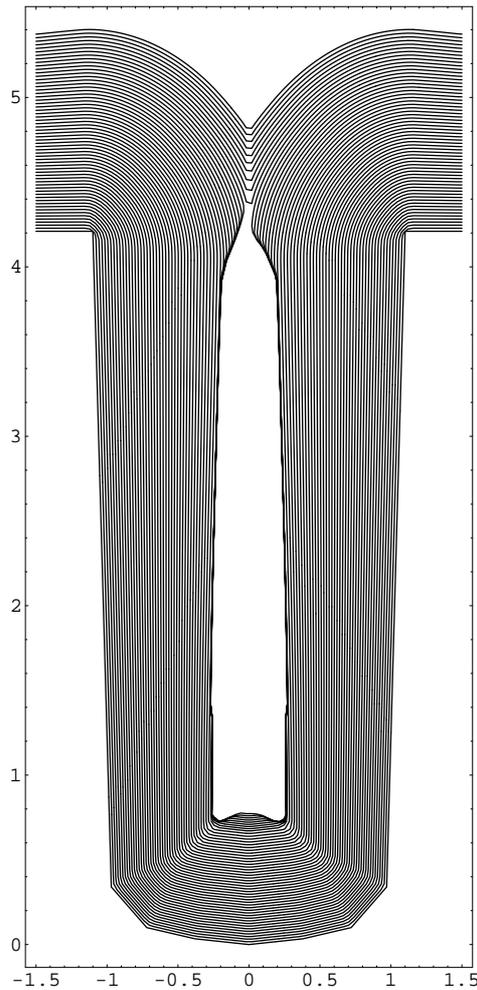


Figure 5.5: Simulation of void formation for a deposition process. A level set grid of 80×160 points was used.

1. First find the grid points whose speed function values are initially known. These values are computed in the physical simulation step and translated to the grid. Next compute the distance for the initial points, tag them as known, and initialize the corresponding grid points of the speed function. Find the trial points which are the neighbors of the initially known points, and compute their tentative distance values. All other points are far points.
2. While there are trial points, do the following:
 - a) Remove the first point from the heap and call it a . It has the smallest distance from the zero level set of all points on the heap.
 - b) If narrow banding is used and the maximum width of the narrow band is smaller than the distance of a , return from the loop.
 - c) Mark a as known.
 - d) For all neighbors b of a , do the following:

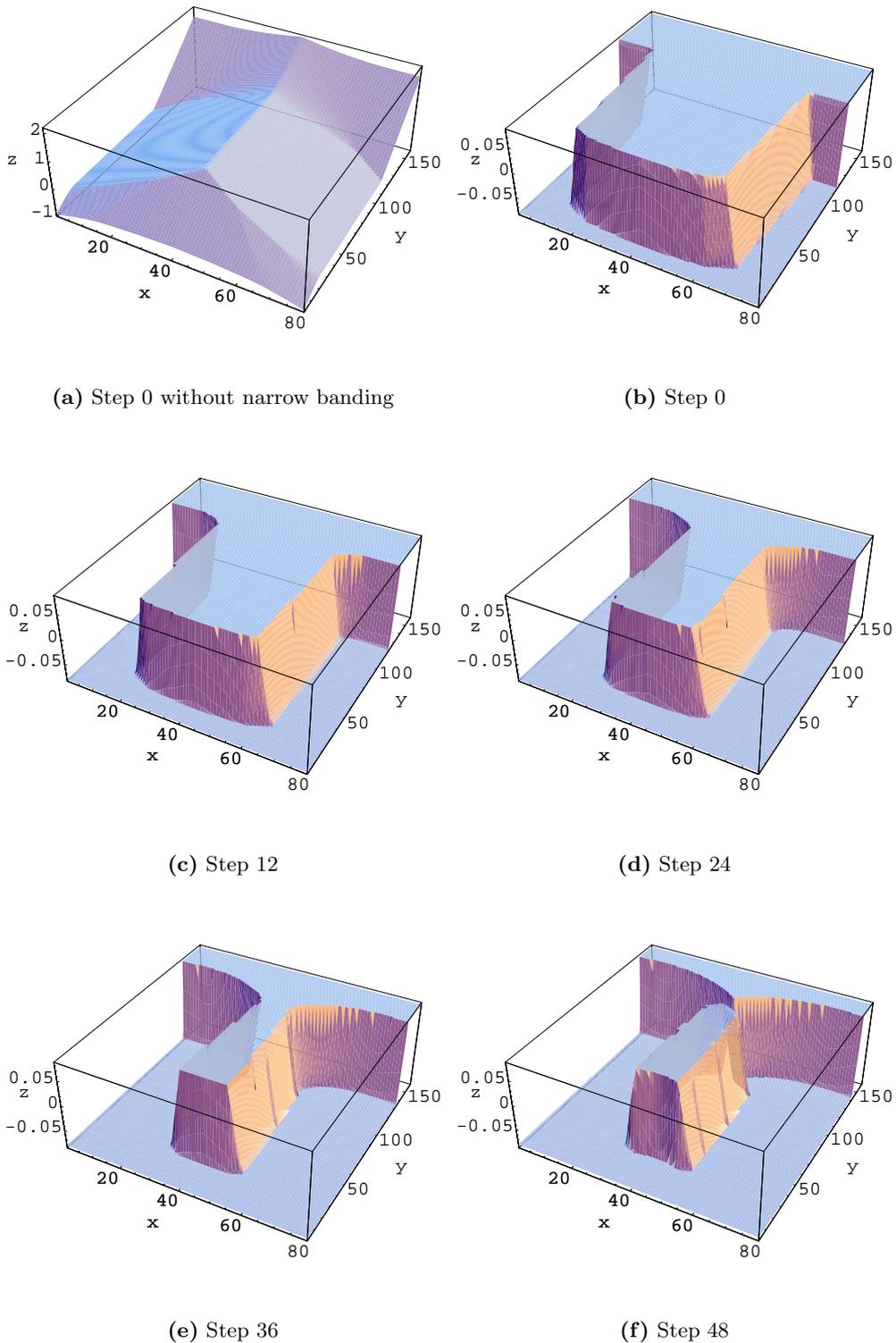


Figure 5.6: The level set functions at step 0, 12, 24, 36, and 48 during the simulation as shown in Figure 5.5. Inside the narrow band the level set function is retained to the end of the simulation, whereas the level set function values of the other points have been substituted with the width of the narrow band multiplied by 1 or -1 depending on their position.

- i. If b is a far point, recompute its distance and speed function values and mark it as a trial point.
 - ii. If b is a trial point, recompute its tentative distance and speed function values, unless it was computed in the previous step.
3. If narrow banding is used, set the distance values of all points which are not marked as known, to the width of the narrow band. Set the sign of the distance function.
4. Finally, return two objects, namely the new signed distance function and the extended speed function.

5.8 Coarsening Algorithm

When using the radiosity model to simulate the transport of particles above the wafer, two operations consume most of the computation time. The first operation is the determination of the visibility between all surface elements, which requires $\binom{n}{2}$ visibility tests, where n denotes the number of surface elements extracted from the level set grid. The second operation is the solution of a certain system of linear equations, which leads to the calculation of the inverse of a dense $n^2 \times n^2$ matrix.

Hence it is mandatory to keep the number of surface elements as low as possible. However, decreasing the number of surface elements must be done in such a way that the high resolution is obtained where it is needed, e.g., near the trench opening and at the bottom of the trench. One approach is to devise a refinement and coarsening strategy for unstructured grids at the level set implementation and the algorithms working on it. This, however, complicates the implementation because of the complex fast marching algorithm necessary at the unstructured grid compared to the algorithm at the rectangular grid which is used normally for the implementation of the level set method. In this work a different approach was taken by coarsening the surfaces after they have been extracted from the level set grid.

The coarsening algorithm works by walking down the list of surface elements extracted as the zero level set and calculating the angle between two neighboring surface elements. Whenever this angle is below a certain threshold value of a few degrees, the neighboring elements are coalesced into one. After one sweep through the list, the algorithm can be reapplied for further coarsening. After k coarsening sweeps, at most 2^k surface elements are coalesced into one. The resulting longer surface elements are used for the radiosity calculation, after which the fluxes are translated back from the coarsened elements to the original ones. This is a heuristic approach and has shown excellent results.

5.9 Advancing the Level Set Function Using Finite Difference Schemes

To discretize the level set equation, one can substitute the time and spatial derivatives with forward and central differences, respectively. We now consider a boundary with a right angle at the corner that is moved with a constant speed function normal to the boundary. Studies in [35, 80] have shown that using the central differences for spatial derivatives leads to false values of the gradient at the corner point. Since the slope $\nabla_{\mathbf{x}}\varphi$

is not defined at corners, the central difference approximation sets it to the average of the left and right slopes. Therefore, this wrong calculation of the slope propagates away from the corner and leads to oscillations.

An alternative approach would be to add a viscosity term to the right hand side of the level set equation as follows [80]:

$$\varphi_t + F(t, \mathbf{x}) \|\nabla_{\mathbf{x}} \varphi\| = \varepsilon \Delta \varphi$$

where ε is a positive constant. Although the solutions φ_ε guarantee the smoothness and their limits yield an appropriate weak solution as $\varepsilon \rightarrow 0$, the smoothness introduced by $\varepsilon \Delta \varphi$ often results in significant rounding of corners.

The best approach to discretize the equations of the form $\varphi_t + (G(\varphi))_{\mathbf{x}}$ are the following space convex schemes, where it is assumed that the flux $G(\varphi)$ is convex, i.e., $d^2 G/d\varphi^2 > 0$ [80]. These approaches ensure that discontinuities and boundaries remains sharp.

The simplest scheme to discretize the level set equation is the first order space convex scheme which is as follows:

$$\varphi^{n+1}(t) = \varphi^n(t) - \Delta t [\max(F_{ijk}, 0) \nabla^+ + \min(F_{ijk}, 0) \nabla^-] \quad (5.6)$$

where the $\varphi^{n+1}(t)$ and $\varphi^n(t)$ are the level set functions at the $(n+1)$ th and n th time steps, respectively, and

$$\nabla^+ = \left[\max(D_{ijk}^{-x} \varphi^n, 0)^2 + \min(D_{ijk}^{+x} \varphi^n, 0)^2 + \max(D_{ijk}^{-y} \varphi^n, 0)^2 + \min(D_{ijk}^{+y} \varphi^n, 0)^2 + \max(D_{ijk}^{-z} \varphi^n, 0)^2 + \min(D_{ijk}^{+z} \varphi^n, 0)^2 \right]^{\frac{1}{2}}$$

$$\nabla^- = \left[\max(D_{ijk}^{+x} \varphi^n, 0)^2 + \min(D_{ijk}^{-x} \varphi^n, 0)^2 + \max(D_{ijk}^{+y} \varphi^n, 0)^2 + \min(D_{ijk}^{-y} \varphi^n, 0)^2 + \max(D_{ijk}^{+z} \varphi^n, 0)^2 + \min(D_{ijk}^{-z} \varphi^n, 0)^2 \right]^{\frac{1}{2}}.$$

For the second order space convex scheme ∇^+ and ∇^- are defined as follows:

$$\nabla^+ = \sqrt{\max(A, 0)^2 + \min(B, 0)^2 + \max(C, 0)^2 + \min(D, 0)^2 + \max(E, 0)^2 + \min(F, 0)^2}$$

$$\nabla^- = \sqrt{\max(B, 0)^2 + \min(A, 0)^2 + \max(D, 0)^2 + \min(C, 0)^2 + \max(F, 0)^2 + \min(E, 0)^2}$$

where

$$A := D_{ijk}^{-x} \varphi^n + \frac{\Delta x}{2} m(D_{ijk}^{-x-x} \varphi^n, D_{ijk}^{+x-x} \varphi^n)$$

$$B := D_{ijk}^{+x} \varphi^n - \frac{\Delta x}{2} m(D_{ijk}^{+x+x} \varphi^n, D_{ijk}^{+x-x} \varphi^n)$$

$$C := D_{ijk}^{-y} \varphi^n + \frac{\Delta y}{2} m(D_{ijk}^{-y-y} \varphi^n, D_{ijk}^{+y-y} \varphi^n)$$

$$D := D_{ijk}^{+y} \varphi^n - \frac{\Delta y}{2} m(D_{ijk}^{+y+y} \varphi^n, D_{ijk}^{+y-y} \varphi^n)$$

$$E := D_{ijk}^{-z} \varphi^n + \frac{\Delta z}{2} m(D_{ijk}^{-z-z} \varphi^n, D_{ijk}^{+z-z} \varphi^n)$$

$$F := D_{ijk}^{+z} \varphi^n - \frac{\Delta z}{2} m(D_{ijk}^{+z+z} \varphi^n, D_{ijk}^{+z-z} \varphi^n).$$

The switch function m is defined as

$$m(a, b) := \begin{cases} \begin{cases} x & \text{if } |x| \leq |y|, \\ y & \text{if } |x| > |y| \end{cases} & \text{if } xy \geq 0, \\ 0 & \text{if } xy < 0. \end{cases}$$

This scheme takes care of shocks by building an appropriate switch. A comparison between these two different schemes can be found in [35].

5.10 Iterative Solver

As mentioned in Section 5.3 the radiosity model assumes that the total flux depends on the flux directly from the source, as well as an additional flux due to the particles which do not stick and are re-emitted. After discretizing the problem the flux vector whose elements are the total flux at different surface elements can be expressed by a matrix equation.

There are two numerical approaches to solve this equation. The first is to use a direct solver for the matrix equation. Although this is practical in two dimensions [11, 13, 14], it becomes impractical due to the computational effort needed to calculate the inverse matrix for three-dimensional problems. In three dimensions the equation is solved iteratively.

The iterative solution developed by Adalsteinsson and Sethian [80] consists of a series expansion of the radiosity matrix. Suitably interpreted, it can be viewed as a multi-bounce model in which the number of terms in the series expansion corresponds to the number of bounces that a particle can undergo before its effect is negligible.

The iterative solution allows one to check the error term to determine how many terms must be kept. Since most of the particles either stick or leave the domain after a reasonable number of bounces, this is an efficient approach.

The reflected intensity after the k -th bounce is defined as $I_{R,k}$. The relationship between reflected intensity and source intensity at the i -th surface element is written (cf. Section 5.3) as follows:

$$I_{R,1}^i = (1 - \beta_0)I_S^i. \tag{5.7}$$

In matrix form, this becomes

$$I_{R,1} = (1 - \beta_0)I_S \tag{5.8}$$

$$I_{R,k+1} = (1 - \beta)\Omega I_{R,k} \tag{5.9}$$

where Ω is a matrix whose elements stand for the influence of the visibility term, diffuse reflection, effective surface area of a surface element, and the distance between the center of mass of two surface elements [80].

Now $I_{S,k}$ is defined to be the portion that sticks after the k th bounce.

$$I_{S,0} = \beta_0 I_S \tag{5.10}$$

$$I_{S,1} = \beta\Omega(1 - \beta_0)I_S. \tag{5.11}$$

In general,

$$I_{S,k+1} = \frac{\beta}{1-\beta} I_{R,k+1} = (1-\beta)\Omega I_{S,k}. \quad (5.12)$$

Therefore, by going back to the initial expression (5.10)

$$I_{S,k} = \beta(1-\beta)^{k-1}(1-\beta_0)\Omega^k I_S \quad (5.13)$$

and thus the total intensity after N reflections is given by

$$I_N = \beta(1-\beta_0) \left[\sum_{k=1}^N (1-\beta)^{k-1} \Omega^k \right] I_S + \beta_0 I_S. \quad (5.14)$$

Each application of the operator may be viewed as either an additional term in the expansion or an additional included bounce. It is important to note that there is a recurrence relation for I_N given by

$$I_{N+1} = \beta(1-\beta_0) \left[\sum_{k=1}^{N+1} (1-\beta)^{k-1} \Omega^k \right] I_S + \beta_0 I_S \quad (5.15)$$

and then

$$I_{N+1} = \beta(1-\beta_0) \left\{ (1-\beta)\Omega \left[\sum_{k=1}^N (1-\beta)^{k-1} \Omega^k \right] + \Omega \right\} I_S + \beta_0 I_S \quad (5.16)$$

$$I_{N+1} = (1-\beta)\Omega(I_N - \beta_0 I_S) + \beta(1-\beta_0)\Omega I_S + \beta_0 I_S \quad (5.17)$$

$$I_{N+1} = (1-\beta)\Omega I_N + (\beta - \beta_0)\Omega I_S + \beta_0 I_S. \quad (5.18)$$

By constructing the remainder term $I_{N+1} - I_N$, the convergence of the expansion can be measured and sufficient terms can be kept to bound the error below a user-specified tolerance.

5.11 Input File of Three-Dimensional ELSA

Three-dimensional ELSA requires a library called IPD (input deck library) developed by the Institute for Microelectronics [51]. It is used for parsing input files and must be installed first. An example of an IPD input file including parameters of the simulator, process parameters, and the initial geometry is as follows:

```
Simulation
{
  Name = "Sample";
  Comment = "a sample deposition with void";
  OutputDirectory = "./output/";
  WriteAfterEachIteration = "yes";
  PrintConfig = "short";
}
```

```
// Parameters of the level-set algorithm
LevelsetAlgorithm
{
  nx=30;
  ny=30;
  nz=30;
}

Sources
{
  SourceGroup1
  {
    z = 2.0;
    x1 = 0.0;
    y1 = 0.0;
    x2 = 1.0;
    y2 = 1.0;
    xSourceCount = 4;
    ySourceCount = 4;
    Intensity = 20;
    n = 1;
    Direction = [0,0,-1];
  }
}

Steps
{
  Deposition1
  {
    Name = "Deposition1";
    Material = "Si3N4";
    Time = 8.0;
    MaxThickness = 0.23;
    SourceStickingProbability = 0.1;
    ReflectionStickingProbability = 0.1;
  }
}

// We define the initial geometry here as a list of triangles:
InitialBoundary
{
  lowerLeft= [0.0, 0.0, 0.0];
  upperRight=[1.0, 1.0, 1.0];
  Points
  {
    wafer\_level = 0.75;
    p11=[~InitialBoundary.lowerLeft[0],
```

```
    ~InitialBoundary.lowerLeft[1],
    wafer\_level];
p12=[~InitialBoundary.lowerLeft[0],
    ~InitialBoundary.upperRight[1],
    wafer\_level];
p13=[~InitialBoundary.upperRight[0],
    ~InitialBoundary.upperRight[1],
    wafer\_level];
p14=[~InitialBoundary.upperRight[0],
    ~InitialBoundary.lowerLeft[1],
    wafer\_level];
p21=[0.45, 0.45, wafer\_level];
p22=[0.45, 0.55, wafer\_level];
p23=[0.55, 0.55, wafer\_level];
p24=[0.55, 0.45, wafer\_level];
p31=[0.4, 0.4, 0.2];
p32=[0.4, 0.6, 0.2];
p33=[0.6, 0.6, 0.2];
p34=[0.6, 0.4, 0.2];
}
Boundary
{
    q1=["p11","p12","p22","p21"]; //q1 ... q4 top planes
    q2=["p12","p13","p23","p22"];
    q3=["p13","p14","p24","p23"];
    q4=["p14","p11","p21","p24"];
    q5=["p21","p22","p32","p31"]; //q5 ... q8 side planes
    q6=["p22","p23","p33","p32"];
    q7=["p23","p24","p34","p33"];
    q8=["p24","p21","p31","p34"];
    q9=["p31","p32","p33","p34"]; //q9 bottom plane
}
}
```

In the next section we present another program library suitable for data exchange between different process simulators even when they are based on different native file formats.

5.12 Fully Three-Dimensional Process Simulation

ELSA is a stand alone application for three-dimensional topography simulation and uses IPD for input file as mentioned in previous section. Furthermore, TOPO3D has been also developed. The kernel of TOPO3D is based on ELSA, but is also linked to a program library, that handles objects for fully three-dimensional semiconductor process simulations. This program library is called WSS (wafer state server) [14].

The idea of WSS stems from necessity that the simulation informations generated by a simulator must be usable not only by the same simulator but also by other tools and

simulators. These tools can be visualization programs, for instance. Mostly the concrete syntax based on the informations are saved, is not important for users. However, a low memory consumption and a fast access during writing and reading an input or output file are very essential. Different simulators save the simulation informations in different file formats which are not compatible to each other. Therefore, in general a certain file format can only be read by the related tool. This incompatibility can be overcome with introducing the common data format presented by WSS [45].

WSS is a program library and file format for handling three-dimensional objects in semiconductor process simulations developed at our institute [14]. It is a solution for the integrated simulation of three-dimensional manufacturing processes. A generic data model suitable for process and device simulations allows an efficient data exchange between simulators even when they are based on different native file formats. It is also able to handle different meshes and distributed quantities stored thereon. The program library also defines algorithms to perform geometrical operations for fully three-dimensional process simulations as they are used in topography simulations.

Figure 5.7 shows an overview of the simulation flow achieved when using TOPO3D. The simulation begins at the WSS. WSS provides us with the initial surface which is then propagated. The initial surface is represented by a set of triangles. In the next step the level set function is initialized with the signed distance function. After this step the time stepping is started. At each time step a data exchange between the simulation model

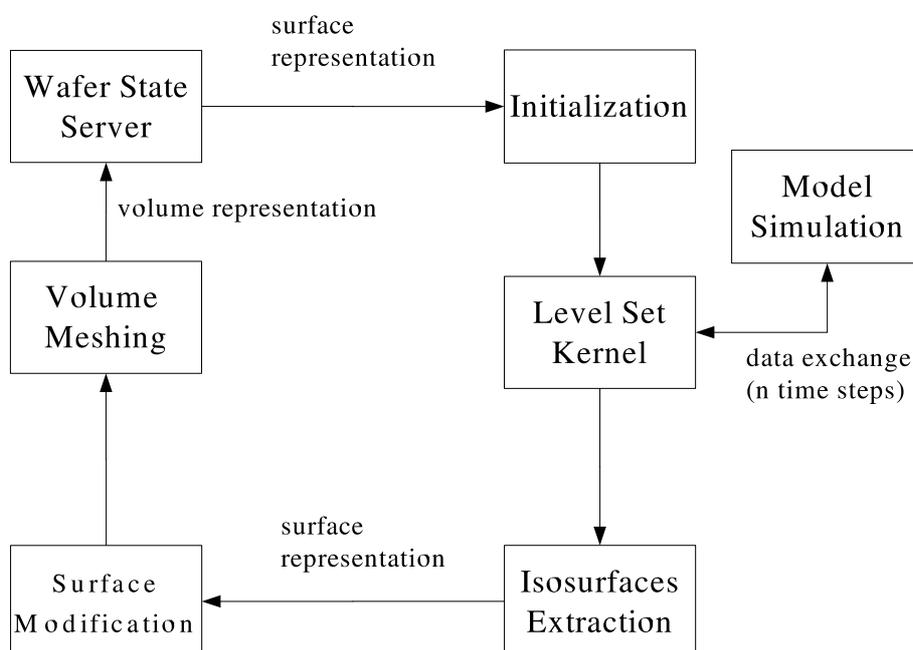


Figure 5.7: Overview of the simulation flow in TOPO3D.

and the level set kernel takes place. The simulation model provides the speed function needed by the level set kernel to propagate the surface. Vice versa the model also needs information about the actual distance function from the surface propagation step. After n time steps the final surface is extracted as the zero level set of the level set function. After coarsening the final surface and merging it with the initial surface, a meshing step is performed and the information is stored in WSS.

5.13 Stability of the Simulator

To advance the level set function we have used a second order space convex finite difference scheme [13, 19, 20, 24]. Consider Δx , Δy , Δz , and Δt as discretization steps in space and time, respectively. As mentioned in Section 5.6, a necessary condition for the stability of this scheme is the CFL condition which requires that

$$\Delta t \cdot F_{\max} \leq \min(\Delta x, \Delta y, \Delta z)$$

where F_{\max} is the maximum value of F at the grid points. The CFL condition guarantees that the front can not cross more than one grid cell during each time step. In order to have a stable simulator based on the finite difference method, the CFL condition must be satisfied [69].

However, there is a problem stemming from the CFL condition, which limits the simulator performance. If we increase the spatial resolution by λ , assuming that F_{\max} remains constant, we have to reduce the maximum Δt by the same factor λ , which increases the number of simulation steps by λ to reach the same thickness. Furthermore, an increase in spatial resolution by λ approximately increases the number of extracted surface elements by λ^2 in three dimensions. Therefore, the computational effort of the visibility determination is increased by λ^4 . In total, an increase in spatial resolution by λ leads to a minimal increase of simulation time by a factor λ^5 , if the most precise visibility calculation is used.

5.14 Summary

State of the art algorithms for surface evolution processes like deposition and etching processes in two and three dimensions have been implemented. A general purpose topography simulator has been developed based on the level set method combining the narrow banding and fast marching methods to extend the speed function. The speed of the simulation has been improved in several steps, e.g., in initialization, visibility determination, and solving the radiosity matrix. To be able to handle the objects for fully three-dimensional semiconductor processes, TOPO3D which has ELSA as its kernel has been developed and is linked to the WSS program library.

6 Application of ELSA to Interconnect Processes

Key issues of the deposition processes are the geometry, modeling of the source, collision in transit from the source to the feature, and the collision and sticking rate of the material being deposited.

In this chapter we present simulation results for the backend of a 100nm process, where the influence of void formation between metal lines profoundly impacts the performance of the whole interconnect stack consisting of aluminum metal lines and titanium nitride local interconnects. Feature-scale topography simulations serve here as input to subsequent capacitance extraction. The entirety of simulations and extracted capacitances characterize a specific technology and are made accessible to the circuit designer via a database.

6.1 Motivation

One of the challenges that TCAD must currently meet is the analysis of the performance of groups of components, interconnects, and – generally speaking – large parts of the IC. This enables predictions that the simulation of single components cannot achieve. In this chapter we focus on the simulation of backend processes, interconnect capacitances, and time delays. The simulation flows start from the blank wafer surface and the final result is device information for the circuit designer using circuit simulators such as SPICE (simulation program with integrated circuit emphasis)¹.

Interconnects are becoming increasingly important as the shrinking of the semiconductor technologies continues, since the timing delays due to metal lines contribute increasingly to the overall delay. Therefore, it is imperative for predictive TCAD applications that capacitance and resistance of interconnect lines are modeled as accurately as possible.

Most RCX (resistance and capacitance extraction) tools assume rectangular metal profiles, either planar or conformal dielectrics, and they use simplistic void models. Even if the metal slope is modeled, it is mostly assumed constant and independent of space. While these idealizing assumptions may be sufficient for past technologies, they are insufficient for today's technologies like the 100nm process considered in Section 6.4, where interconnects show a number of special features which are nowhere close to ideal.

For proper modeling of the capacitance, one has to know the metal profile, e.g., bottom and top CDs (critical dimension) and metal slope, the profile of the deposited layer with

¹SPICE is a program that simulates electronic circuits and calculates voltages and currents versus time (transient analysis) or versus frequency (AC analysis). Most SPICE programs also perform other analysis like DC, sensitivity, noise and distortion. SPICE is available from many vendors who have added schematic drawing tools to the front end and graphics post processors to plot the results. SPICE simulators and applications have expanded to analog and digital circuits, microwave devices, and electromechanical systems.

and without CMP, and the profile of the void, if it forms. Generally these three profiles depend heavily on the conditions of the deposition process, on metal thickness and line-to-line spacing, and to a lesser degree on the metal width [8,10].

In order to join topography and backend simulations, deposition, etching, and CMP processes in the various metal lines are used to build up the backend stack starting from the flat wafer surface. Depending on the metal combination, line-to-line spacing, and line width, thousands of simulations are required whose results are stored in a database.

6.2 Feature-Scale Simulation

Having described the handling of moving boundaries in Chapter 5, this section focuses on the chemical surface reactions. Starting from a plain substrate, the principal topography simulation steps are etching trenches, depositing thin films, and CMP (cf. Figure 6.1). Finally we outline how the single topography simulations are integrated to yield larger backend structures.

6.2.1 The Deposition Processes Used by Investigations

In the considered backend process the deposited films are silicon nitride and silicon dioxide films (cf. Section 6.4). Here the transport of particles happens in the radiosity regime and the deposition processes are governed by luminescent reflection.

The silicon nitride films were deposited by PECVD (plasma enhanced CVD) from silane and NH_3 and were not doped. The chemical reaction is $\text{SiH}_4 + \text{NH}_3 \rightarrow \text{SiNH} + 3\text{H}_2$ [74]. For simulation purposes this was considered as the essential reaction, a detailed model

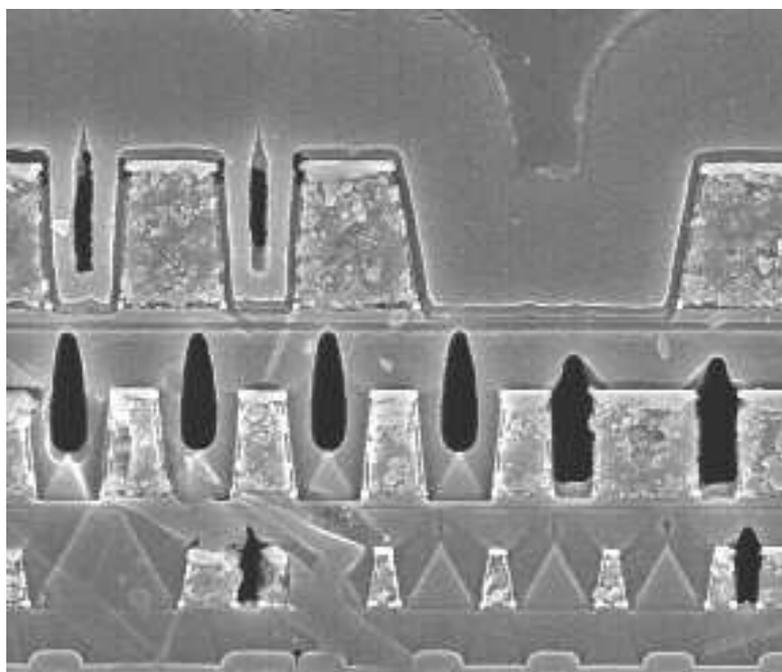


Figure 6.1: SEM image of a whole backend stack comprised of three Al metal lines M_1 , M_2 , and M_3 , bottom-up, respectively, and a Ti-nitride local interconnect.

including triaminosilane condensation can be found in [94]. The silicon dioxide film is deposited from a TEOS process which has been treated in Chapter 4.

In order to calculate the thickness Δd of the film deposited during a time interval of length Δt , we observe that Δd is proportional to Δt , to an Arrhenius term, and to the deposition rate R corresponding to the chosen deposition model. This implies $\Delta d = \Delta t \cdot k_e e^{-E/kT} \cdot R$. Here $k_e e^{-E/kT}$ is the Arrhenius term with activation energy E , absolute temperature T , a pre-exponential constant k_e , and R is the deposition rate [67].

When modeling topography processes it is generally possible to write down complicated reaction paths and list dozens of possible surface reactions. However, it is not straightforward to determine the vital reactions and their constants. Thus it is important to reduce the possible reaction paths to an essential minimum (cf. Chapter 4).

Figure 6.2 shows the simulation result for the process mentioned above which has been used for the calculation of capacitance.

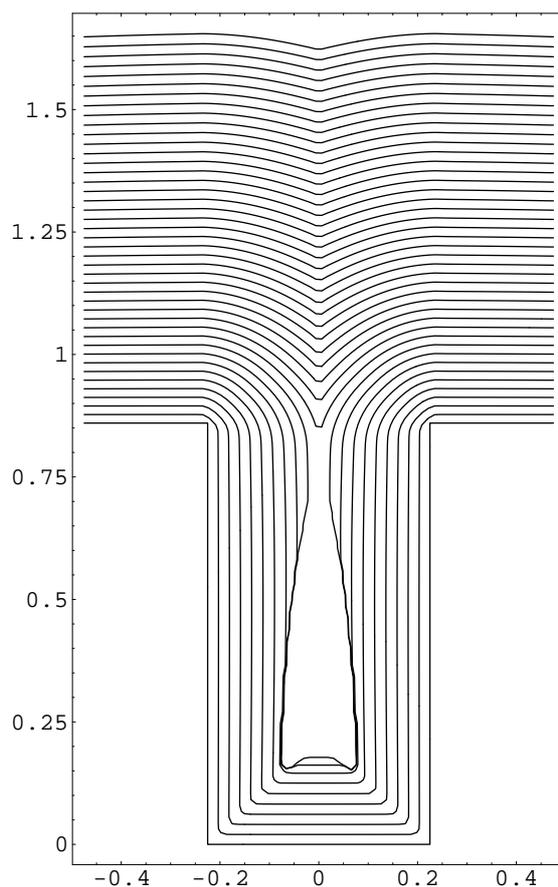


Figure 6.2: Simulation of the deposition process used for a line-to-line spacing of $0.45\mu\text{m}$.

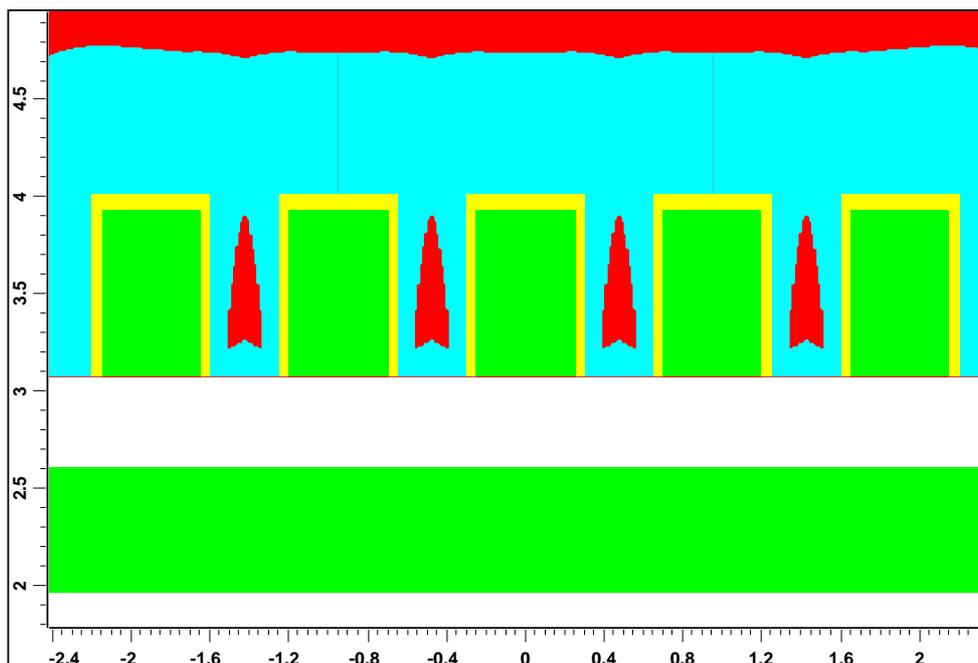


Figure 6.3: M_3 lines ($0.5\mu\text{m}$ top width) at $0.45\mu\text{m}$ line-to-line spacing above the M_2 plane. Cap oxide was deposited (thin layer surrounding M_3 lines) before the top nitride (thick layer) was deposited. Void formation occurs between the lines.

6.2.2 CMP

On the feature-scale level the simulation of CMP can be performed in a straightforward manner, since the thickness of the remaining part of the layer is known. In this simulation step the boundary is modified so that all parts above the given thickness are removed and the remaining points are joined accordingly.

6.2.3 Integration

Simulations of single features, performed by the above steps, can be duplicated using affine transformations $\mathbf{x} \mapsto A\mathbf{x} + \mathbf{b}$ to obtain more complex structures. For example, to arrive at the structures shown in Figures 6.3, 6.4, and 6.5, it is necessary to simulate the processes for a single feature including etching and subsequent deposition. The resulting boundaries are duplicated by affine transformations. At the left and right boundaries, other simulations have to be performed, as they are formed by half trenches. The results for the left hand boundary are mirrored to yield the right hand boundary.

6.3 Backend Simulation

The coordinates of the structures simulated by topography simulator serve as input to calculate the electric field. For the following simulations RAPHAEL [7] was used. RAPHAEL is a solver for electrical field and calculates the charge densities and various capacitances. Depending on the required resolution, the simulator yields a large number

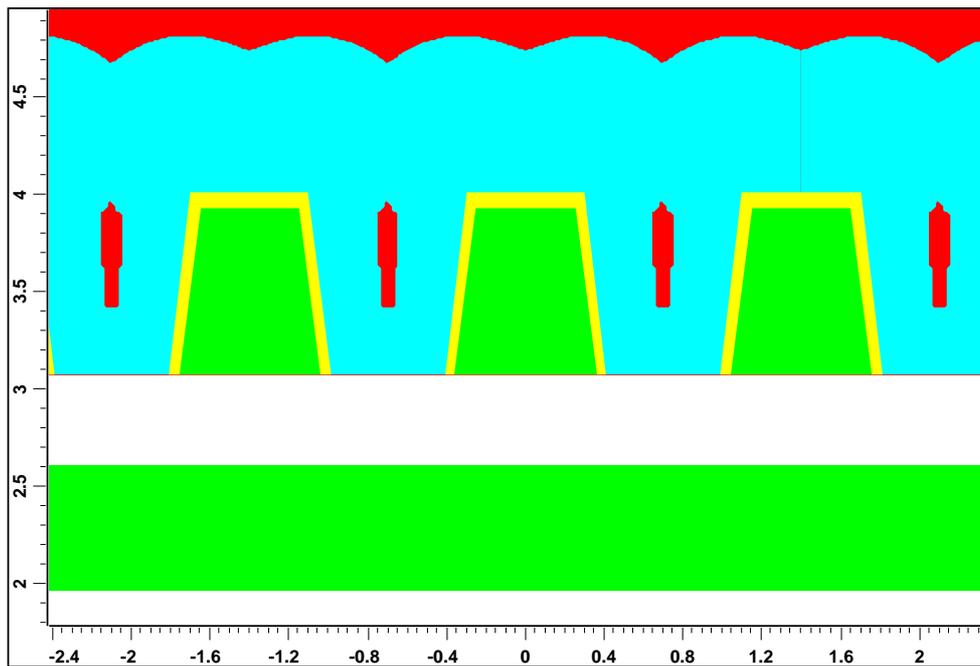


Figure 6.4: M₃ lines (0.5 μm top width) at 0.90 μm line-to-line spacing above the M₂ plane. The voids are smaller than in Figure 6.3.

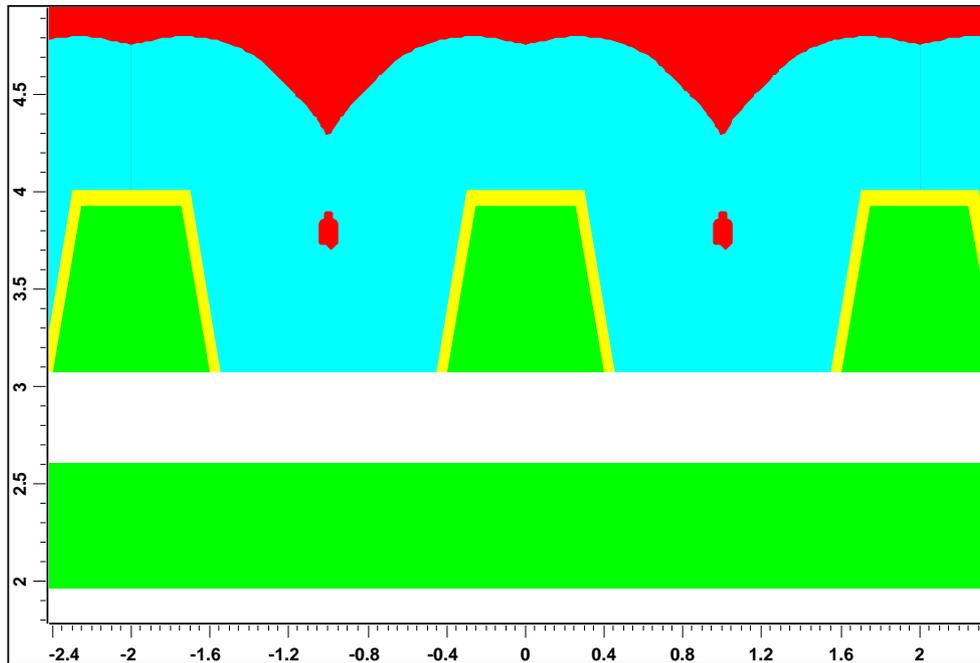


Figure 6.5: M₃ lines (0.5 μm top width) at 1.50 μm line-to-line spacing above the M₂ plane. In this case the voids formed are quite small.

of points describing ILD (interlevel dielectrics) and voids. Since this number of surface

elements determines the number of RAPHAEL grid points and simulation time is an important factor, a significant reduction of the number of points is necessary. Otherwise simulation times would be orders of magnitude larger than those of equivalent simplified structures. Hence we use a surface-coarsening algorithm to rework the output and to reduce the number of points supplied to the RAPHAEL [36].

6.3.1 Capacitance Types

A typical multi-level interconnect structure consists of one layer containing a few parallel conductors at different voltages, embedded and electrically isolated from each other by dielectric materials, closed at the top and at the bottom by two other metal layers consisting of other parallel conductors or by ground planes. Such structures are used to extract the total and mutual capacitance per unit length of each conductor. The calculated capacitance is then used for the worst-case evaluation of the integrity parameters of the interconnect structure such as cross-talk and propagation delay. This parameters are dependent on materials and on the geometry of the structure, e.g., number of conductors and their spacing and width.

For example one can assume that a signal line is at high voltage and surrounded by two lines on the left, two lines on the right, a plane underneath, and, if necessary, a plane above. The surrounding lines and planes are assumed to be grounded. For example an M_2 signal line could be surrounded by M_2 grounded lines above the M_1 plane and underneath the M_3 plane. This skeleton is shown in Figure 6.6.

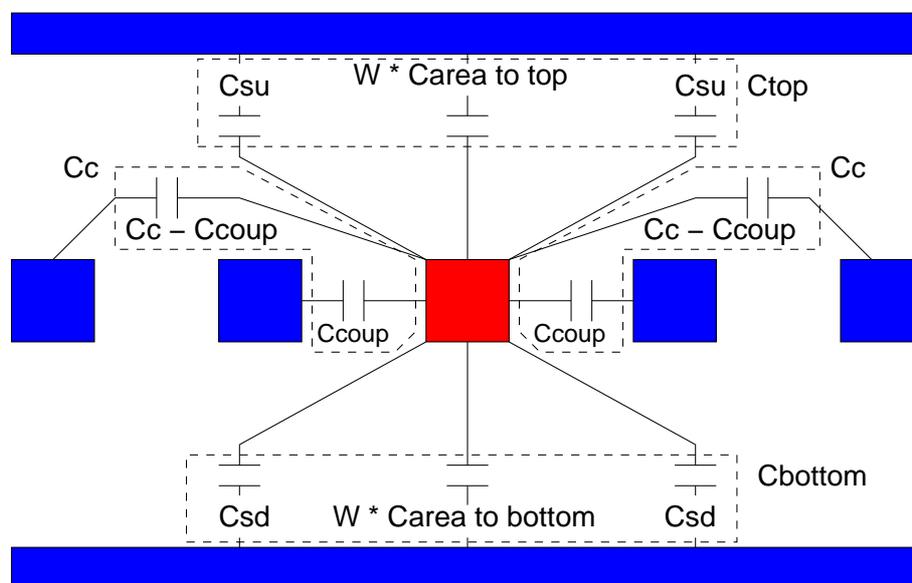


Figure 6.6: This figure shows the two-dimensional schematics of a signal line (middle) surrounded by grounded lines and planes. The total capacitance equals the sum of twice the coupling capacitance plus top and bottom capacitances.

6.3.2 Capacitance Models

Capacitance simulations are performed depending on three variables: First, they depend on the combination of metals. The number of these combinations can be high for a six-layer technology [17, 21].

The second variable is line-to-line spacing. Simulations start from the minimum allowed line-to-line spacing (e.g., $0.14\mu\text{m}$) and end in the range of a few microns (e.g., $6\mu\text{m}$). Generally, initial line-to-line spacing increments are fine to capture the strong dependence of the capacitance on line-to-line spacing, while the final increments are coarse to capture capacitance saturation.

Third, capacitance simulations depend on the line width. Simulations start from the minimum allowed width to approximately 60 times the minimum width. Since the dependence on width is well behaved, only a few intermediate widths are usually needed.

6.3.3 Interfacing to Circuit Design

First the designer instantiates a capacitance element, e.g., for an M_3 line above the substrate. The designer must then specify the metal type and the surrounding planes as well as metal width, length, and line-to-line spacing. Then the designer creates a SPICE input file. Finally the database and the designer's options are read, the capacitor of interest is located, line-to-line spacing and width are interpolated or extrapolated, and the capacitance instance with a numeric value for the capacitance at that node is replaced. Now the designer can run the SPICE program and observe circuit performance. If timing requirements are not met, the designer changes the properties of the capacitance, e.g., makes it narrower for lower capacitance, and repeats the process.

6.4 Simulation Results

In order to verify ELSA, different interconnect and metal lines structures provided by our industry partner have been considered to be simulated. As an example, we consider the case of M_3 lines above the M_2 plane. These backend stacks are part of a 100nm Aluminum/TEOS process (cf. the SEM image shown in Figure 6.1). The films deposited are silicon nitride and silicon dioxide films and the interconnect lines are made of aluminum. The experiments performed during the development of a RAM process were performed in a LAM 9600 reactor [12].

The M_3 lines have a width of $0.50\mu\text{m}$, and a line-to-line spacing varying between $0.45\mu\text{m}$ and $1.9\mu\text{m}$. Figure 6.3 shows the RAPHAEL structure constructed from ELSA coordinates at minimum line-to-line spacing. Note that at a minimum line-to-line spacing the metal lines are vertical and voids have their maximum size. For a line-to-line spacing of $0.9\mu\text{m}$, as shown in Figure 6.4, the side walls are sloped and the voids are considerably smaller.

Next we build the structure with a line-to-line spacing of $1.5\mu\text{m}$. Figure 6.5 shows the corresponding RAPHAEL structure, again constructed from simulation results. Note that in this case, however, the metal lines have a larger slope, which duplicates the real process geometry. Voids are quite small in this case. At $1.9\mu\text{m}$ line-to-line spacing the metal slope has saturated and no voids are formed.

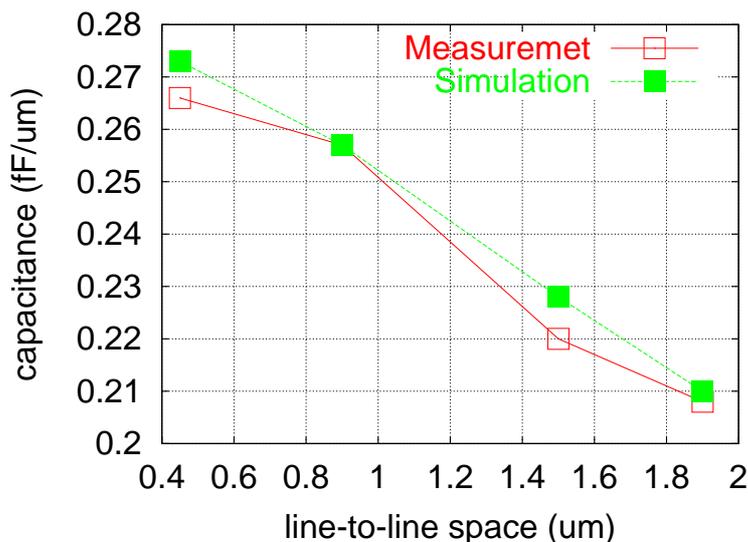


Figure 6.7: This figure compares the M_3 middle line capacitance as a function of line-to-line spacing between simulations and measurement.

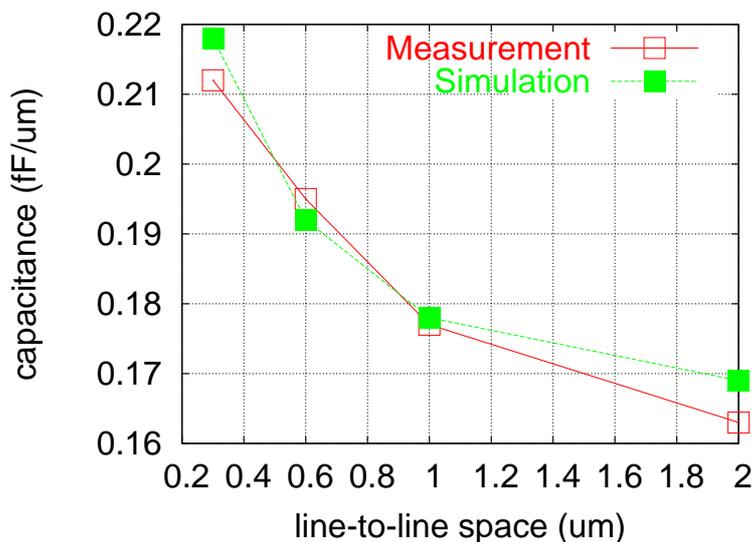


Figure 6.8: This figure compares the M_2 middle line capacitance as a function of line-to-line spacing between simulations and measurement.

The capacitance of the middle line was simulated for the above structures and compared to CBCMS (charge based capacitance measurement)². The simulation results and measurements are compared in Figure 6.7. Simulation results show very good agreement with data obtained from measurements with a maximum error below 4%.

As a second example, we compare the capacitances extracted after silicon dioxide deposition in the M_2 plane to CBCMS. Simulations were performed for line-to-line spacings of $0.3\mu\text{m}$, $0.6\mu\text{m}$, $1.0\mu\text{m}$, and $2.0\mu\text{m}$. The simulated and measured capacitances are shown in Figure 6.8 and again the error is below 4%.

²CBCM is an often used technique which provides a simple way for measuring the overall parasitic capacitance of on-chip interconnects [95].

The two-dimensional models for lines surrounded by other lines, as shown by these examples, are important since there is an abundance of cases where they appear on a chip. One of the most important cases is the last layer of the metal lines which are used as paths from one side of the chip to the other. Such an example is a TCO (total cost of ownership) path whose length is 22 000 μm in a 72Mbit DRAM chip which is 1 cm in length. The TCO path is divided into eight portions, each portion has a different width and different spacing to adjacent lines. It is very important that this path is modeled accurately and optimized, as it is used to fabricate products working at high operation frequency. To predict and optimize the performance of this line, very accurate models are needed motivating these simulations.

6.5 Void Extraction Step

Depending on the resolution of the grid which is used by ELSA during the deposition processes, ELSA may yield a large number of points to describe a void. This number of void points determines the number of grid points used by RAPHAEL and subsequently the simulation time. Although, we have used a coarsening algorithm to reduce the number of points that represent the boundary or voids, we could have obtained a much lower number of points if we had extracted the void at a different simulation step, namely, just after the formation of the void. The standard method also used in [80] is to extract the void at the end of the simulation. From the point of view of the speed function the void has to be frozen in its place once it has formed. Therefore, it must not matter when we extract the void, i.e., at the end of the simulation or immediately after the void

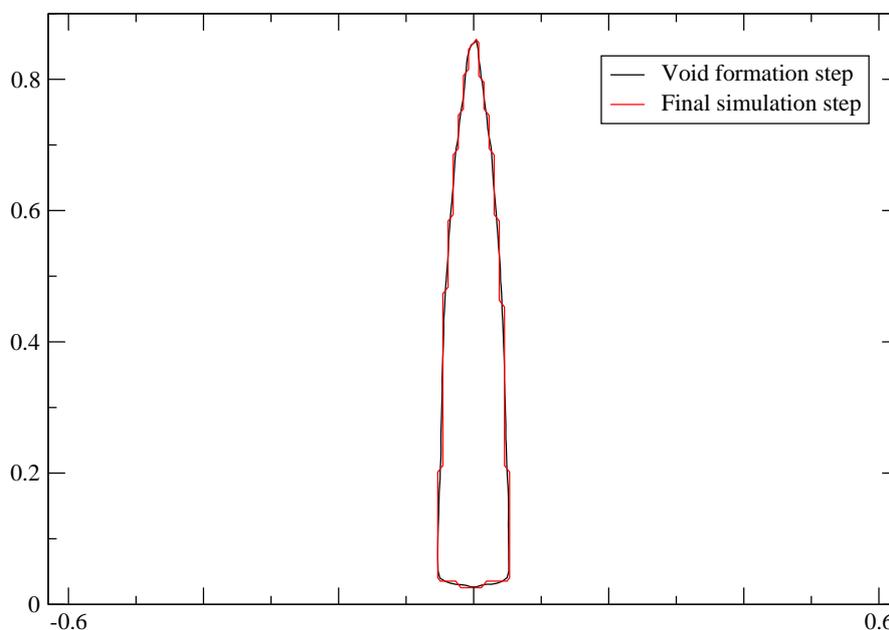


Figure 6.9: Void extraction at the end of simulation and right after the formation of the void by aspect ratio=1 for axes.

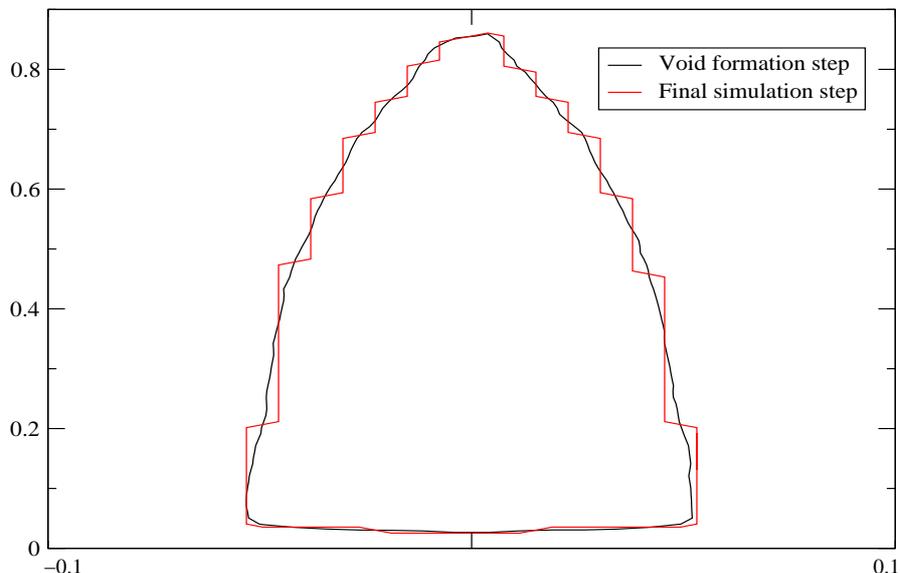


Figure 6.10: Void extraction at the final and the void formation step of the simulation by aspect ratio $\neq 1$ for axes.

formation, but the different points in time when the void is extracted have produced different void profiles. Figure 6.9 shows the extracted voids at these different points in time where the aspect ratios between the axes is one. It is very difficult to discern any difference of the two voids. To more clearly see the difference, we have changed the aspect ratio between the axes to a different ratio which is not equal to one. This is shown in Figure 6.10.

This difference originates from the extension of the speed function. Practically once a void forms, there is no more visibility between the void and source of deposition and the void and the deposited boundary, as well. Therefore, it is expected that the void is no longer displaced. However, depending on the width of the narrow band and the duration of a time step some points of the void do not leave the narrow band for a few simulation cycles and their adjacent grid points are assigned a non zero speed value during the extension of the speed function. This continues until the void is no longer inside the narrow band and leads to the change of shape of the void compared to its shape just after its formation.

As can be seen clearly in Figure 6.10, the form of the void extracted at the final step of the simulation is unrealistic since it contains steps which are not seen in the measurements. In addition, by extracting the void immediately after its formation, redundant points along vertical segments are eliminated and the subsequent coarsening is no longer required. However, the difference between the shapes does not influence the accuracy of the capacitance calculations and demands only additional simulation time due to the coarsening algorithms.

The immediate advantage of knowledge obtained from this study was a high reduction of the time of simulations achieved by our industry partner for further capacitance calcu-

lations in two dimensions because they are investigating a great number of simulations. Furthermore, this knowledge has been used by implementation of three-dimensional ELSA where the number of void points are drastically more than in two dimensions and each reduction of point number plays a very important role to make the simulator more efficient.

6.6 Optimizing the Voids for the Metal Profiles with Constant Line-to-Line Spacings

The effects of changing line-to-line spacing with varying slopes has been studied in the previous sections. In this section we focus on the other geometrical effects considering different metal profiles to further optimize the voids in order to reduce the capacitance of conductors. Figure 6.11 shows the simulation result of different metal profiles. The first profile is an rectangular trench which is considered as a reference. The line-to-line spacing is constant for all profiles. The metal profiles after the reference profile from left to right are considered for the effect of outward slope, hard mask, inward slope, cap layer, and undercut.

Here one can see the advantage of the line source model presented in Section 4.1.1. As mentioned there, the model enables to simulate a set of trenches simultaneously compared to models used in our first attempts in [19, 35].

Figure 6.12 shows the different voids which have formed during the deposition of material into the metal profiles as shown in Figure 6.11. The interesting effect can be seen during the void formation into a profile with a hard mask. The hard mask considerably reduces the size of the void and continuously shifts the bottom of the void to a higher position.

According to the simulations presented in the previous sections one still expects to see the largest void during the deposition of material into a vertical structure. Although this is not a very wrong expectation, but these new simulations show that the largest and smallest voids are formed at profiles with inward- and outward slopes, respectively.

The strange form of the void obtained from the profile with undercutting originates from the fact that there is no visibility from the source to the line segments located at the undercut regions.

The other effects which are important to our industrial partner are the influence of slopes with varying top CD from 50nm to 15nm. Figure 6.13 shows the simulation of the deposition of material into this varying top CD. The simulations have shown interesting effects. Whereas the position of the top of the voids does not change, the bottom of the voids is shifted upwards as the top CD is decreased. This can be seen more clearly in Figure 6.14.

6.7 Summary

Topography and RCX simulation were joined to predict the timing delays in the backend stacks of a 100nm CMOS process for memory cells. A rigorous simulation approach such as the one presented is indispensable for today's technologies since timing delays become increasingly important due to shrinking. The complex interconnect structures are built from the structures at the feature scale yielding many configurations depending on the

different metal combinations, line-to-line spacing, and line width. The interconnect structures serve as input to the electric field calculator, in this case RAPHAEL, whose results from the capacitance simulations are stored in a database. The circuit designer accesses the results of this simulation flow and uses them in SPICE circuit simulations. The significant influence of void formation on the capacitances was quantified, as using voids in a controlled and reproducible manner can be an economically advantageous substitute for low- k materials. The simulations show very good agreement with CBCMS and hence they play a significant role during the development of backend processes and circuit design.

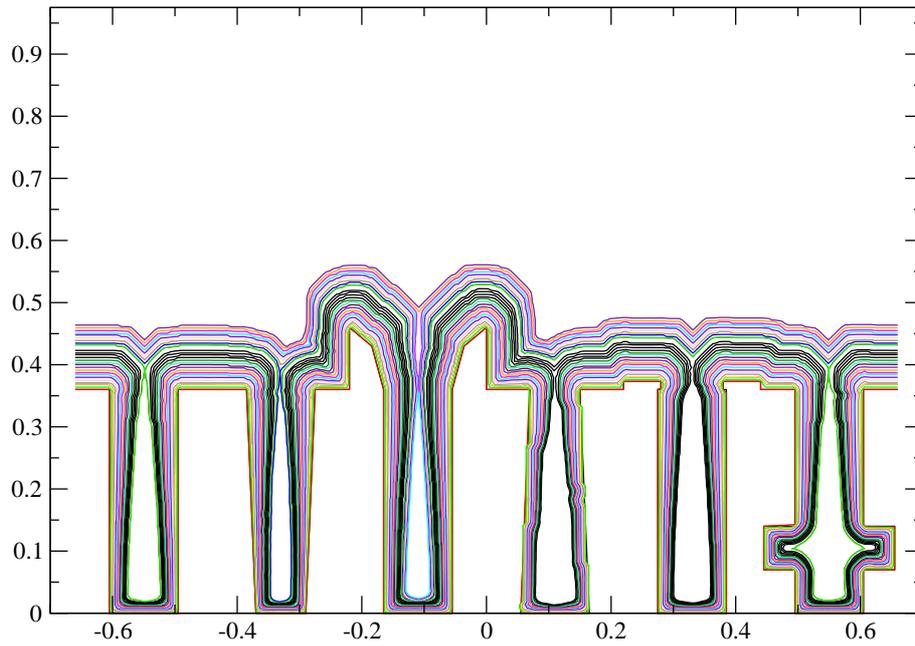


Figure 6.11: Deposition simulation for studying the effects of different shapes of trenches.

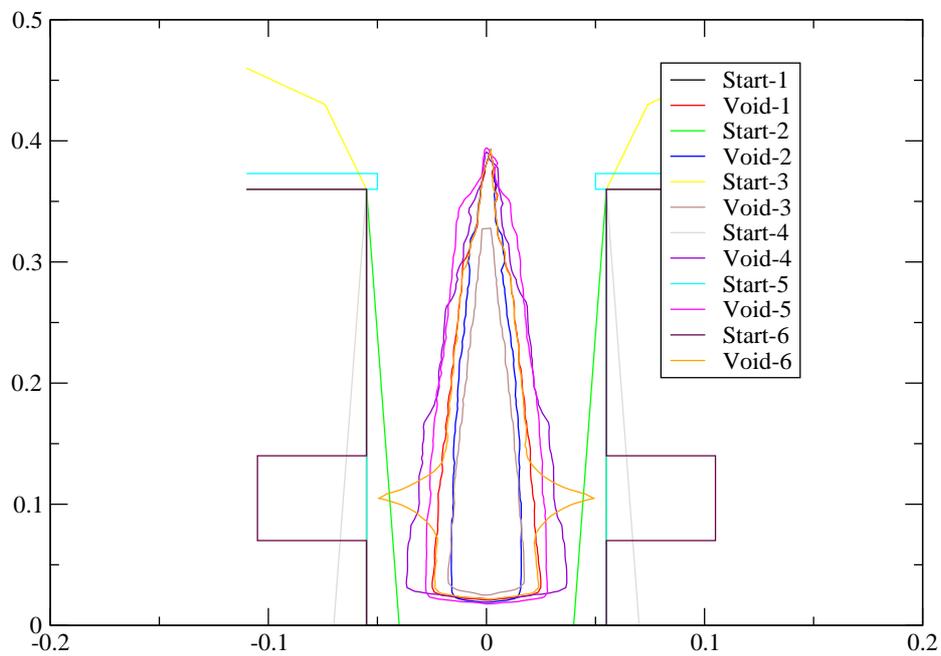


Figure 6.12: Void characteristics during the deposition simulation shown in Figure 6.11.

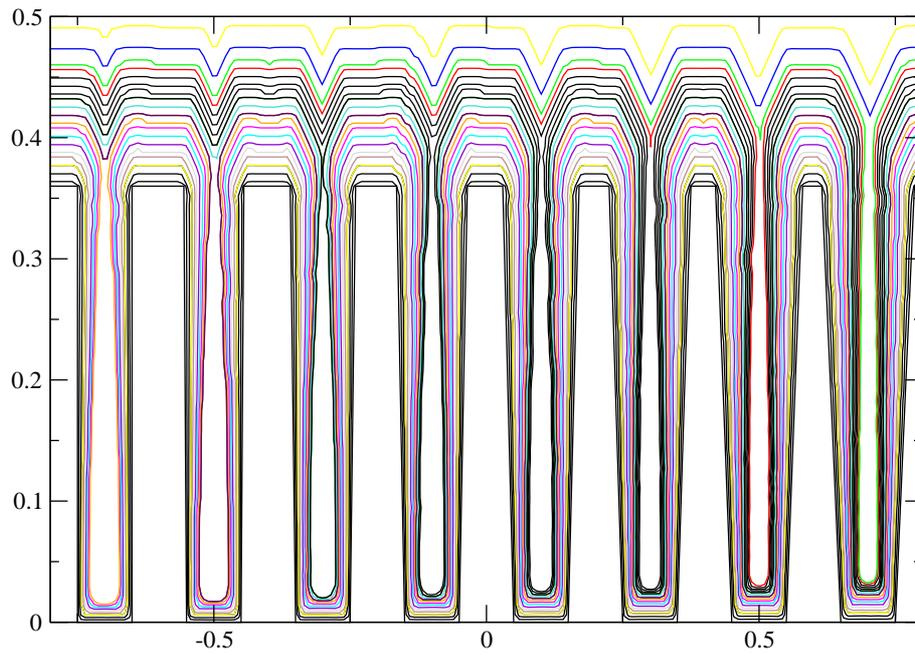


Figure 6.13: Deposition simulation for eight different slopes and top *CD*.

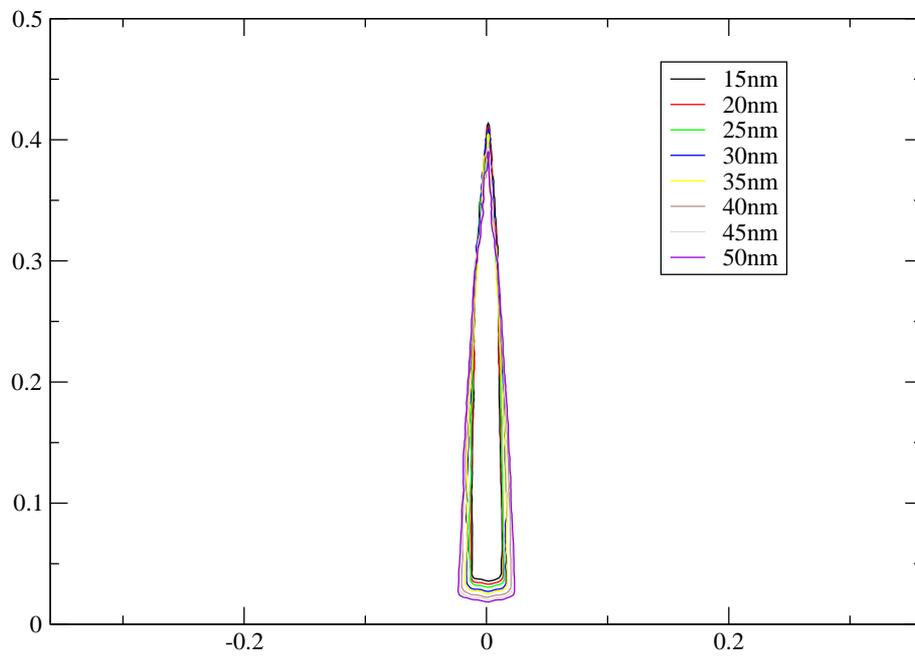


Figure 6.14: Void characteristics during the deposition simulation shown in Figure 6.13.

7 Application of ELSA to the Simulation of Plasma Etching

As the device feature size continues to be scaled down, increasingly severe requirements are being imposed on plasma etching technology, including the anisotropy of etching, profile control, feature size or CD control relative to the mask width, and etch selectivity to the mask materials and underlying layers [100]. In general, gate etching is a considerable challenge in the fabrication of MOS transistors. In practice, an extremely high etch selectivity of poly-silicon with respect to an ultrathin gate oxide is required for gate etch processes with extremely precise CD control. Furthermore, these requirements must be satisfied for a variety of etched features with greatly differing dimensions or aspect ratios on the wafer.

Microscopic uniformity or aspect ratio dependent etching is one of the most important issues of plasma etching technology [32]. In plasma etching, etch rates and profiles are often observed to depend on pattern feature size or aspect ratios [47], e.g., slower etch rates for features of larger aspect-ratios (reactive ion etching lag) [25], stronger side-wall tapering for features of smaller aspect-ratios [34], more thinning and breaking of gate oxides for features of smaller aspect ratios [13] and vice versa. Such phenomena are generally attributed to a decrease or an increase of incident flux of neutrals onto the bottom surface of an etched feature as the aspect ratio of the feature is increased. It is important to reveal the mechanisms responsible for such microscopic non-uniformities in order to achieve microscopically uniform and aspect ratio independent etching, which in turn results in microscopically uniform channel lengths of the fabricated MOS transistors.

Etching of a poly-silicon gate is frequently performed to achieve anisotropy and selectivity, which are critical as the minimum feature size shrinks. A thorough understanding of the chemical mechanism in ion enhanced plasma etching is required for better process modeling to predict the etching directionality and feature profiles.

Ion-enhanced etching of poly-silicon has been well characterized by many researchers over the last 20-25 years [22, 23]. The etching rate can be decomposed into three components [20]: physical sputtering by ions, spontaneous etching by atoms, and ion-enhanced etching which is the combined effect of ion flux, surface coverage, and ion energy.

The decrease of the dimensions of features in IC manufacturing demands more anisotropy, directionality, and compact etching profiles [93, 100]. Plasma etching is able to produce highly anisotropic etching profiles. Therefore, it is and will be a very important processing step in IC manufacturing. A better understanding of this important process is crucial for further improvements in this field and for the development of better processing models. In this chapter we will present simulation results for highly anisotropic etching [23].

7.1 Calculation of Ion Flux

Assuming a collisionless, time independent plasma sheath¹ and an isotropic Maxwellian velocity distribution of ions at the sheath edge, the incident angular distribution of ion fluxes onto the substrate can be expressed as a Gaussian distribution [6,31,99] as shown in Figure 7.1. This function is known as IADF (ion angular distribution function). After calculating the direct ion flux to the surface one has to calculate the indirect flux due to ion reflections. It has been assumed in the literature [1] that the ions are reflected at specular angles with a distribution about the angle of reflection as shown in Figure 7.2. An open question is why perfect specular reflection is not used? Many experiments [1] have been performed by researchers on the reflection of different ions from different target surfaces. In common to all reported results is the distribution of the reflected ions about the angle of the specular reflection.

The distribution about the angle of the specular reflection is modeled as $\cos^n(\theta)$ where θ is the deviation from the angle of the specular reflection. Obviously higher n means tighter distribution and more in the direction of perfect specular reflection. The quantity n is called specularity and depends on different parameters such as surface material,

¹When an object of finite size is placed in a plasma with approximately equal electron and ion temperatures, it acquires a net negative charge because the electron thermal speed is much greater than the ion thermal speed. This causes more electrons to hit the object than ions. As the object charges negatively, the electrons start to be repelled, just as when a negative test charge is introduced into the plasma. Equilibrium occurs when the electron current collected by the object balances the incident ion current. An electrically polarized region is thereby formed around the object. This polarized region is called a plasma sheath, or sometimes a positive ion sheath, because the electrons are largely excluded from the sheath.

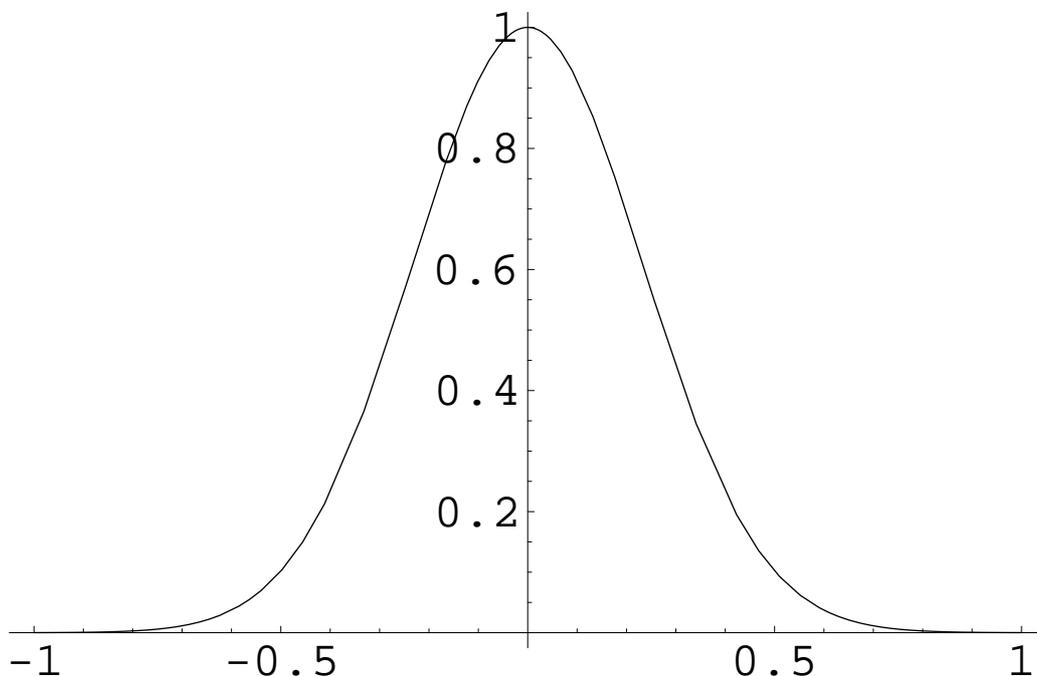


Figure 7.1: A typical IADF for ions.

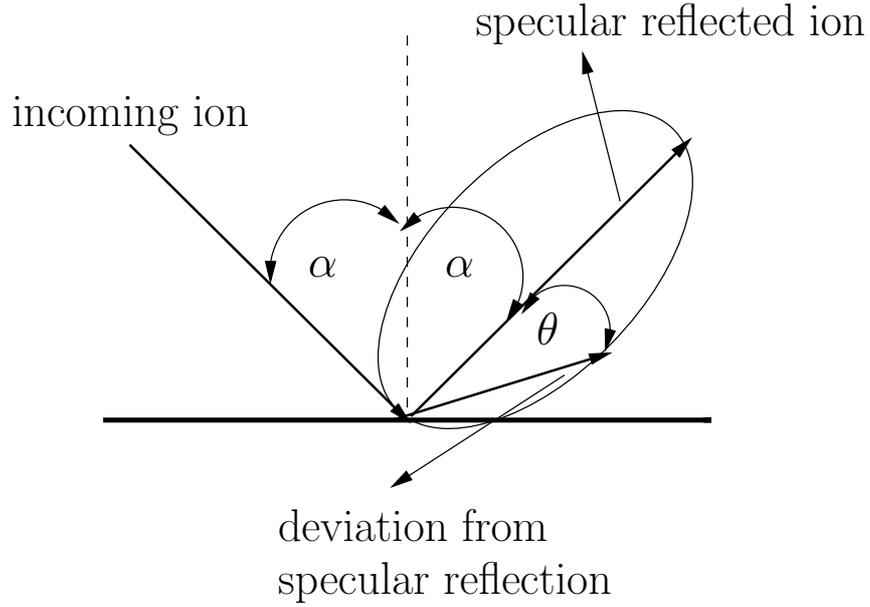


Figure 7.2: Illustration of a not perfectly specular reflection.

ion mass, ion energy, and ion angle of incidence. For example, specularity tends to decrease with increasing ion mass relative to the surface material. As can be seen later in simulation results the specularity plays an important role in the prediction of the correct shape and depth of microtrenching.

7.2 Etching Kinetics

In the etching process considered, two kinds of neutrals have been assumed: the first kind are the etchants with F_c as their flux and the second kind are the inhibitors with F_d as their flux.

Two different sources can be considered for inhibitors. One source is the plasma gas phase. During the etching process volatile etch products will go to the gas phase. If their residence time is long enough, they will produce molecules which can return and stick on the surface of the feature.

The other source for inhibitors is molecules locally produced at the feature during etching. The way these products desorb from the surface depends on the actual etching mechanism.

The best known model for etching kinetics is the Langmuir adsorption model [1,47,99] which gives the following equations

$$\sigma \frac{d\theta_c}{dt} = F_c S_c^0 (1 - \theta_c - \theta_d) - \gamma_c F_i \theta_c = 0 \quad (7.1)$$

$$\sigma \frac{d\theta_d}{dt} = F_d S_d^0 (1 - \theta_c - \theta_d) - \gamma_d F_i \theta_d = 0 \quad (7.2)$$

where σ is the site density, θ_c and θ_d are the surface coverages for etchants and inhibitors, respectively. F_i is the ion flux, S_c^0 and S_d^0 are the clean surface sticking probabilities for

etchants and inhibitors, and finally γ_c and γ_d are the ion sputtering yields for adsorbed etchants and inhibitors.

Equalizing the surface coverages to zero is based on the fact that the surface coverage, at room temperature, reaches its steady state much faster than the etching rate, i.e., the rate of change in the feature and so in the fluxes. In the equations above, only ion enhanced chemical etching is considered. Spontaneous etching is not considered, because it has been assumed that the etchant does not etch spontaneously at room temperature. In addition, the physical sputtering yield is much lower than the ion enhanced chemical etching yield which is also ignored.

Eliminating θ_d in equations (7.1) and (7.2) gives θ_c as

$$\theta_c = \frac{S_c^0 \gamma_d F_c}{S_c^0 \gamma_d F_c + S_d^0 \gamma_c F_d + \gamma_c \gamma_d F_i}. \quad (7.3)$$

The etching rate R_E is given as follows [1]:

$$R_E = \frac{Y F_i \theta_c}{\sigma} \quad (7.4)$$

where Y is the etching yield which defines the atoms removed per incident ion. The etching yields γ_c , γ_d , and Y are assumed to be proportional to $\sqrt{E_i} - \sqrt{E_t}$ [1] where E_i and E_t are the ion energy and the threshold energy, respectively. Substituting (7.3) in (7.4) gives

$$R_E = \frac{Y F_i S_c^0 \gamma_d F_c}{\sigma (S_c^0 \gamma_d F_c + S_d^0 \gamma_c F_d + \gamma_c \gamma_d F_i)}. \quad (7.5)$$

To calculate the neutral fluxes inside the feature, surface coverage dependent sticking probabilities have to be used. This means that the flux reaching each segment of the feature depends on the surface coverage. However, the surface coverage itself depends on the flux received by a segment according to (7.1) and (7.2). So the fluxes and surface coverages are solved iteratively to obtain a self-consistent solution.

7.3 Neutral-Ion Synergy Model

In order to analyze (7.5) we summarize all parameters except for F_c and F_i as follows:

$$R_E = \frac{F_c F_i}{a F_c + b F_i + c} \quad (7.6)$$

where a , b , and c summarize the influence of the parameters S_c^0 , S_d^0 , γ_c , γ_d , and F_d . If the ratio between F_c and F_i is much larger than one, i.e., $F_c/F_i \gg 1$, the influence of F_c can be neglected because (7.6) can be rewritten as follows:

$$R_E = \frac{F_i}{a + b \frac{F_i}{F_c} + \frac{c}{F_c}}. \quad (7.7)$$

According to the above equation the process is in an ion-enhanced etching regime, because it is saturated from neutral fluxes.

In the other case the equation can be written as follows:

$$R_E = \frac{F_c}{a \frac{F_c}{F_i} + b + \frac{c}{F_i}} \quad (7.8)$$

where the influence of the ion flux can be neglected. The etching process is in a neutral-enhanced regime.

7.4 Etching Profile with Minimal Spurious Corner Rounding

Each nanometer deviation from the target gate length directly translates into the operational speed of the devices. Gate control in transistors is a critical determinant of the device's ultimate operational speed. In IC fabrication, one of the main process sequences determining the transistor's gate length is the gate etch. Therefore, a topography simulator for etching processes must be able to predict the gate length. One of the critical effects emerging in the simulation of etching processes is the corner rounding effect in an etched profile. This problem and its origin have been described in great detail in Section 3.1.6.

There we have also explained how these effects can be avoided by changing the conventional calculation of the speed function. The conventional method for the translation of the speed function is to take the average of two different speed values of surface elements and translating it to an adjacent grid point. The simulation result of a directional etching using this method is shown in Figure 7.3 where the corner rounding is increasing more and more as the etch depth increases.

Using the new method described in Section 3.2 we have obtained an etching profile for the same etching process, of course, with minimal spurious rounding of the corners as shown in Figure 7.4.

7.5 Simulation Results

Figures 7.4, 7.5, and 7.6 show etched profiles for different neutral-to-ion flux ratios (F_c/F_i), namely, 0.01, 1, and 100, respectively. Note that all the etching processes stopped at the same time. The figures show that increasing the neutral-to-ion flux ratio increases the etching rate. As F_c/F_i is increased from 0.01 to 100, the surface coverage first increases and then tends to level off. At high F_c/F_i , the etched surface is almost saturated with neutral reactants, where the etch rate is limited by the incident ion flux as we have shown in (7.7). On the other hand, at lower F_c/F_i , the surface atoms are scarcely covered with etchants and thus the etch rate is limited by the incident neutral flux as shown in (7.8).

Based on calculations in Section 7.3, at a high neutral-to-ion flux ratio, all the side-walls and bottom surfaces of the trench are almost saturated with neutrals. In this situation the etch rate is primarily determined by the incident ion flux, and thus the etched profiles are governed by the directionality of ion fluxes. On the other hand, at a low flux ratio, the surface coverage of the etchant is low at the bottom of the surface. However, on the side-walls, the saturation condition for etchants is still satisfied, because the incoming ion flux is much lower on the side-walls than at the bottom. Thus

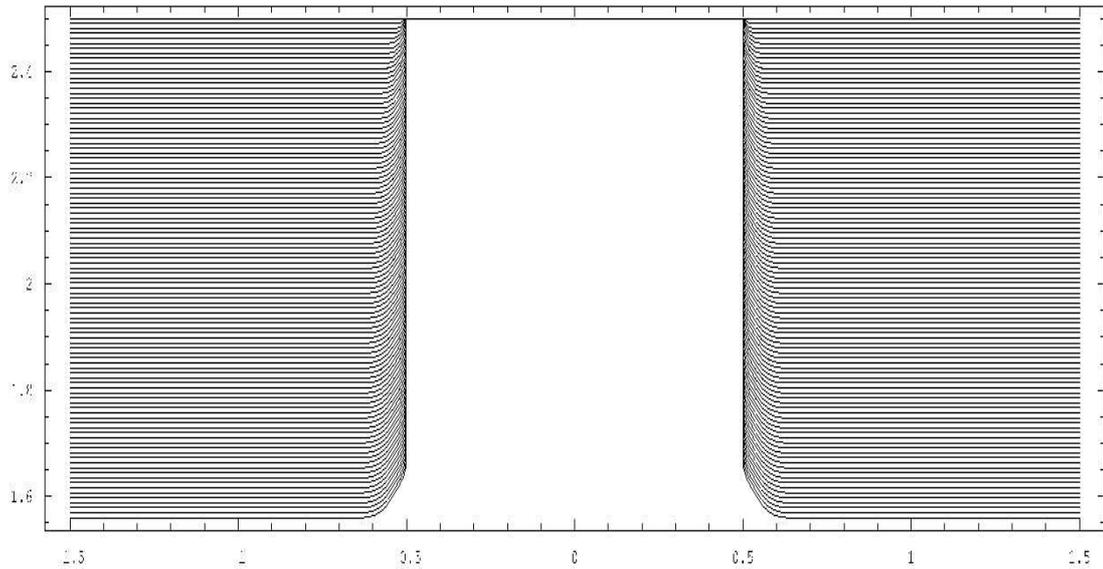


Figure 7.3: The simulation result of a directional etching using a conventional method to translate the speed function from surface elements to grid points. The propagation of the spurious rounding effect with increasing simulation time can be seen easily.

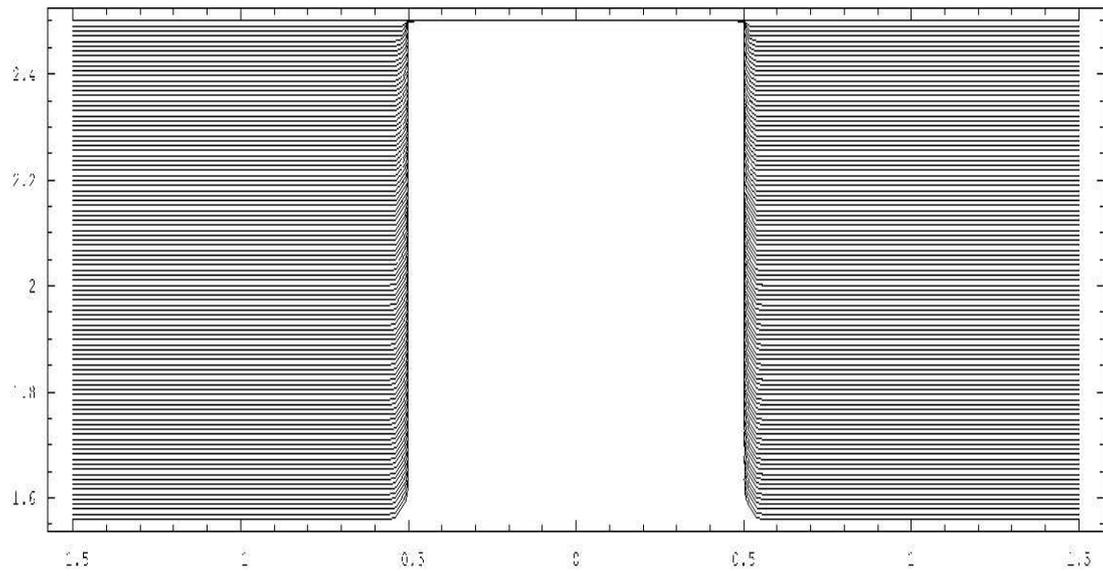


Figure 7.4: The simulation result of a directional etching with the method described in Section 3.2 to translate the speed function from surface elements to grid points. Spurious corner rounding is kept to a minimum.

the surface coverage becomes microscopically nonuniform at the etched features. From these results, it follows that side-wall passivation effects and/or more directional ions are required for the anisotropic etching at low flux ratios.

In addition microtrenching effects can be seen where the etching rate at the corner because of ion reflection is larger than in other places at the bottom.

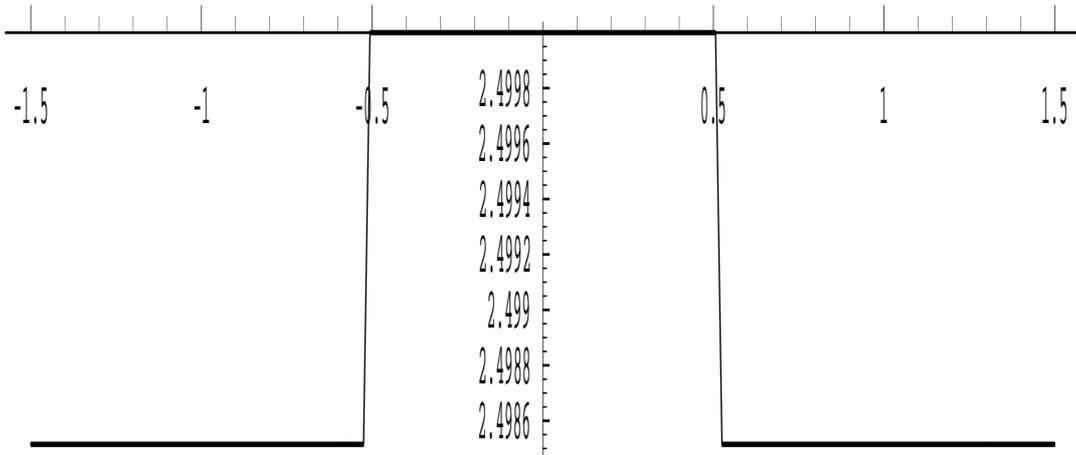


Figure 7.5: The etched profile for a neutral-to-ion flux ratio of 0.01.

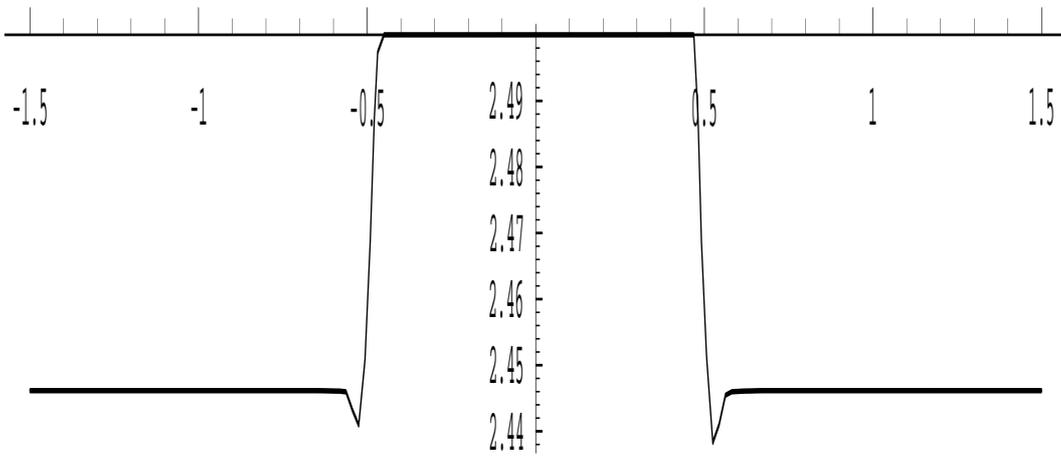


Figure 7.6: The etched profile for a neutral-to-ion flux ratio of 1.

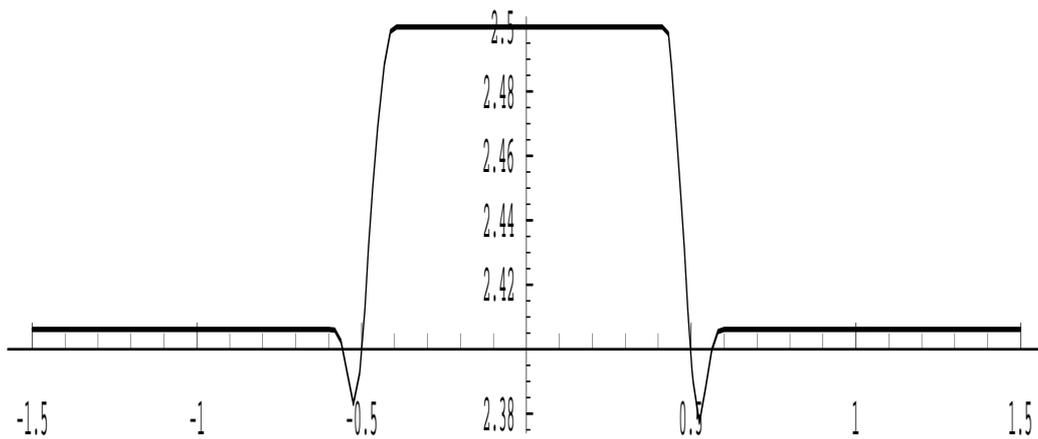


Figure 7.7: The etched profile for a neutral-to-ion flux ratio of 100.

7.6 Summary

An etching model based on the Langmuir adsorption model has been implemented. Using mathematical techniques etching profiles with minimal corner rounding have been obtained. The effect of neutral-to-ion flux ratio on the etching profiles has been simulated and discussed.

8 Applications of Three-Dimensional ELSA to Crack Prediction

Cracks may be created at any stage of a manufacturing process, but the deposition process step is generally the most problematic. The cracks are observed during the deposition of the passivation layers that cover IC chips in the areas where the top metalization layout geometry yields a three-dimensional profile for the deposition of the passivation layers.

To avoid such cracking and subsequent device failure, it is essential to characterize the deposition profile of the passivation layers as a function of the layout geometry. This characterization can then be used to establish a set of layout design rules to mitigate the formation of crack. An efficient and fast approach is the use of deposition simulation tools. Therefore, having a general purpose topography simulator capable of handling different physical etching and deposition models is essential. We present investigations during deposition of silicon nitride and silicon dioxide to gain insight into possible layout design rules that may be taken into account to avoid crack formation.

8.1 Description of the Considered Deposition Processes Used by Investigations

As mentioned in Section 6.2.1, the transport of particles is in the radiosity regime [80] for the considered processes. The deposition processes are governed by luminescent reflection. The deposited films are silicon nitride and silicon dioxide films.

Since measurements can only be made from cross sectional SEM images in two dimensions, for three-dimensional deposition simulations we have used the same parameters which were extracted with the optimization and calibration tool SIESTA [35] for two-dimensional simulations. The first set of parameters comes from the simulation results of the deposition of silicon nitride into interconnect lines as shown in [12] and the second set comes from the simulation results of the deposition of silicon dioxide from a TEOS process performed in [9]. These parameters led to very good agreement of simulation results with measurements in two dimensions.

8.2 Three-Dimensional Void Characteristics for the Prediction of Cracks

Figure 8.1 shows a schematic of three-dimensional structure used in our investigations. The geometrical parameters for which we obtain the void characteristics are line-to-line spacings (S), metal thickness (T), metal width (W), displacement parameter (L), and a diagonal parameter (P). The last two parameters result in pronounced three-dimensional effects.

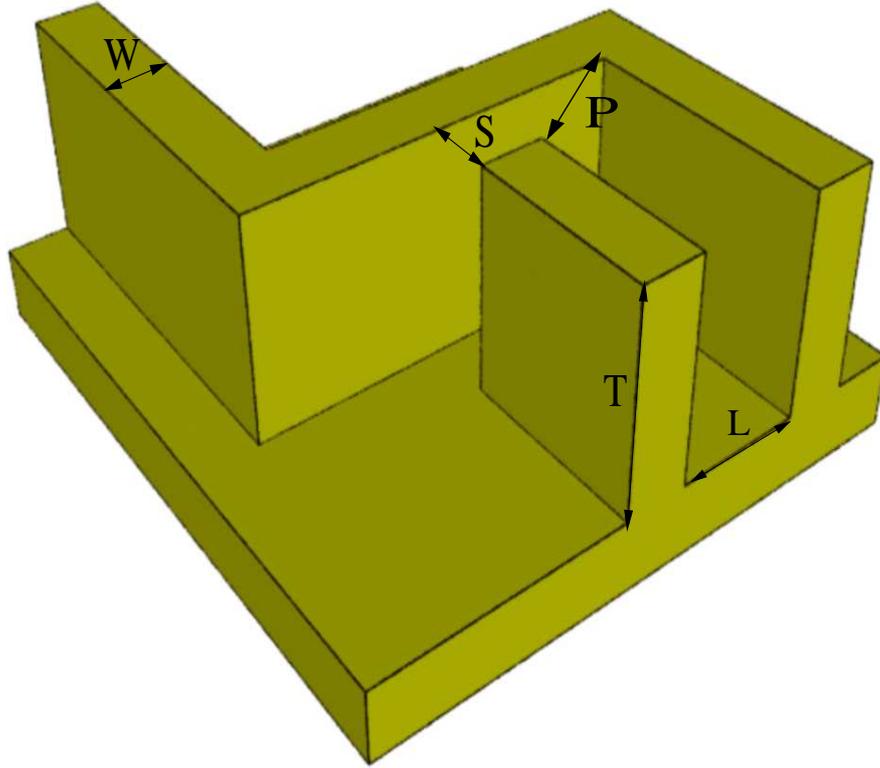


Figure 8.1: Schematic of the investigated three-dimensional interconnect structure.

Since our simulations [10] have shown that the metal width does not play an important role for void characteristics, it will be held constant during all investigations. The first set of simulations was performed for different line to line spacings holding the metal thicknesses at $T_1 = 0.845\mu\text{m}$ and $T_2 = 1.045\mu\text{m}$. As mentioned in Section 8.1 the deposited layers were silicon dioxide and silicon nitride with thicknesses of $D_1 = 0.1\mu\text{m}$ and $D_2 = 0.9\mu\text{m}$, respectively.

One of the initial structures considered for the first set of investigations can be seen in Figure 8.2. The simulation of the deposition processes into this structure has led to a result as shown in Figure 8.3. To analyze the cracking effects we introduce a parameter C which is calculated as follows:

$$C(S, T, D, L, P) = T + D - Z_{void}(S, T, D, L, P)$$

where Z_{void} (the Z coordinate of top of the void) and C are shown in Figure 8.3.

The simulations have generally shown that increasing S shifts the void upwards while it simultaneously decreases C as can be seen by a comparing Figure 8.3 and Figure 8.4. In addition, increasing S causes the void to be wider. To see the formation of the void more clearly, a cross section of the simulation result shown in Figure 8.4 is given in Figure 8.5.

In order to find the influence of the metal thickness on C , we have performed another set of simulations. The dependence of C on different metal thicknesses is illustrated in

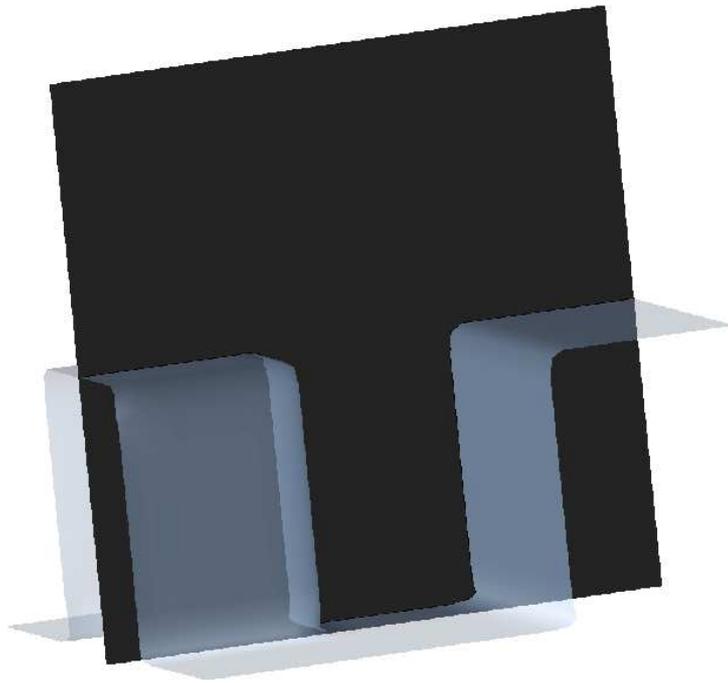


Figure 8.2: Initial structure for T_2 , and $S = 0.72\mu\text{m}$.

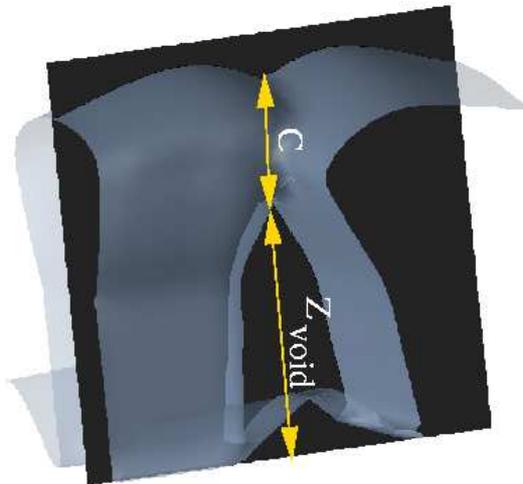


Figure 8.3: Void formation during deposition into the structure as shown in Figure 8.2.

Figure 8.6. Whereas the metal thickness does not considerably affect C for small S , its effect is stronger once S crossed a threshold value, and the thicker the metal the larger is C .

So far we have presented three-dimensional simulations with results which could also have been estimated with two-dimensional simulations at the expense of a lower accuracy.

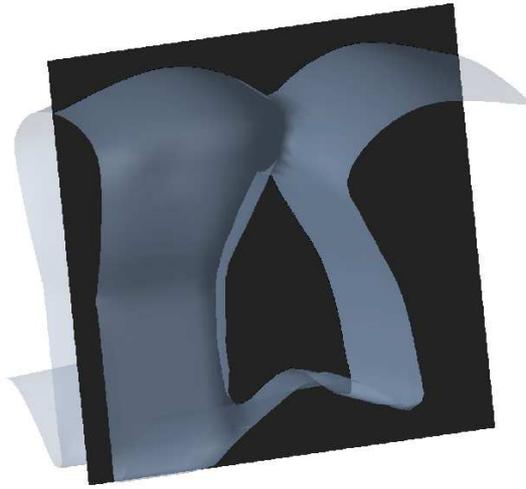


Figure 8.4: Simulation result for $S = 1\mu\text{m}$ and T_2 .

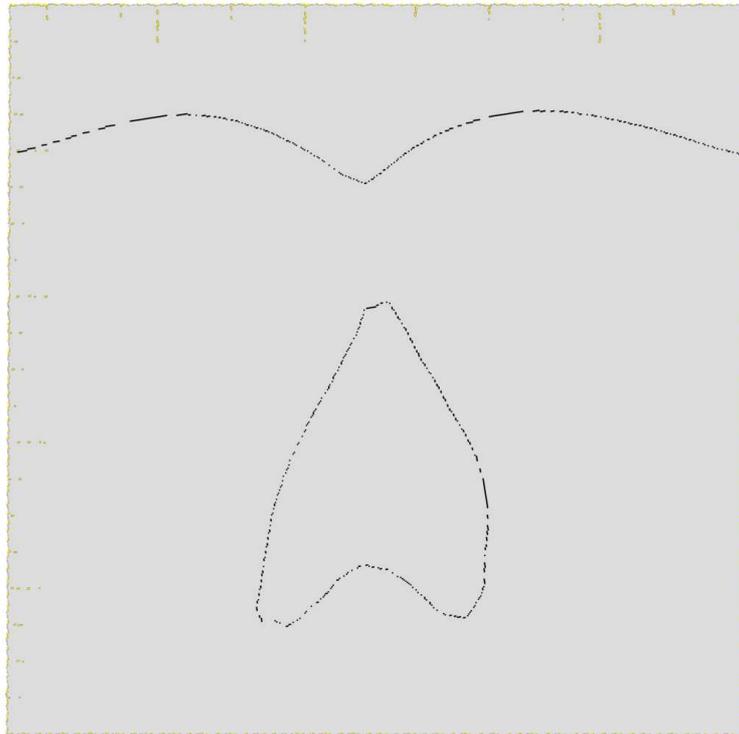


Figure 8.5: A cross section of the simulation results shown in Figure 8.4.

We now present investigations which can only be performed using three-dimensional simulations [8]. In a first attempt L is varied while keeping the remaining parameters constant. Although increasing L shifts the voids upwards, the dimensions of the voids do not increase as when increasing S .

Introducing a parameter P and its variation results in pronounced three-dimensional effects. Because $P = \sqrt{S^2 + L^2}$ is not a single-valued function of S and L as shown in Figure 8.1, considering the dependence of C on P is difficult. Therefore, it is very important to have a profile of C depending on S and L that leads to the same value of P with different combinations of S and L .

Figures 8.7, 8.8, and 8.9 show three of many investigations for different S and L . As in Figure 8.5 we show cross sections of simulation results shown in Figures 8.7, 8.8, and 8.9, in Figures 8.10, 8.11, and 8.12, respectively. These figures show that simultaneous increase of S and L results in three different effects. First, the voids are shifted upwards. Second, they will be wider. Finally, their height is decreased. These investigations have led to a profile of C as shown in Figure 8.13. The important characteristic of Figure 8.13 is that there are different regions which guarantee a stable process, i.e., a large C . Using such profiles, C can be predicted and therefore process engineers will be able to choose the optimal geometrical parameters to avoid cracks. The cracks are avoided by choosing C as large as possible because the smaller C the more probable is the formation of cracks.

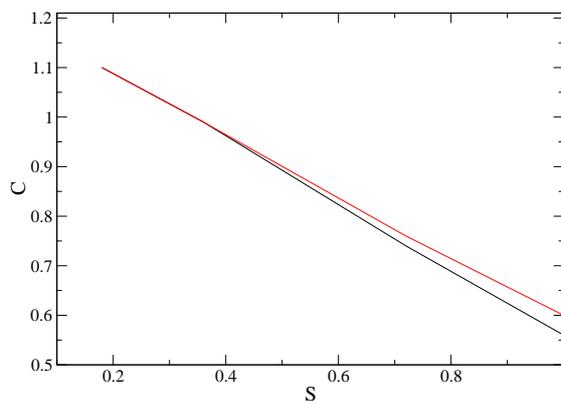


Figure 8.6: Dependence of C on T_1 and T_2 . The lower and upper curve stand for T_1 and T_2 , respectively.

8.3 Summary

The void characteristics during the deposition of silicon dioxide and silicon nitride layers into interconnect lines are predicted. We have obtained a profile of C which determines the probability of cracking effects. Process engineers can set layout design rules depending on geometrical parameters while they choose such parameters leading to larger C because the smaller C the more probable are cracking effects.

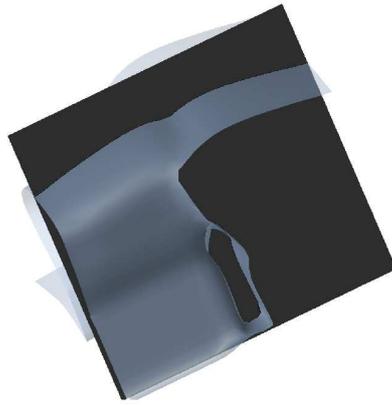


Figure 8.7: Void formation for T_1 and $S = L = 0.3\mu\text{m}$.

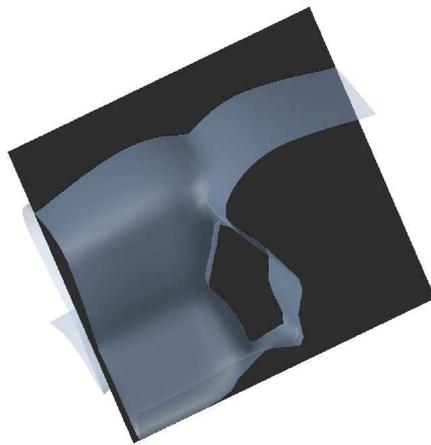


Figure 8.8: Void formation for T_1 and $S = L = 0.6\mu\text{m}$.

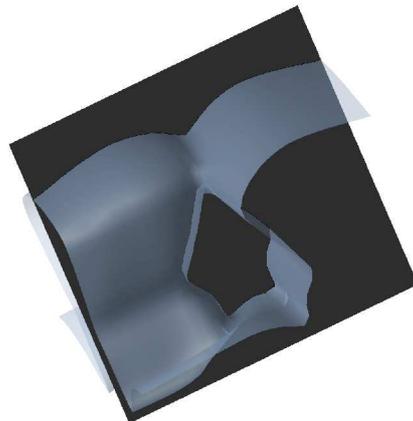


Figure 8.9: Void formation for T_1 and $S = L = 0.9\mu\text{m}$.

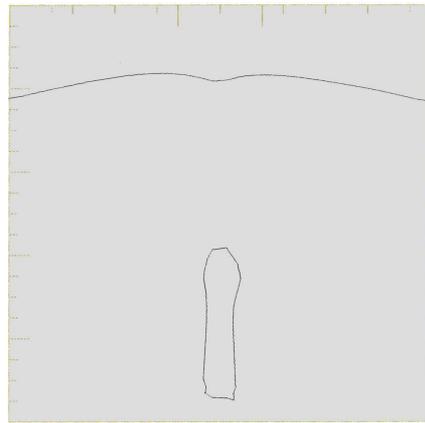


Figure 8.10: A cross section of simulation result shown in Figure 8.7.

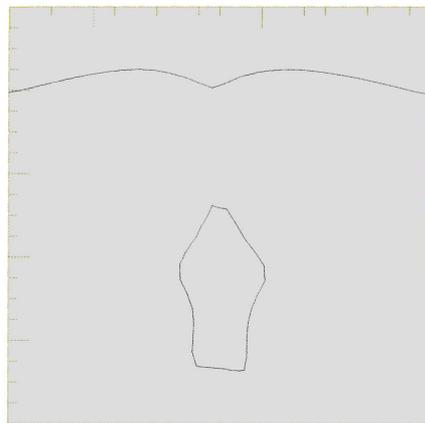


Figure 8.11: A cross section of simulation result shown in Figure 8.8.

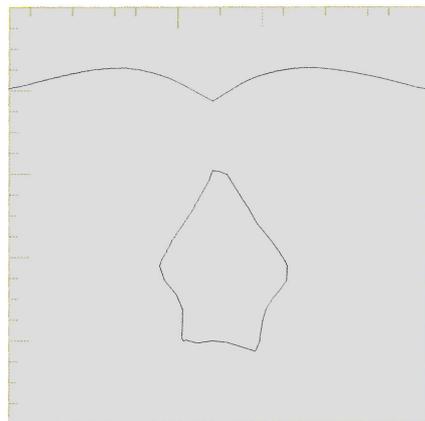


Figure 8.12: A cross section of simulation result shown in Figure 8.9.

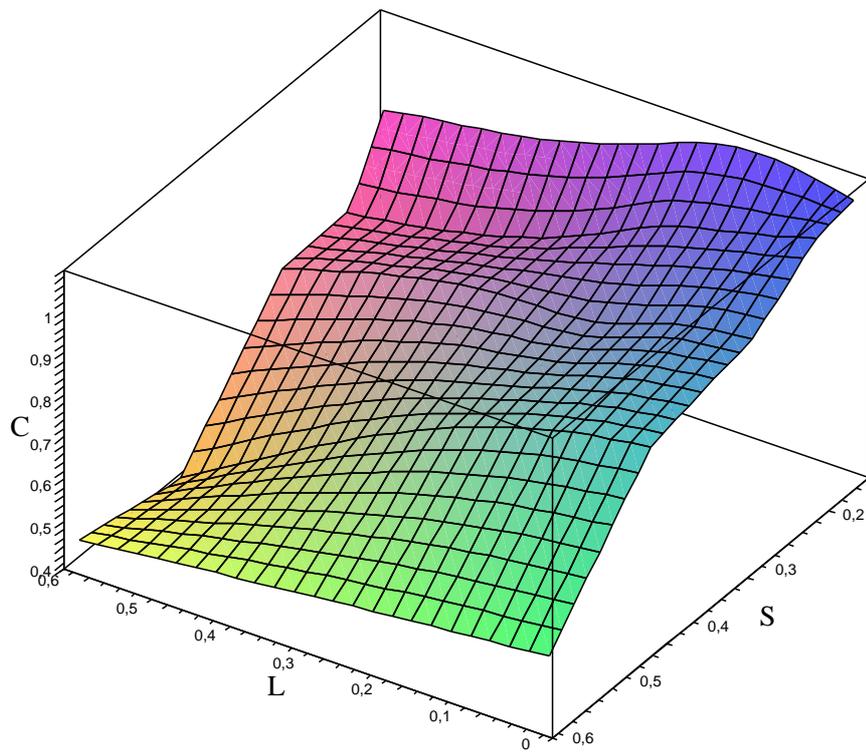


Figure 8.13: Dependence of C on S and L .

9 Application of ELSA to Mesh Generation

In this chapter we present the application of ELSA to an area which is not especially considered in the literature. It is the use of the level set method for the generation of structurally aligned grids. The grids are generated using ELSA based on the technique proposed in [80]. However, the grid generation is performed by a few extensions.

Examples of a trench gate MOSFET and an RF (radio frequency) SOI (silicon-on-insulator) LDMOS (laterally diffused MOS) power device using the device simulator are presented to show how practicable this method is. The device simulations are performed on a grid generated by this new algorithm. In order to accurately resolve the interesting regions of the above mentioned devices, several areas of refinement were defined where the grid was constructed based on varying resolutions.

9.1 Motivation

The quality of a mesh plays a very important role for the numeric solution of semiconductor device equations using a finite element or finite difference method. Because of this quality dependence on the underlying mesh, structurally aligned grids are a crucial prerequisite for accurate device simulation, which needs to solve partial differential equation. In addition, for aligning the meshes within the structures, it is also desirable to enforce quality criteria like the Delaunay criterion or the minimum angle criterion [33].

We present a new method to generate structurally aligned grids with optional anisotropy. The basic idea is using a level set algorithm for advancing a front through the simulation domain. This leads to construct a suitable set of edges for the next steps of the mesh generation. After extracting and reworking the boundaries these edges are used in a second step as the input to a specialized grid generator that enforces the specified quality criteria. Although a technique based on the level set method has been used for the generation of structurally aligned grids [77], that method cannot generate anisotropic grids and no condition concerning the quality of the grid, e.g., minimum angles or the Delaunay criterion, can be guaranteed. However, our approach has been successfully applied to semiconductor device simulation. The generated grids were used with the simulator MINIMOS-NT.

9.2 The Semiconductor Equations

The Poisson and the continuity equations for electrons and holes [5, 58, 75], are the basic equations used for semiconductor device simulations. The default carrier transport model in MINIMOS-NT is the drift-diffusion model which can be derived from the Boltzmann equation by the method of moments.

The main difficulties in the numerical treatment of the drift-diffusion equations are first their nonlinearity and second the large differences among the magnitude of the variables

which are involved in these equations. These differences cause an almost singular behavior of the solution of drift-diffusion equations [58]. It is also known that the solutions of the drift-diffusion equations behave variably in different regions of a device. This is referred to the layer structure of the solutions, i.e., they show large gradients [57]. These steep gradients occur locally across p - n junctions and in channel regions, e.g., in the narrow regions underneath semiconductor-oxide interfaces. The singular behavior and layer structure of the solution permit to use singular perturbation analysis [58], which is based on locally replacing the basic equations in different subregions of the device by simpler problems. The solutions of these simplified problems have to guarantee all the essential qualitative features of the original solution. These approximations enable to gain insight into the behavior of the solution which can not be obtained normally by the complex original system.

The information about the layer structure of the solutions is vital when generating grids from a priori information. In contrast, grid refinement techniques are of course based on a posteriori information from error estimators. The solutions of the device equations depend on the location of the junctions, the iso-lines and the distribution of the doping, and the operating conditions. Because of the layer behavior in the vicinity of junctions, the grid can be constructed suitably for certain operating conditions based on the extracted iso-lines before attempting a numerical solution.

9.3 Main Steps of the Grid Generation

In order to generate our structurally aligned grids two main steps have to be taken into account. The first one (cf. Section 9.4) is using a level set algorithm to advance one or more fronts with constant speed functions through the simulation domain. The second one is feeding TRIANGLE [91, 92] with the edges constructed in the first step to obtain a Delaunay triangulated grid. A Delaunay triangulation of a vertex set is a triangulation of the vertex set with the property that no vertex in this set falls in the interior of the circumcircle (circle that passes through all three vertices) of any triangle in the triangulation. As mentioned previously, the minimum angle criterion is obeyed using a refinement algorithm for quality mesh generation [70]. The TRIANGLE program used in this work, is written in C and computes two-dimensional Delaunay triangulations. TRIANGLE can be fed using two different kinds of input files. The first kind is a .node file [91, 92] which only defines the region for the triangulation based on introducing the vertices. Because a parameter to control the quality when using .node files is lacking we have used the second kind of input file accepted by TRIANGLE, namely .poly file [91, 92].

9.4 Construction of a Device Using the Level Set Method

In this section the details of the algorithm devised for the generation of edges which are introduced as input into TRIANGLE, are presented [7].

As mentioned in Section 5.2, the level set function must be initialized to the signed distance function. Within the numeric application the level set function is represented by values on grid points. In order to find the coordinates of the current boundary the surface must be extracted from this grid using linear interpolation. One or more fronts is advanced with constant speed functions through the simulation domain. For each moving

front a certain number of boundaries are extracted and reworked. The number of these boundaries and the spacing between them can be defined arbitrarily and depend on the number of advancing level set steps and their time steps. Clearly the spacing between the intermediate boundaries obtained by the level set algorithm will later determine the diameters of the triangles of the resulting grid.

Figure 9.1 shows the triangulated simulation domain after introducing the edges obtained by the level set algorithm into TRIANGLE. Because of the different lengths of the segments which are obtained at each boundary extraction, we can clearly see that this triangulation contains triangles which are too small. An enlarged view of this undesirable situation is shown in Figure 9.2.

This problem originates from a boundary extraction algorithm which is implemented in ELSA and considered firstly just for the deposition and etching processes. It uses an interpolation method to find the points of the boundary and represents these as a list of segments with different lengths. Figure 9.3 shows a part of the last five steps of advancing the front at a larger scale to show more clearly the varying lengths of the segments. The segments may become arbitrarily small and are the cause for the finely triangulated areas. To overcome this problem we need to ensure that all segments of the boundary have about the same lengths as shown in Figure 9.4 [18, 22].

We start the algorithm by choosing a certain length d for all segments. In our example we chose the minimum value of the vertical or horizontal distance between the points of

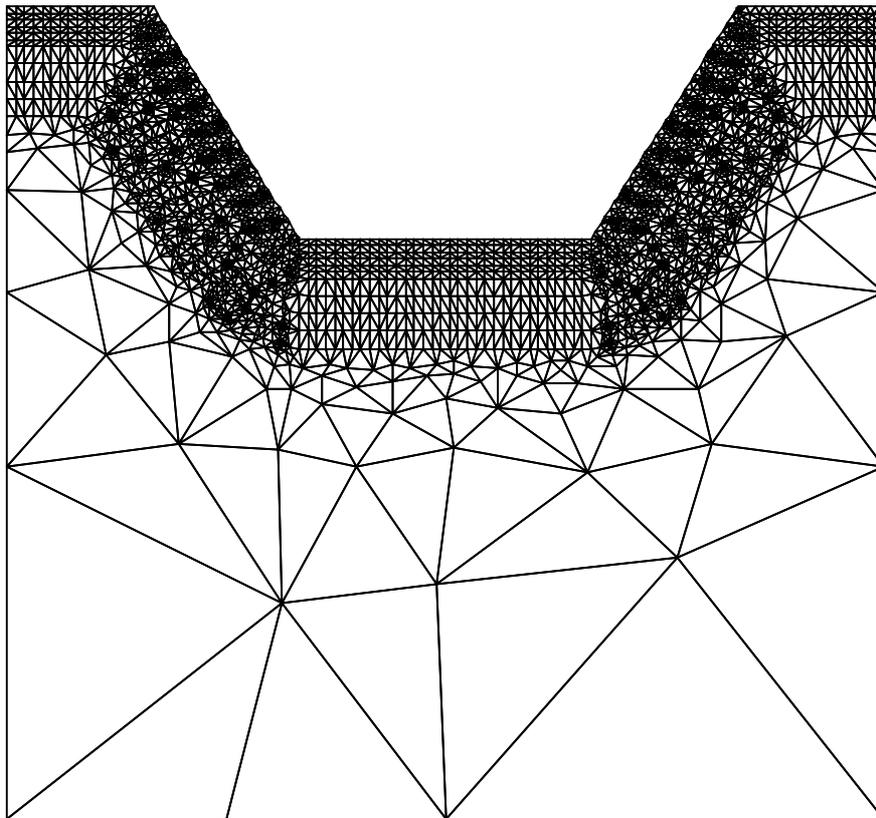


Figure 9.1: The triangulated grid without using a segment length equalizer.

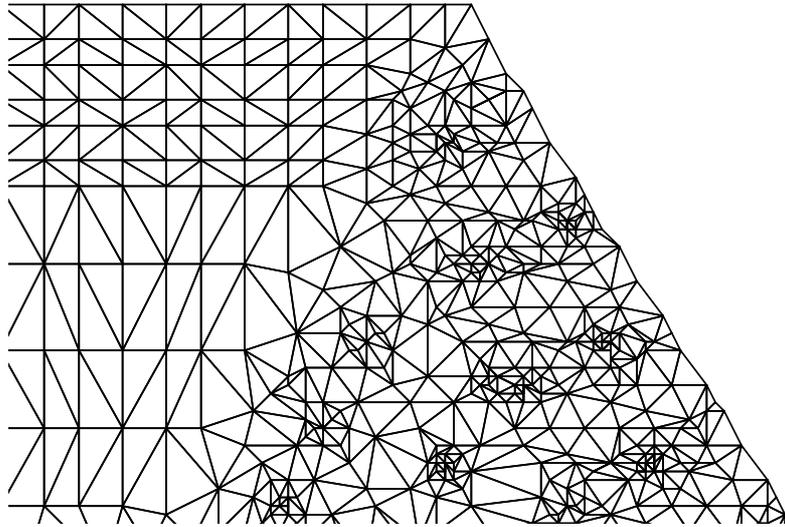


Figure 9.2: An enlarged part of the mesh structure shown in Figure 9.1.

our original rectangular grid which is used in the level set step. The first point of the extracted boundary remains without any changes but to locate the other points we have to discern two cases. In one case the distance between the first point and the second point is equal to or greater than d . In other case this distance is smaller than d .

In the first case the second point of the recalculated boundary is computed fulfilling the two following restrictions: first, the new segment must be along the first segment of the old segment and second, the length of the new segment must be equal to d .

In the second case we compute the second point of the new boundary along the next segment of the original boundary and as in the first case fulfilling the length requirement. These steps are iterated until we reach the boundary of the domain.

This first part of the grid generation is highly customizable and anisotropy can be introduced here by choosing the spacing between the intermediate boundaries and the distance between the points of the normalized boundary accordingly.

Now the grid segments are normalized by choosing points on the boundary that are equidistant when their distance is measured along the boundary. The normalized intermediate boundaries consist of straight lines which are edges of the final grid to be respected again in the second part of the algorithm which uses TRIANGLE.

This allows to produce meshes with no small angles while using relatively few triangles. Figure 9.5 shows the triangulated grid after using TRIANGLE without the dense triangles. This can be seen more clearly in Figure 9.6 which depicts exactly the same enlarged area of the meshed structure shown in Figure 9.2.

The benefits of this algorithm can be summarized as follows. The grid resolution is customizable and the areas of higher resolution can be chosen arbitrarily. The grid resolution may vary over several orders of magnitude. The algorithm can deal with arbitrary initial structures and an arbitrary number of starting fronts, defining areas of high resolution. Anisotropy may be introduced by choosing appropriate parameters for the algorithm. At the same time quality criteria like the Delaunay criterion and

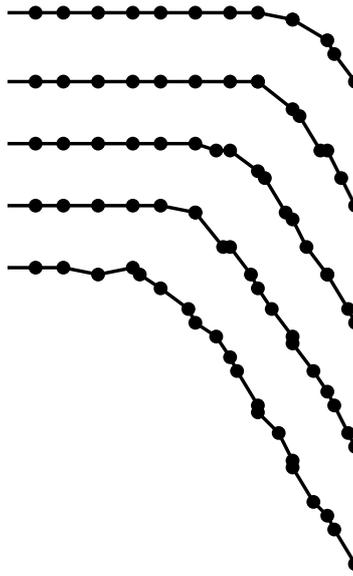


Figure 9.3: Enlarged view of the last five steps of the advancement of the front. The varying lengths of the segments are clearly visible.

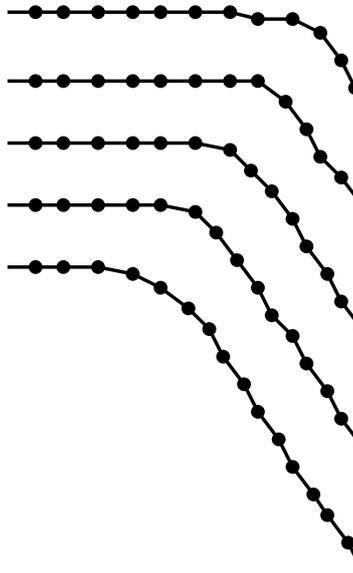


Figure 9.4: Enlarged view of the last five steps of the advancement of the front after equalizing the lengths of the segments. The length of the segments are now approximately the same.

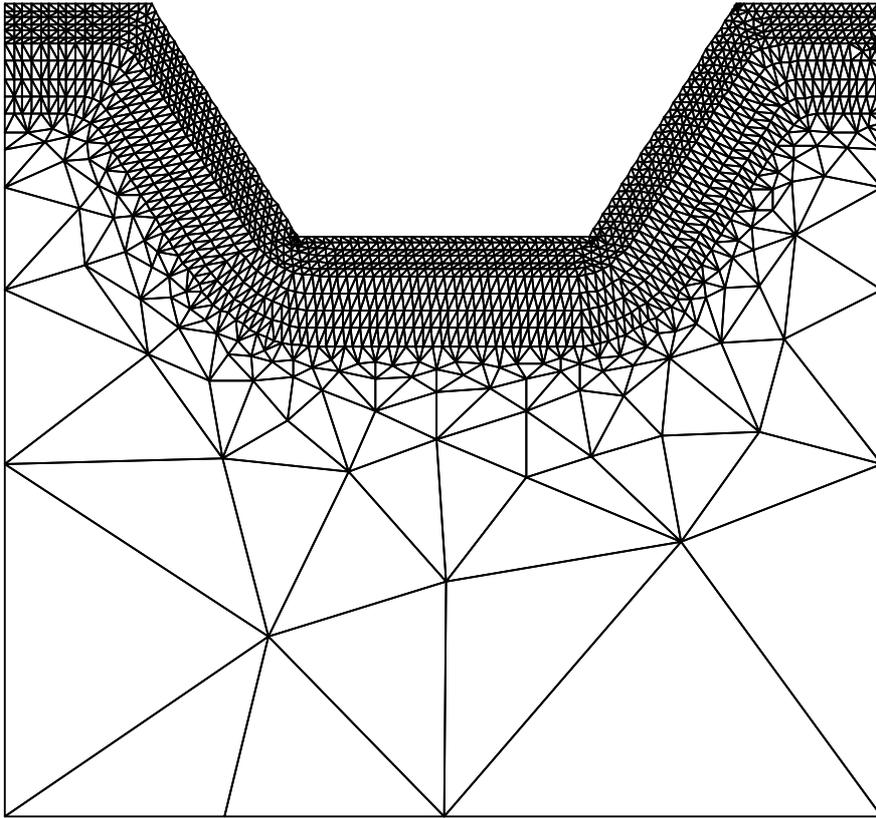


Figure 9.5: The triangulated grid is caused using the segment length equalizer.

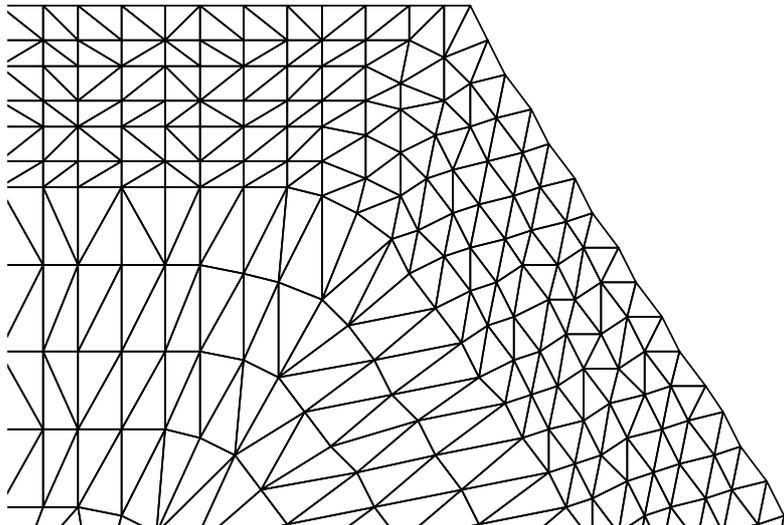


Figure 9.6: A part of the above grid on a larger scale.

the requirement that all angles of the triangulation are larger than a certain minimum angle are enforced. It is important to note that the algorithm works reliably, since it is based on edges in contrast to just prescribing sets of points, hence preserving directional information.

In [102] a different approach to grid generating using a level set algorithm is presented. Previous work along these lines includes [52,61]. Compared to grid generation algorithms using iso-lines or iso-surfaces obtained as solutions of a Poisson equation [96], the advantage of this algorithm is its flexibility. This is important, e.g., near the buried layers of SOI devices. The initial boundaries where the advancing fronts start, the prescribed number of intermediate boundaries and their spacing determine the properties of the final grid in a straightforward manner in contrast to the Poisson equation approach.

9.5 Grid Generation for a TMOSFET

TMOSFETs are useful for power switching at high voltages [16, 27, 28, 90, 101]. Their geometric layout also provides advantages, because their inversion and accumulation channel regions are perpendicular to the wafer surface. Hence they maximize the ratio of cell perimeter to its area, thus increasing packing density. The TMOSFET considered is a 120V trench gate UMOS transistor. The simulated characteristics of the device after its generating using our approach are presented.

The device structure of the trench gate UMOS transistor is shown in Figure 9.7 and its parameters in Table 9.1. Its trench depth is $3\mu\text{m}$ and its gate oxide thickness is $0.1\mu\text{m}$. It is designed to achieve a forward blocking voltage of 120V.

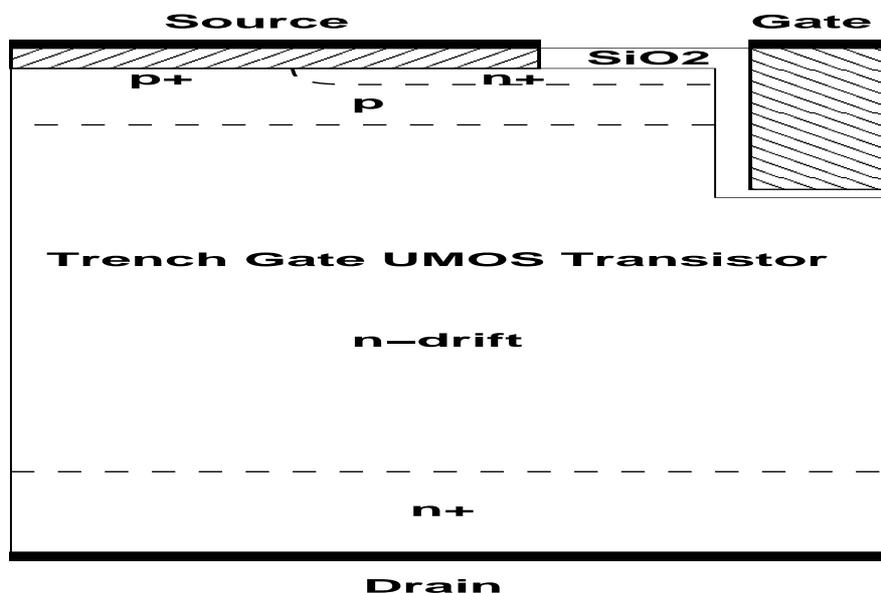


Figure 9.7: Structure of the TMOSFET. The half cell pitch of the device is $2.5\mu\text{m}$ and its n drift length is about $9.5\mu\text{m}$.

Parameter	Value
n drift doping	$1.5 \times 10^{15} \text{cm}^{-3}$
p well doping	$1 \times 10^{17} \text{cm}^{-3}$
p well	$\approx 1.4 \mu\text{m}$
p^+ buffer	$5 \times 10^{18} \text{cm}^{-3}$
n^+ source depth	$\approx 0.38 \mu\text{m}$
Gate oxide thickness	$0.1 \mu\text{m}$
Trench depth	$3 \mu\text{m}$
n drift length	$\approx 9.5 \mu\text{m}$

Table 9.1: The technological and geometrical parameters of the TMOSFET.

9.5.1 Grid Generation

For the grid generation we used four boundaries following the three junctions (cf. Figure 9.7) and one in the p -region near the gate oxide. First, at the $n^+ - p$ junction we used three boundaries in each direction of the initial boundary following the junction with a distance of $0.02 \mu\text{m}$ between any adjacent boundaries.

At the $p - n$ junction we used one boundary above and below the initial boundary and a distance of $0.02 \mu\text{m}$. At the $n - n^+$ junction in the lower part of the device we constructed two boundaries with a distance of $0.5 \mu\text{m}$ going downwards from the initial boundary following the junction. For the last set of prescribed edges we started at the right hand side of the p -region and moved to the left constructing three boundaries at a distance of $0.005 \mu\text{m}$.

In the second step we used the TRIANGLE program requiring a minimum angle of 25° with the prescribed edges as input. The resulting mesh produced and two enlargements thereof are shown in Figure 9.8 and Figure 9.9. The junction areas are resolved very finely as demanded.

9.5.2 Device Simulation

The device simulations were performed using MINIMOS-NT. Figure 9.10 shows typical on-state characteristics of the high voltage TMOSFET. The $I - V$ curves of the figure show that good saturation currents behavior is obtained by increasing the drain voltage. Transfer characteristics are shown in Figure 9.11 for drain voltages of $V_d = 0.1\text{V}$ and 0.5V . From this figure a threshold voltage V_T of 2.5V is obtained. It is important to note that the threshold voltage is independent of the drain voltage.

9.6 Grid Generation for an SOI Power Device

The second example is the simulation of an RF SOI LDMOS power transistor. Several regions of refinement had to be chosen and the specific structure of the device and the location of the junctions have been taken into account. SOI is a promising technology for monolithic integration of digital, analog, and RF devices. For RF power applications the reduced capacitance and the low leakage current of SOI devices are highly demanded.

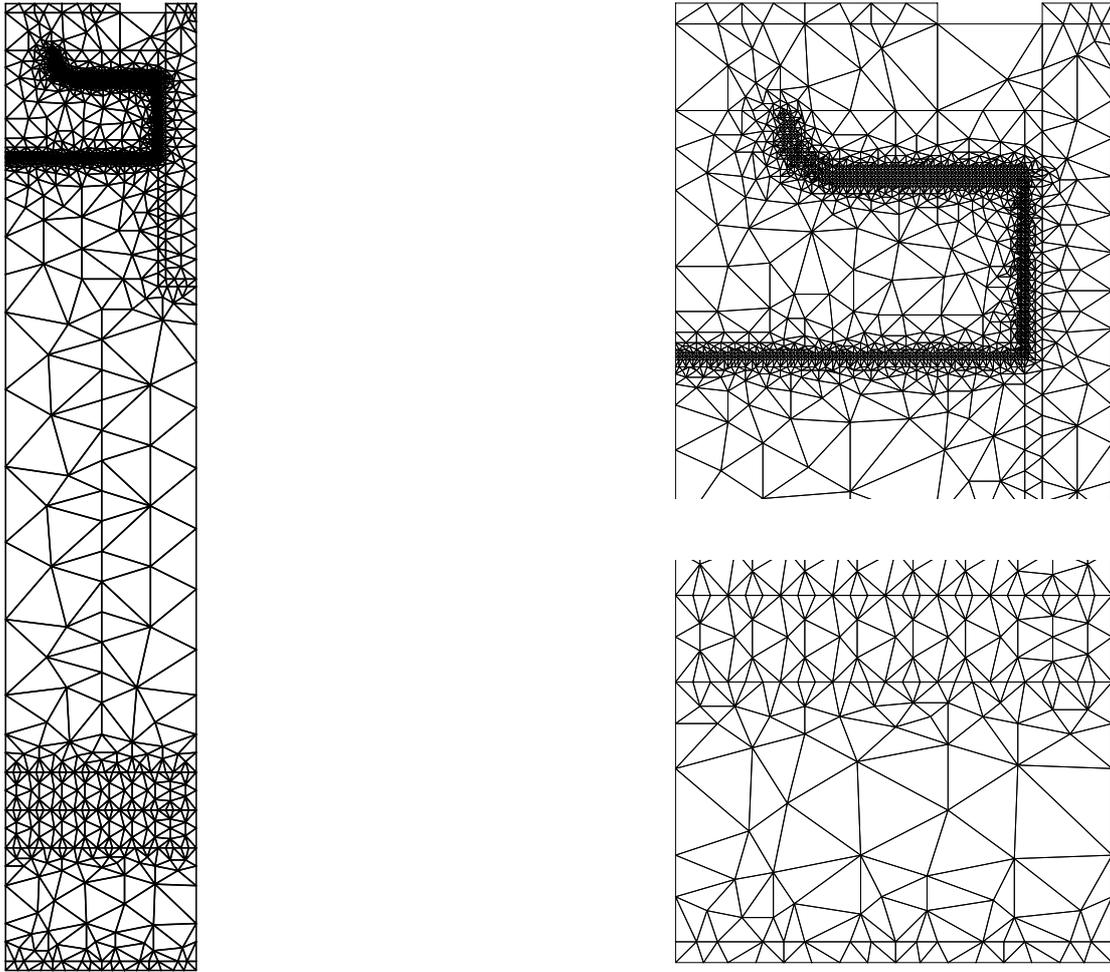


Figure 9.8: The grid generated for the TMOSEF device in Figure 9.7. Two enlargements are shown on the right hand side.

The simulation results presented are the two-dimensional device simulation of a 110V RF SOI-LDMOSFET.

Again, the final grid was obtained by TRIANGLE starting from prescribed edges. The minimum required angle was 20° . The final grid is shown in Figure 9.12 and an enlargement in Figure 9.13. The parameters of the device is described in Table 9.2. It is designed to achieve a forward blocking voltage of 110V with an SOI thickness t_{soi} of $1.5\mu\text{m}$ and with a buried oxide thickness t_{ox} of $1.0\mu\text{m}$. The doping of the device is given by analytic functions or, more precisely, Gaussian profiles (cf. Table 9.2).

9.6.1 Grid Generation

To generate the grid we used six boundaries following the four junctions (cf. Figure 9.12), one in the channel, and one at the silicon-insulator interface. First, at the p -body- n + junction we used one boundary in each direction of the initial boundary following the junction with a distance of $0.1\mu\text{m}$ between two adjacent boundaries.

Second, at the n -drift- p -epi junction we used one boundary above and below the initial

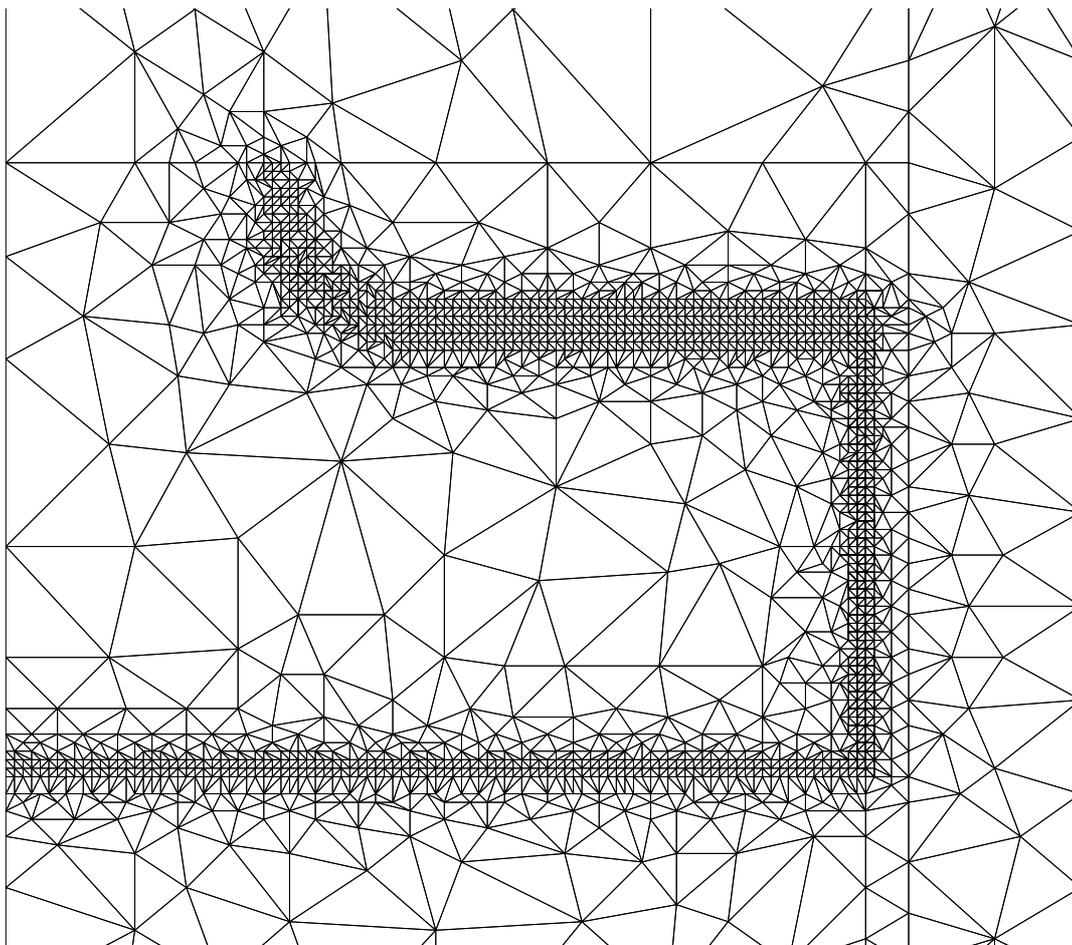


Figure 9.9: Enlargement of the grid shown in Figure 9.8.

Parameter	Value
n drift length	$6\mu\text{m}$
n drift doping (P)	$3 \times 10^{16}\text{cm}^{-3}$
SOI thickness	$1.5\mu\text{m}$
p epi doping (B)	$1 \times 10^{14}\text{cm}^{-3}$
$p+$ buffer doping (B)	$5 \cdot 10^{18}\text{cm}^{-3}$
p body doping (B)	$7 \times 10^{17}\text{cm}^{-3}$
Sub doping (P)	$1 \times 10^{18}\text{cm}^{-3}$
SiO ₂ layer thickness	$1\mu\text{m}$

Table 9.2: The technological and geometrical parameters of the RF SOI LDMOS power transistor. The lateral factor of all Gaussian profiles is 0.8.

boundary and a distance of $0.02\mu\text{m}$. Third, at the n -buff- p -epi junction we constructed one boundary above and below at a distance of $0.02\mu\text{m}$. For the $n+$ - n -buff junction boundaries, again one boundary above and below at a distance of $0.1\mu\text{m}$ were used.

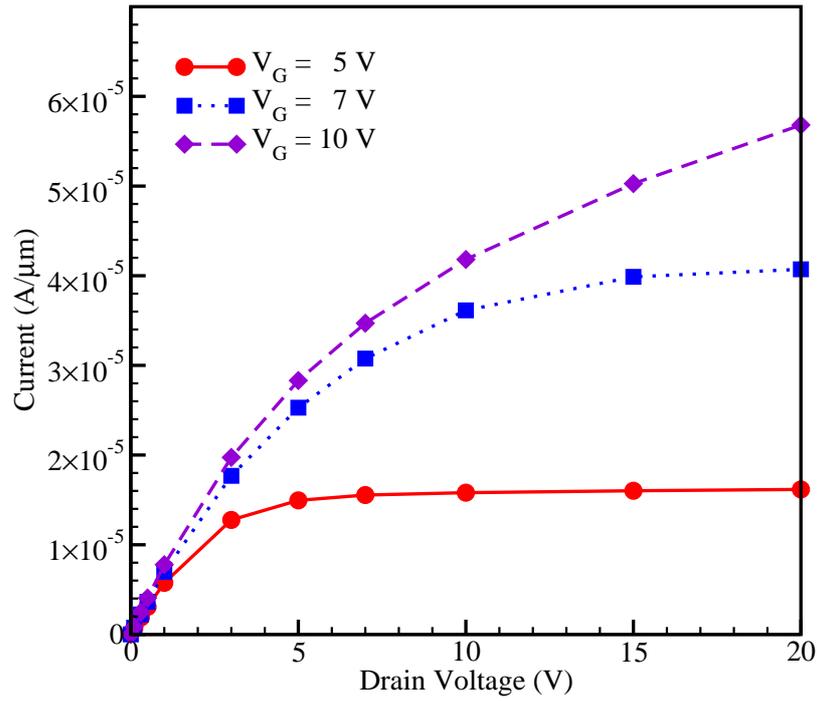


Figure 9.10: The on-state characteristics of the vertical TMOSFET for gate voltages of 5V, 7V, and 10V.

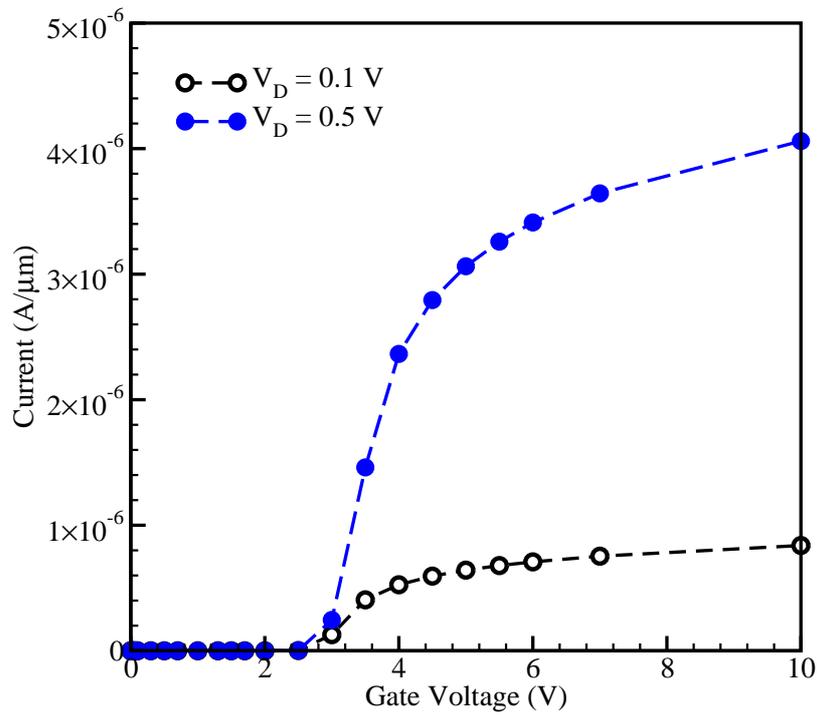


Figure 9.11: The transfer characteristics of the high voltage TMOSFET for drain voltages of 0.1V and 0.5V.

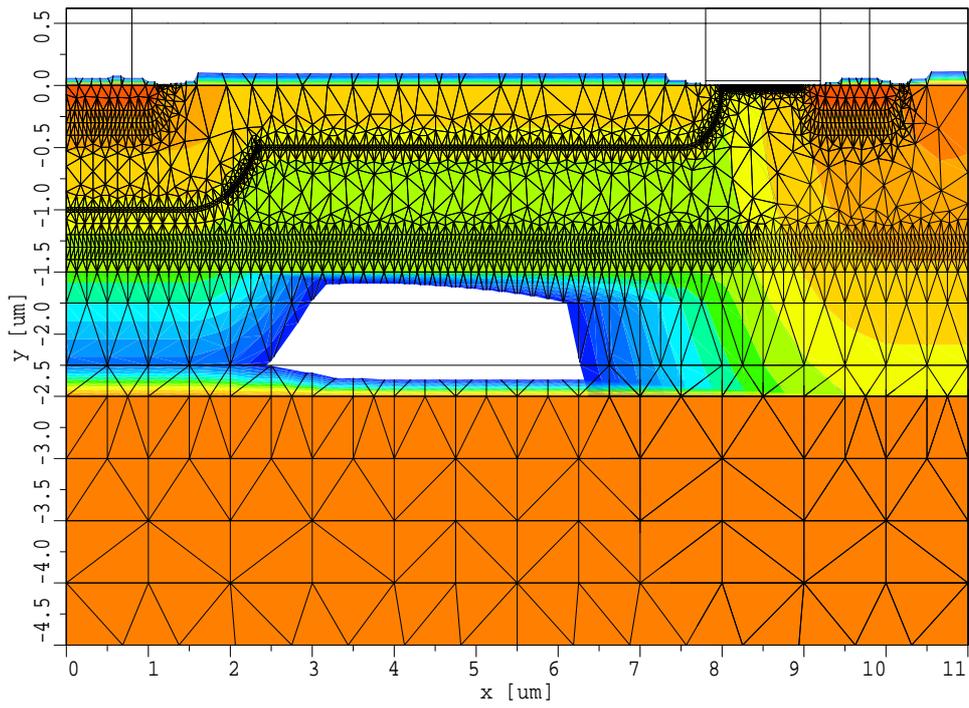


Figure 9.12: The structure of the RF SOI LDMOS power transistor and the generated grid.

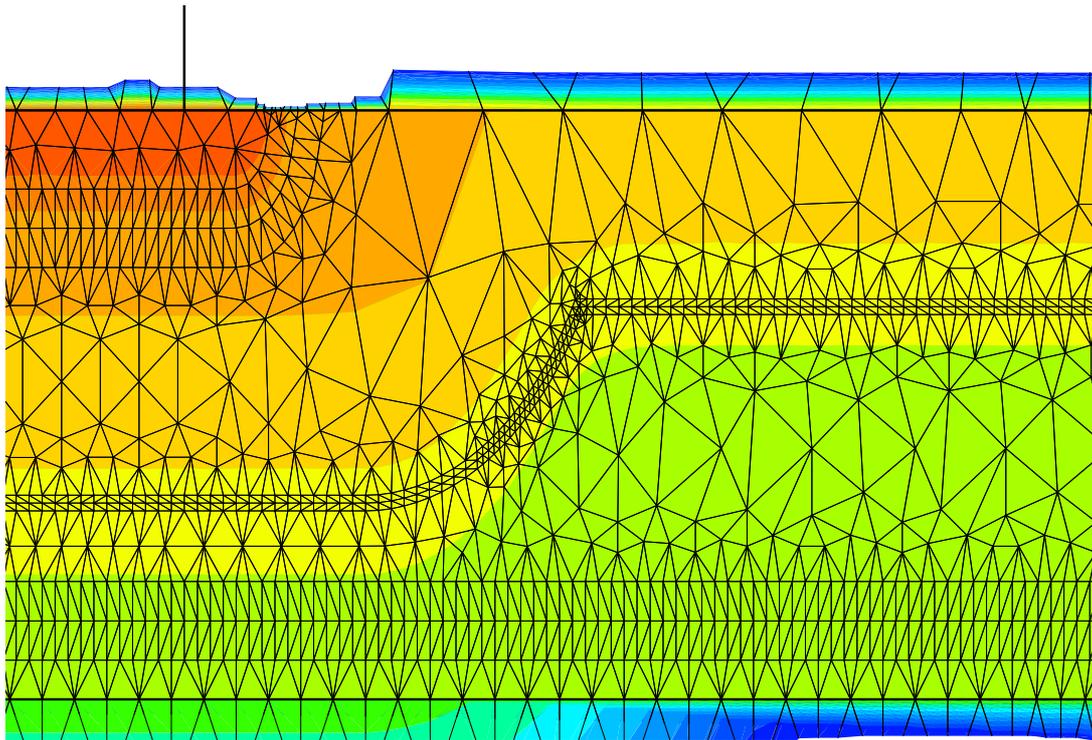


Figure 9.13: Enlargement of the drain region (left) from Figure 9.12.

In the channel region we started at the interface and moved down constructing four boundaries at a distance of $0.005\mu\text{m}$. For the last prescribed edges we started at the boundary between the silicon and the silicon dioxide layers and moved up and down at a distance of $0.1\mu\text{m}$.

9.6.2 Results and Discussion of Device Simulation

The optimum drift length and doping concentration are considered by the RESURF (reduced surface field) principle. With the proposed grid generation algorithm mesh structures suitable for device simulation can be obtained along the junctions (parallel to the junction) and at the buried oxide interface. Again the typical on-state characteristics were obtained using MINIMOS-NT and are shown in Figure 9.14. The I - V curves imply that good saturation currents behavior is obtained by increasing the drain voltage. Transfer characteristics are shown in Figure 9.15 for drain voltages of $V_d = 0.1\text{V}$ and 0.5V . From this figure a threshold voltage V_T of 1V is obtained.

9.7 Summary

A new method to generate structurally aligned grids and guaranteeing quality criteria on the resulting triangulation was presented. It provides a lot of flexibility, since the resolution and anisotropy of the grid is customizable and the diameter of the triangles may vary over several orders of magnitude within one simulation domain. Compared to the approach of using iso-lines or iso-surfaces of solutions of a Poisson equation [96], this method allows to propagate several fronts through the simulation domain and thus to precisely tailor the areas of high resolution in a straightforward manner.

Furthermore the algorithm is robust since the generation of the final triangulation is based on edges that have to be respected (and not on single points). Finally the grids generated satisfy the Delaunay criterion and the minimum angle criterion which ensures high grid quality with respect to its numeric properties.

Two examples demonstrate the method's applicability even to non-trivial geometries. The on-state and transfer characteristics were calculated using the meshes obtained by this method.

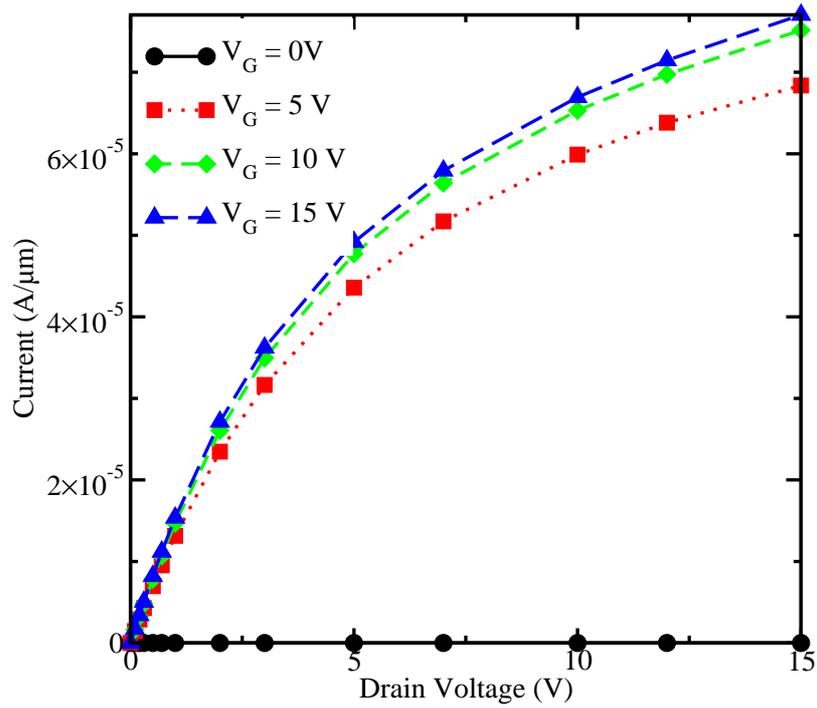


Figure 9.14: The on-state characteristics of the RF SOI LDMOS power transistor for gate voltages of 5V, 10V, and 15V.

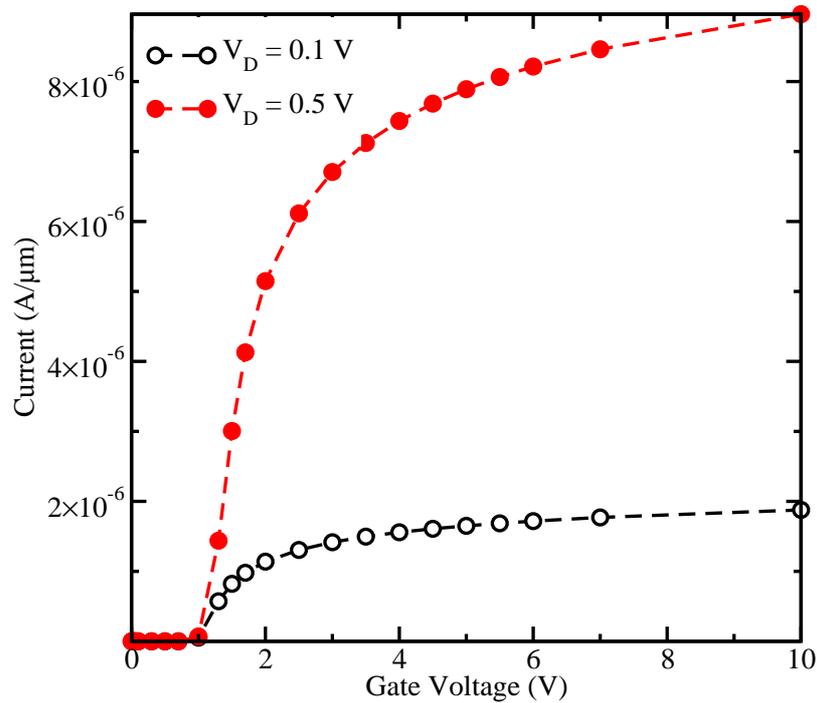


Figure 9.15: The transfer characteristics of the RF SOI LDMOS power transistor for drain voltages of 0.1V and 0.5V.

10 About Efficiency

In this section we present some three-dimensional topography simulation results which serve to get insight into the efficiency and time consumption of the simulator.

We begin with a deposition of the material into a rectangular trench shown in Figure 10.1. The transport of the particles is based on the radiosity model. Figure 10.2 shows the simulation result of this material deposition from a plane located above and parallel to the trench leading to the void formation, because of shading effects due to the visibility determination between surface elements and source plane, and between surface elements themselves. Since the angle of visibility of the source is smaller at the bottom of the trench compared to the top of the trench, more material is deposited at the top of the trench. This in turn leads to the effect that the visibility angle of the source plane at the bottom is decreased more and more as the material deposition continues, until the top left and right sides of the trench come together and form a void.

The next example considered is a straightforward simulation of isotropic etching of the same trench. The simulation is easily performed by setting the speed function $F(t, \mathbf{x}) = F$ at each grid point, where F is negative. As expected, the sides of the trench are etched away cleanly and are rounded as shown in Figure 10.3.

Finally, Figure 10.4 shows directional etching of the same trench [15]. The total flux at the surface element has been assumed to be a cosine function of the angle between the surface normal and the normal vector of the source plane. Because of considering a mathematical function for the speed function, the visibility and reflection calculation parts of the simulator are turned off. These parts are needed when calculating the flux by using physical models. The trench has been etched less compared to the selective isotropic etching at the sides and tends to be etched more in vertical direction.

Table 10.1 shows a comparison of the simulation times of these different simulation processes for different grid resolutions [13]. The most time consuming simulation is the deposition simulation, because all expensive steps, e.g., visibility determination, extension of the speed function, and the iterative solver are required. For directional etching, extension of the speed function is the only time consuming part of the simulation. Therefore, the simulation time is considerably smaller than that of the deposition process. For isotropic etching neither visibility determination, nor the iterative solver, nor an extension of the speed function are required. Thus the simulation time is very small compared to the other simulations. In the third column of Table 10.1 the simulation times for a grid with twice the resolution of the original resolution are presented. For instance, the deposition time has increased by about a factor of 31 when doubling the grid resolution from $30 \times 30 \times 30$ to $60 \times 60 \times 60$. This is in accordance with the expected minimal factor which we have estimated in Section 5.13. There we have discussed that doubling the grid resolution approximately increases the number of surface elements by a factor of 4 which in turn increases the complexity of the visibility determination by the radiosity model by a factor of 16. Therefore the simulation time has increased by a factor $\frac{47.4}{1.54} = 30.77$ which comes up to the expectation of a minimum factor of $2^4 = 16$.

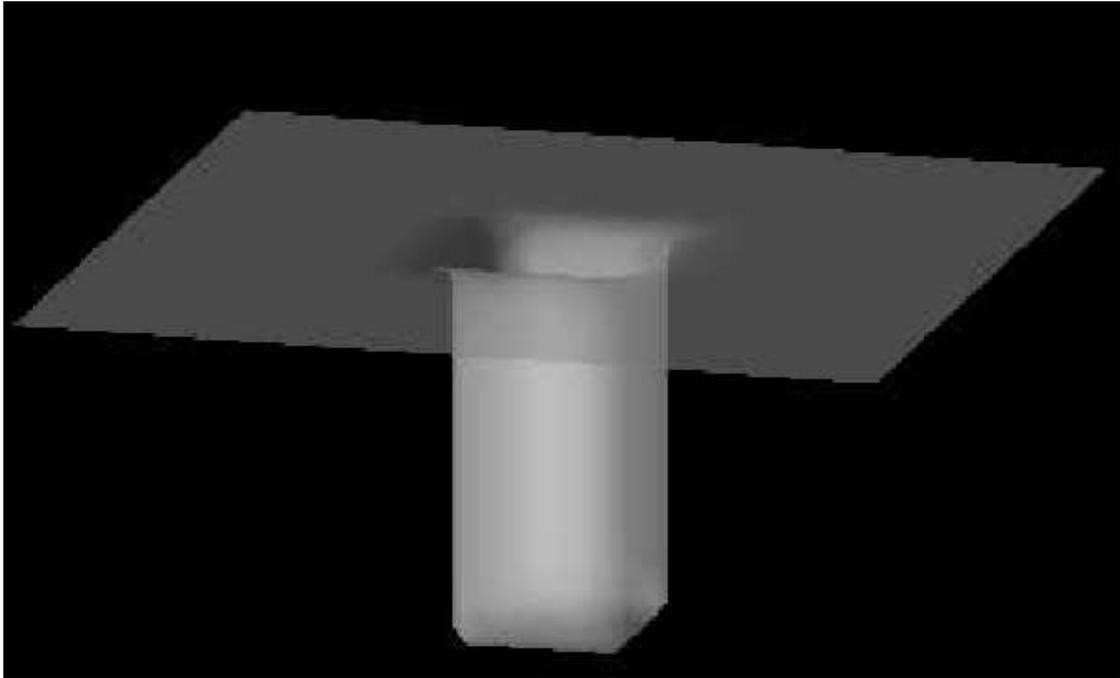


Figure 10.1: Initial boundary.

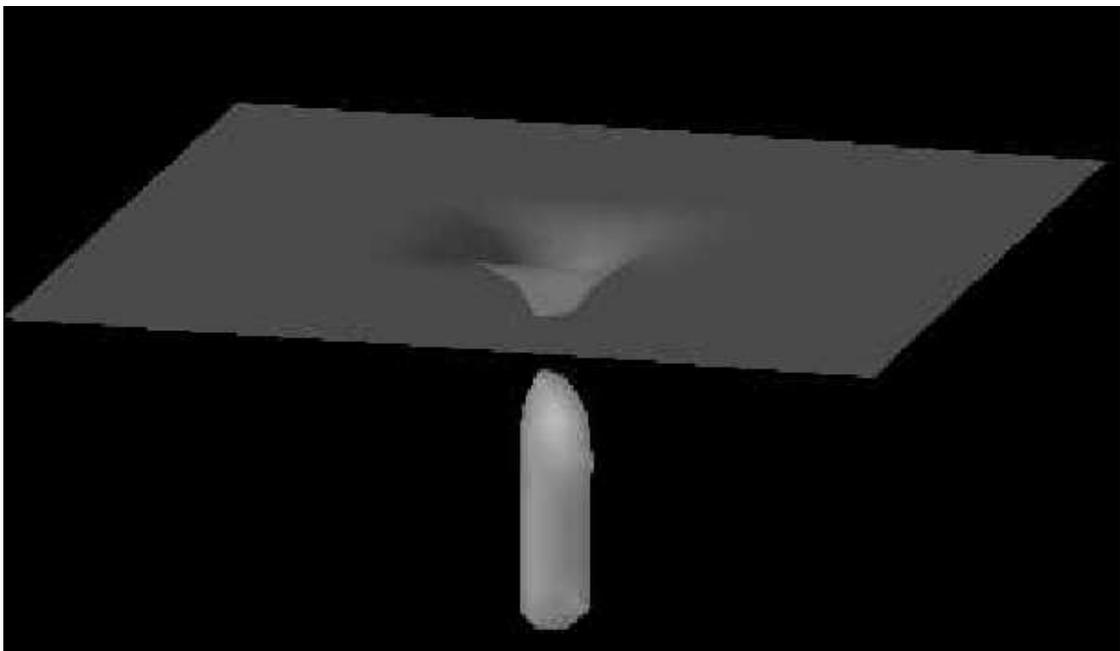


Figure 10.2: Void formation after a deposition process into the initial boundary shown in Figure 10.1.

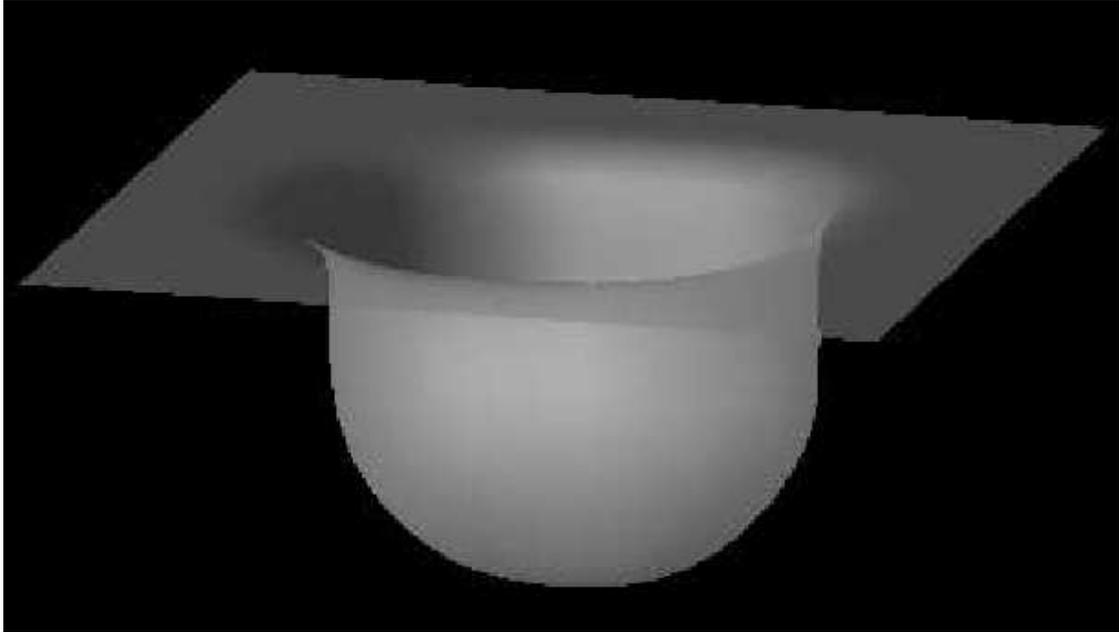


Figure 10.3: Isotropic etching the initial boundary shown in Figure 10.1.

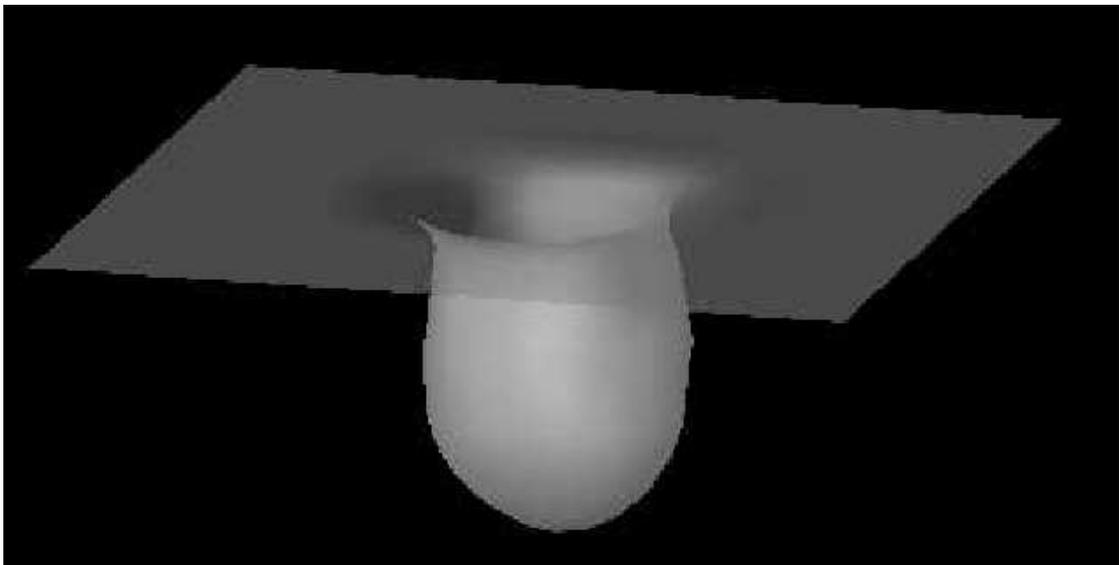


Figure 10.4: Directional etching the initial boundary shown in Figure 10.1.

Table 10.1: Simulation times for the different simulations presented here.

Grid resolution	30×30×30	60×60×60
Deposition time/step	1.54s	47.4s
Isotropic etching/step	0.53s	2.77s
Directional etching time/step	0.97s	21.1s

11 Conclusion and Outlook

Conclusion

State of the art algorithms for two- and three-dimensional surface evolution processes, namely, deposition and etching processes were developed and implemented. The simulator is based on the level set algorithms and can be used to simulate all common deposition and etching processes. The level set method has been shown to be the best alternative for overcoming the problems emerging in other surface tracking methods, e.g., high memory consumption and CPU time. This improvement was obtained by using different techniques such as calculating the signed distance function by a fast marching algorithm, extending the speed function, and dynamically moving the narrow band according to the new zero level set.

A basis for understanding the desired and undesired effects on topography simulation during the semiconductor manufacturing processes was presented. The techniques for overcoming the undesired problems were discussed and were used for obtaining an etching profile with minimal corner rounding, for instance.

In order to obtain the best model for the deposition processes, different physical models were tested by using SIESTA which uses the inverse modeling technique. This helped to model two important processes, namely, the deposition of the silicon dioxide from TEOS and silicon nitride. These deposition processes were used to simulate the capacitances which contribute to the timing delays in interconnect lines. The final capacitance calculation was done by joining ELSA and RCX tools. The significant influence of void formation on the capacitances was quantified, as using voids in a controlled and reproducible manner can be an economically advantageous substitute for low- k materials.

Furthermore the optimized parameters of the deposition models obtained by SIESTA were used in the three-dimensional topography simulator to predict the void characteristics during interconnect processes. These characteristics enabled to set layout design rules depending on geometrical parameters to avoid the formation of cracks.

Finally a new level set based method to generate structurally aligned grids while guaranteeing quality criteria of the triangulation was presented. It provides a lot of flexibility, since the resolution and anisotropy of the grid is customizable and the diameter of the triangles may vary over several orders of magnitude within one simulation domain.

Outlook

Simulations of the deposition and etching processes allow to gain insight into the considered processes. The more chemistry is considered in physical models the more accurate is this insight. Therefore, physical models which are more related to the chemistry of the processes must be developed for the simulation of different deposition and etching processes. Simultaneously a balance between the complexity of the models and the simulation time has to be considered to avoid very long simulation times. The models

should be first implemented in two dimensions because of simplicity. After successfully finding the models which are in a good agreement with measurements, they have to be implemented for three dimensional simulations.

Having a full three-dimensional process tool capable of the simulation of the whole process steps is becoming more and more important. Topography simulation is a very essential issue in the simulation of most of process steps. Therefore, the topography simulator has to be integrated into a fully three-dimensional process tool. In addition, the different physical models proposed and implemented in the future in ELSA will also be incorporated into a fully three-dimensional process tool.

Finally, the two- and three-dimensional development and implementation of a multi level set algorithm are planned. This is, for instance, absolutely essential for the simulation of plasma etching processes where different regions of materials and masks have to be defined. Furthermore, a multi level set approach has to be used for the simulation of growing a number of crystals. Each individual crystal grows until it hits another crystal, forming a grain boundary. The detection of a grain boundary and its later moving need to be handled with multi level set method.

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Curriculum Vitae

- Septemeber 17th, 1971 Born in Babol, Iran
- June 1989 High School Graduation
at Shahid Beheshti High School, Babol
- July 1989 Entrance Examination for University
- October 1989 Qualified for Electrical Engineering
at University of Science and Technology, Tehran, Iran
- October 1994 Received Degree of “B.Sc.”
in Electrical Engineering
- June 1995 – June 1997 Compulsory Military Service
- Oktober 1998 Enrolled in Electrical Engineering
at TU Vienna, Austria
- January 2002 Received Degree of “Diplom-Ingenieur”
in Electrical Engineering from TU Vienna
- March 2002 Entered Doctoral Program
at the Institute for Microelectronics, TU Vienna