DISSERTATION

Experimental Characterisation of Smart Power Technology Devices Stressed by High Energy Pulses

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Kurzfassung

Die Zusicherung der Zuverlässigkeit von integrierten Halbleiterschaltungen (Integrated Circuits, ICs) ist eine der Hauptaufgaben in deren Konstruktion. Es gibt ein breites Spektrum von thermischen, mechanischen und elektrischen Belastungen, welche die Zuverlässigkeit von Halbleiterbauelementen beeinflussen. Um die verschiedenen Ausfallsmechanismen zu identifizieren, ist es notwendig die Bauelemente realen Tests zu unterziehen. Detaillierte Analysen der Testergebnisse führen zu einem besseren Verständnis der involvierten physikalischen Effekte. Dies wiederum trägt zur Spezifizierung von Entwurfsregeln bei, welche in Zukunft eine verbesserte Zuverlässigkeit bringen.

Eine der härtesten elektrischen Belastungen ist die elektrostatische Entladung (ElectroStatic Discharge, ESD). So eine Belastung kann einzelne Halbleiterbauelemente oder sogar den ganzen Mikrochip zerstören. Da dieser Vorgang oft von spezifischen Begleiterscheinungen (z.B. Ausbildung von Strompfaden) geprägt ist, ist ein experimenteller Zugang zum internen Verhalten der zu untersuchenden Bauteile von großem Interesse. Das transiente interferometrische Abbildungsverfahren (Transient Interferometric Mapping, TIM) ist ein leistungsstarkes Werkzeug, welches bereits mehrere Male das interne Bauteilverhalten aufgezeigt hat. Es erlaubt die Abbildung von Temperatur- und freien Ladungsträger Konzentrationsverteilungen und daher die Verfolgung von Strompfaden in den untersuchten Bauelementen. Während der letzten Jahre ist dieses interferometrische Abbildungsverfahren herangereift und kann nun zu komplexen Analysen des Bauteilverhaltens und auch zur Überprüfung von Bauelementmodellen herangezogen werden. Diese Methode wird in dieser Arbeit zur Analyse von Halbleiterbauelementen, welche in einer Smart Power Technologie (SPT) hergestellt sind, angewendet.

Zuerst wird die TIM-Methode zur detaillierten Analyse der SPT ESD-Schutzelemente angewendet. Drei Layout Variationen der npn Struktur wurden unter zwei ESD Belastungstypen (HBM und CDM) untersucht. In diesen Bauelementen wurden die ESD-Robustheit, die Homogenität des Stromflusses und die Lokalisierung von heißen Flecken und Fehlerstellen experimentell untersucht. Weiters wurden die Unterschiede im Betriebsverhalten von Bauelementen mit variiertem Layout analysiert. Die experimentellen Ergebnisse wurden mit den zweidimensionalen Bauteilsimulationen verglichen.

Eine weitere Klasse der auf ESD-Robustheit untersuchten Bauelemente sind die Smart Power DMOS Transistoren. Die Ausbildung von Strompfaden in der aktiven Zone der Bauelemente und deren Entwicklung während eines Stress-Impulses ist im Detail analysiert worden. Es wurde experimentell nachgewiesen, dass sich die Strompfade in den Bauelementen bewegen. Mit Hilfe von zwei- und dreidimensionalen Bauteilsimulationen konnte der Mechanismus der Bewegung von Strompfaden verstanden werden.

Zum Abschluss wurde die TIM-Methode zur Untersuchung von DMOS-Transistoren im Millisekundenbereich verwendet. Die Eignung dieser Methode für solch Untersuchungen wurde erstmals aufgezeigt. Es wurde gezeigt, dass zur Analyse des Bauteilverhaltens in dieser Zeitskala es von Vorteil ist, nicht die gemessene physikalische Größe (Phasenverschiebung) sondern die zweidimensionale Leistungsdichte (P_{2D}) zu verwenden, welche von der gemessenen Phasenverschiebung berechnet werden kann. Es wurde die Genauigkeit des P_{2D}-Bestimmungsvorganges analysiert. Der Vorgang der Berechnung der Oberflächentemperatur konnte ebenso beschrieben werden.

Abstract

Assurance of the reliability of semiconductor integrated circuits (ICs) is one of the main tasks of the IC design. There is a broad spectrum of thermal, mechanical or electrical stresses, which influence the reliability of semiconductor devices. In order to identify various failure mechanisms it is therefore necessary to perform testing of the devices. Detailed analysis of the results afterwards yields an understanding of the effects involved. This in return helps in specification of design rules, which will in future guarantee an improved reliability.

One of the most severe electrical stresses is the electrostatic discharge (ESD). Such stress can be fatal for a semiconductor device, or even for the whole IC. As this event can be accompanied with specific phenomena, e.g. occurrence of current filaments, experimental access to the internal behaviour of investigated device is of great interest. Transient interferometric mapping (TIM) technique is a powerful tool, which already proved its capability to do the task several times. It allows mapping of the thermal and free-carrier concentration distributions and thus pursuing of the current paths in the studied devices. During previous years the technique has matured into the state that it can be applied for complex analysis of the device behaviour as well as for the verification of device models. The technique is utilised in this work for the analysis of semiconductor devices built within the smart power technology (SPT) process.

Foremost the TIM technique is applied for detailed analysis of the SPT ESD protection devices. Three layout variations of the npn structure are investigated under two types of ESD stress: HBM- and CDM-like. The ESD robustness, homogeneity of the current flow, localisation of hot spots and failures are experimentally studied in the devices. Differences in operation of the devices with varied layout are analysed. The experimental results are compared with the 2-dimensional device simulation.

Another class of studied devices are the smart power DMOS transistors, whose ability to withstand the ESD stress is investigated. The formation of current filaments in the device active area and their evolution during a stress pulse is in detail analysed. It is experimentally proved that the filaments move in the device. With a help of 2D and 3D device simulation the mechanism of filament movement is understood.

Finally the TIM technique is applied for the investigation of DMOS transistor operation in the *ms* time scale. Applicability of the technique for such kind of study is presented for the first time. It is demonstrated that for analysis of device behaviour in this time scale it is beneficial not to use the measured physical quantity (phase shift), but the *2D* power dissipation density (P_{2D}), which can be extracted from the experimentally obtained phase shift. Precision of the P_{2D} extraction procedure is analysed. Perspective way for calculation of surface temperature is discussed as well.

Content

Chapter 1

Introduction

1.1 Motivation

During the history of integrated circuit (IC) technology, the primary attention was mostly placed on advance in the signal processing and data storage capabilities of logic circuits. Besides this branch of electronic "brains", which is nowadays dominated by CMOS technology, a branch of semiconductor devices dedicated to a control of energy was developing too. These power devices were initially realised as discrete components. When a need to improve their performance, functionality, versatility and reliability arose, they were integrated with logic circuitry and power ICs appeared. The power ICs were first implemented using bipolar technologies, until a new power IC class based on the MOS technology emerged in the mid-eighties [Andr86]. It was named *Smart Power Technology* (SPT).

Smart power technology ICs serve as an interface between the control logic and a load [Bali91]. They integrate into one chip power devices for regulation of the output power flow, analogue circuitry necessary to drive and protect the power devices, and logic circuitry for communication with a control unit. These functions are implemented using mixed bipolar (analogue), CMOS (logic) and DMOS (power) process. Smart power technology is therefore often addressed as *BCD technology*. SPT devices nowadays penetrate into all areas, where discrete power devices have been used, and they are available for wide range of voltage and current ratings [Bali91]. These devices can be found e.g. in video, telecommunication, multimedia or power supply applications, as well as in the automotive electronics.

Whatever is expected from a smart power IC, in the first place it should be reliable [Mura97]. In addition to an elementary functionality of a device under regular operating conditions, smart power ICs must also withstand potential electrical, thermal or mechanical stress, because they often operate in a severe environment. For example devices installed in the engine compartment of a car can be exposed to temperatures from -40ºC up to 175ºC

and vibrations up to 50g [Berg02]. Designers have to take into account also variety of electrical stresses, which threaten smart power devices during their lifetime [Casi04].

One of the major electrical threats, which a device has to face, is the electrostatic discharge (ESD) [Amer95]. Single high-current short-duration pulse occurring for instance when a charged person touches a pin of an integrated circuit can cause its fatal degradation. This becomes even more critical with the downscaling of characteristic sizes of microelectronic devices, which are more vulnerable to over-voltage and over-current events. It is therefore inevitable to protect ICs against such events. Protection is usually realised by means of special class of devices dedicated to this purpose. In case of power devices the latest trend is to design them as self-protecting, which is solution that saves space on the chip and consequently reduces the production costs.

Apart from the ESD, which in general constitutes hazard to any element of any IC, power elements of the smart power chips can be additionally encountered with situations, which leads to critical operation conditions: short circuit, unclamped inductive switching (UIS), or so-called load dump are few of them. These operating conditions cause excess power dissipation in the device, which should be capable to withstand it until the fault is recognised by control logic and the power supply is switched off.

Semiconductor companies are forced to evaluate robustness of their devices against the above-mentioned stresses. Each new technology generation brings new process steps, which also influence reliability of devices, and therefore testing has to be performed systematically. It is usually electrical and mostly intended for the determination of maximum allowable stress level a device can withstand (e.g. in case of the ESD it is the maximum applicable pre-charge voltage, typically few kV). However, in many cases it is advantageous to reveal internal behaviour of a device under critical operating conditions. This is useful for the understanding of device physics, it helps in the verification of device models, and afterwards shorten time and reduces costs, which is needed to optimise devices for required robustness.

This work presents the results of experimental investigation of internal behaviour of SPT devices studied by means of the Transient Interferometric Mapping (TIM) technique. This technique was presented as powerful tool for investigation of internal device operation under ESD-like operating conditions in the past [Furb00, Poga02c]. It represents a unique possibility of non-invasive and non-contacting mapping of thermal and free carrier dynamics in the semiconductor devices. The main focus of the thesis is placed on the study of ESD phenomenon (time scale in order of hundreds of ns), but the internal device behaviour is studied also in longer time scales (ms).

The thesis is divided into four chapters:

Chapter 1 provides an introduction into the ESD problem. Three standardised ESD models are briefly mentioned, concept of the ESD protection of ICs is introduced, and methods

for testing of the ESD robustness are explained. The reliability issues of power DMOS transistor is shortly introduced too, because a significant part of this thesis is devoted to this device.

Chapter 2 introduces the TIM technique. The principle of TIM is explained together with the physical meaning of measured quantity. The chapter additionally provides description of three TIM set-ups, which were used during the experiments. Technical parameters of these set-ups are given as well as their applicability for investigation of various phenomena. The chapter closes with a short description of two auxiliary optical techniques that were also used.

Chapter 3 provides detailed analysis of internal behaviour of SPT ESD protection devices under two types of ESD stress: HBM- and CDM-like. Electrical and optical experimental techniques were used to study the ESD robustness, homogeneity of the current flow, and locations of hot spots and failures in the devices. Behaviour of the devices under the HBM- and CDM-like stress is compared and differences in the operation of the devices with varied layout are analysed. A 2-dimensional device simulation supports the experimental results.

Chapter 4 is dedicated to the power DMOS transistors and it is divided into two main parts: The first part deals with the investigation of smart power DMOS devices exposed to the ESD-like stress. Experimentally observed inhomogeneous current distribution is explained with a help of 2- and 3-dimensional device simulations. The second part of this chapter presents results of the experimental characterisation of large DMOS transistor in the ms time scale under short-circuit operating conditions. Applicability of the TIM technique for such kind of investigation is studied, and hints for the extraction of physical quantities from the measured one are provided.

1.2 Electrostatic discharge (ESD)

1.2.1 ESD models

When the need to systematically investigate the ESD phenomenon arose in the past, it was foremost necessary to describe different real-world conditions under which such events occur. This led to a specification of three ESD models, which are nowadays used for testing of ESD robustness of semiconductor devices.

Human body model (HBM) describes the situation, when a contact of charged human body with a grounded device causes an electrostatic discharge. Typical HBM discharge waveform is shown in Fig. 1.1: the rise time of the discharge current pulse is about 10 ns,

and the decay time is around 150 ns. The equivalent circuit of this model is shown in Fig. 1.2. It consists from 100 pF charged capacitor C_C, which models the capacity of human body, and from 1.5 kΩ resistor (R_1), which models the skin resistance. The parasitic inductance L_1 determines the rise time of the pulse. Final waveform depends on the parasitic stray capacitance C_S of the discharge resistor R_1 and interconnects (cf. Fig. 1.1).

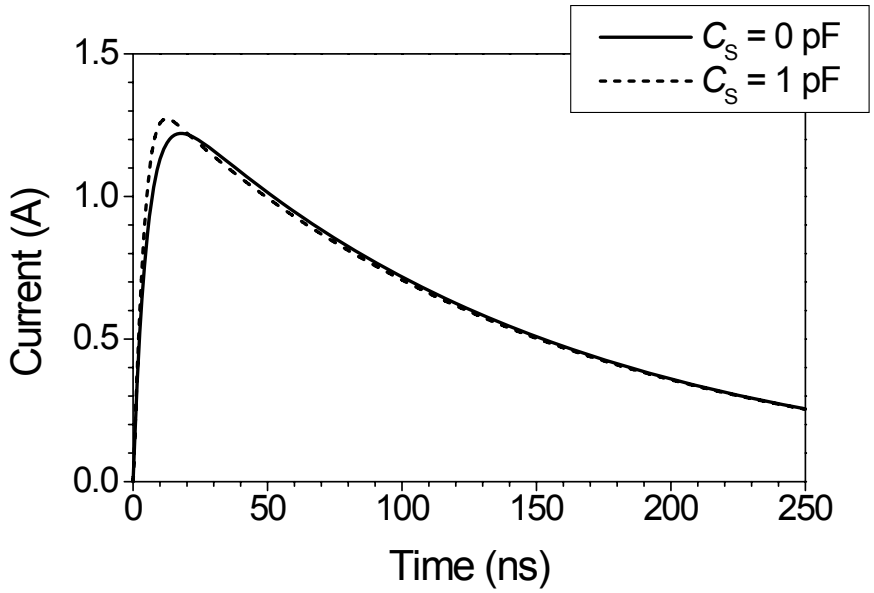


Fig. 1.1: An example of the HBM discharge waveform through 0 Ω load. The charging voltage is 2 kV. The shape of the waveform is influenced by the parasitic element C_s, cf. Fig. 1.2.

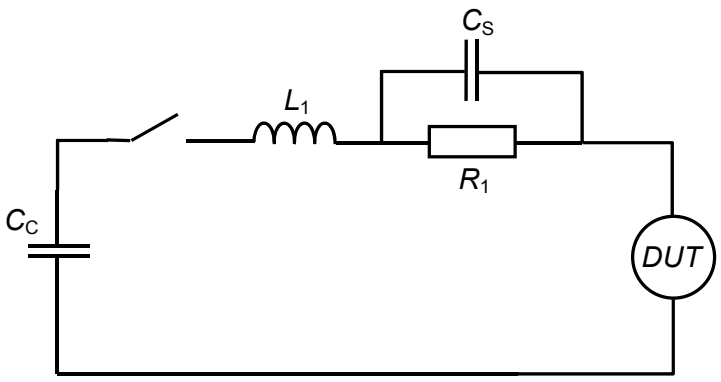


Fig. 1.2: Equivalent circuit for modelling of the HBM and MM discharge waveforms. C_C is the charged capacitance; and R_1 is the resistance of the discharge path. Elements L_1 and C_s are parasitic components, which influence the final waveform of the discharge current as it is shown in Fig. 1.1 and 1.3.

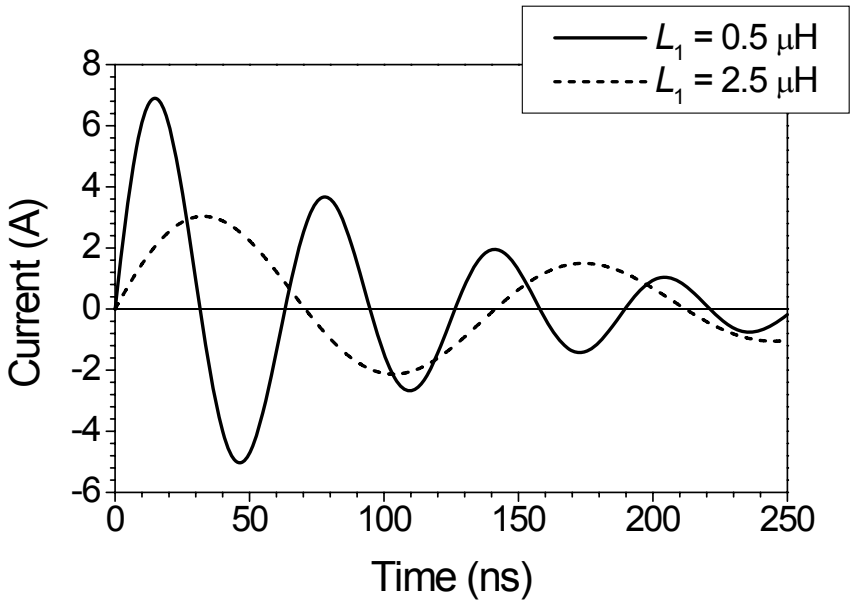


Fig. 1.3: An example of the MM discharge waveform through 0 Ω load. The charging voltage is 400 V. Shape of the waveform is influenced by the parasitic element L_1, cf. Fig. 1.2.

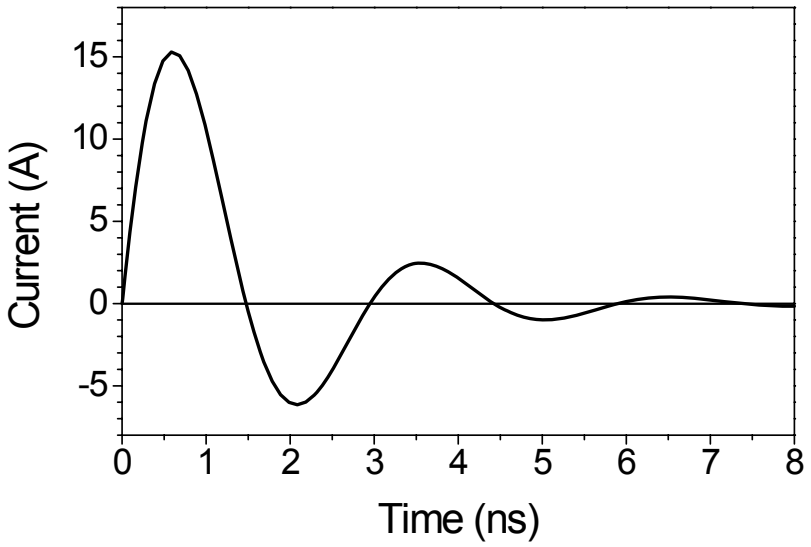


Fig. 1.4: An example of the CDM discharge waveform. The charging voltage is 1 kV.

Machine model (MM) describes discharges with a low-resistance path, such as may occur during mechanical handling of semiconductor devices. The equivalent circuit is a modification of the HBM circuit (Fig. 1.2), with the capacitor C_C of value 200 pF and ideally zero discharging resistance R_1 (in reality $R_1 > 0$). The final waveform of the discharge current, which is shown in Fig. 1.3, again depends on the parasitic components.

Charged device model (CDM) becomes important with increasing fabrication automation. It describes discharge of a charged device to the ground. Device can be charged for instance during a transportation over conveyor belt, and discharged through the metallic arm of a robot touching it. Such ESD event leads to very short (< 10 ns) pulses with short rise time (< 1 ns) and extremely high currents (> 10 A). An example of the CDM discharge waveform is shown in Fig. 1.4.

The HBM and MM events cause excess heat dissipation, and therefore usually induce a thermal damage inside the semiconductor structure, mostly in the pn junctions. The CDM stress is too short to significantly increase temperature in the device. It usually causes the breakdown of gate oxide in an IC. The reason is that the self-inductance and the fast ramp-rate of this type of pulse induce a high voltage drop in the metal interconnects.

1.2.2 ESD protection

The demand to confront with the ESD phenomenon gave rise to a special class of devices dedicated purely to the ESD protection. They protect each pin of an IC as it is schematically shown in Fig. 1.5. Protection devices have two basic functions: to clamp the voltage at the input pin to a level below the gate oxide breakdown, and to limit the current to a level below the damage threshold of the junction being protected. Protection device should be effectively

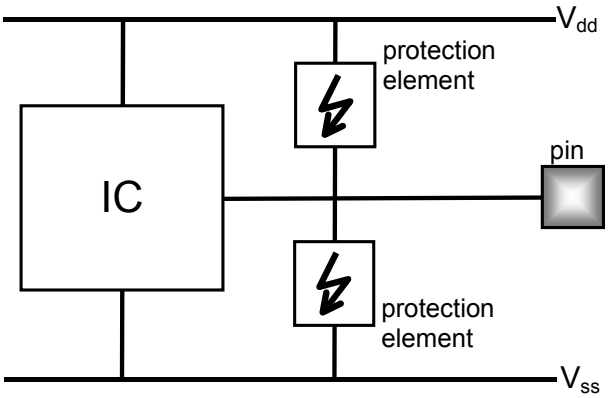


Fig. 1.5: Principal scheme of the ESD protection of an IC.

and fast triggered, when an ESD event occurs. On the other hand, it should be "invisible" during normal operating conditions, i.e. it should not degrade the DC and AC characteristics of the protected IC.

I-V characteristics of the protection element has to fit into the design window between the power supply voltage (lower limit) and the gate oxide breakdown voltage (upper limit), as it is shown in Fig. 1.6. Typically these devices have *S*-shaped I-V characteristics: they are activated at high voltage (V_t – trigger voltage), and once turned-on, they switch into low voltage regime (V_h – holding voltage). The latter limits the heat dissipation in the protection device and thus increases its current handling capability.

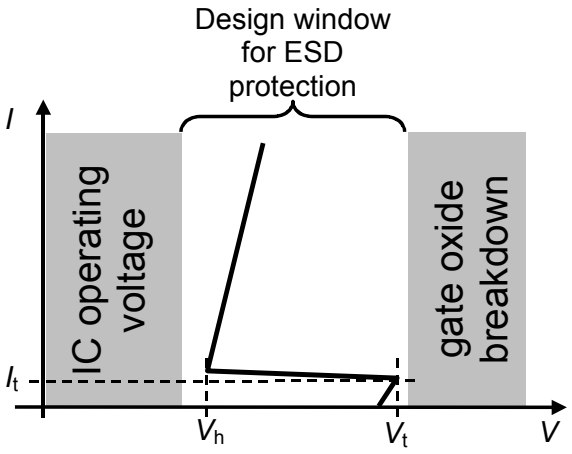


Fig. 1.6: Design window in the I-V plane of an IC, which is used by ESD protection element.

Operating principle of the ESD protection device with the *S*-shaped I-V characteristics can be explained on example of the npn structure, which internal behaviour is in detail investigated in Chapter 3. This device is realised as the lateral npn transistor with short-circuited base and emitter (Fig. 1.7(a)). When a positive voltage is applied to the anode, n^+-collector/p-base junction is reverse-biased. Eventually the breakdown voltage is reached. The impact ionisation starts, and electron-hole pairs are generated in the junction (① in Fig. 1.7(a)). The avalanche current is given by

$$I_{aval} = (M - 1) \cdot I_{in}, \tag{1.1}$$

where I_{in} is the current incident into the high electric field region; and M is the multiplication coefficient described by empirical formula

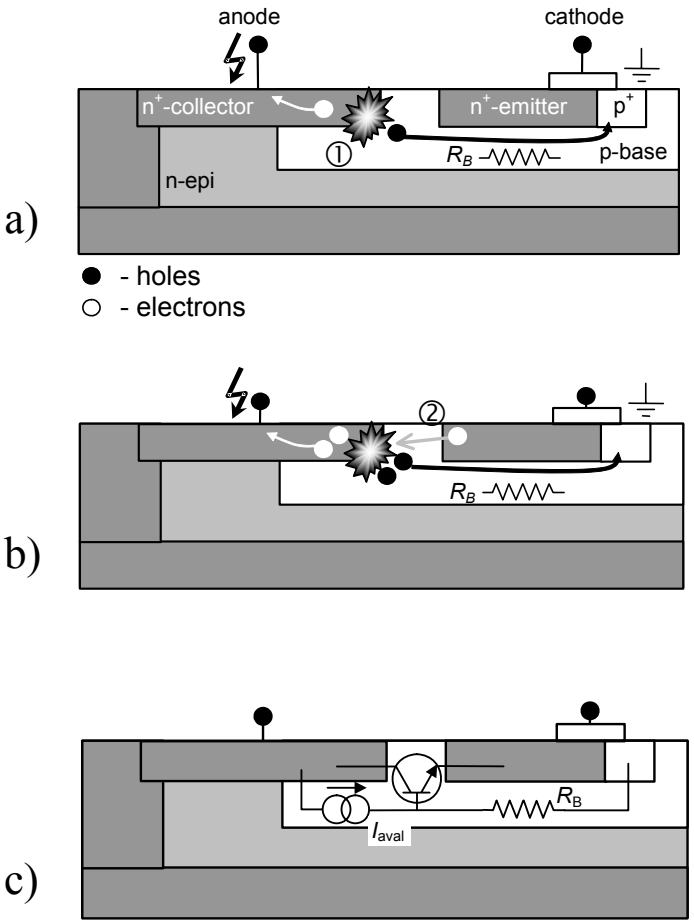


Fig. 1.7: Operating principle of the lateral npn ESD protection device: (a) breakdown; (b) turn-on of the BJT; (c) equivalent circuit of the device.

$$M = \frac{1}{1-\left(\frac{V}{V_{\mathrm{BD}}}\right)^{n}}, \tag{1.2}$$

where V is the voltage applied to the device; V_{BD} is the breakdown voltage; and n is the fitting parameter, which depends in general on the type of considered junction. At this moment I_{in} is only composed of the junction saturation current I_{C0}. The multiplication coefficient M is large, because $I_{\mathrm{aval}} = I_{\mathrm{ESD}}$ (the ESD stress current).

The electrons generated by impact ionisation are attracted towards the n^+-collector (anode), and generated holes flow through the p-base toward the p^+ cathode contact. Resistance of the p-base region R_{B} is non-zero, and the hole current I_{h} causes a voltage drop, which starts to forward-bias the p-base/n^+-emitter junction:

$$V_{BE} = I_h \cdot R_B. \tag{1.3}$$

If the hole current reaches certain level, the junction is opened, and the emitter starts to inject electrons into the base (② in Fig. 1.7(b)). This is the moment, when the bipolar npn transistor is turned on. The electrons injected from the emitter and flowing to the collector contribute to the impact ionisation in the avalanching collector junction and I_{in} becomes

$$I_{in} = I_C \approx I_{C0} \cdot \exp(V_{BE}/V_T), \tag{1.4}$$

where I_C is the bipolar collector current; and $V_T = kT/q$ is the thermal voltage. Therefore

$$I_{aval} = (M - 1) \cdot I_C. \tag{1.5}$$

Thus, to sustain the same total ESD current, the multiplication coefficient M of the impact ionisation can be decreased. This leads to a sudden drop of the voltage at the device (from V_t to V_h, cf. Fig. 1.6), which is observed in the I-V characteristics. This effect is called *snapback*. After the snapback device operates in the low voltage, high current regime, with roughly constant differential resistance. The latter is mainly determined by the series resistance of involved device regions.

Fig. 1.7(c) shows a simple equivalent circuit of the ESD protection device [Amer96, Lim97]: current source I_{aval} represents the current generated in the avalanching n^+-collector/p-base junction.

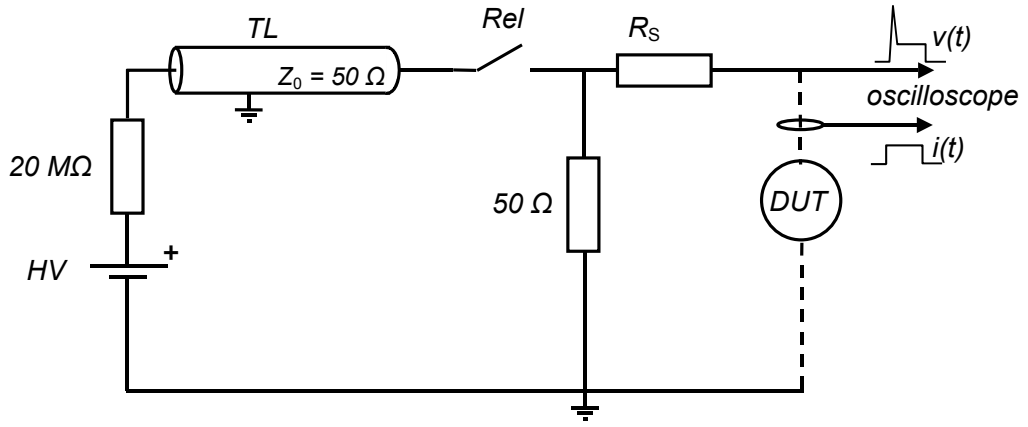
1.2.3 ESD testing

Commercially available ESD testers, generally based on the equivalent circuits of the ESD models (cf. section 1.2.1), are usually employed for ESD testing. Besides them the Transmission Line Pulse (TLP) technique [Malo85] and the very-fast Transmission Line Pulse (vf-TLP) technique [Gies98] are often utilised in the HBM and CDM time domains, respectively. These two techniques provide rectangular pulse stressing with appropriate rise time and duration, and into some extent emulate the real life ESD stress. They are also used in the experimental investigations presented in this thesis.

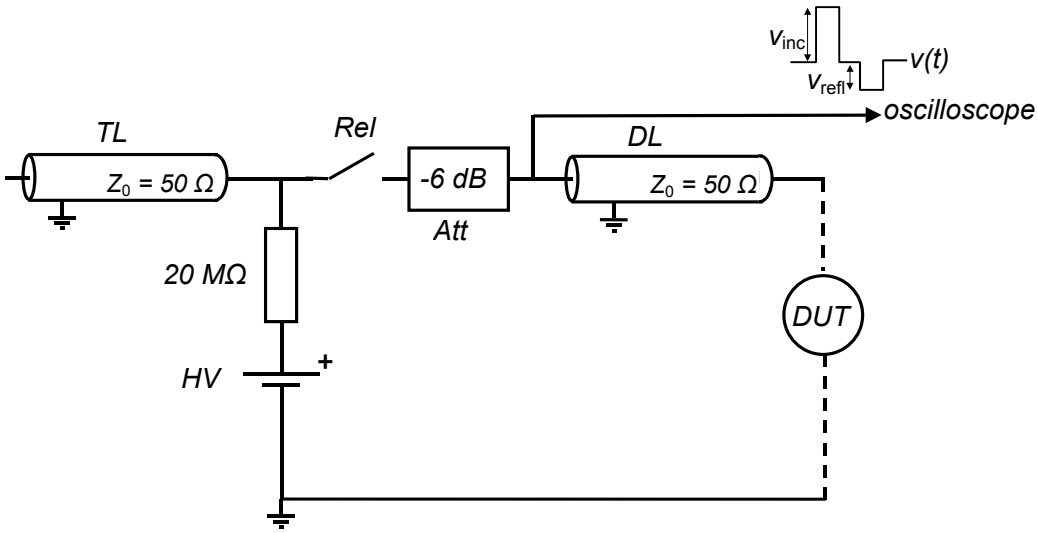
Fig. 1.8 shows the principal scheme of the TLP and vf-TLP set-ups. In both cases the output pulse is generated by discharge of a charged transmission line (*TL*). The length of the output pulse t_p is set by the length of the transmission line: $t_p = 2l_{TL}/v$, where l_{TL}

is the length of the transmission line; and v is the speed of electromagnetic wave propagating in the *TL*. Typically 100 ns TLP pulses are used for the HBM-like testing and up to 10 ns vf-TLP pulses are used for the CDM-like testing.

The TLP operates in the constant current regime. This is achieved by appropriate choice of the series resistance R_S (Fig. 1.8(a)), which guarantees that voltage at the device under test



a)



b)

Fig. 1.8: Principal scheme of (a) the constant current transmission line pulser (TLP); and (b) the constant impedance very-fast TLP (vf-TLP): *HV* is the high-voltage source; *TL* is the transmission line; *Rel* is the relay switch; R_S is the voltage to current transformer; *DUT* is the device under test; *v(t)* and *i(t)* are the voltage and current probes, respectively; *Att* is the attenuator; and *DL* is the delay line.

(*DUT*) is much smaller than the voltage at R_S. In such case the output current level can be calculated as

$$I_{TLP} \approx \frac{1}{2}\frac{V_{charge}}{R_S}. \tag{1.6}$$

The 50 Ω resistor serves as matching for the transmission line to avoid the back reflections. Voltage and current probes are used to monitor respective quantities on the oscilloscope.

The current source TLP output pulse is distorted during the first few nanoseconds because of reflections from parasitics, which are introduced e.g. by current and voltage probes. This is the reason, why the constant current TLP is not suitable for investigation in the CDM time domain. The vf-TLP set-up intended for such type of investigation is therefore designed to be 50-Ω matched. It is based on the principle of time domain reflectometry. The stress pulse propagates towards the *DUT* where it is partially absorbed and partially reflected. The actual voltage and current at *DUT* can be calculated from the amplitudes of the incident and reflected pulses, which are separated in time by the delay line *DL* (Fig. 1.8(b)):

$$V_{DUT} = aV_{inc} + \frac{1}{a}V_{refl}, \tag{1.7a}$$

$$I_{DUT} = \frac{aV_{inc} - \frac{V_{refl}}{a}}{Z_0}, \tag{1.7b}$$

where V_{inc} and V_{refl} are incident and reflected pulses measured by the voltage probe, respectively; a is the attenuation of the delay line; and Z_0 is the characteristic impedance of the system (50 Ω). Accurate estimation of the delay line attenuation a is necessary for the precise determination of the V_{DUT} and I_{DUT}. The 6 dB attenuator (*Att*, Fig. 1.8(b)) is placed between *TL* and *DL* to suppress repeated stressing of the *DUT* due to multiple reflections.

Although the CDM testing cannot be directly substituted by the vf-TLP one [Gies98, Stad03], and there still exists a controversy, whether the results obtained by the TLP correlate with the HBM testing [Muss96, Bart00, Stad97, Note98], both TLP and vf-TLP enables investigation of devices under reproducible conditions. These techniques allow construction of the high current I-V characteristics, determination of failure thresholds and together with failure analysis techniques provide valuable information about the weak points of investigated device.

1.3 Smart power DMOS

Double-diffused MOS (DMOS) transistor is the power MOSFET [Bali96a]. It is the most common power device used in low voltage (< 100 V) applications nowadays [Bali96b]. Power MOSFETs have replaced power bipolar transistors in the past, because they offer several advantages: higher switching speed, no DC driving current consumption, and thermally stable operation in a wide interval of drain currents are the most important ones [Mura96]. Consequently, the DMOS has been chosen as the power device for the Smart Power Technology ICs.

Fig. 1.9 shows the cross-sections of two basic n-channel DMOS devices designed within the SPT process: vertical DMOS (VDMOS, Fig. 1.9(a)) and lateral DMOS (LDMOS, Fig. 1.9(b)). It has to be mentioned at this place that the layout of an SPT IC is influenced by requirement to electrically isolate individual devices on the chip. This is inevitable to avoid any unwelcome crosstalk between different parts of the IC, e.g. from the power device (DMOS) to the control logic circuits (CMOS). Usual solution of the problem is junction isolation, which is also the case of devices studied in the present work. Another possibility is the silicon on insulator (*SOI*) process [Mura96]. The smart power technology process utilising junction isolation starts with a p-doped substrate, into which highly doped n^+-buried layer and p^+-bottom isolation are implanted. Afterwards a low doped n-epitaxial layer (n-epi) is grown, where a p^+-top isolation is implanted, and an n^+-sinker contacting the buried layer is realised. Thereafter the DMOS block is processed: The p-body and n^+-source regions of the device are diffused to the n-epi self-aligned through the gate-polysilicon openings. The channel length results from the differential out-diffusion of the p- and n-dopants. This process is origin of the name "*double-diffused*". Note also that the channel length is independent of the lithography process accuracy. The p-body and n^+-source are short-circuited to establish a fixed potential of the p-body region during device operation. The main distinction between the VDMOS and LDMOS devices is in the current flow path. In the VDMOS the buried layer serves as drain and the electron current flows vertically through the epi layer (grey arrow in Fig. 1.9(a)). On the other hand in the LDMOS the drain is realised by shallow n^+-region and current flows laterally along the silicon top surface (grey arrows in Fig. 1.9(b)).

The presented structures of the power DMOS transistor are the very basic ones, and there exist variety of improved concepts of the transistor, which uses RESURF principle or trenches. These are summarised e.g. in [Deni04a].

The most important characteristics of the DMOS transistor are voltage-blocking capability and on-resistance. When the device is off, i.e. the gate-to-source voltage is smaller

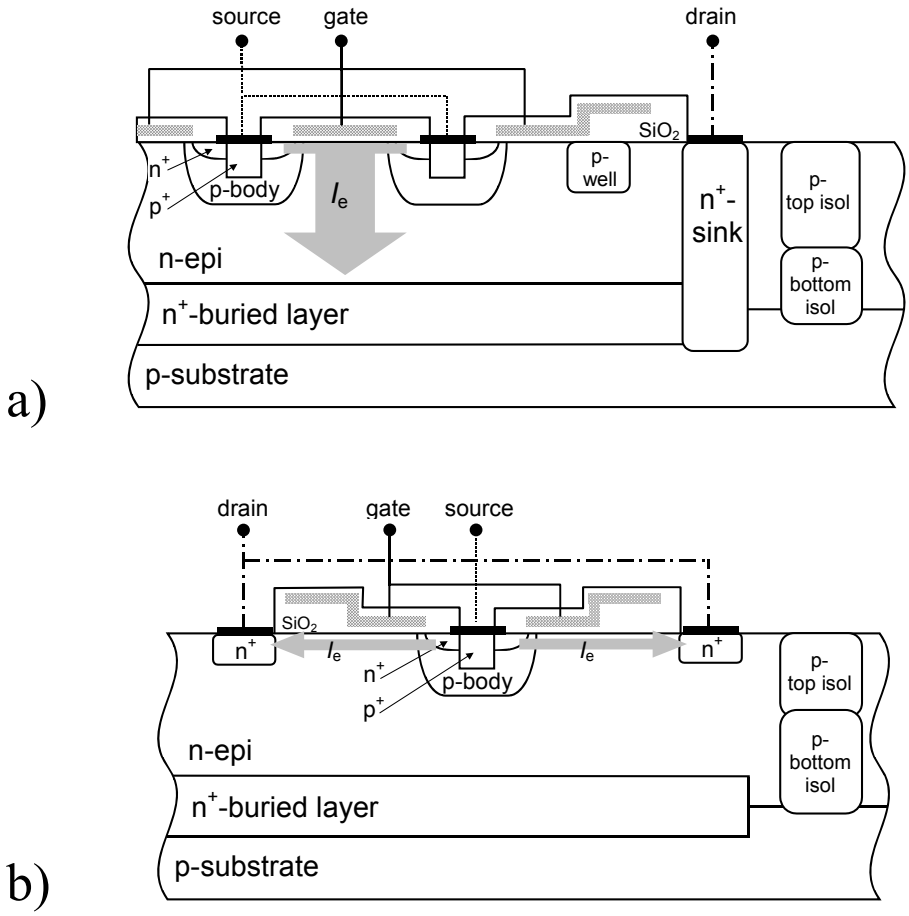


Fig. 1.9: Principal cross sections of SPT DMOS transistors: (a) vertical and (b) lateral. The displayed devices are n-channel ones. The electron current flow paths are also indicated.

than the threshold voltage ($V_{GS} < V_{TH}$), the drain-to-source voltage V_{DS} is supported by the reverse biased n-epi/p-body junction. To achieve high breakdown voltage, doping of the n-epi layer has to be low. However, resistance of this layer substantially influences the on-resistance of device, which is desired to be as small as possible. From such point of view it is beneficial to increase the n-epi doping. It is one of the main goals of the DMOS design to handle this trade-off between the breakdown voltage and on-resistance as well as to optimise the DMOS layout with respect to these parameters [Char96, Efla97, Mora97, Plik97, Kim01].

Another important characteristic of the DMOS is so-called *Safe Operating Area* (SOA). This term defines an interval of the drain current I_{DS} and drain-to-source voltage V_{DS}, where the device can operate without suffering damage [Howe02]. As an ultimate operating limit of the DMOS is usually taken the turn-on of the parasitic bipolar transistor inherent in any MOSFET device [Yilm89]. This transistor is formed by the source (emitter)/body (base)/drain (collector) structure. It is turned on, when a sufficient

voltage develops across the body/source (= base/emitter) junction. The junction is forward biased due to a current flow through the body region. This current can be supplied by impact ionisation, thermal generation, or it is the displacement current in case a voltage pulse with high rise-time is applied to the drain (so-called *dV/dt-triggering* [Bali96a]).

Depending on the mechanism, which dominantly controls the device operation, one can distinguish between *electrical* SOA and *thermal* SOA:

ESD pulse runs DMOS transistor into the avalanche breakdown and activity of the parasitic BJT is controlled by the impact ionisation. DMOS device sensitivity to the ESD is therefore determined by its electrical SOA. The triggering of the parasitic BJT is in this case basically the same process as the one described for the npn ESD protection device in chapter 1.2.2. However, when the DMOS gate is biased, I_{DS} provides additional carriers into the avalanching region and Eq. (1.5) in general extends into a form

$$I_{aval} = (M - 1)(I_C + I_{DS}), \tag{1.8}$$

which could lead to the reduction of parasitic BJT triggering voltage V_t. Nevertheless, this effect takes place only if the I_{DS} path crosses the high electric field region [Merg00].

There are several approaches how to protect DMOS device against ESD:

- by external protection device, e.g. SCR parallel with the device [Duvv94];
- using Zener diodes clamp, which provides the gate bias to open the channel [Duvv97, Mene00];
- the device is intended to be self-protecting [Part02, Kawa02, Deni04b]. This approach requires knowledge of the physical effects, which governs behaviour of the device during an ESD event.

The turn-on of the parasitic BJT in the self-protected DMOS transistor leads to an electrical instability related to the existence of the negative differential resistance (NDR) region in the I-V characteristic. This instability can induce a strongly inhomogeneous current flow [Howe01, Stei03, Deni04b]. In case of the LDMOS devices, the snapback is often destructive [Bess02]. This originates from the triggering of the lateral npn structure accompanied by formation of the high electric field region at the Si/SiO_2 interface, where a thermal degradation takes place soon [Bess02]. On the other hand VDMOS have proved to be more robust against ESD, because in this case the high electric field region is localised in the bulk [Deni04b, Moen04].

The thermal SOA of DMOS transistors becomes more important and consequently gets more into the field of view of device designers in recent years, when the downscaling of the devices led to a growth of the power dissipation density. Significant rise of temperature

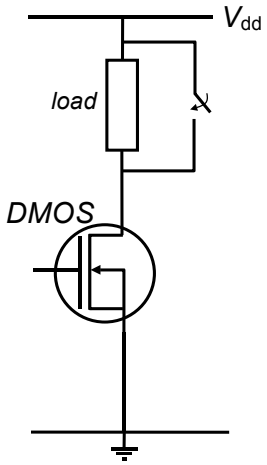


Fig. 1.10: Circuit representation of the DMOS transistor operation with short-circuited load.

in the device, which is caused by self-heating during high energy pulses, can alone induce a failure of the device. An example of such high energy stress is the short circuit operation, when the whole power supply voltage appears on the DMOS (Fig. 1.10). However, it is important to note that the thermal SOA is not inevitably linked with the turn-on of the parasitic BJT [Deni04a].

The DMOS thermal SOA is considerably affected by the operating point dependent power distribution [Breg99, Deni04c]. Fig. 1.11 demonstrates dependence of the DMOS transfer characteristic on temperature. While at higher gate voltages the drain current decreases with increasing temperature (temperature coefficient of I_{DS} is negative), at small gate voltages total drain current increases with increasing temperature (temperature coefficient of I_{DS} is positive). This behaviour is caused by two competing mechanisms, which affect the device operation at elevated temperatures [Doln92].

The first mechanism is a decrease of the free-carriers mobility with increasing temperature according to the formula [Doln92]

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-2.5}. \tag{1.9}$$

This effect is dominant at high current regime and leads to a homogenisation of current flow in the device, thus making its operation thermally stable.

The second mechanism is a decrease of the threshold voltage V_{TH} with increasing temperature. V_{TH} of MOS transistor is given by:

$$V_{TH} = \phi_{ms} + 2\phi_f + \frac{\sqrt{4\varepsilon q N_{max}\phi_f}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}, \tag{1.10}$$

where ϕ_{MS} is the work function difference between metal and semiconductor; ϕ_f is Fermi potential; ε is the semiconductor permitivity; N_{max} is maximum net doping concentration of the p-body region; C_{ox} is the gate oxide capacity; and Q_{ox} is the charge trapped in the gate oxide. The temperature dependence of Eq. (1.10) comes mostly from the temperature dependence of Fermi potential:

$$\phi_f = \frac{kT}{q}\ln\left(\frac{N}{n_i(T)}\right), \tag{1.11}$$

where k is Boltzman constant and n_i is the intrinsic concentration. The effect of the threshold voltage decrease with increasing temperature is dominant at small gate and high drain voltage regime, and it leads to a thermally unstable operation, which could limit the thermal SOA [Breg99, Cons99, Spirit02, Deni04c].

When the two effects mentioned above are compensated, the drain current of the DMOS is temperature independent. This point is called *temperature compensation point* (TCP).

In summary it is therefore of great interest to follow the dynamics of power dissipation distribution and temperature rise in the DMOS transistor in order to understand effects limiting its thermal SOA.

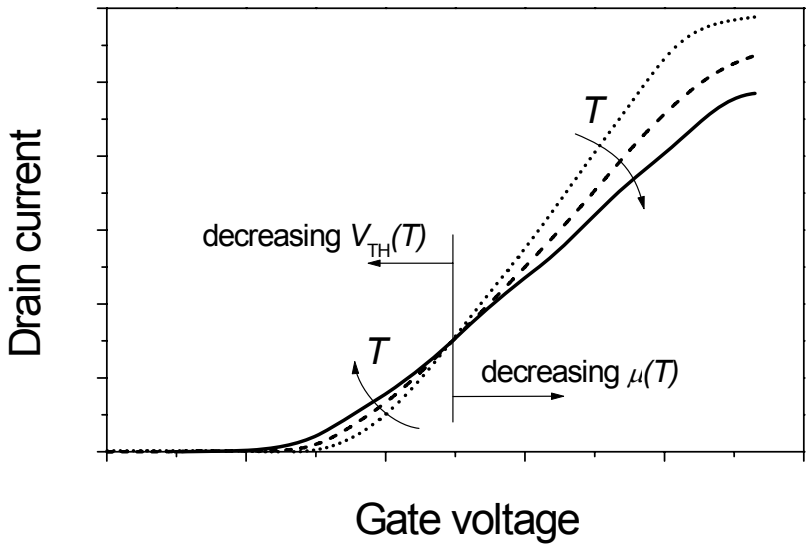


Fig. 1.11: Dependence of the DMOS transfer characteristics on the temperature.

Chapter 2

Experimental Technique

2.1 Transient interferometric mapping technique

2.1.1 Operating principle

The transient interferometric mapping (TIM) technique is based on a probing of localised variation of the refractive index n due to a temperature change [Bert90, Stur92] and/or a change in the free-carrier concentration [Sore87, Schr78]. The refractive index changes are probed by a laser beam and they are detected as a phase shift using an interferometer.

In the interferometer the laser beam is split into reference and probe branches. The probe beam, which propagates in the probe branch, enters the investigated device from the backside, and it is reflected by top metal (Fig. 2.1). Its phase profile is modified due to a spatial and time variation of the refractive index $\Delta n(x,y,z,t)$ caused by electrical stress. The reflected probe beam interferes with the reference beam, which propagates in the reference branch and which is reflected by the reference mirror. Optical detector detects the resulting interference signal. Any phase shift introduced into the probe beam is hence transferred into an intensity change of the detector signal.

The operating principle of the TIM technique requires the probing laser beam not to be absorbed in the sample. Wavelength of the laser source used for investigation of silicon devices is therefore chosen to be around 1.3 μm, which is beyond absorption edge of the silicon. This choice is also determined by availability of laser sources.

The measured phase shift $\Delta\varphi$ is given by [Seli97]

$$\Delta\varphi(x,y,t) = 2 \cdot \frac{2\pi}{\lambda} \int_0^l \Delta n(x,y,z,t)\,dz\,, \tag{2.1}$$

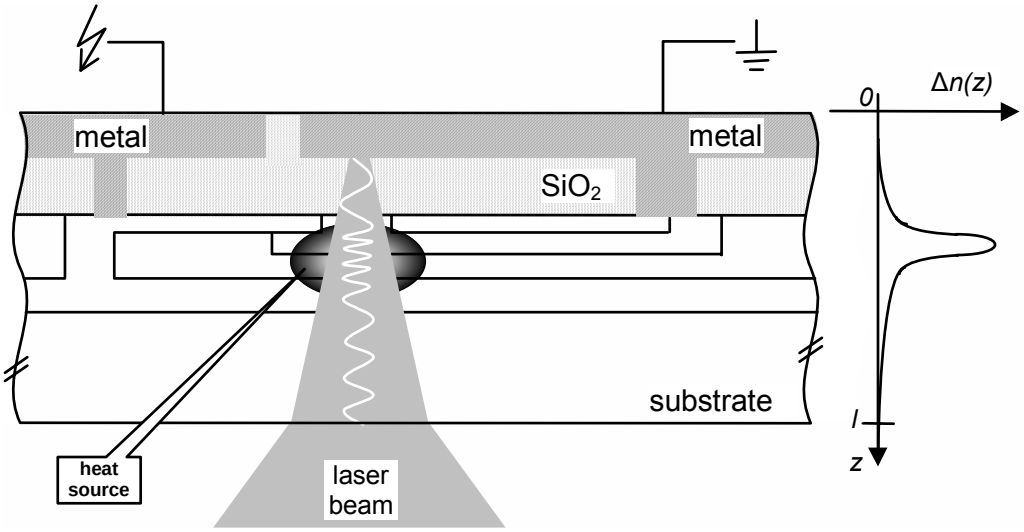


Fig. 2.1: Operating principle of the transient interferometric mapping technique: self-heating in the investigated structure gives rise to a local variation of the refractive index in the hot area (see the $\Delta n(z)$ distribution along the probe beam path on the right hand side of the figure). This causes a phase modulation of the probing laser beam.

where λ is the free-space wavelength of the laser beam; l is the thickness of semiconductor substrate; and $\Delta n(x,y,z,t) = n(x,y,z,t)-n_0(x,y,z,t)$ is the local change of refractive index from its initial value $n_0(x,y,z,t)$ when *DUT* in not stressed, to a new value $n(x,y,z,t)$ when *DUT* is under electrical stress.

The total refractive index change $\Delta n(x,y,z,t)$ can be in the first approximation divided into thermal (Δn_{th}) and free carrier (Δn_{fc}) contributions:

$$\Delta n(x,y,z,t) = \Delta n_{th}(x,y,z,t) + \Delta n_{fc}(x,y,z,t). \tag{2.2}$$

Thermally induced change of refractive index can be expressed using the thermo-optical coefficient dn/dT, which is positive and for silicon in the first approach temperature independent:

$$\Delta n_{th}(x,y,z,t) = \frac{dn}{dT}\Delta T(x,y,z,t) \tag{2.3}$$

The value of dn/dT for silicon is approximately 1.9×10^{-4} K^{-1} for 1.3 μm wavelength [MCau94].

Free-carrier induced refractive index change is negative for increasing concentration, and it can be expressed as the sum of electron ($\Delta n_{fc,e}$) and hole ($\Delta n_{fc,h}$) contributions

$$\begin{aligned}\Delta n_{fc}(x,y,z,t) &= \Delta n_{fc,e}(x,y,z,t) + \Delta n_{fc,h}(x,y,z,t) = \\ &= k_e\left[N_e^{\alpha}(x,y,z,t) - N_{e0}^{\alpha}(x,y,z,t)\right] + k_h\left[N_h^{\beta}(x,y,z,t) - N_{h0}^{\beta}(x,y,z,t)\right]\end{aligned} \tag{2.4}$$

where $N_e(x,y,z,t)$ and $N_h(x,y,z,t)$ are the electron and hole concentrations during electrical stress, and $N_{e0}(x,y,z,t)$, $N_{h0}(x,y,z,t)$ are the corresponding quantities in the steady state conditions. The parameters k_e, k_h, α and β are coefficients obtained from the fitting of experimental data [Sore87].

2.1.2 Extraction of physical quantities from the phase shift

From the Eqs. (2.1) and (2.2) follows that the total phase shift can be calculated as

$$\Delta\varphi(x,y,t) = \Delta\varphi_{th}(x,y,t) + \Delta\varphi_{fc}(x,y,t), \tag{2.5}$$

where $\Delta\varphi_{th}(x,y,t)$ and $\Delta\varphi_{fc}(x,y,t)$ are the thermal and free carrier components of the total phase shift, respectively. The latter one can be sometimes neglected, especially when high power is dissipated in the investigated device or in case of longer time scales. If also temperature independent thermo-optical coefficient *dn/dT* and volume specific heat c_v is assumed, the phase shift $\Delta\varphi$ is found to be directly proportional to the *2*-dimensional energy density E_{2D} stored inside the semiconductor [Poga02a], which can be written in a form:

$$E_{2D}(x,y,t) = \frac{\lambda c_v}{4\pi}\frac{1}{\dfrac{dn}{dT}}\Delta\varphi(x,y,t) \approx 0.88\cdot\Delta\varphi(x,y,t)\ \text{[nJ.µm}^{-2}\text{]}. \tag{2.6}$$

The temperature induced phase shift is a memory quantity, i.e. it reflects the complete history of power dissipation in a device, not the instantaneous one. Hence, all experimental results have to be carefully analysed to uncover any possible dynamic changes in the heat dissipation. It is therefore advantageous to extract the instantaneous *2*-dimensional power dissipation density P_{2D} from the phase shift [Poga02b]:

$$P_{2D}(x,y,t) = \frac{\lambda}{4\pi \frac{dn}{dT}} \left\{ c_v \frac{\partial \Delta\varphi(x,y,t)}{\partial t} - \kappa \left[\frac{\partial^2 \Delta\varphi(x,y,t)}{\partial x^2} + \frac{\partial^2 \Delta\varphi(x,y,t)}{\partial y^2} \right] \right\} + j_{th,z}(x,y,0,t), \quad (2.7)$$

where κ is the temperature independent heat conductivity, and $j_{th,z}(x,y,0,t)$ is the normal component of the heat flow density vector at the device top surface. The latter represents the thermal power transferred from silicon to top device layers and it can be in some cases neglected.

2.1.3 Experimental set-ups for Transient Interferometric Mapping

Following part provides a brief description of three set-ups, which were used for transient interferometric mapping within the frame of this work.

2.1.3.1 Dual beam Michelson interferometric set-up

Dual-beam Michelson interferometric set-up [Dube03] provides information about the time evolution of the phase shift at two places on a *DUT*.

Fig. 2.2 shows the set-up schema. It is a combination of two independent Michelson interferometers. Two DFB laser diodes (*LD1*, *LD2*) generate linearly polarised light beams of 1.3 μm wavelength. The laser beams are split to the reference and probe beams by two beam-splitters (*BS1* and *BS2*). The probe beams are focused onto different locations of the *DUT* by a microscope objective (*MO*). The laser beam positions on the *DUT* can be visualised using an IR *vidicon camera* and the distance between them can be changed by rotation of the mirror *M3*. Minimum laser spot diameter is about 2 μm, which determines maximum space resolution. Reference mirrors *M1* and *M2* mounted on piezo-controlled *x*-stages allow precise adjustment of the reference branches lengths for maximum sensitivity. Interference signals from respective interferometers are detected by two InGaAs photo-detectors (*DET1*, *DET2*) with 1 GHz bandwidth. The detectors are chosen as a compromise between the large bandwidth and acceptable signal-to-noise ratio. Time resolution of the set-up is 0.4 ns. Output signal from the detectors is measured by a fast digital oscilloscope.

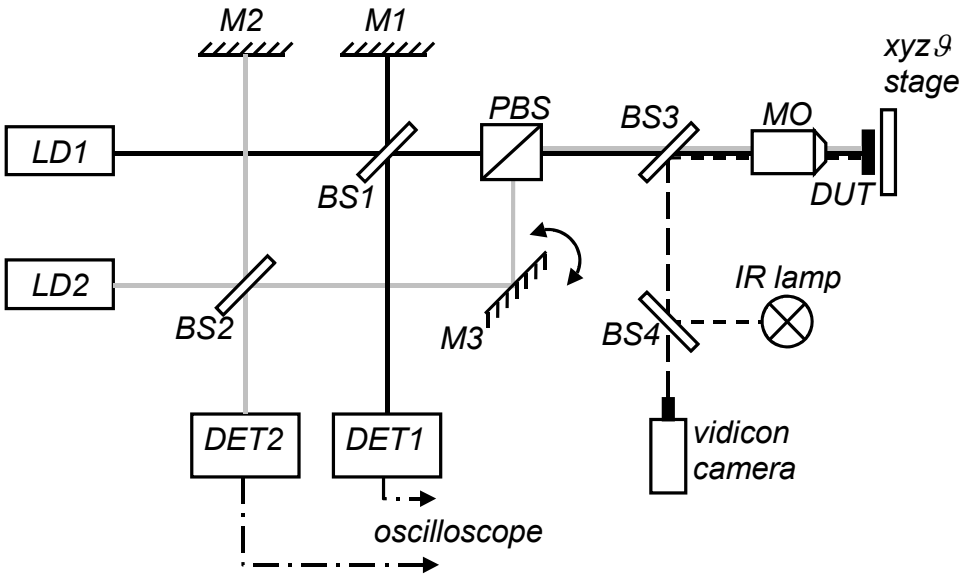


Fig. 2.2: Schematic diagram of the dual-beam Michelson interferometric set-up: *LD1* and *LD2* are the laser diodes; *M1* and *M2* are the reference mirrors; *BS1 – BS4* are the beam splitters; *DET1* and *DET2* are the optical detectors; *PBS* is the polarising beam splitter; *M3* is the mirror for adjustment of laser beam separation on the *DUT*; and *MO* is the microscope objective.

When an electrical stress is applied to the *DUT* and a refractive index change occurs at the position probed by the laser beam, a sinusoidal signal *s(t)* is measured. It can be generally expressed as

$$s(t) = B(t)\, sin[\Delta\varphi(t) + \varphi_0], \tag{2.8}$$

where *B(t)* is the amplitude of the sinusoidal signal; $\Delta\varphi$ is the phase shift due to electrical stress; and φ_0 is set by the reference mirror. No DC component is present in the measured signal, because AC output of the detector is used. The phase shift is not large in most cases ($\Delta\varphi < \pi/4$), therefore the working point of the interferometer is usually adjusted to a "half-fringe" ($\varphi_0 = 0$), where the sensitivity to the optical path changes is the highest. The absolute phase shift can be then calculated as

$$\Delta\varphi = \arcsin\left(\frac{S}{A}\right) \approx \frac{S}{A}, \tag{2.9}$$

where the meaning of the symbols is clear from Fig. 2.3. To improve the signal to noise ratio, averaging over several pulses is used, if the signal is reproducible.

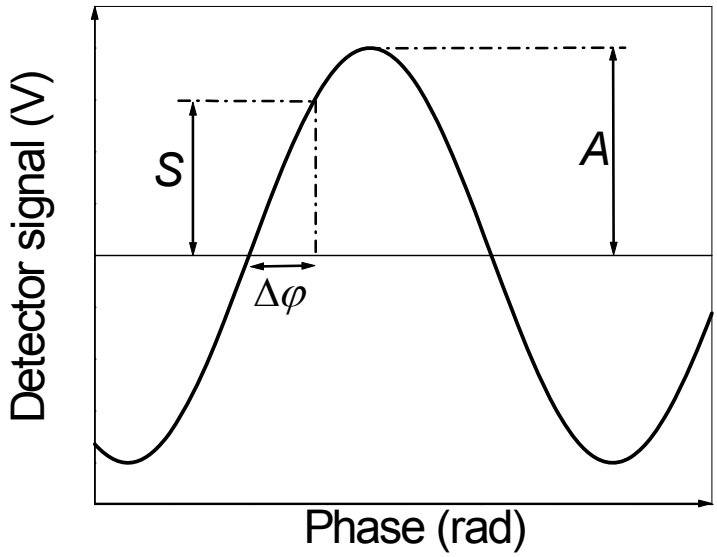


Fig. 2.3: Detector signal vs. phase shift dependence in the dual-beam Michelson interferometric set-up.

Because of good time resolution, the set-up is applied for investigations of very fast transients, e.g. for investigation of trigger delays in ESD protection devices under vf-TLP stress [Bych03]. The employment of two laser beams also enables simultaneous investigation of activity at two different places on a device.

2.1.3.2 Scanning heterodyne interferometric set-up

Scanning heterodyne interferometric set-up [Furb98] provides information about the time evolution of phase shift at certain position alike the previous set-up, but the present one additionally allows automatic scanning for investigation of the phase shift distribution along *x* and/or *y* direction.

Fig. 2.4 shows two utilised configurations of the set-up: so-called "slow" (Fig. 2.4(a)) and "fast" (Fig. 2.4(b)). They differ in the time resolution and signal-to-noise ratio parameters (cf. Table 2.1). Laser beam of 1.3 μm wavelength is generated by a DFB laser diode (*LD*). It is split into the probe and reference beams by an acoustic optic modulator (*AOM*), which is driven by one ("fast" configuration) or two ("slow" configuration) frequency generators (ω_1, ω_2).

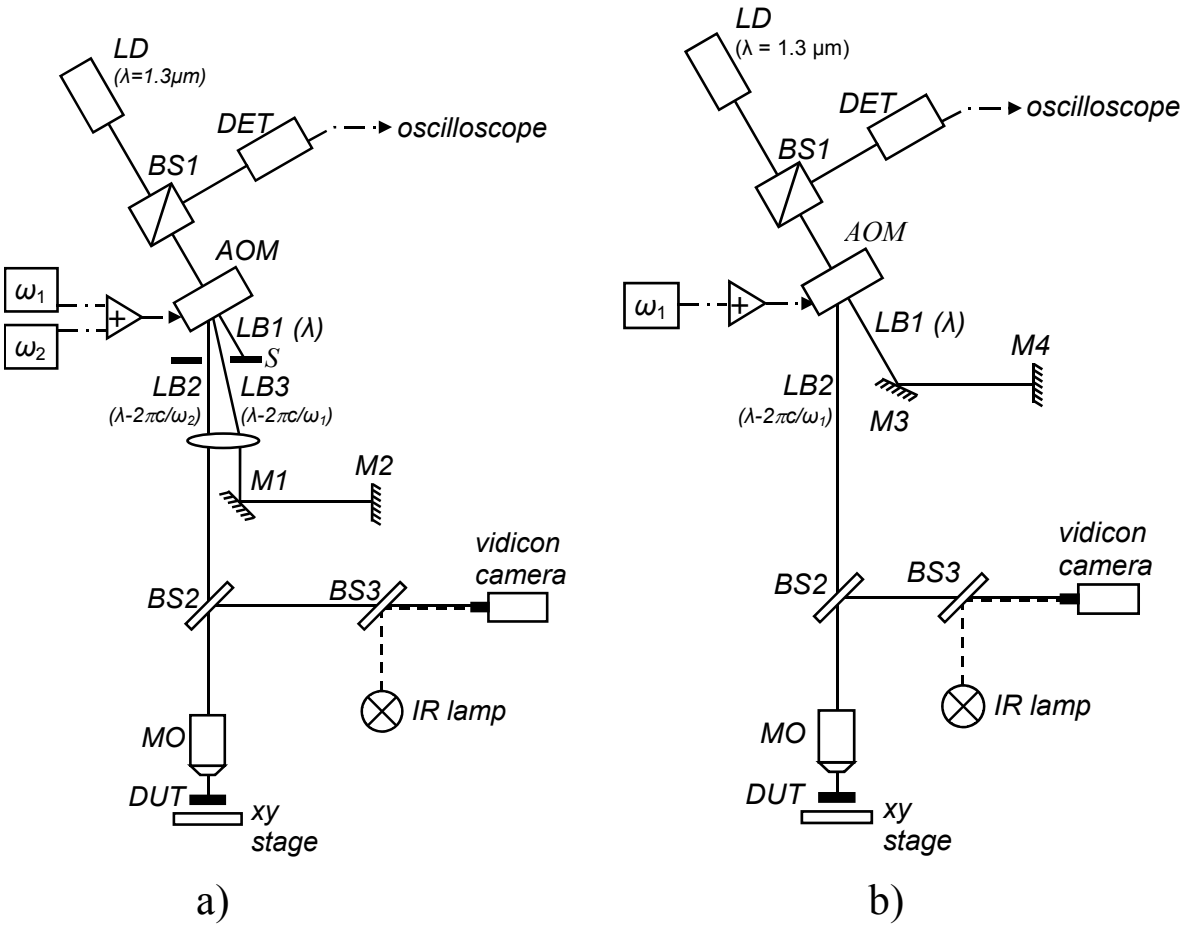


Fig. 2.4: Schematic diagram of the scanning heterodyne interferometric set-up used for TIM: (a) "slow" configuration; and (b) "fast" configuration: *LD* is the laser diode; *DET* is the photodetector; *BS1 – BS3* are the beam splitters; *AOM* is the acoustic optic modulator; ω_1 and ω_2 are the frequency generators; *LB1 – LB3* are the refracted laser beams; *S* is the slit; *M1 – M4* are the mirrors; *MO* is the microscope objective and *DUT* is the device under test.

Besides splitting, the AOM also shifts the frequency of refracted beam(s). The reflected probe and reference beams interfere in the photo-detector (*DET*). The detector output signal, which is measured by an oscilloscope, is the heterodyne beat signal, and can be expressed as

$$s(t) = s_{\mathrm{r}}(t) + s_{\mathrm{p}}(t) + s_{\mathrm{d}}(t) + 2\sqrt{s_{\mathrm{r}}(t)s_{\mathrm{p}}(t)} \cdot \cos\left(2\Delta\omega t + \Delta\varphi(t)\right), \tag{2.10}$$

where $s_{\mathrm{r}}(t)$, $s_{\mathrm{p}}(t)$ and $s_{\mathrm{d}}(t)$ are the time dependent amplitudes of the reference beam, probe beam and possible signal disturbances, respectively; $2\Delta\omega$ is the beating frequency; and $\Delta\varphi(t)$ is the phase shift due to electrical stress. The beating frequency is given by the difference in frequencies of the reference and probe beam:

- for “slow” configuration: $2\Delta\omega = 2(\omega_1 - \omega_2)$,
- for “fast” configuration: $2\Delta\omega = 2\omega_1$,

where ω_1 and ω_2 are the frequencies of the signals that drive the *AOM*. The beating frequency is higher in case of the “fast” configuration, and consequently a faster photo-detector is used. This brings the advantage of better time resolution, however this configuration suffers worse signal-to-noise ratio. Important parameters of both variations of the set-up are summarised in Table 2.1:

	SET-UP CONFIGURATION	
	“slow” (Fig. 2.4a)	“fast” (Fig. 2.4b)
beating frequency	6 MHz	137 MHz
detector bandwidth	28 MHz	198 MHz
time resolution	15 ns	3 ns
space resolution	1.5 μm	1.5 μm
S/N –ratio	~ 60	~ 14

Table 2.1: Technical parameters of the two variations of the scanning heterodyne interferometric set-up

When long pulses (in μs – ms time scale) are applied to the *DUT*, the “slow” configuration of set-up is used, and the detector signal is first mixed with a local oscillator to mix down the beating signal frequency. Only then is the mixer output signal measured by the oscilloscope:

$$s(t) = s_0 \cos\left[(2\Delta\omega - \omega_{LO})t + \Delta\varphi + \varphi_{LO}\right], \tag{2.11}$$

where s_0 is the amplitude of the mixer output signal; and ω_{LO} and φ_{LO} are the frequency and phase of local oscillator signal, respectively. The φ_{LO} is typically chosen to be zero.

Measurement with the scanning heterodyne set-up is fully computer controlled. The sample is mounted on a stepping motor controlled *xy*-stage of 0.1 μm precision. Several stress pulses per scan position are usually applied to improve the signal-to-noise ratio. The phase shift is extracted from the heterodyne signal by home made software, which uses Fast-Fourier Transformation method [Litz03].

This set-up is of general-purpose. It can be used for investigation of temperature and free-carrier dynamics in the devices [Blah03a], and also allows to follow different device activity modes in case of trigger instabilities [Poga01a, Poga03a]. However, it suffers the disadvantage of necessity of multiple stressing, which constitutes the threat of gradual

degradation of the investigated device. The set-up is not applicable for investigation of destructive phenomena.

2.1.3.3 *2*-dimensional holographic set-up

The *2*-dimensional holographic set-up [Poga02c] provides information about *2*-dimensional phase shift distribution in one or two time instants during a single stress pulse.

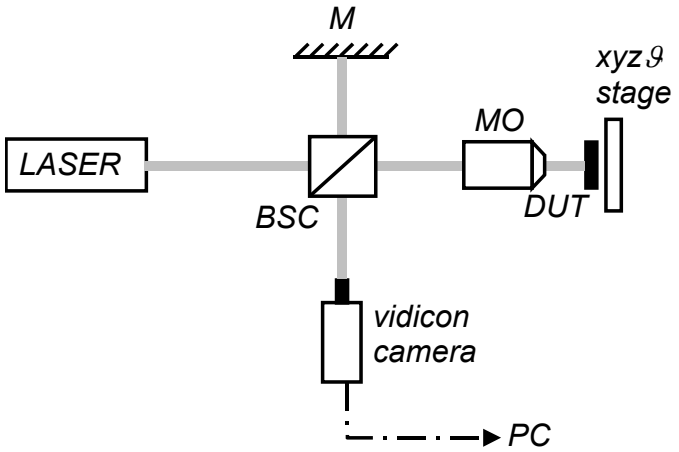


Fig. 2.5: Schematic diagram of the *2*-dimensional holographic set-up: *M* is the reference mirror; *BSC* is the beam-splitting cube; *MO* is the microscope objective; and *DUT* is the device under test.

The principal set-up schema is shown in Fig. 2.5. An optical parametric oscillator (*OPO*) pumped by a Q-switched YAG:Nd laser is used as the pulsed light source (*Laser*). The wavelength of the laser beam can be adjusted in a wide range of VIS and NIR spectrum (410 – 2000 μm), but usually 1.25 μm is used, because the light of this wavelength is not absorbed in the silicon even at high temperatures, and maximum output energy of the laser pulse is reached at this wavelength. The laser beam is split into the probe and reference beams in the beam splitting cube (*BSC*). The probe beam is collimated by the microscope objective (*MO*) in such way that it illuminates the whole *DUT*. The beam diameter can be adjusted in the range of 100 μm – 5 mm, which defines the field of view. Interference of the reference and probe beams transforms the phase profile into intensity changes, which have the form of interference fringes. These are visualised using an IR *vidicon camera* and saved in a computer for further processing. Generally the recorded fringe pattern *I(x,y)* can be expressed as

$$I(x,y) = A(x,y) + B(x,y)\cdot cos[\mathbf{k}\cdot\mathbf{r} + \Phi(x,y)] \quad (2.12),$$

where $A(x,y)$ is the background signal; $B(x,y)$ is the amplitude of the fringes; $\Phi(x,y)$ is the total phase shift profile; $\mathbf{k}$ is the wave vector of the laser beam; and $\mathbf{r}$ is the spatial vector. $\Phi(x,y)$ carries not only information about the phase shift induced by electrical stress, but also information about the phase shift induced by device topology. The latter is eliminated during the phase shift extraction procedure, which is based on the Fast Fourier Transformation method [Dube04a].

Timing is critical for the optimal operation of the laser source used in this set-up. It is therefore fully computer controlled[1]. Stress pulse is synchronised with the laser flash, and user can specify the time instant within the stress pulse, when the image is taken (laser flashes). The time resolution of the imaging is determined by the laser pulse duration, which is 5 ns. Recent improvement of the set-up, employing the second laser and camera, enables to record two fringe images taken in two different time instants during a single stress pulse [Dube04b].

Thanks to the ability of the set-up to record the phase shift profile in the whole device active region during a single stress pulse, it is optimally suited for investigation of non-repeatable events, such as the pulse-to-pulse instabilities [Deni03] or destructive events [Poga03a]. The set-up extension by the second laser flash makes it also suitable for extraction of the *2D* power dissipation density P_{2D} [Dube04b].

2.2 Sources of electrical stress

During the transient interferometric mapping of devices studied under ESD-like stress conditions, a home-made TLP or vf-TLP pulsers were used. The parameters of these two pulsers are listed in Table 2.2. In addition to them, a commercial pulse generator DEI SV-4000 was used for electrical stressing with the *2*-dimensional holographic set-up. The reason for that is that the instrument can be electronically controlled and it allows exact timing. This is not possible with the TLP and vf-TLP pulsers, because their relay switches have a high jitter. However, the rise time of 20 ns and minimal pulse length of 180 ns of the SV-4000 pulser does not allow direct comparison with the 100 ns TLP. On the other hand, this pulse generator allows study of the rise time effects when compared with the 150 ns TLP with 1 ns rise time [Litz01].

The above mentioned pulsers were also used for measurements of the high current I-V characteristics. This measurement is fully computer controlled. Voltage at the device and current

[1] The control routines for automatic measurement sequence were programmed within the framework of this thesis.

through the device are visualised on a fast digital oscilloscope and saved in a computer. Points of the I-V characteristics are obtained by averaging of the voltage and current values over appropriately chosen time interval within the stress pulse (Fig. 2.6). After each stress level the leakage current is measured, which gives information about the leakage current evolution with the stress current level and enables to determine failure threshold.

	TLP	vf-TLP	DEI SV-4000	
Pulse duration	100 ns, 300 ns	10 ns	180 ns – 250 ns	
Rise time	1 ns	0.5 ns	20 ns	
R_S	1 kΩ	-	1 kΩ	500 Ω
Output (max.)	4 A	8 kV	4 A	8 A

Table 2.2: Parameters of the pulse generators used for electrical stressing during the transient interferometric mapping.

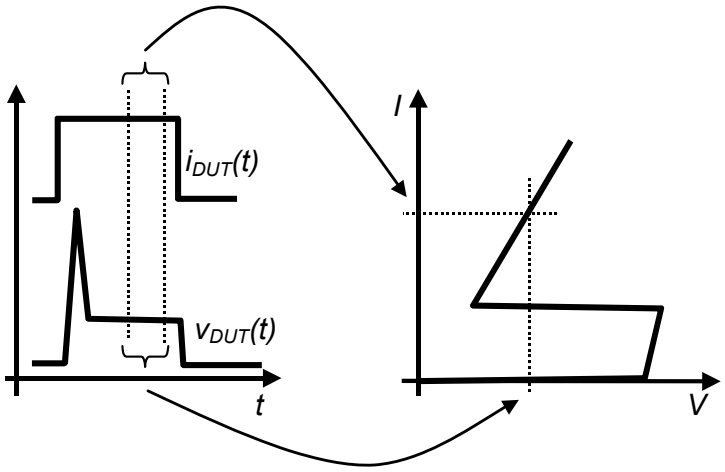


Fig. 2.6: Extraction of the high current I-V characteristics using the TLP or vf-TLP technique.

2.3 Auxiliary optical characterisation techniques

2.3.1 Optical beam induced current (OBIC)

Optical beam induced current (OBIC) technique is widely used in the failure analysis, where it helps to identify the exact position of a damage in semiconductor devices [Beau02, Beau03]. Nevertheless, it can be similarly used for identification of high electric field regions [Poga02d], for which sake it was also employed in this work.

The scanning heterodyne set-up is adopted for the OBIC measurements. The same DFB laser diode is used as a source of light, and the laser beam is focused on a *DUT* from the backside. The device is reverse-biased. Any optically generated carriers are separated by electrical field, and cause a change of the measured current. This can be afterwards related to the illuminated position. Sensitivity of the technique can be increased, when the device is biased close to the breakdown voltage, where the impact ionisation increases the measured current.

2.3.2 Emission microscopy

This technique involves recording of the electroluminiscence resulting from the transformation of electrical energy into light [Debo94]. In this work it is mainly used in the failure analysis (localisation of damages) [Russ99, Teh97]. It is sensitive to junction and dielectric related failures. It can be also used for identification of high electric fields or investigation of homogeneity of current flow in the studied devices [Blah02].

Emission microscopy can be performed in any of the TIM set-ups presented in this chapter. *DUT* is reverse biased and current through the device results in the electroluminiscence. This is observed using IR vidicon camera with spectral sensitivity of 400 nm – 1600 nm. The region, where the electroluminiscence takes place, localises the damage.

Chapter 3

BCD ESD protection devices under TLP and vf-TLP stress

This chapter presents results of the experimental investigation of low voltage BCD ESD protection devices, which are intended for protection of power supply pins and low voltage I/O pins of Smart Power Technology ICs. These devices are built in the 0.8 μm BCD4 technology of STMicroelectronics.

Single finger devices were tested in the HBM time domain, and proved a very high ESD robustness [Blah02]. Furthermore few layout variations, which included structural and dimensional changes, were investigated. Additional investigations were performed in the CDM time domain using the vf-TLP [Blah04].

3.1 Devices

Fig. 3.1 shows simplified cross-sections of three structural variations of the tested devices. These are basically npn bipolar transistors with short-circuited base and emitter. All devices are fabricated on a p-substrate with the n^+-buried layer implantation. Then the n-epi layer is grown where the p-body/p-well is diffused. Two shallow n^+ regions create collector and emitter. The first type of the device (referred as device *D1*) has an n^+-sinker, which connects the buried layer with the n^+-collector (Fig. 3.1(a)). Devices with this layout have widths 50 μm, 100 μm, 170 μm and 300 μm. Next kind of the investigated device is without sinker (Fig. 3.1(b), referred as device *D2*). The last device type is also without sinker, and in addition the collector region is isolated from the n-epi layer by an extension of the p-body region (Fig. 3.1(c), referred

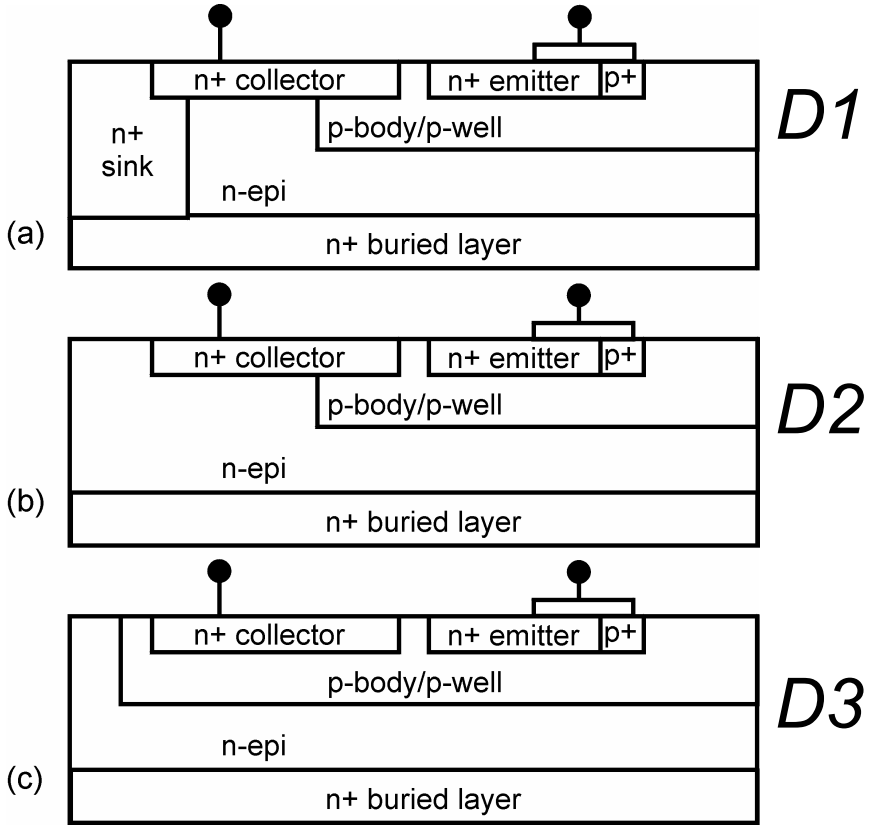


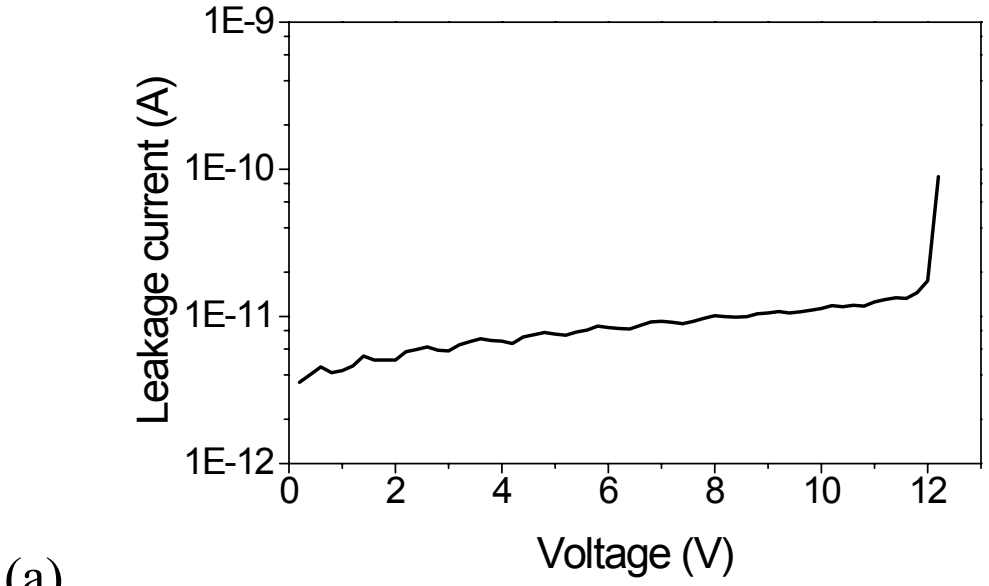
Fig. 3.1: Principal cross sections of the investigated devices: (a) with sinker – *D1*; (b) without sinker – *D2*; and (c) with isolated collector – *D3*.

as device *D3*). The width of the two latter types of the devices is 170 μm. During the experiments, positive polarity stress was applied to the collector, and the emitter/base contact was kept grounded.

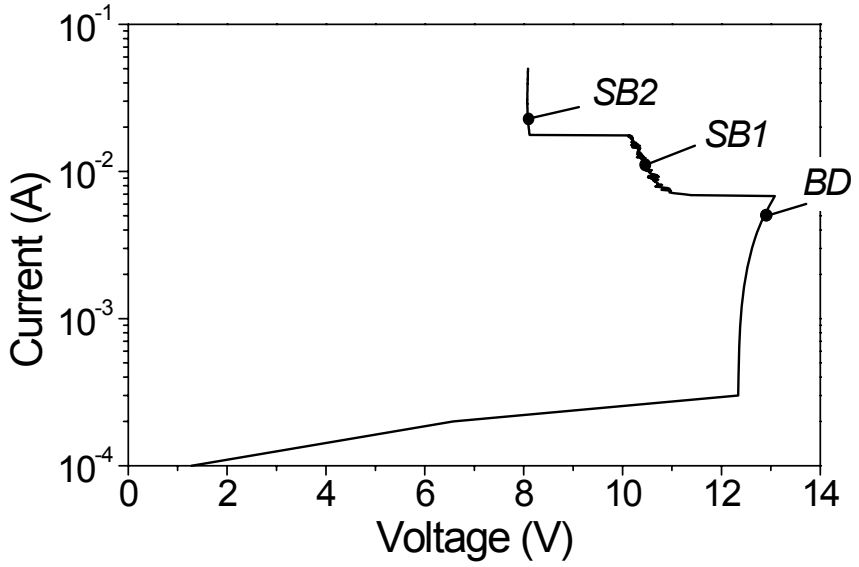
Operating principle of the devices has been explained in the Section 1.2.2.

3.2 Characterisation under DC operating conditions

Figure 3.2(a) shows the DC I-V characteristics of the device *D1*, measured by a semiconductor parameter analyser operating in the voltage-source mode. Leakage current (the n^+-collector/p-body junction reverse current) of the device is in order of few *pA*. The breakdown voltage is about 12 V. Fig. 3.2(b) shows the DC I-V characteristics measured in the current source mode. In this case the characteristics exhibit double-snapback behaviour.



(a)



(b)

Fig. 3.2: DC I-V characteristics of the device *D1* (*w* = 170 μm) measured (a) in the voltage-source mode; and (b) in the current-source mode.

The first snap-back is reached at about 7 mA, and the voltage on the device drops down from about 13 V to about 10 V. When the current level increases further (above 18 mA), the second snapback is observed, and the voltage drops down to 8 V.

Behaviour of the device in various operating points marked in Fig. 3.2(b) (*BD*, *SB1* and *SB2*) was studied by DC emission microscopy in the constant current mode. Fig. 3.3 shows the emission microscopy images, which are aligned with the device backside infrared image. When the device operates in the breakdown (point *BD* in Fig. 3.2(b)), the light is emitted from the place marked by an arrow (Fig. 3.3(a)). The latter indicates position of the lateral edge of the collector junction. This implies that the impact ionisation is dominant in the lateral part of the n^+-collector/p-body junction and not in the vertical one. This is consistent with a high electric field expected at this place due to high curvature of the n^+-collector region there. Uniform emission along the whole width of the device also shows that the current flows quite

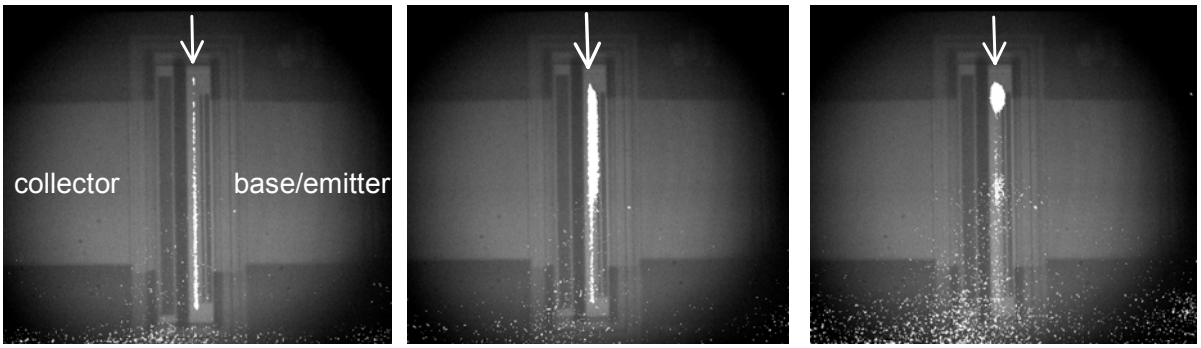


Fig. 3.3: DC emission microscopy images of the device *D1* (*w* = 170 µm) taken at various working points marked in Fig. 3.2(b): (a) *BD*; (b) *SB1*; and (c) *SB2*. The arrow marks the lateral edge of the collector junction.

homogeneously in this regime. Transition to the first snapback (working point *SB1* in Fig. 3.2(b)) leads to a widening of the emitting area toward the n^+-emitter, indicating the triggering of the bipolar transistor (Fig. 3.3(b)). The emission also indicates that the transistor is turned on only in a part of the device. Finally, the second snapback in the I-V characteristics (point *SB2* in Fig. 3.2(b)) is accompanied with a collapse of the light emitting region into one device corner (Fig. 3.3(c)), which is caused by the self-heating.

In order to identify high electric field regions, an OBIC scan along the device length was performed at voltages below the breakdown (V = 5 V) and in the breakdown (V = 12.1 V).

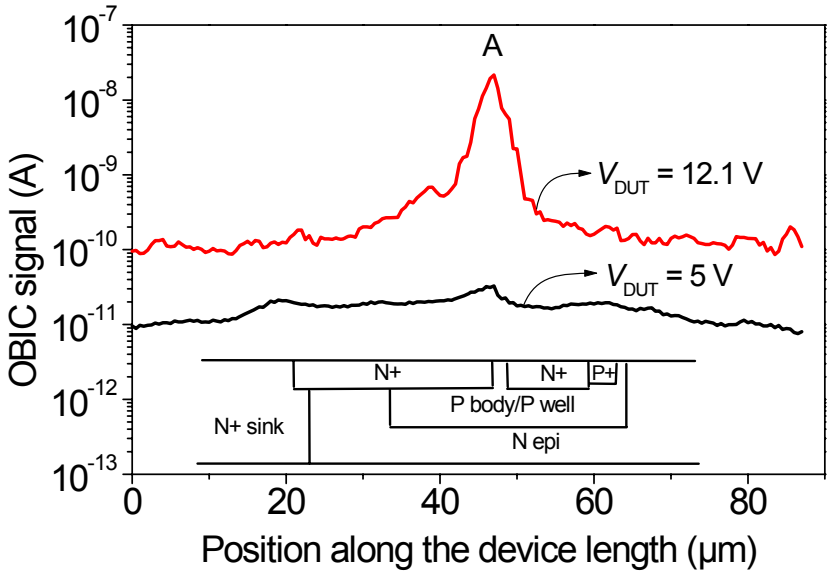


Fig. 3.4: OBIC signal distribution along the length of the device D1 (w = 170 μm) biased to V = 5 V and *V* = 12.1 V

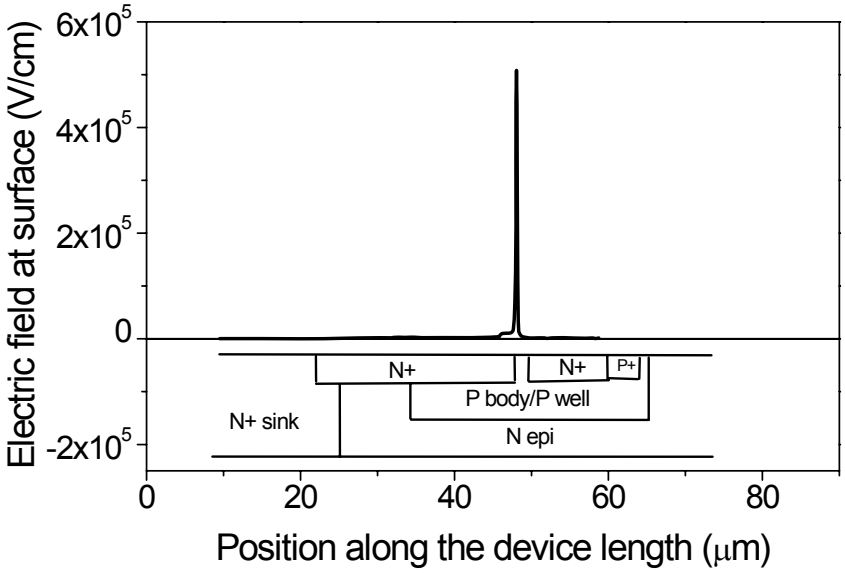


Fig. 3.5: Simulated surface electric field distribution along the length of the device *D1*. (Courtesy of L. Zullino)

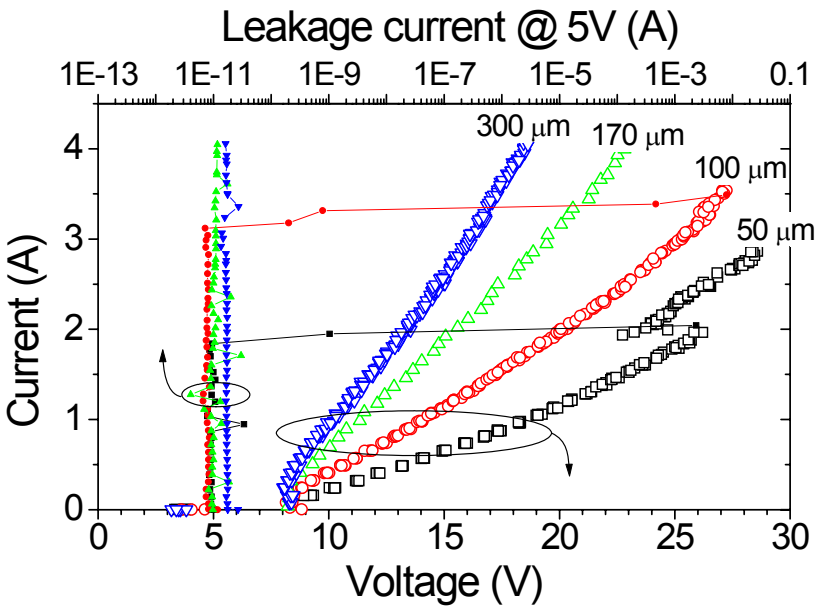
Fig. 3.4 shows the OBIC signal as a function of the position along the device length. The signal exhibits a peak at the lateral collector/body junction ("A" in Fig. 3.4), indicating the highest electric field in this point. No other pronounced high electric-field regions are found. This result agrees with the EMMI observations in the breakdown operating point (Fig. 3.3(a)) and also with the simulated surface electric field distribution, which is shown in Fig. 3.5. Note that the OBIC signal in the breakdown (V = 12.1 V) is more than two orders of magnitude higher than at V = 5 V. Origin of the OBIC signal under this below band-gap light excitation (wavelength of the laser is λ = 1.3 μm) is attributed to the photo-carrier generation processes related with the energy tails in the highly doped n^+-collector region and/or with the intrinsic states at the Si/SiO_2 interface. The amplified OBIC signal in the breakdown originates from the avalanche multiplication of the photo-generated carriers in the region with a high electric field.

3.3 Characterisation under pulsed (ESD-like) operating conditions

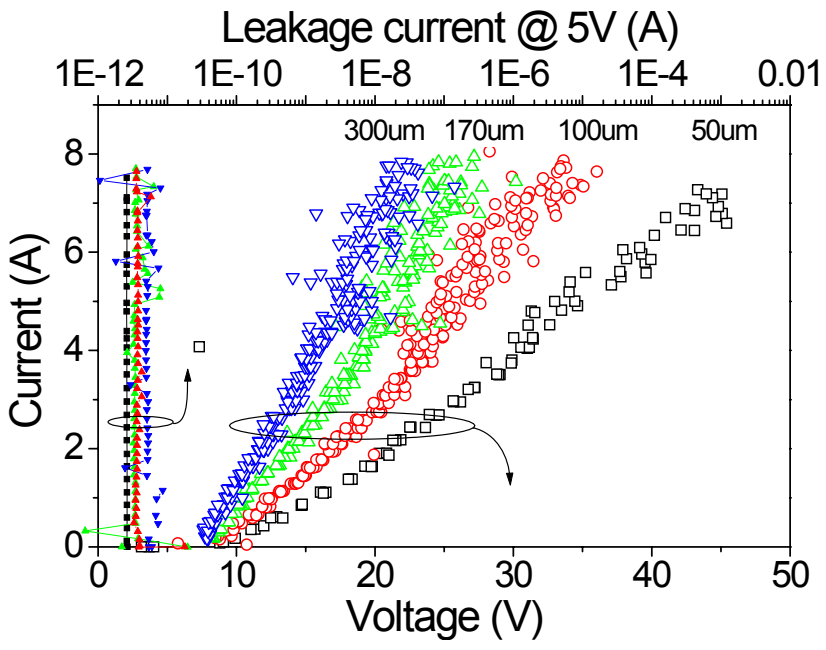
3.3.1 Electrical characterisation

Figs. 3.6(a) and (b) show the high current I-V characteristics of the devices *D1* of different widths measured using the 100 ns TLP and 10 ns vf-TLP, respectively. The holding voltage is about 8 V for both stress types, which corresponds to the second snapback labelled as *SB2* in Fig. 3.2(b). Since the turn-on of the npn transistor, the I-Vs exhibit a slightly super-linear behaviour, which means that the differential resistance R_{diff} of the devices decreases with increasing stress current level. This is probably caused by the conductivity modulation in the p-body region, and this effect is discussed in more details in the section 3.3.2.1. The main contribution to the R_{diff} is attributed to the resistance of collector and emitter regions. When the $1/R_{diff}$ is extracted from the TLP I-Vs and plotted as a function of the device width (Fig. 3.7), nearly linear dependence is found. The scaling suggests that the current flow is homogeneous in the devices under the TLP operating conditions.

Figs. 3.6(a) and (b) also exhibit the leakage current evolution with the stress current level. Sudden increase of the leakage current I_{leak} to the *mA* region indicates a failure of the device. This is observed for the devices with 50 μm and 100 μm widths stressed by the 100 ns TLP (Fig. 3.6(a)). The current levels at which it occurs are about 1.8 A and 3.2 A,



(a)



(b)

Fig. 3.6: High current I-V characteristics of the devices *D1* of various widths measured using (a) 100 ns TLP; and (b) 10 ns vf-TLP.

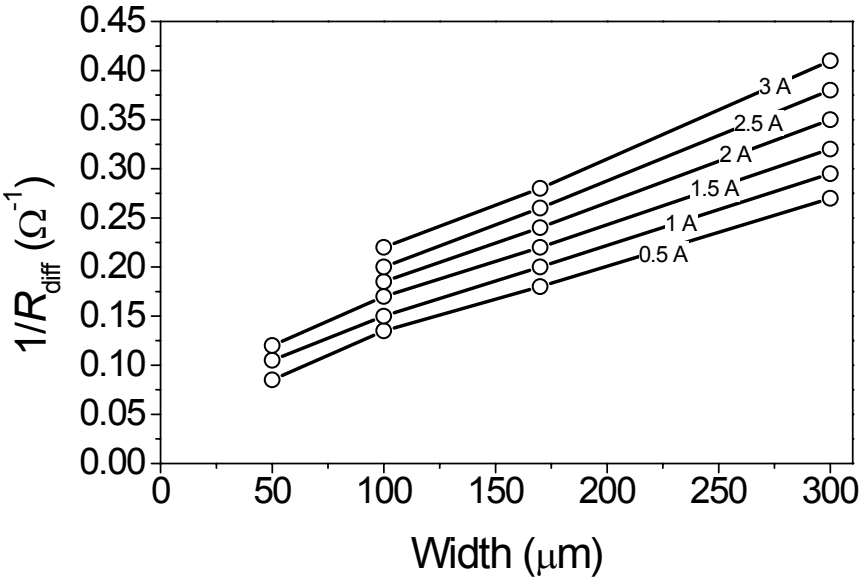


Fig. 3.7: The $1/R_{diff}$ extracted from the 100 ns TLP I-V characteristics of the devices *D1* (Fig. 3.6(a)) as a function of the device width. The stress current level is a parameter.

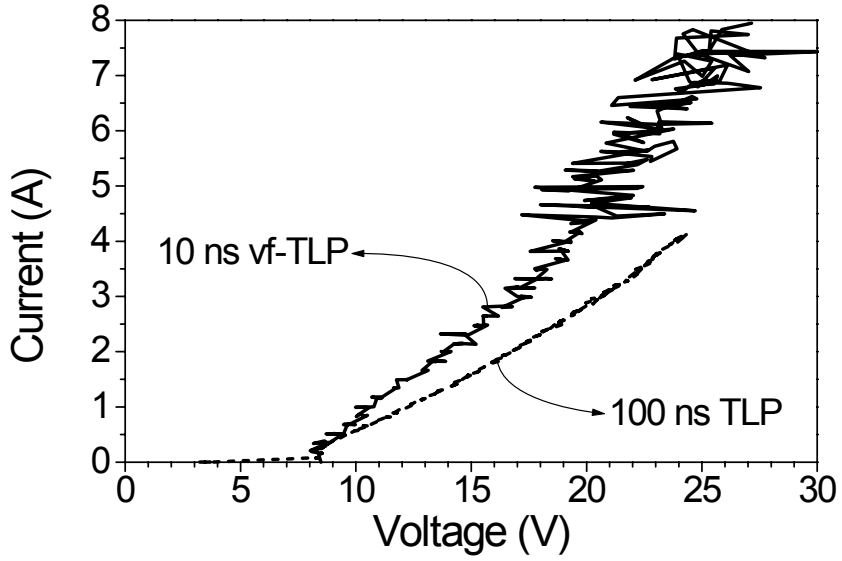
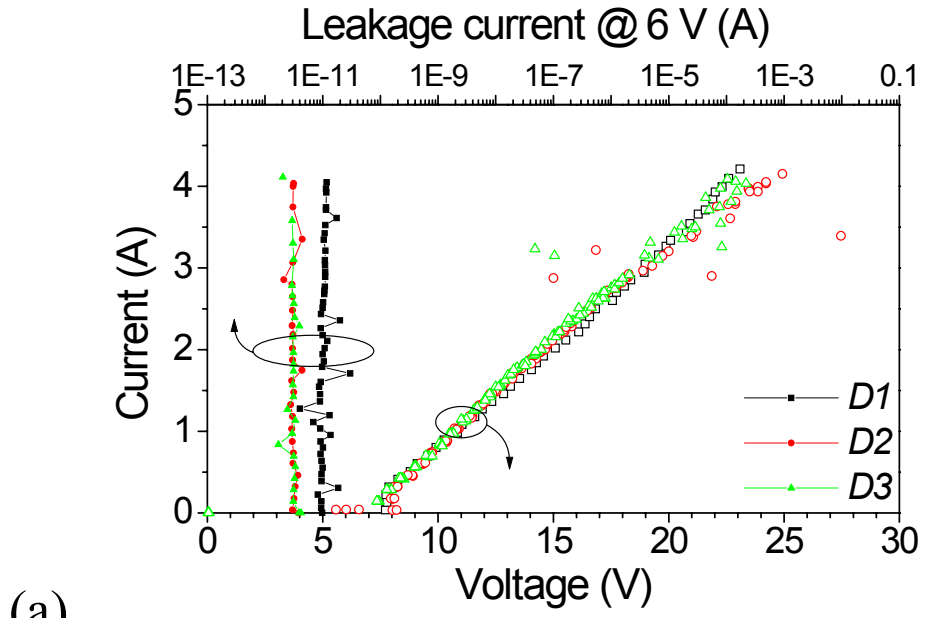
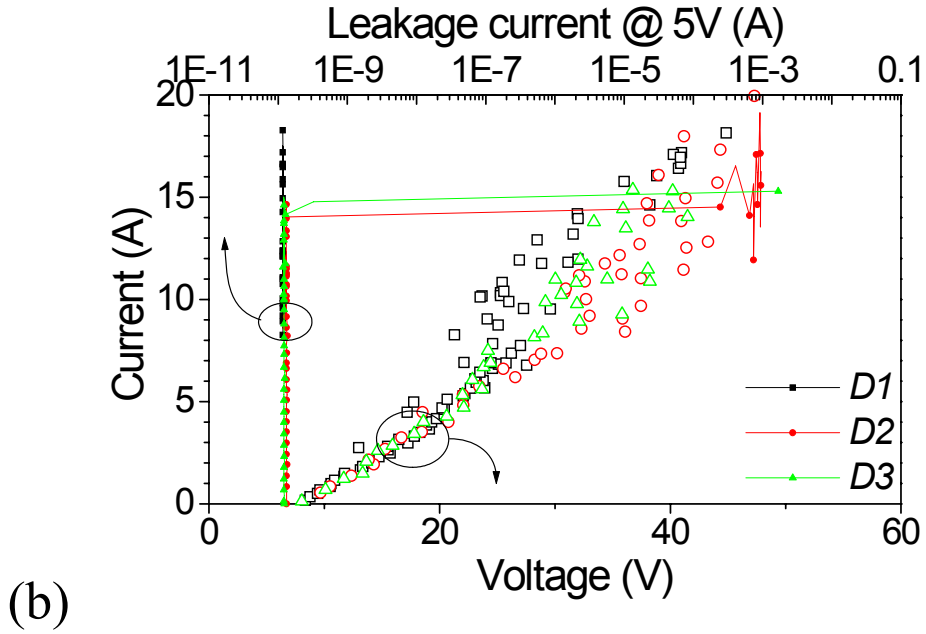


Fig. 3.8: Comparison of the high current I-V characteristics of the device *D1* of width 170 μm measured using the 100 ns TLP and 10 ns vf-TLP.



(a)



(b)

Fig. 3.9: High current I-V characteristics of the devices *D1*, *D2* and *D3* (*w* = 170 µm) measured using (a) 100 ns TLP; and (b) 10 ns vf-TLP.

respectively. For the devices with $w \geq 170$ µm the TLP failure threshold is beyond 4 A. On the other hand, all devices can withstand 7 A of the 10 ns vf-TLP stress, because no increase of the leakage current is observed until then (Fig. 3.6(b)).

If the TLP and vf-TLP I-Vs of the device *D1* are compared, a difference can be found: the R_{diff} is higher for the TLP case (Fig. 3.8). This can be related to the self-heating effect. At the end of the longer TLP pulse the device is hotter, and consequently its total resistance is higher.

The subsequent electrical characterisation was concentrated on the influence of the device layout on the high current I-V characteristics. Figs. 3.9(a) and (b) compare the high current I-V characteristics of the devices *D1*, *D2* and *D3* of the same width (170 µm) measured using the 100 ns TLP and 10 ns vf-TLP, respectively. The R_{diff} obtained from the 100 ns TLP measurements is the same for all three types of devices (Fig. 3.9(a)). The same is valid for the vf-TLP measurements, at least for $I_{stress} < 7$ A (Fig. 3.9(b)). At higher currents ($I_{stress} > 7$ A) the data are rather scattered, and it is difficult to draw any conclusion. The scattering comes mostly from the sparking resistance of the switching TLP relay and from a digitising error of the oscilloscope. All devices can sustain 4 A TLP stress, which is the set-up limit (Fig. 3.9(a)). Moreover, device *D1* does not degrade up to the vf-TLP stress level of 18 A (Fig. 3.9(b)), which is again the set-up limit. On the other hand, devices *D2* and *D3* fail at the vf-TLP current level of approximately 14 A. This means that although there is no remarkable difference in the I-V characteristics, the devices without sinker are less robust.

Summary of the failure thresholds obtained during the electrical characterisation is given in Table 3.1.

	TLP				**vf-TLP**			
	50	**100**	**170**	**300**	**50**	**100**	**170**	**300**
D1	1.8 A	3.2 A	> 4 A	> 4 A	> 7 A	> 7 A	> 18 A	> 7 A
D2	-	-	> 4 A	-	-	-	14 A	-
D3	-	-	> 4 A	-	-	-	14 A	-

Table 3.1: Failure thresholds of the investigated devices.

3.3.2 Optical characterisation

Optical characterisation employing the heterodyne scanning set-up and the *2*-beam Michelson interferometric set-up was performed to investigate the internal behaviour of the devices by localising the heat dissipation sources and the places with an excess free-carrier concentration.

3.3.2.1 Device *D1*

Fig. 3.10 shows the phase shift distributions along the length of the device *D1* of 170 µm width at the end of the 100 ns TLP stress pulses of different current levels: 1 A, 2 A, and 4 A. Dominant phase shift peak is found at the lateral n^+-collector/p-body junction (see "A" in Fig. 3.10). This is the same place, where the maximum electric field was found (cf. Fig. 3.5). Accordingly one can deduce that this peak arises from the heat dissipation caused by the impact ionisation in the junction (cf. Fig. 3.3). With increasing stress current the amplitude of the phase shift signal increases at this place, as more and more power is dissipated. Besides the dominant

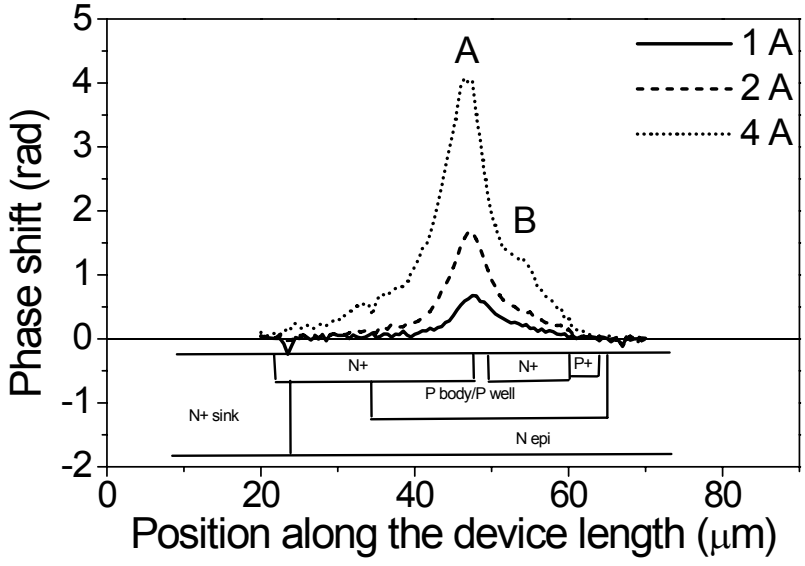


Fig. 3.10: Phase shift distribution along the length of the device *D1* of width 170 µm at the end of the 100 ns TLP pulse of amplitudes 1 A, 2 A and 4 A. An aligned simplified cross-section of the device is also given.

peak, a side hump in the phase shift distribution is found in case of the 4 A stress, but not at 1 A and 2 A stress (see "B" in Fig. 3.10). This suggests an existence of the second heat-dissipating region visible at high currents.

The time evolution of the phase shift distribution along the length of the device *D1* (w = 170 μm) during the 100 ns TLP pulse of 4 A amplitude is shown in Fig. 3.11. At position "A" the phase shift is found positive from the very first moments of the stress pulse, and it rises with time at this place. On the other hand the phase shift is negative after first 10 ns at position "B". It means that there is an excess free-carrier concentration at this place. However, after 50 ns the phase shift signal becomes positive there, and at the end of the pulse the above-mentioned side-hump is observed.

To provide insight into the behaviour at locations "A" and "B", Fig. 3.12 shows the phase shift evolution at these places. The phase shift signal increases linearly at "A" until the end of the stress pulse, indicating constant power dissipation. The situation is more complex at "B": the phase shift signal is in the first moments negative, then linearly increases into positive values and reaches maximum after the stress pulse end. This behaviour results from a superposition of the positive and linearly increasing thermal signal, and the negative and constant free-carrier signal. The dashed lines in Fig. 3.12 schematically show the assumed evolution of these two

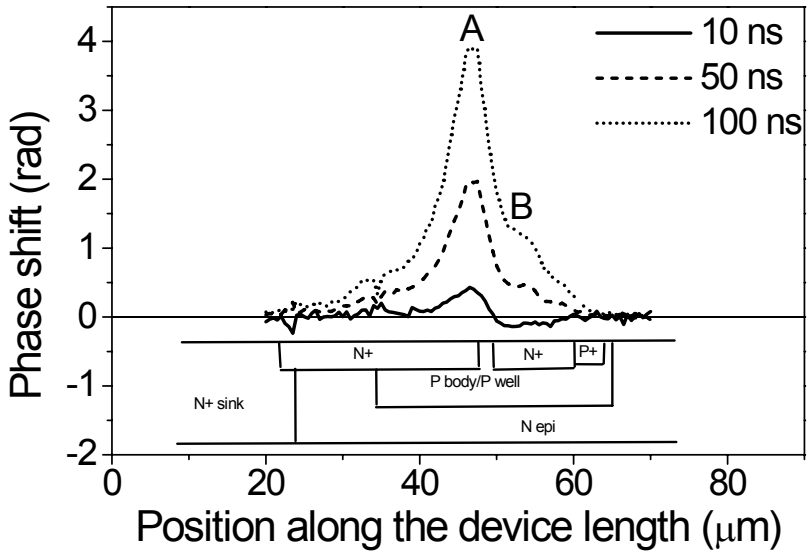


Fig. 3.11: Evolution of the phase shift distribution along the length of the device *D1* of width 170 μm stressed by the 100 ns TLP pulse of amplitude 4 A. An aligned simplified cross-section of the device is also given.

components. The amplitude of the free carrier signal saturates within few nanoseconds at the beginning of the stress pulse, then it is constant, because constant current pulses are applied to the device, and it decays longer after the stress pulse, particularly due to a lifetime of the free-carriers. The slow decay and the heat transfer from the neighbouring place "A" are also the reasons, why the phase shift maximum at "B" is reached after the stress pulse end.

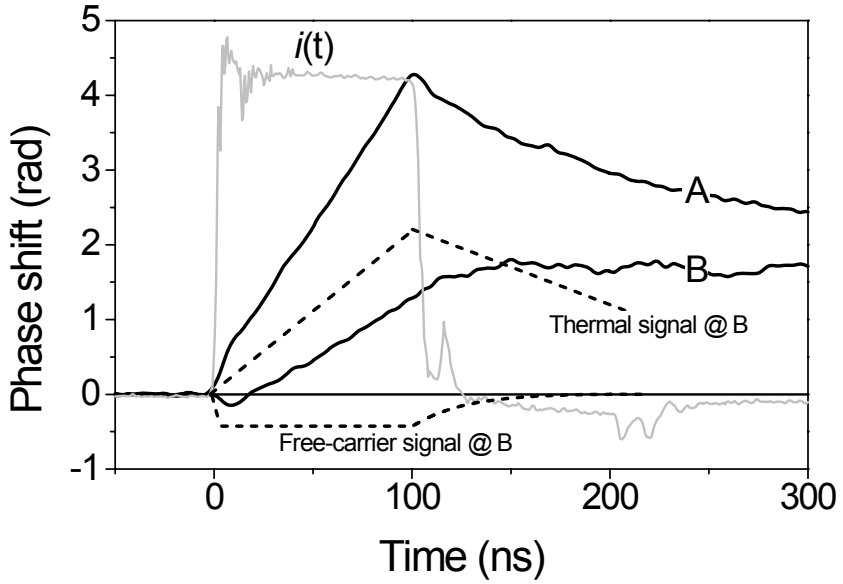


Fig. 3.12: Phase shift evolution at positions "A" and "B" (cf. Fig. 3.11) in the device *D1* (w = 170 µm) stressed by 100 ns TLP pulse of amplitude 4 A.

These experimental observations can be compared with the results of the *2D*-simulation:

Fig. 3.13 shows the simulated electron current density in the device *D1* at the end of the 100 ns TLP stress pulse of amplitude 2.5 A. This figure reveals that there are two current paths in the device. The first one is lateral, where the current flows along the device surface. The second current path is vertical, where the electron current flows through the vertical npn transistor formed by n^+-emitter/p-body/n-epi regions and then it follows the low resistive paths through the n^+-buried layer and n^+-sinker to the collector. Note that the current through the lateral transistor is about one order of magnitude higher then the current through the vertical transistor.

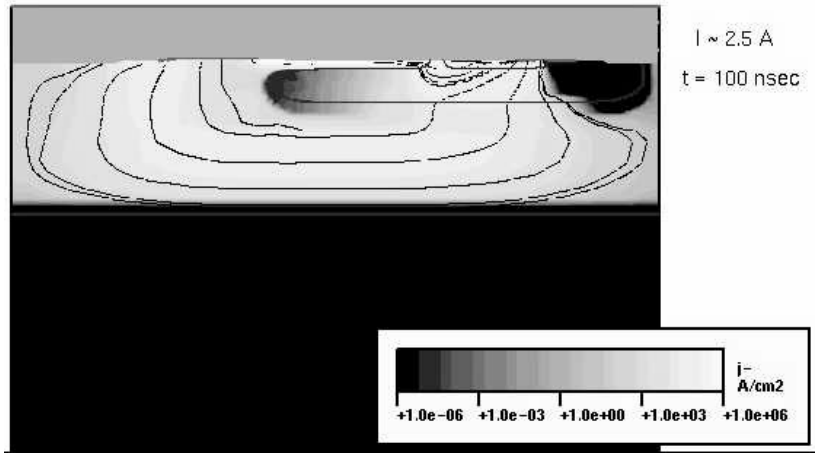


Fig. 3.13: Simulated electron current density in the device *D1* at the end of the 100 ns TLP pulse of 2.5 A amplitude. The current flow lines are indicated as solid lines. (Courtesy of L. Zullino)

High electron current density found in the p-body regions consequently leads to a high excess electron density there. Simulation shows that it reaches the order of 10^{18} cm^{-3} during the 100 ns TLP pulse of 2.5 A amplitude (Fig. 3.14). These are the free electrons injected from the emitter, when the npn transistor is turned on. This simulation result explains the experimental observation of the negative phase shift signal at that place ("B" in Fig. 3.11, t = 10 ns). So high excess electron density can also cause a conductivity modulation, which is the proposed reason for the decrease of the R_{diff} with increasing stress current level (cf. Fig. 3.7).

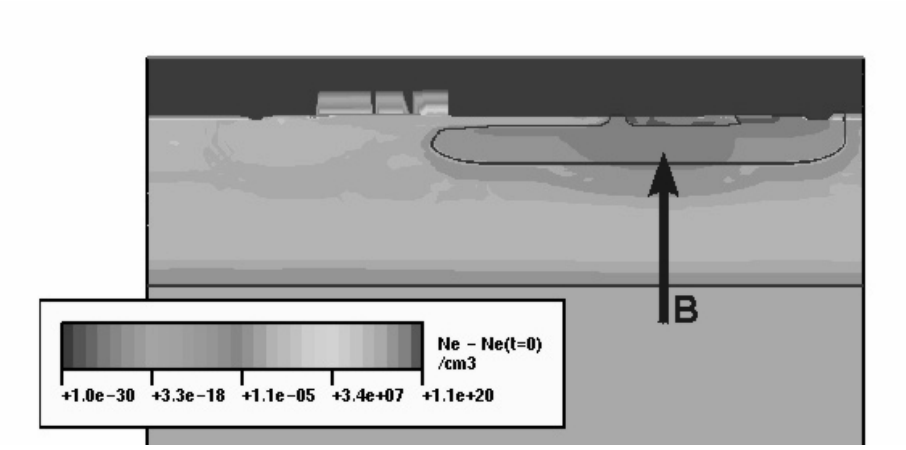


Fig. 3.14: Simulated excess electron concentration in the device *D1* at the end of the 100 ns TLP pulse of amplitude 2.5 A. (Courtesy of L. Zullino)

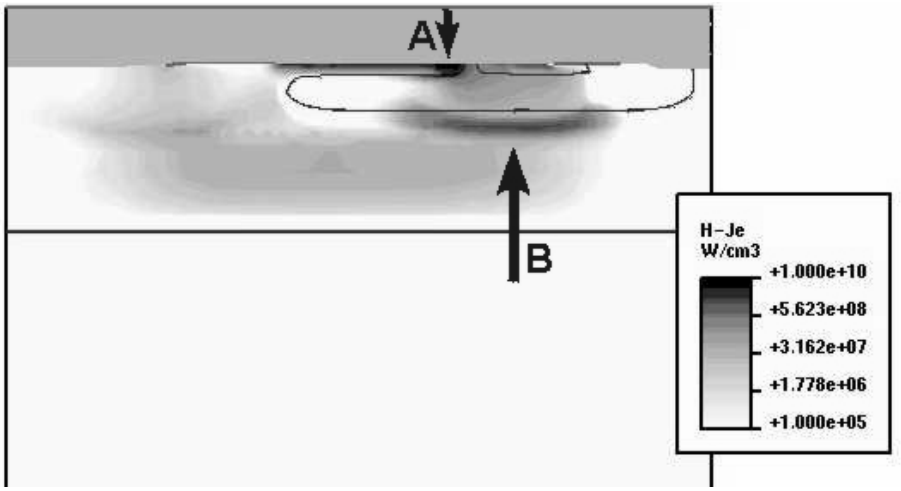


Fig. 3.15: Simulated heat dissipation caused by the electron current flow in the device *D1* at the end of the 100 ns TLP pulse of amplitude 2.5 A. (Courtesy of L. Zullino)

Finally the simulated heat-dissipation originating from the electron current flow is shown in Fig. 3.15. The main heat-dissipating region is located at the lateral n^+-collector/p-body junction. This is in agreement with the experiment, because the dominant thermal phase shift peak was observed at this place (hot spot "A" in Fig. 3.10). The second heat-dissipating region is observed at the n-epi/p-body junction under the n^+-emitter. This is the second place in the device, where the avalanching takes place. It explains existence of the side-hump observed experimentally at the end of the 100 ns TLP pulses in this structure (see "B" in Fig. 3.10, I_{stress} = 4 A).

It was suggested in the part related with the electrical characterisation (section 3.3.1) that the current flow is homogeneous under pulsed conditions in the devices *D1*. To verify it, optical mapping was performed along the width of the devices crossing the points "A" and "B".

Fig. 3.16 shows the phase shift distribution along the dominant heat-dissipating region ("A" in Fig. 3.10) at the end of the 100 ns TLP stress pulses of various amplitudes. Flat phase shift profiles indicate homogeneous current flow under all stress current levels. Such behaviour was observed in the *D1* devices of all sizes. This result is consistent with the linear scaling of the inverse differential resistance $1/R_{diff}$ as a function of the device width (Fig. 3.7), and it also explains very high ESD robustness of the devices.

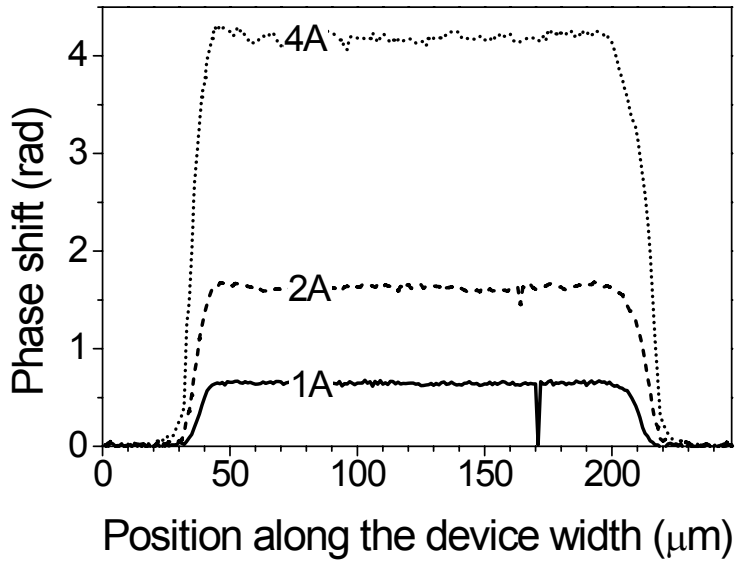


Fig. 3.16: Phase shift distribution along the line “A” (cf. Fig. 3.10) in the device *D1* (w = 170 μm) at the end of the 100 ns TLP pulse of amplitudes 1 A, 2 A and 4 A.

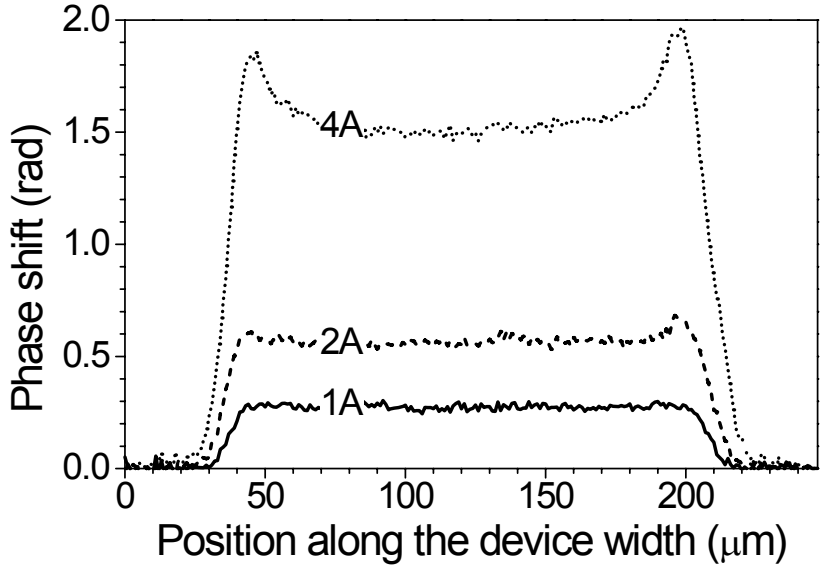


Fig. 3.17: Phase shift distribution along the line “B” (cf. Fig. 3.10) in the device *D1* (w = 170 μm) at the end of the 100 ns TLP pulses of amplitudes 1 A, 2 A and 4 A.

Fig. 3.17 shows the phase shift distribution along the second ("vertical") heat-dissipating region ("B" in Fig. 3.10) for the same current levels as in the previous figure. In this case, the phase shift distribution is flat only for current of 1 A. When the 2 A and 4 A current stresses are applied, an increased phase shift signal appears at the device corners. This is attributed to the layout:

- collector contact is wider than the emitter/base one (Fig. 3.18(a)), which can cause the current crowding.
- the vertical part of the npn transistor has also a surface component at the corner (Fig. 3.18(b)).

Simultaneous action of these two effects causes the increased heat dissipation in the corners.

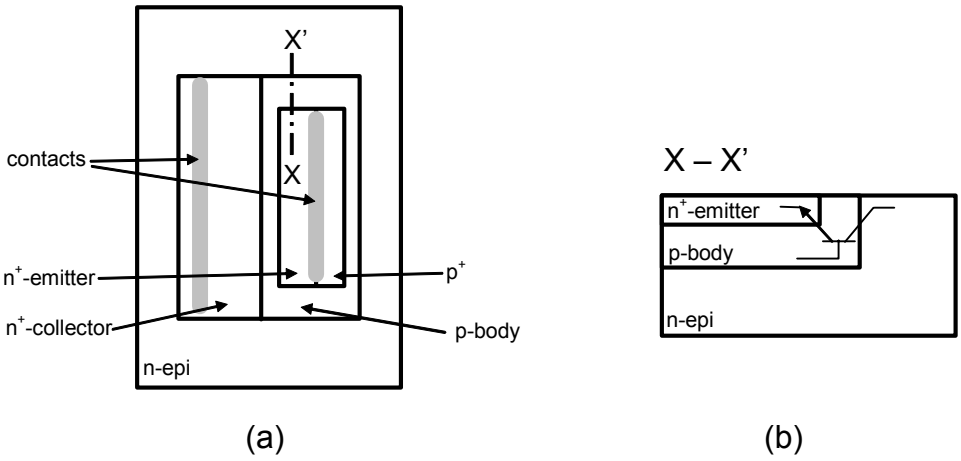


Fig. 3.18: (a) Layout of the device *D1*; and (b) the cross-section along axis X - X' showing surface component of the vertical npn transistor.

The device behaviour under the vf-TLP stress is not very much different from that one under the TLP stress presented until now. Fig. 3.19 shows the phase shift distribution along the length of the device under the 10 ns vf-TLP stress of amplitude 4 A at time instances of 5 ns and 10 ns. The dominant phase shift peak is still localised at the lateral n^+-collector/p-body junction ("A" in Fig. 3.19). At position "B" the phase shift signal is negative at the pulse end, because the stress pulse is too short to allow the thermal signal from the vertical transistor to dominate over the negative free-carrier signal.

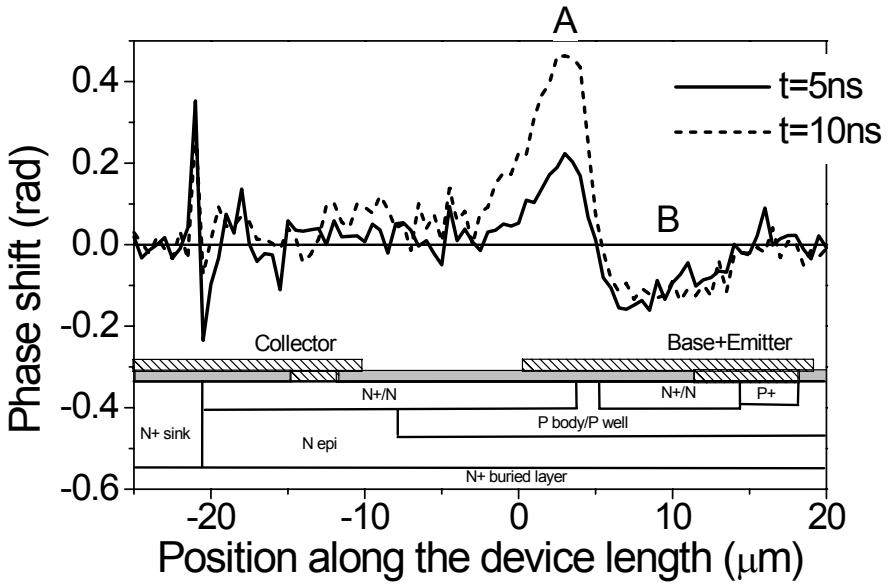
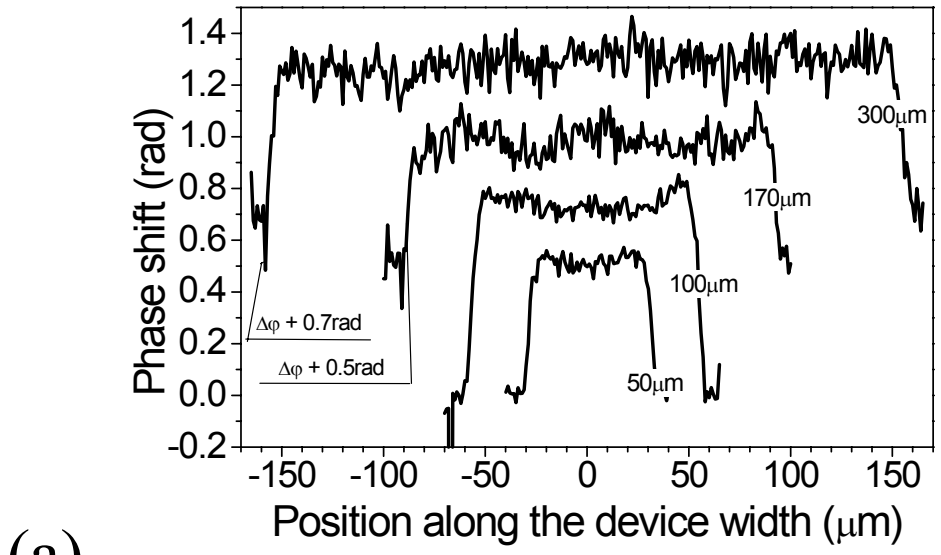


Fig. 3.19: Evolution of the phase shift distribution along the width of the device *D1* (w = 170 μm) during the 10 ns vf-TLP pulse of amplitude 4 A. An aligned simplified cross-section of the device is also given.

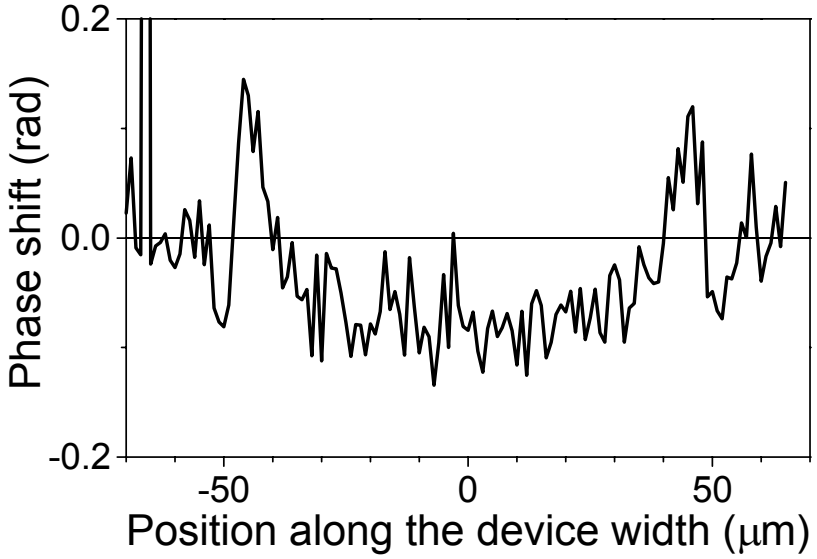
The homogeneous current flow along the dominant hot spot "A" was found also under the vf-TLP stress, which is shown for all *D1* devices in Fig. 3.20(a). The phase shift distribution along the second peak "B" exhibits increased heat dissipation at device corners (Fig. 3.20(b)), which is qualitatively the same result as in the case of TLP stress.

There is still one open question: do the lateral and vertical transistors trigger at the same time, or is there some delay between their activities? Such delay was observed e.g. in [Bych03] and it influenced the device behaviour in such a way that the voltage drop on the device was dependent on the pulse duration.

Fig. 3.21 shows the time evolution of the phase shift at locations "A" and "B" (cf. Fig. 3.19) measured by the *2*-beam Michelson interferometric set-up. The phase shift evolutions are qualitatively the same as those presented in Fig. 3.12. However the time resolution is much higher (0.4 ns) in the present case. There is no observable delay between activity at "A" and "B", and one can therefore conclude, that the delay between the turn on of the vertical and lateral npn transistors is less than 0.4 ns. Moreover the figure proves that the device *D1* is effectively turned-on also during very short CDM-like stress.



(a)



(b)

Fig. 3.20: (a) Phase shift distribution along the line “A” (cf. Fig. 3.19) in the devices *D1* of various widths at the end of the 10 ns vf-TLP pulse of the same current density (*I*/*w* = 40 mA/μm). (b) Phase shift distribution along the line “B” (cf. Fig. 3.19) in the device *D1* (w = 100 μm) at the end of the 10 ns vf-TLP pulse (*I* = 4 A).

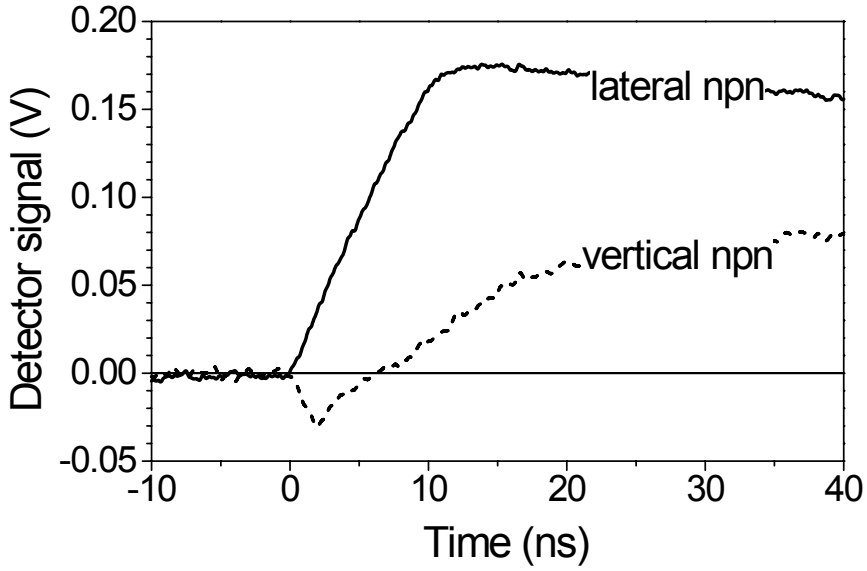


Fig. 3.21: Phase shift evolution at positions “A” and “B” (cf. Fig. 3.19) in the device *D1* under the 10 ns vf-TLP pulse of amplitude 4 A.

3.3.2.2 Device *D2*

Fig. 3.22 shows the evolution of the phase shift distribution along the length of the device *D2* for several time instances during the 100 ns TLP stress of amplitude 2 A. The picture is a bit different in comparison with the one observed for the previous device (*D1*, Fig. 3.11). The dominant thermal phase shift peak is still there, but the second peak does not become positive anymore, and an additional positive peak occurs next to the collector contact.

The fact that the phase shift measured at the emitter locus (“B” in Fig. 3.22) stays negative even at the end of the 100 ns TLP pulse indicates that the heat-dissipation at this place is decreased compared to the device *D1* (cf. Fig. 3.11). The electric field in the vertical n-epi/p-body junction seems to be too small to start the avalanching there. Nevertheless, the vertical npn transistor can be still active, because the base/emitter junction is opened thanks to holes fed from the avalanching collector junction of the lateral npn transistor.

The *2D*-simulation confirms the above assumptions. Fig. 3.23 shows the simulated electron current density in the device *D2* under the 100 ns TLP stress pulse of amplitude 2.5 A. The lateral current path is still dominant. The vertical npn transistor is also active, and a fraction

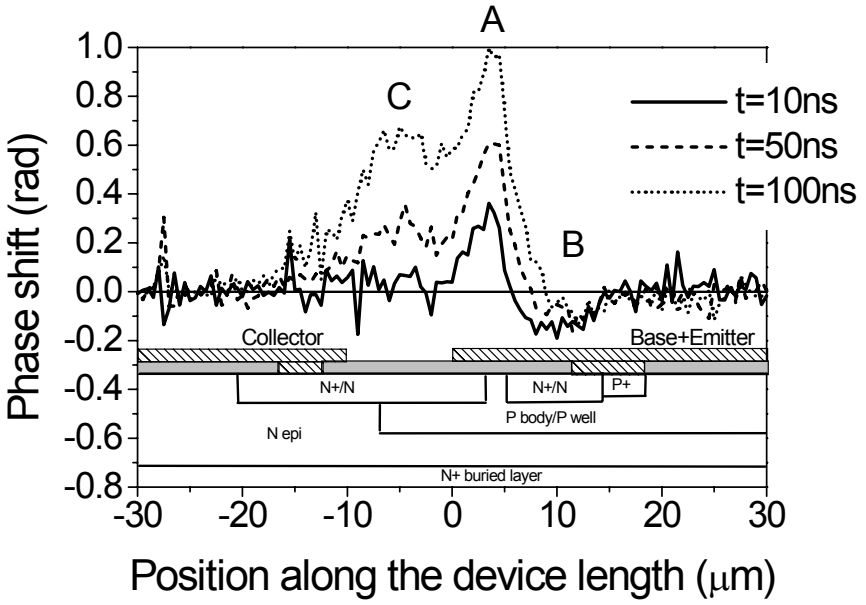


Fig. 3.22: Evolution of the phase shift distribution along the length of the device *D2* stressed by the 100 ns TLP pulse of amplitude 2 A. An aligned simplified cross-section of the device is also given.

of the current flows along the buried layer. Note that the flow-lines of the "vertical" electron current cross the p-body region for the second time under the n^+-collector region. This is only possible if the n-epi/p-body junction under the n^+-collector becomes forward biased. This suggests that the resistance of the n-epi region under the n^+-collector contact causes so high voltage drop that the p-body has positive potential with respect to the n-epi at that place.

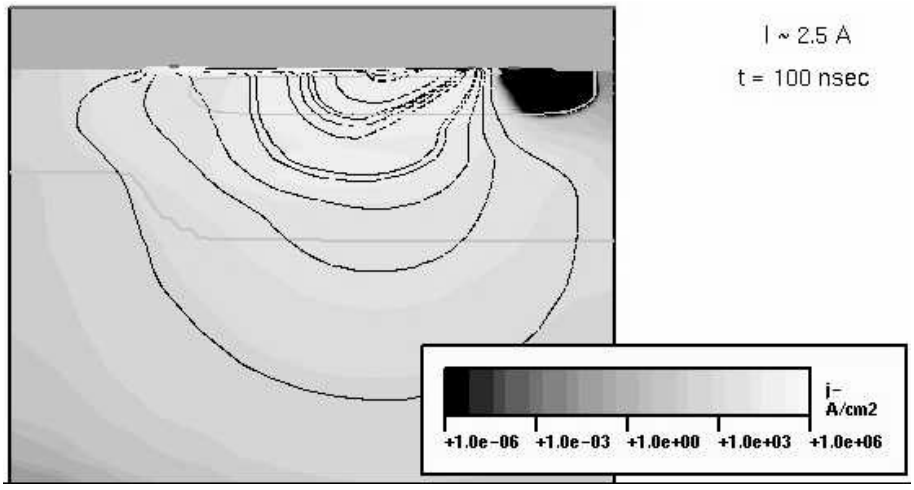


Fig. 3.23: Simulated electron current density in the device *D2* exposed to 100 ns TLP stress pulse of amplitude 2.5 A. Current flow lines are indicated as solid black lines. (Courtesy of L. Zullino)

The simulated heat-dissipation caused by the electron current in the device *D2* at the end of the 100 ns TLP pulse of amplitude 2.5 A is shown Fig. 3.24. The main heat-dissipating region is the lateral n^+-collector/p-body junction ("A" in Fig. 3.24) similarly as in the device *D1* (cf. Fig. 3.15). In contrast to the device *D1*, the heat dissipation at the n-epi/p-body junction under the n^+-emitter in the device *D2* is much lower (compare "B" in Fig. 3.24 and in Fig 3.15). It is in agreement with the experiment, where no positive thermal peak was observed at this place ("B" in Fig. 3.22). Another pronounced heat dissipating region is under the n^+-collector ("C" in Fig. 3.24). It arises from the "vertical" electron current in the high resistive n-epi region when flowing around the p-body region. This is the origin of the second thermal peak observed in the device *D2* ("C" in Fig. 3.22). The simulated profile of maximum temperature at the end of the 100 ns TLP pulse of amplitude 2.5 A, which is shown in Fig. 3.25, also confirms existence of this peak. The absence of this peak in case of the device *D1* is caused by the presence of the highly doped n^+-sinker, which enables a low-resistive current path with a low heat dissipation (compare Fig. 3.15 and 3.24).

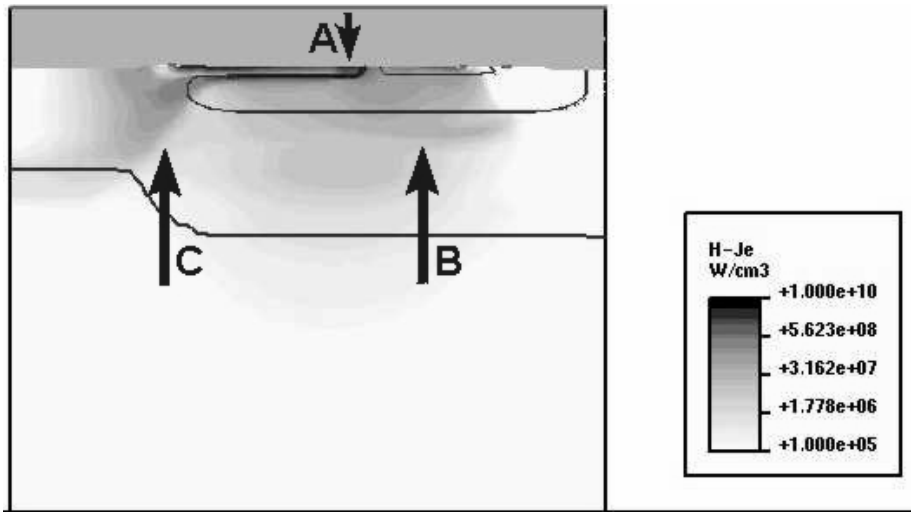


Fig. 3.24: Simulated heat-dissipation caused by electron current flow in the device *D2* exposed to the 100 ns TLP stress pulse of amplitude 2.5 A. (Courtesy of L. Zullino)

The phase shift distribution along the length of the device *D2* stressed by the 10 ns vf-TLP pulse, which is shown in Fig. 3.26, is qualitatively similar to the one observed for the TLP stress (cf. Fig. 3.22). The phase shift distribution along the width under this stress condition exhibits a homogeneous current flow along all three lines of interest ("A", "B", and "C" in Fig. 3.26) as shown in Fig. 3.27.

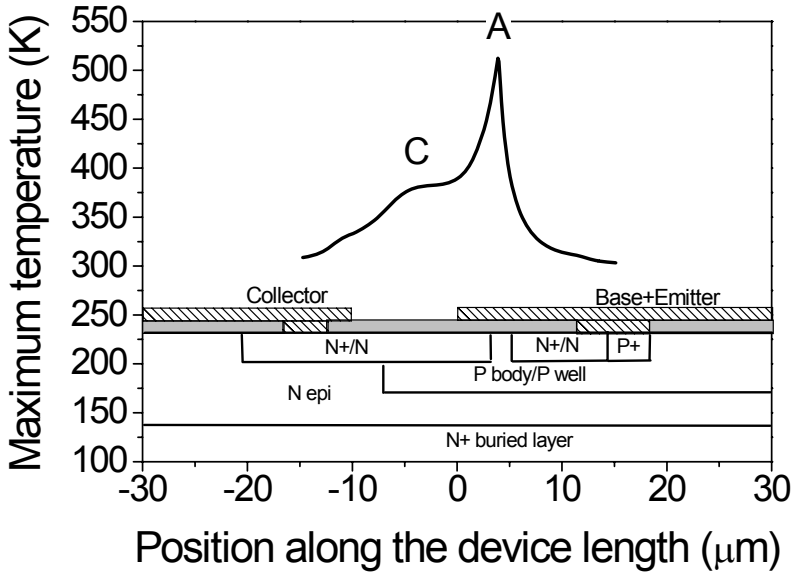


Fig. 3.25: Simulated distribution of maximum temperature along the length of the device D2 exposed to the 100 ns TLP stress of amplitude 2.5 A. (Courtesy of L. Zullino)

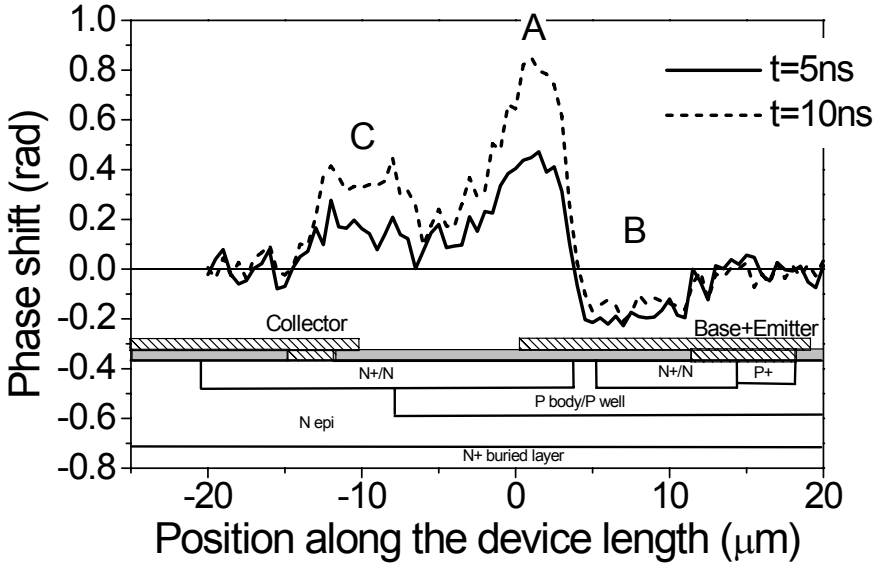


Fig. 3.26: Evolution of the phase shift distribution along the length of the device *D2* stressed by the 10 ns vf-TLP pulse of amplitude 7 A. An aligned simplified cross-section of the device is also given.

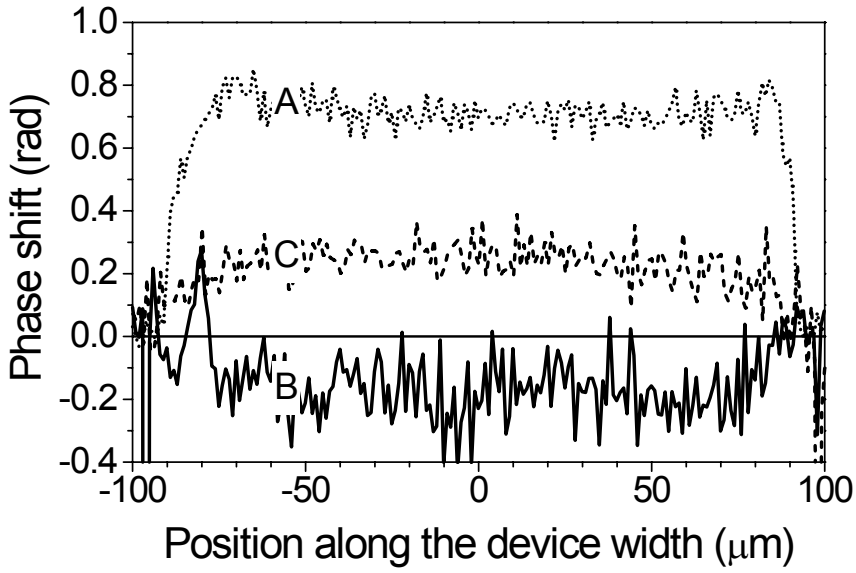


Fig. 3.27: Phase shift distribution along the lines “A”, “B” and “C” (cf. Fig. 3.26) in the device *D2* at the end of the 10 ns vf-TLP pulse of amplitude 7 A.

Finally it is interesting to present the result of failure analysis performed on the device *D2*. Fig. 3.28 shows an emission image overlapped with the backside infrared image of the device *D2* after its degradation. The device degraded when the 10 ns vf-TLP pulse of amplitude 14 A was applied (see Fig. 3.9(b)). The emission places indicate the positions of failure. One failure point is found at the n^+-collector/p-body junction, which could be expected taking into account strong heating at that place (hot spot “A” in Fig. 3.26). The second failure point is found close to the collector contact, and it is attributed to the heat dissipation in the second thermal peak (“C” in Fig. 3.26). The result indicates that the heat dissipation at this point can be strong at high current levels and it can cause a failure of the device. This can be the explanation of lower ESD robustness of the device *D2* in comparison with the device *D1* (cf. Fig. 3.9(b)).

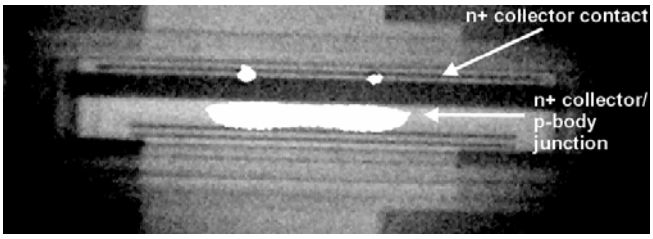


Fig. 3.28: Emission image overlapped with the backside infrared image of the device *D2* after its degradation.

3.3.2.3 Device *D3*

Fig. 3.29 shows the evolution of the phase shift distribution along the length of the device *D3* during the 10 ns vf-TLP stress of level 7 A. The dominant power dissipation occurs, as in the previous devices, at the collector edge of the lateral part of the npn transistor ("A" in Fig. 3.29). The dominant peak is wider in this case, and the heat-dissipating region spreads up to the collector contact ("C" in Fig. 3.29). As the whole collector is embedded into the p-body in this device, this partially isolates it from the n-epi and n^+-buried layer. The vertical npn transistor is therefore expected to be even less active than in the device *D2*. Note that the maximum value of the phase shift in the dominant hot spot is higher than in the device *D1* (compare phase shift value for vf-TLP at "A" in Fig. 3.19 and 3.29). This is because the part of the thermal energy related to the activity of the vertical npn transistor is dissipated in the lateral one.

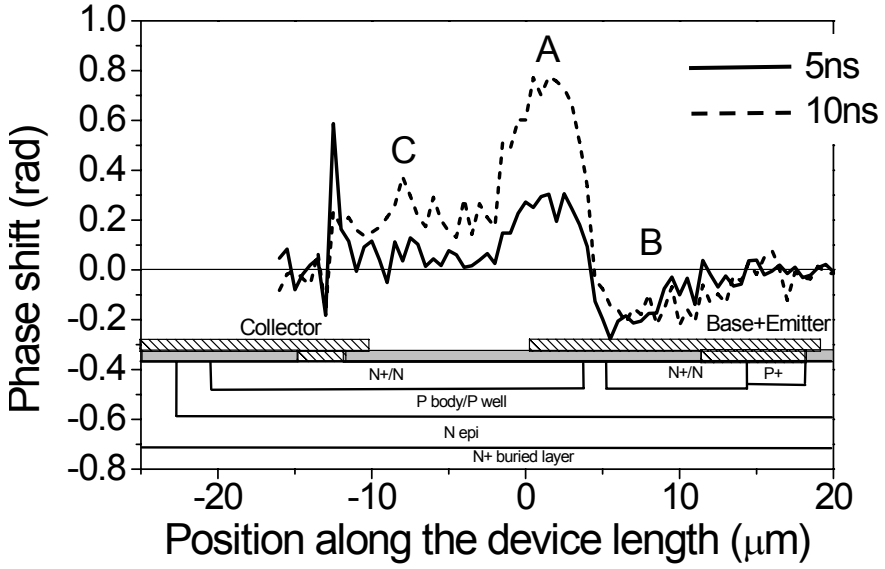


Fig. 3.29: Evolution of the phase shift distribution along the length of the device *D3* stressed by 10 ns vf-TLP pulse of amplitude 7 A. An aligned simplified cross-section of the device is also given.

3.4 Summary

A detailed study of the internal behaviour of BCD ESD protection devices with structural variations stressed by the TLP and vf-TLP has been presented in this chapter. The most important observations are summarised in the following points:

- The OBIC technique was found capable for the localisation of the high electric field regions. The sensitivity of the technique has been improved by biasing of the investigated device into the breakdown-voltage region.
- The transient interferometric mapping technique has been found useful for identification of various current flow dynamics in the devices with different layout. The experimental observations are consistent with the *2D*-simulation results.
- Behaviour of the devices studied in the DC regime by emission microscopy indicated homogeneous current flow in the breakdown regime, however, the turn-on of the npn transistor has been accompanied with current constriction into one point. On the other hand during the pulsed operation with turned-on npn transistor the current flow was found homogeneous.
- Homogeneous current flow in the pulsed regime is the main reason for scaling of the inverse differential resistance with size of the devices. It is also beneficial for the ESD robustness, which was found very high in case of all investigated devices.
- The internal device behaviour during different types of stress has been found very similar and the distinctions are related only to the different stress pulse length.
- The failure analysis showed that the robustness of the investigated devices depends on their layout. The most robust is the device *D1*, where the current flows through both, lateral and vertical transistors. In case of the devices *D2* and *D3* the lateral current flow is dominant over the vertical one, and these devices are less robust than the device *D1*. The failure has been localised at the lateral n^+-collector/p-body junction and under the collector contact in these types of devices.

Chapter 4

Investigation of the smart power DMOS transistors

4.1 Investigation of the VDMOS devices under ESD-like stress

This chapter presents the results of experimental investigation of VDMOS devices built in a smart power process of *Infineon Technologies*, which are exposed to short, high current pulses. Ability of the devices to withstand the ESD-like stress is experimentally studied. Applied pulses are of length varying from 100 ns up to 300 ns, and stress current reaches levels up to 8 A. Experimental results are explained with a help of device simulation.

4.1.1 Devices under study

The investigated SPT VDMOS transistors have the cross section similar as that one shown in Fig. 1.9(a). They are built with the square cell topology and they are of different size varying from 25 to 440 cells. Fig. 4.1 shows the backside IR image of the smallest device with 25 (5×5) cells and IR image of the largest device with 440 (11×40) cells. The white rectangles in the figure mark the device active area, so-called *source field*, which is the region, where the parallel connected source/body cells are built.

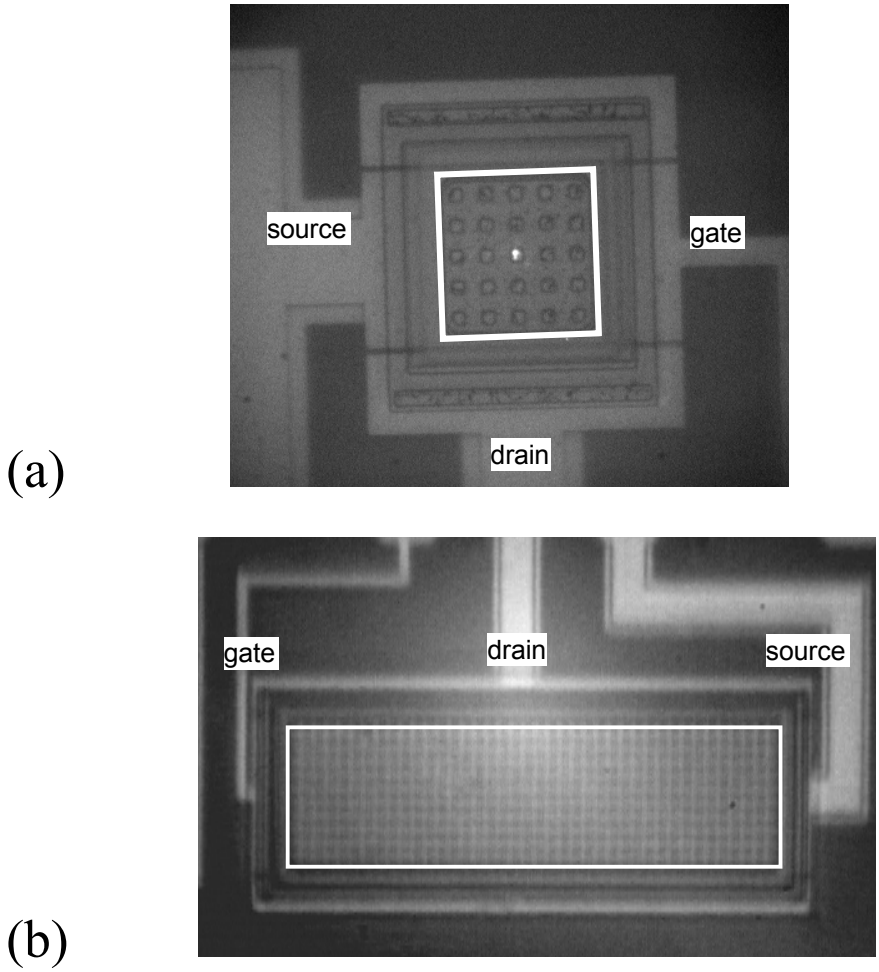
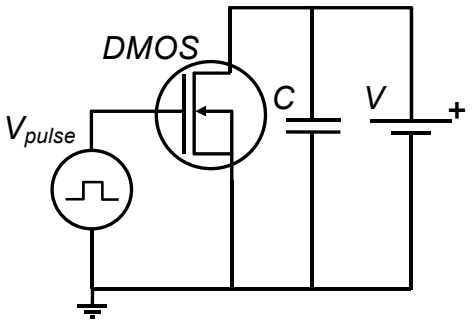


Fig. 4.1: Backside infrared images of the investigated VDMOS devices with (a) 25 cells; and (b) 440 cells. The white rectangles mark border of the source-field.

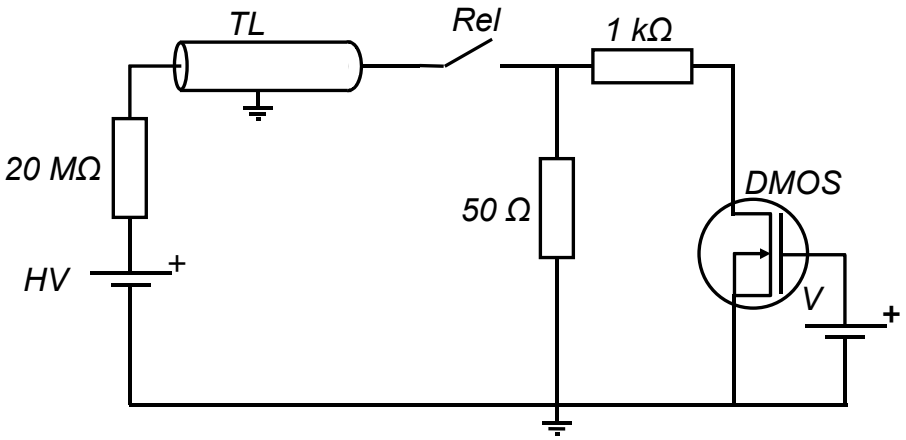
Fig. 4.2 shows the circuit connections, which were used during the investigations:

- Forward bias operation mode with pulsed gate (*FB-PG*, Fig. 4.2(a)): the source is grounded, a constant bias is applied to the drain, and voltage pulses are applied to the gate. The capacitor *C* (*C* = 1000 μF) serves as a "charge reservoir" and its capacitance is chosen sufficiently high, so that the drain voltage is constant during the pulse.
- Forward bias operation mode with pulsed drain (*FB-PD*, Fig. 4.2(b)): the source is grounded, a constant bias is applied to the gate, and current pulses are applied to the drain. The current pulse generator is the TLP. Under this condition only electrical characterisation was performed.
- ESD-like stress with grounded gate (*GG-ESD*, Fig. 4.2(c)): the source and gate are grounded (*GG/FG* switch in Fig. 4.2(c) is closed), and constant current pulses are applied to the drain. The current pulse generators are either the TLP (as indicated in the figure)

a) FB-PG



b) FB-PD



c) GG-/FG-ESD

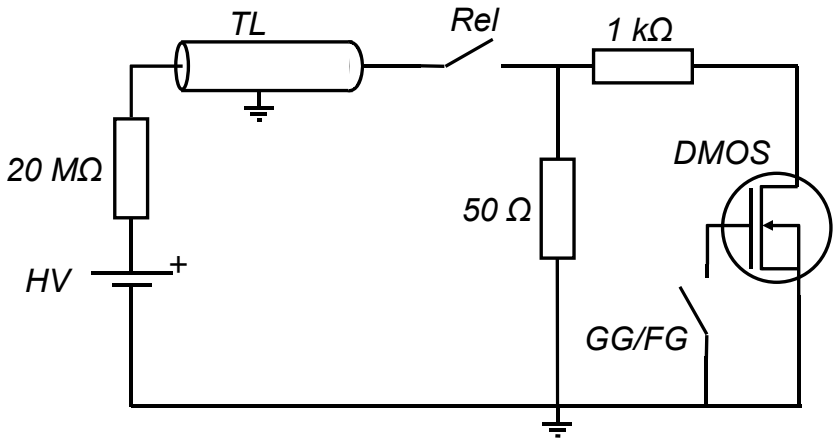


Fig. 4.2: Circuit connection used for investigation of the DMOS devices under various operating conditions: (a) forward-bias operation with pulsed gate; (b) forward-bias operation with pulsed drain, in this specific case using the TLP; and (c) ESD-like stress with grounded or floating gate and pulsed drain, in this specific case using the TLP.

or the SV-4000 pulser. Under this condition the ability of the DMOS devices to withstand ESD pulses is investigated.

- ESD-like stress with floating gate (*FG-ESD*, Fig. 4.2(c)): the same as in the *GG-ESD*, but the gate is left floating (*GG/FG* switch in Fig. 4.2(c) is opened).

4.1.2 Electrical characterisation

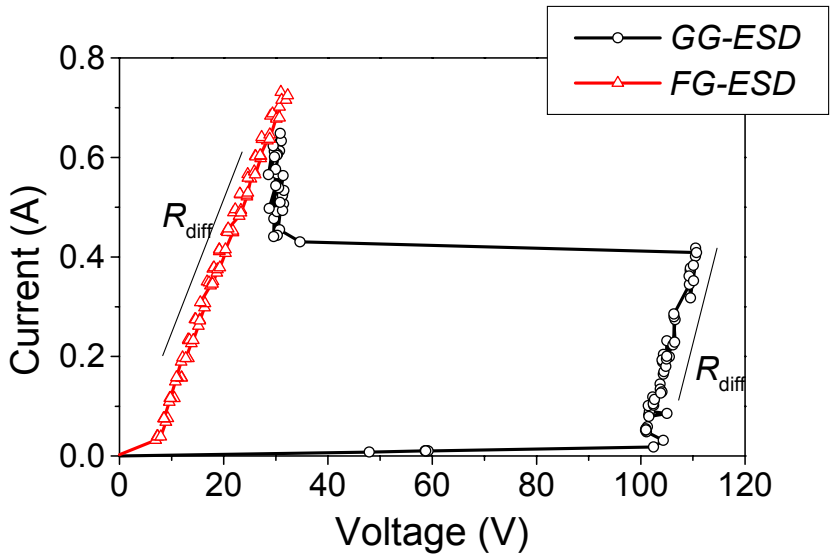
The high current I-V characteristics of the device with 440 cells measured under the *GG-* and *FG-ESD* operating conditions using the 100 ns TLP is shown in Fig. 4.3.

The device breakdown voltage is reached at about 100 V in the *GG-ESD* case (see the black line in Fig. 4.3(a)). Then the I-V exhibits a linear rise with the finite differential resistance $R_{diff} \approx 25\ \Omega$. When the stress current reaches level of 0.4 A, the parasitic bipolar transistor is turned-on. This is accompanied with a drop of the voltage at the device to about 30 V. From this moment the I-V curve is steeper, in other words, the R_{diff} is reduced in comparison with the breakdown region.

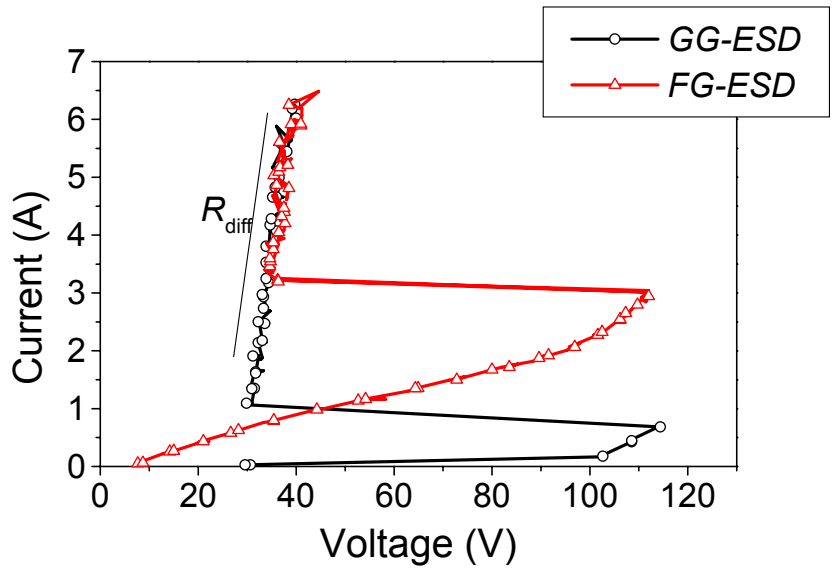
The voltage at the device is substantially smaller under the *FG-ESD* stress compared to the *GG-ESD* case for $I < 0.7$ A (compare the black and red lines in Fig. 4.3(a)). This is caused by opening of the DMOS channel due to capacitive coupling between the drain and gate, which is the consequence of overlap between the gate and n-epi layer (Fig. 4.4). The charge supplied by this capacitive coupling is sufficient to open the channel, which carries the whole injected current. However, at higher current levels the avalanching is started and the parasitic bipolar transistor is activated. This occurs at $I_{stress} \approx 3$ A (Fig. 4.3(b)). From that moment the *FG-ESD* I-V curve follows the *GG-ESD* one, because the device operation is no more controlled by the gate, but by the activated parasitic BJT.

The high current I-V characteristics of the devices with different number of cells (different size) measured under the *GG-ESD* stress are compared in Fig. 4.5. The leakage current (I_{leak}) evolution with the stress current level is also shown, but the reader must be aware that the failure threshold of the devices, which is recognised as a sudden increase of the I_{leak}, can differ from one sample to another.

The $1/R_{diff}$ extrapolated from the breakdown region of the I-V curves measured under the *GG-ESD* stress condition scales with the device size, which is shown in Fig. 4.6. The same holds also for the *FG-ESD* stress condition. Moreover the values of the R_{diff} are very similar under both operating conditions. It is the resistance of the n-epi layer and buried layer, which mainly contributes to the overall R_{diff} in the breakdown regime. When the parasitic bipolar transistor is turned-on, the R_{diff} decreases considerably (more than one order of magnitude



(a)



(b)

Fig. 4.3: High current I-V characteristics of the DMOS device with 440 cells measured under the *GG-ESD* and *FG-ESD* operating conditions using the 100 ns TLP: (a) at stress current levels < 1 A and (b) up to 6 A.

in comparison with the breakdown region), but still depends on the device size. However, the dependence is much weaker than it is in the breakdown region. The decrease of the R_{diff} when the parasitic BJT is activated is caused by conductivity modulation in the n-epi layer.

The high current I-V characteristics of the device operating under the *FB-PD* condition is shown in Fig. 4.7. Four plotted curves correspond to the gate biases of 0 V (which is indeed the *GG-ESD* operating condition and it is shown for comparison); 3 V; 6 V; and 9 V, respectively. Typical MOSFET output characteristics can be clearly distinguished, before the parasitic BJT turns-on. However, once the BJT is triggered, the I-Vs follow the same steep curve regardless of applied V_{GS}. The current level at which the parasitic BJT is activated increases with increasing gate bias, but the triggering voltage seems to be nearly the same up to V_{GS} = 6 V.

Effect of the rise-time on the high current I-V characteristics was also investigated. The I-Vs of the devices were measured under the *GG-ESD* operating condition using the SV-4000 pulser (rise-time of 20 ns), and they were compared to the 150 ns TLP I-Vs (rise-time of 1 ns). No difference between them was found, and it is therefore assumed that the rise-time has also no influence on the overall device behaviour under the *GG-ESD* operating condition.

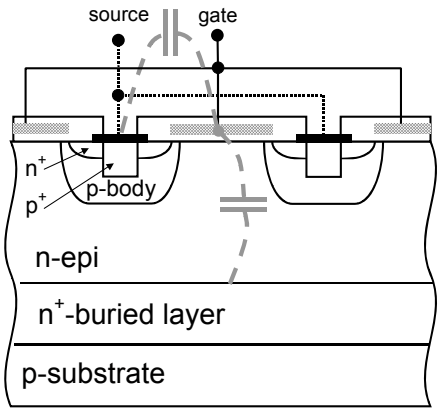


Fig. 4.4: Parasitic gate-coupling in the VDMOS device with floating gate.

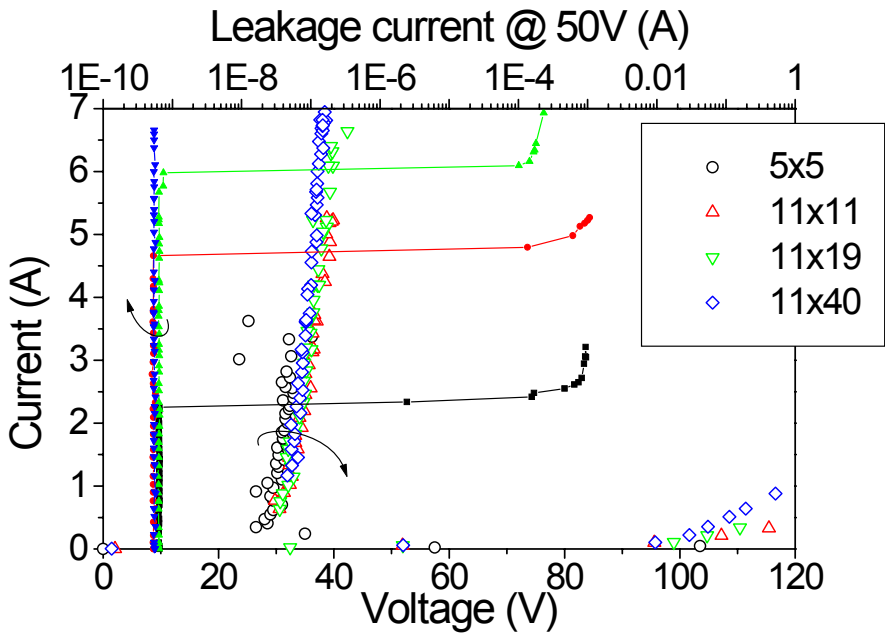


Fig. 4.5: High current I-V characteristics of the DMOS devices of different sizes measured under the *GG-ESD* operating condition using the 100 ns TLP. The leakage current evolution with the stress current level is also given.

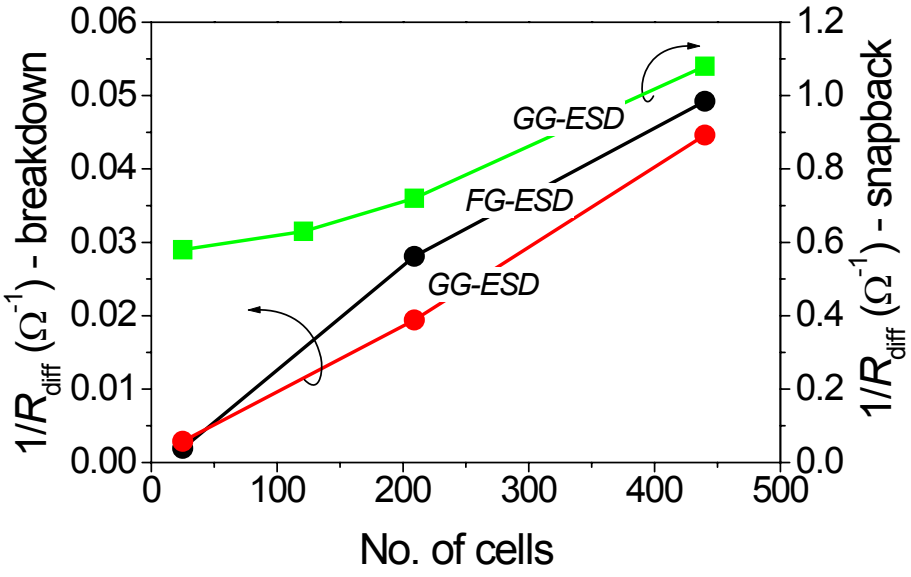


Fig. 4.6: Dependence of the $1/R_{diff}$ of the investigated DMOS devices on the device size.

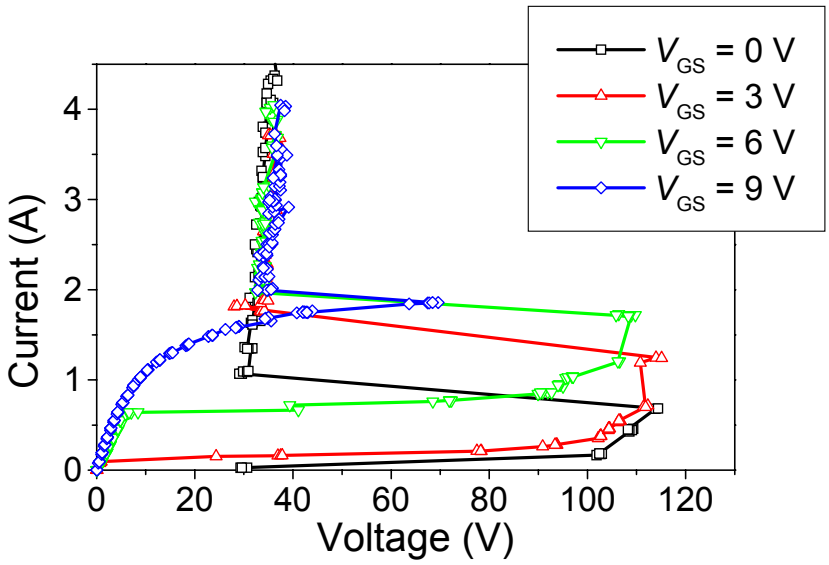


Fig. 4.7: High current I-V characteristics of the DMOS device with 440 cells operating under the *FB-PD* operating condition at various gate biases.

4.1.3 Optical characterisation in the breakdown regime (the parasitic BJT transistor is not active)

Fig. 4.8 shows the results of optical mapping under the *FB-PG*, *GG-ESD* and *FG-ESD* stress conditions in the regime, when the parasitic BJT transistor is not yet activated [Blah03b]. The scanning heterodyne interferometer was used for the investigation. The measured phase shift distributions along 5 cells of the DMOS device are aligned with its simplified cross section.

The green curve shows the phase shift distribution in the device operating in the *FB-PG* mode. Pulses of 8 V amplitude and 150 ns duration were applied to the gate and the drain was biased to 34 V, which resulted in 0.8 A drain current. Localised phase shift peaks are found between the source cells. Interpretation of the results is straightforward: the channel was opened thanks to the voltage pulses applied to the gate, hence the electrons flew through it and then vertically towards the n^+-buried layer (green arrow in Fig. 4.8). The heat dissipation caused by the current flow through the low-doped n-epi layer is the main reason for the observed phase shift signal.

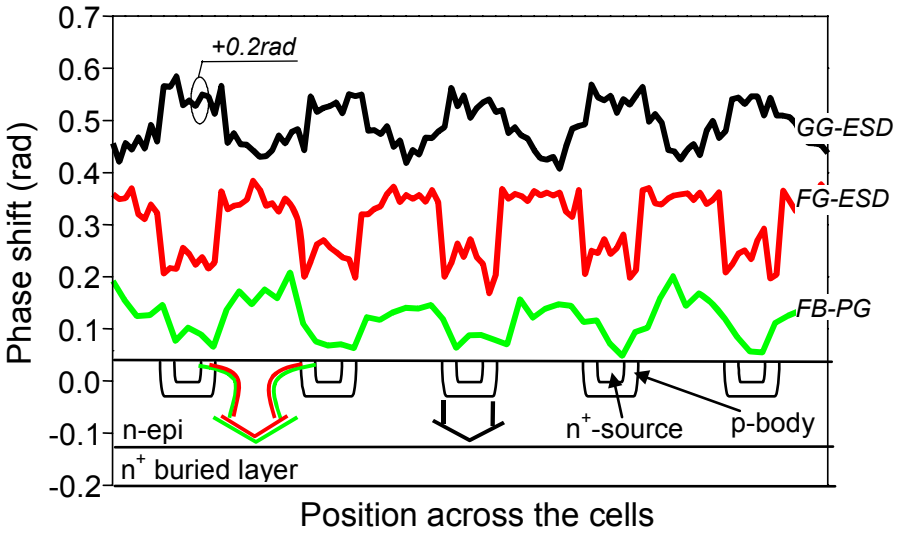


Fig. 4.8: Phase shift distribution along 5 cells of the DMOS device under the *FB-PG* (V_{DS} = 34 V, V_{GS} = 8 V - 150ns, I_D = 0.8 A); *GG-ESD* (I_D = 0.2 A - 300ns); and *FG-ESD* (I_D = 0.8 A - 300 ns) operating conditions at the end of the stress pulse. Simplified cross section of the device with indicated current paths under various operating conditions is also given.

Very similar picture is obtained when the device operates under the *FG-ESD* stress (red line in Fig. 4.8). Current pulses of 0.8 A amplitude and 300 ns duration were applied to the drain in this case. Interpretation is the same as for the *FB-PG* case, but the reason causing the opening of channel is different: it originates from the capacitive coupling between the drain and gate, as explained earlier (cf. Fig. 4.4).

The black curve in Fig. 4.8 shows the phase shift distribution in the device operating under the *GG-ESD* condition. Stress current level was 0.2 A, and stress pulse length was 300 ns. The phase shift peaks are localised at the source/body cells in this case. The channel was not opened and the device was driven into the avalanche breakdown. The impact ionisation took place in the reverse biased p-body/n-epi junction. The phase shift distribution indicates that the maximum electric field and current density were located under the p-body diffusions (black arrow in Fig. 4.8), as expected.

It is also worth to note that the phase shift, and consequently the current, was distributed homogeneously in the device. This is consistent with the linear scaling of the $1/R_{diff}$ as a function of device size in the breakdown region (cf. Fig. 4.6).

4.1.4 Optical characterisation in the snapback regime (the parasitic BJT transistor is active)

As it was presented in the part related to the electrical characterisation (section 4.1.2), once the parasitic BJT transistor turns-on, the I-V curves follow nearly the same trace regardless operating conditions or device dimensions (cf. Fig. 4.3, 4.5 and 4.7). This strongly suggests inhomogeneous current flow of the same nature and it is in detail investigated in the following. All experimental results presented from here on were performed under the *GG-ESD* operating condition.

Fig. 4.9 shows phase shift profiles in the device with 25 cells at the end of consecutive stress pulses of 180 ns duration and 1 A amplitude generated by the SV-4000 pulser. These figures, which were obtained using the *2D* holographic set-up, demonstrate that the triggering of the parasitic bipolar transistor leads to a constriction of the current flow to localised positions, where an excess heat-dissipation takes place. These small localised areas with a high current density are called *current filaments*. It is also obvious that the thermal distribution in the DMOS devices for a constant stress magnitude varies randomly from one stress pulse to another. Localisation and also number of the hot spots are altered. This pulse-to-pulse instability of the triggering position of the parasitic npn transistor is activated by small fluctuations of the current distribution during the first moments of the stress pulse. Despite this unrepeatable behaviour some general features, common to all measurements, were tracked after extensive investigations.

A set of experiments was performed to study the phase shift distribution in the devices at various time instants and current levels. Fig. 4.10 shows typical results of these experiments

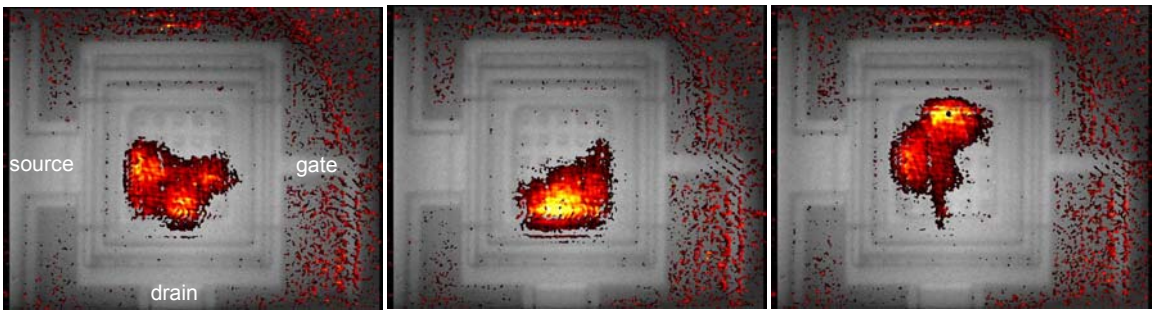


Fig. 4.9: Phase shift distributions in the DMOS devices with 25 cells at the end of consecutive pulses of 180 ns duration and amplitude of 1 A generated by the SV-4000 pulser.

in the device with 25 cells. It was stressed by 180 ns pulse (SV-4000 pulser) of current levels 0.5 A; 1 A; 2 A; and 3 A, and the phase shift was measured in the time instants of 50 ns; 100 ns; and 150 ns. Note that these figures were obtained using the *1*-time instant *2D* holographic set-up, thus only one phase shift profile was captured during a single stress pulse. Nothing can be therefore stated about the specific filament evolution during a stress pulse.

In the first moments of the stress pulse the hot spots are found at the edge of the source field (Fig. 4.10(a),(d),(g)). This is caused by slightly lower breakdown voltage of the source field termination. Usually only one hot spot is observed, but at higher current levels ($I_{stress} \geq 1$ A) two hot spots are sometimes found (Fig. 4.10(d),(g)). The hot spots are randomly localised, and they evolve toward the inner part of the device area with time. The heated area enlarges with increasing stress current level. The whole device active area is heated at t = 180 ns of the 2 A pulse (Fig. 4.10(i)). The stress pulse of 3 A amplitude finally caused a soft degradation[1] of the device.

Fig. 4.11 shows the phase shift distributions in the device with 440 cells at the end of 180 ns pulse (SV-4000 pulser) of variety of current levels from 1 A to 8 A. The inhomogeneous current flow is found again, similarly as in the case of device with 25 cells. The hot spots arise at the longer sides of the source field termination, and never along the shorter one. This is assumed to be caused by layout of the device: the n^+-sinker is realised around the whole source field region, but it is contacted only along the longer sides of the device. Consequently, the voltage at the avalanching junction is the highest at these places, because the voltage drop in the sinker and buried layer causes junction de-biasing at other places. Such behaviour was not observed in the device with 25 cells, most probably due to smaller dimensions. Voltage drop in the metallic lines starts to play a role at higher current levels ($I_{stress} > 2$ A), and thus the hot spots appear only at the side closest to the external drain metallic line (bottom edge of the device in Fig. 4.11). The number of hot spots increases with increasing stress current level. With time the hot spots evolve into the device centre, and the speed of the evolution increases with the stress current level, similarly as in the device with 25 cells. At very high stress current levels (I_{stress} = 8 A) the hot spots seems to be bound to the termination. This is caused by considerable voltage drop in the buried layer. A soft failure was detected after the application of the 8 A stress. Note that the device area is never completely heated.

[1] Soft degradation is called a damage, which causes a small increase of the leakage current or some small change in the reverse I-V characteristics (for more details see the section 4.1.6).

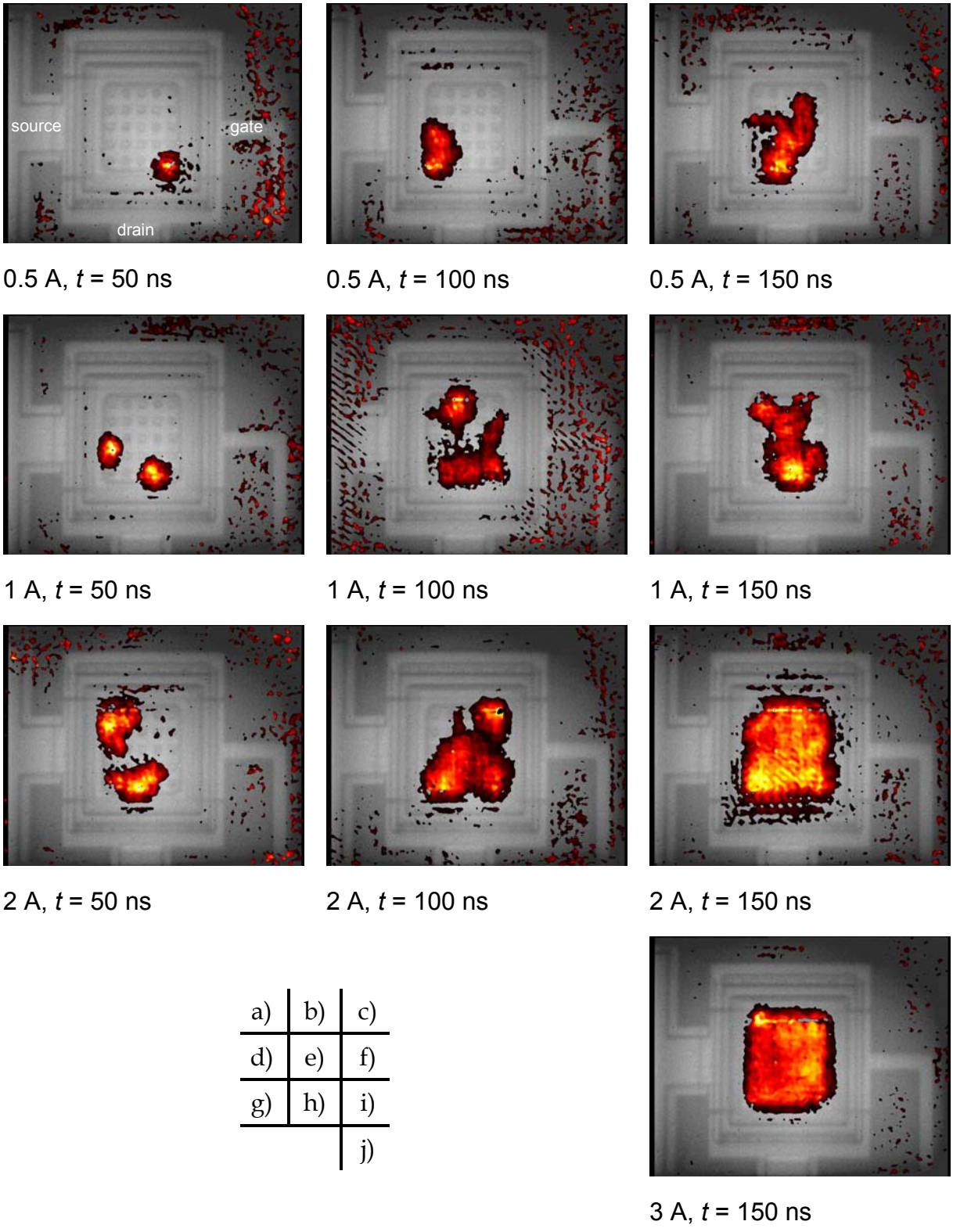
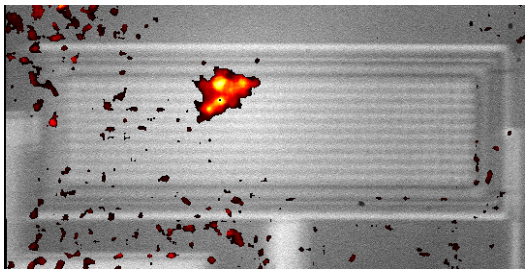
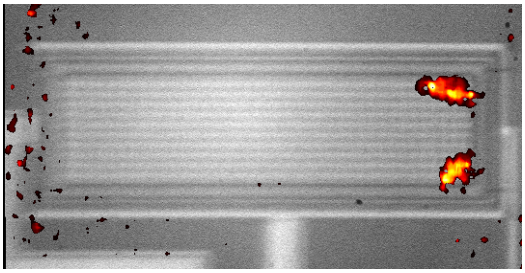


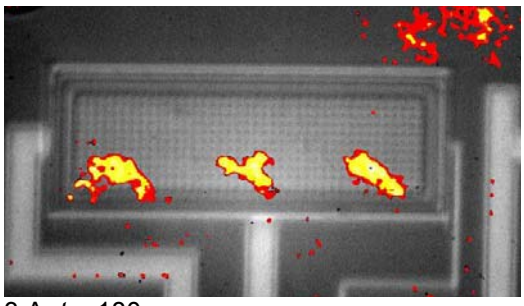
Fig. 4.10: Phase shift distribution in the DMOS device with 25 cells at various time instants and stress current levels. The stress pulses were applied using the SV-4000 pulser.



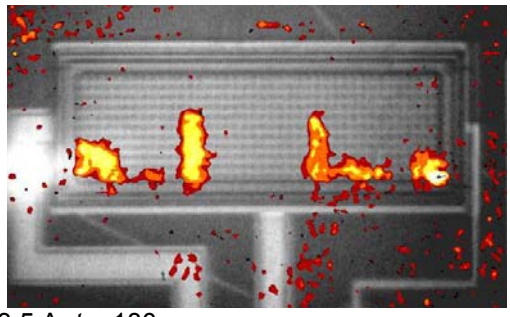
1 A, *t* = 180 ns



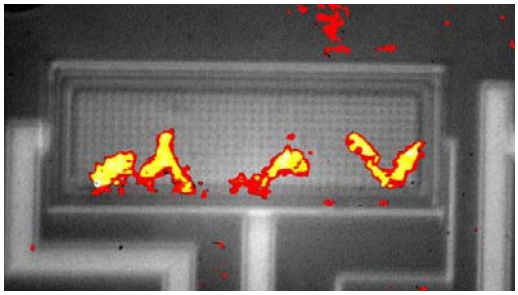
1.5 A, *t* = 180 ns



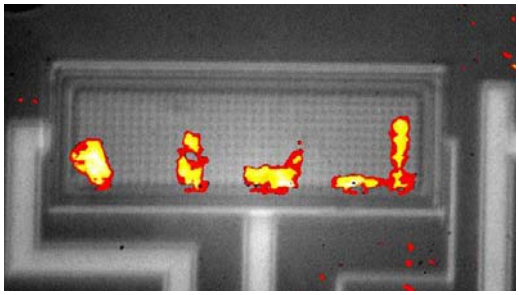
3 A, *t* = 180 ns



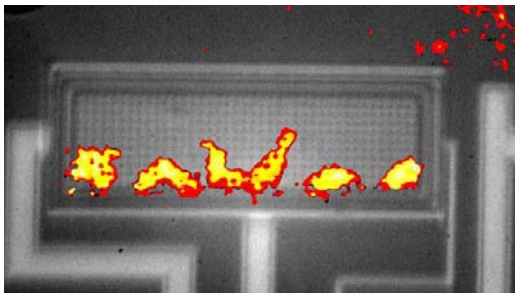
3.5 A, *t* = 180 ns



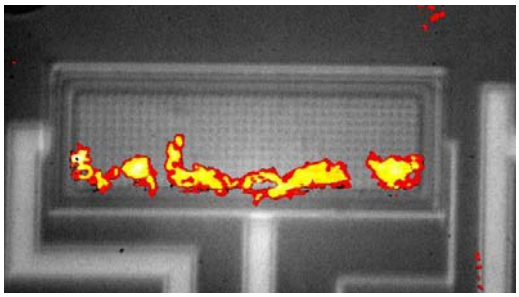
4 A, *t* = 180 ns



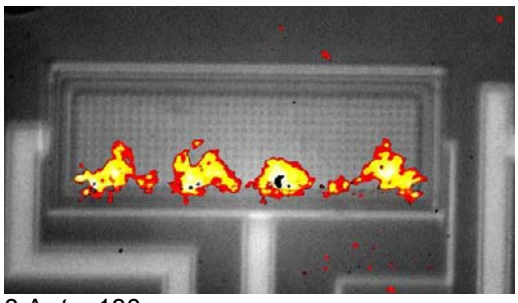
5 A, *t* = 180 ns



6 A, *t* = 180 ns



7 A, *t* = 180 ns.



8 A, *t* = 180 ns

a)	b)
c)	d)
e)	f)
g)	h)
i)	

Fig. 4.11: Phase shift distribution in the DMOS device with 440 cells at the end of the 180 ns long stress pulses of various current levels. The stress pulses were applied using the SV-4000 pulser.

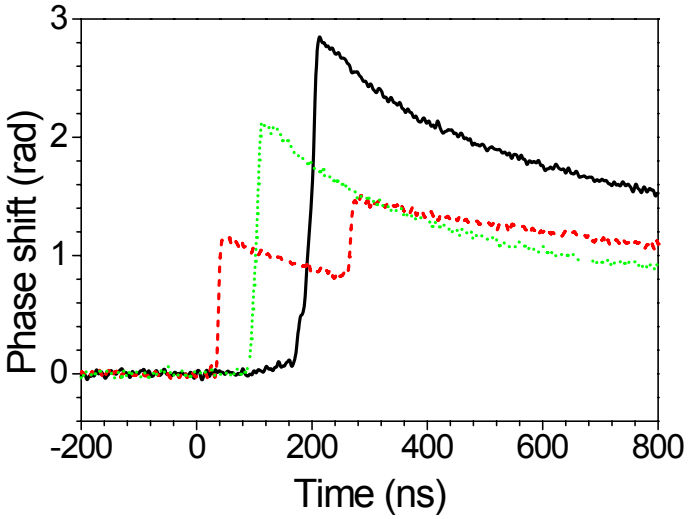
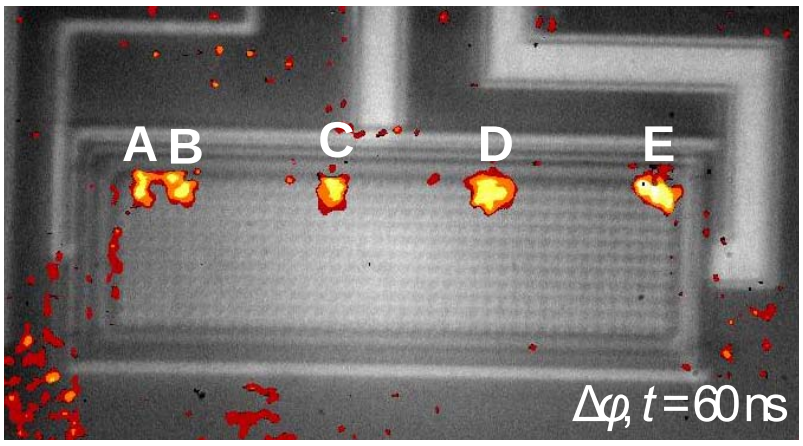


Fig. 4.12: Time evolution of the phase shift at three different positions in the device with 25 cells stressed by 300 ns TLP pulse of amplitude 0.35 A.

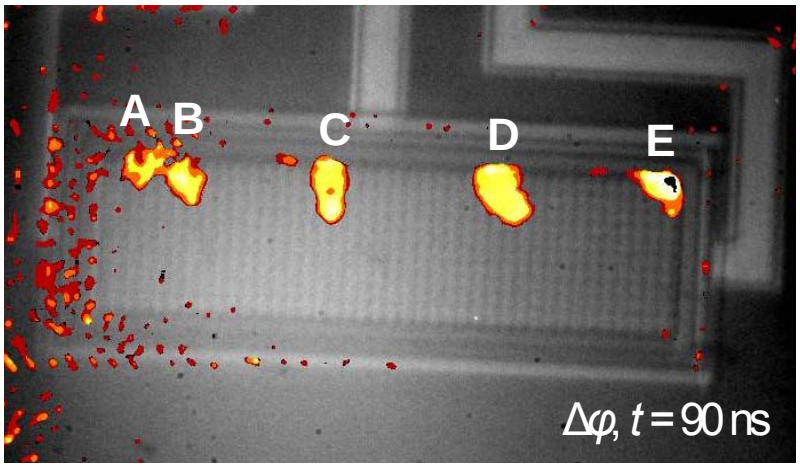
The dynamics of the hot spots evolution presented above suggests that the current filaments move or spread in the investigated devices. *Moving* means that the current density in the filament is roughly constant and filament of approximately constant size "travels" within the device. *Spreading* means that the current conducting area enlarges, i.e. the current density in the filament decreases. In order to find out whether the filaments spread or move with time, transient phase shift measurements at single positions were applied employing the scanning heterodyne set-up. Fig. 4.12 shows the time evolution of the phase shift at three different positions in the device with 25 cells stressed by 300 ns TLP pulse of amplitude 0.35 A. The phase shift evolutions exhibit a fast increase (heating) followed by a slow decrease (cooling). The heating phase lasts only few *ns*. The stopping of the heating indicates that the filament moves, rather than spreads. The power dissipation would only decrease, not stop entirely, if the filament spreading took place, and the phase shift would still rise although with lower slope. Note that the phase shift increase can happen several (2, or even 3) times at certain place during a single stress pulse (dashed red line in Fig. 4.12). This means that the current filament can cross the same place several times during a stress pulse.

Extra evidence of the current filament movement is presented in Fig. 4.13. It shows two *2*-dimensional phase shift distributions in the device with 440 cells aligned with its backside IR image. The device was stressed by 180 ns pulse of amplitude 3 A generated by the SV-4000 pulser. This result is obtained by the *2*-time instant *2D* holographic set-up,

a)



b)



c)

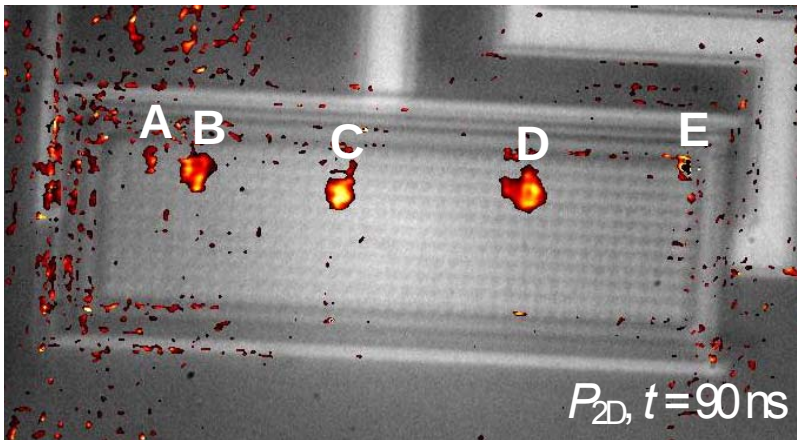


Fig. 4.13: Phase shift distributions in the DMOS device with 440 cells taken at time instants of (a) 60 ns and (b) 90 ns. The device was stressed by 180 ns pulse of amplitude 3 A generated by the SV-4000 pulser. (c) P_{2D} distribution extracted from the phase shift distributions shown in (a) and (b).

i.e. both phase shift profiles are captured within a single stress pulse, specifically in the time instances of 60 ns and 90 ns (taken from the pulse begin). This means that one can follow activity of the filaments in time.

Five hot spots are observed in t = 60 ns ("A" to "E" in Fig. 4.13(a)). After next 30 ns (i.e. in t = 90 ns, Fig. 4.13(b)) the hot spots "A" to "D" has extended, the hot spot "E" does not seem to change. As was presented in [Dube04b], it is possible to calculate the P_{2D} profile at t = 90 ns from these two figures. This is shown in Fig. 4.13(c). Four separate P_{2D} peaks are all found inside the source-field region ("A" to "D" in Fig. 4.13(c)). This confirms that the filaments *moved* from the termination where they were observed at the beginning of the stress pulse inside

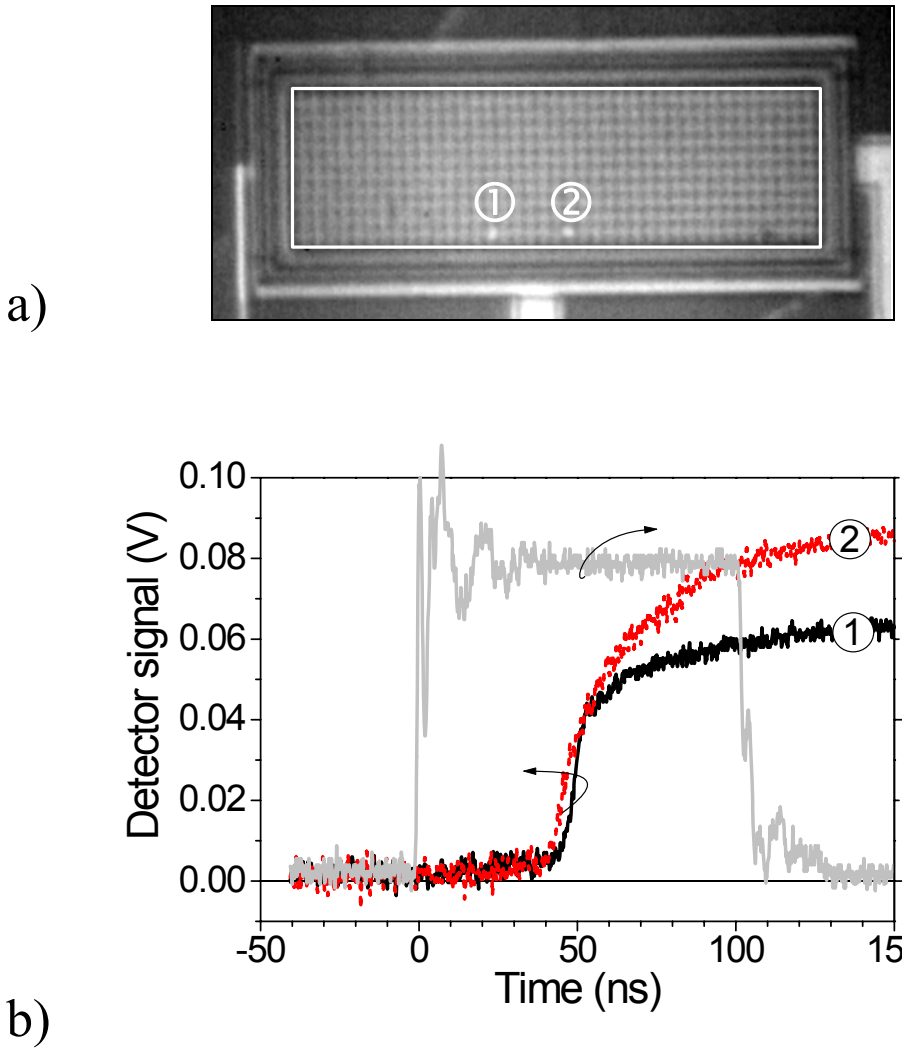


Fig. 4.14: (a) Positions probed by the laser beams during the investigation of coexistence of current filaments in the DMOS device with 440 cells. (b) Phase shift evolution at positions ① and ② indicated in (a). The stress current waveform is also given (100 ns TLP pulse of amplitude 2 A).

the active region. But this figure (Fig. 4.13(c)) provides even more information. It can be seen that the size of the current filament spans over several cells ("B" and "C" in Fig. 4.13(c)). Moreover it is seen that current filament "E" is no more active at $t = 90$ ns.

Another question that arose during the investigation was, whether the multiple filaments coexist at the same time, or the current oscillates between the hot spots. Fig. 4.13(c) suggests that the filaments could coexist, but one has to keep in mind that the uncertainty of this result is 30 ns. If a fast current oscillation between filaments exists (cf. Fig. 4.12, where heating phase lasts < 10 ns), it is not seen, but one gets only an averaged picture. To check the coexistence with a better time resolution, the dual-beam Michelson interferometer set-up was employed.

Two laser beams were positioned on the device as shown in Fig. 4.14(a). These places were chosen according to the highest probability of the filament occurrence. After application of several stress pulses, the time evolutions of the phase shift shown in Fig. 4.14(b) were observed. They prove simultaneous heat dissipation at the locations ① and ②, and demonstrate the coexistence of the current filaments. Note that the phase shift rises at both places even after the stress pulse end. This can be explained by a heat transfer from the neighbouring position toward which the filament has moved.

4.1.5 Discussion

In order to understand processes related with the activity of the parasitic bipolar transistor in the investigated devices, *2D* and *3D* electro-thermal simulation has been performed [Deni03, Deni04b].

Fig. 4.15 shows the results of the *2D* simulation of two neighbouring VDMOS cells at current level slightly above snapback. Temperature distribution (greyscale), electron current flow-lines (black arrows) and the avalanche region (white contour line) are shown at four time instances during the stress pulse. As has been already proved experimentally, the breakdown under the *GG-ESD* stress takes place under the DMOS cells, where also the highest current density is expected (cf. Fig. 4.8). A residual temperature is still observable at these places ("A" in Fig. 4.15, $t = 15$ ns). When the parasitic npn transistor is turned on, the current path is shifted toward the side of a cell (Fig. 4.15, $t = 15$ ns), where the gain of the parasitic transistor is the highest. With the parasitic BJT turned-on, the n-epi region is overwhelmed by the free carriers injected from the source (emitter of the parasitic BJT transistor). Increased free carrier concentration modulates the conductivity of the n-epi region, which is observed as the decrease in the differential resistance R_{diff} in the high current I-V characteristics (cf. Fig. 4.6). Besides, the high electric field region is shifted from the p-body/n-epi junction toward the n-epi/n^+-buried

layer junction (Fig. 4.15, t = 35 ns). This is so-called *Kirk*, or *base push-out* effect [Kirk62], which has been previously reported to take place also in LDMOS devices [Bose01, Merg00]. As temperature increases in the pushed-out avalanche region, the impact ionisation rate decreases, because the temperature coefficient of the impact ionisation is negative [Sze81]. Hence, the avalanche region starts to move to colder areas (to the left, compare t = 35 ns and t = 45 ns in Fig. 4.15). The left cell is activated (Fig. 4.15, t = 45 ns) and finally takes over the current completely. The right cell is turned off (Fig. 4.15, t = 65 ns). At higher current levels the triggering of the left cell is faster and the current is then shared between both cells [Deni04b]. Any other movement is afterwards impossible in this limited system of 2 cells.

Apart from the transfer of bipolar activity from one cell to another, the movement of the current filament is possible also along the p-body, i.e. around a single cell [Deni04b]. It is controlled by the same mechanism of thermally driven motion of the impact ionisation region. It depends on the actual thermal gradient, distance between the cells and buried layer resistance, whether the transfer of activity from one cell to another or the movement along the p-body of a cell occurs.

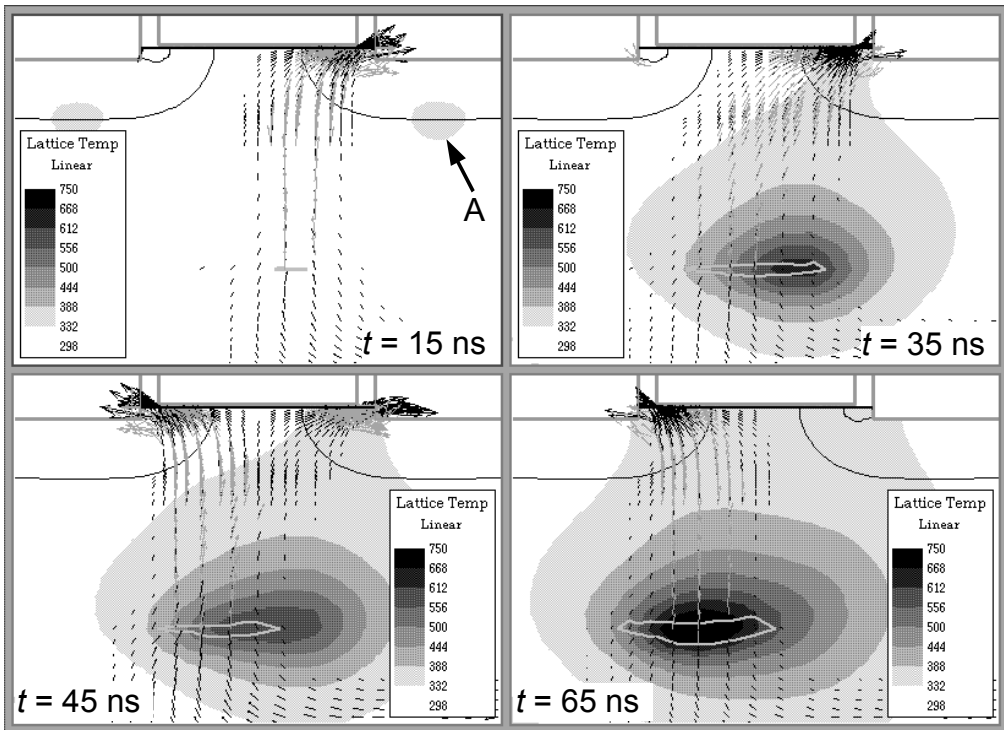


Fig. 4.15: *2D* simulation of two neighbouring DMOS cells at current level slightly above the snapback level. Lattice temperature (greyscale), current density (black arrows), and impact ionisation region (white contour line) are shown. (Courtesy of M. Denison)

The movement of the current filament within an array of cells can be visualised using 3D simulation. Fig. 4.16(a) shows the structure used for the simulation: it consists of four quarter-cells. The simulated impact ionisation rate and temperature in the depth of the base pushed-out region are shown in Figs. 4.16(b) and (c), respectively. The simulated electron current density in the depth of the source contact is shown in Fig. 4.16(d). When the stress pulse is applied, cell ① triggers first. Cell ② is triggered after about 10 ns, while the cell ① is still active (Fig. 4.16(c), t = 15 ns). The impact ionisation region is located between the cells ① and ② in that moment (Fig. 4.16(a), t = 15 ns). As the temperature rises at the initial position (Fig. 4.16(b), t = 15 ns), the centre of the impact ionisation starts to move against the temperature gradient towards cooler region, in this specific case towards the cell ① (Fig. 4.16(a), t = 32 ns). The filament moves around it and in few moments the cell ③ is activated (Fig. 4.16(c), t = 35 ns). The cell ② is turned off (Figs. 4.16(c), t = 42 ns). The initial hot spot cools down and temperature increases at the new position (Fig. 4.16(c), t = 42 ns). This process is repeated clockwise around the four cells.

These simulation results reveal that the filament movement in the studied DMOS devices is thermally driven process. Spatial fluctuations of temperature initialise the movement and thermal gradient guides it [Rodi04, Poga05]. Three factors are crucial for the movement:

- Sufficient spatial separation of the heat dissipating avalanche region from the source/body (emitter/base) junction due to base push-out effect. This limits thermal coupling between the mentioned regions. One has to keep in mind that the bipolar transistor has positive temperature coefficient of the current gain [Sze81]. If the hot spot was localised too close to the injecting junction, the thermally influenced bipolar activity could dominate the action and stop the movement of the current filament. The positive feedback would soon lead to thermal runaway and cause a failure of the device.
- Continuous buried layer. It allows a free movement of the avalanching region towards colder regions.
- Discrete cell layout. It allows transformation of the current conduction from one cell to another in two dimensions. It was shown that if not cells but stripes were used, movement only along one dimension - along the stripe - would be possible [Deni04a].

With this knowledge one can better understand the experimental observations. Higher stress current level increases the speed of the filaments, because the temperature gradient is larger as a consequence of the increased heat dissipation in a filament. It was shown in [Poga05] that the speed of the moving current filament is $v_f \propto \sqrt{P}$, where P is the total power dissipation in the filament. However, at very high current levels the filament movement is not fast enough to prevent local overheating, which could initialise thermal generation of free

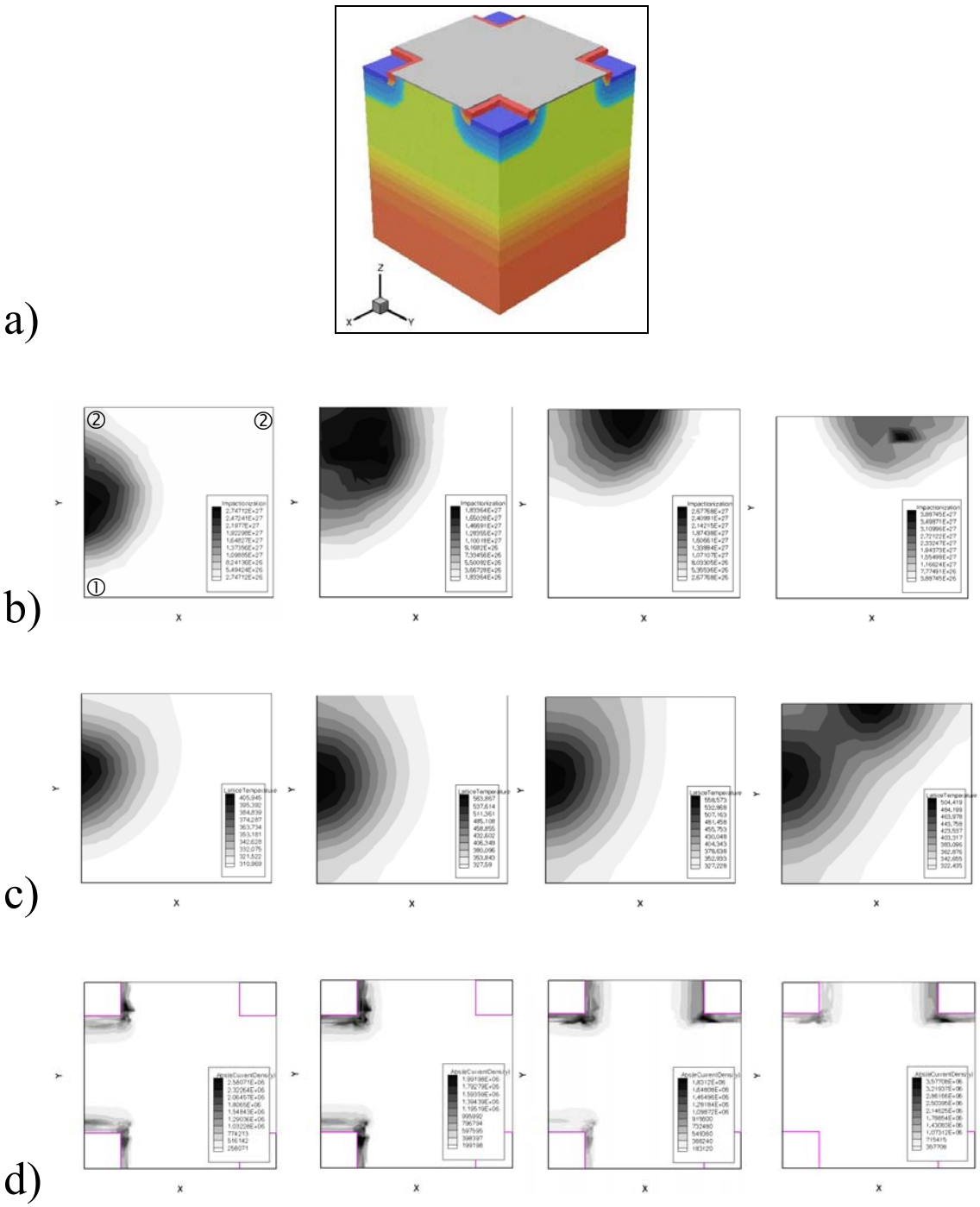


Fig. 4.16: *3D* simulation of the filament movement in the structure with 4 quarter-cells: (a) cross section of the simulated structure; (b) impact ionisation rate in the depth of the base pushed-out region; (c) temperature in the depth of the base pushed-out region; and (d) electron current density in the depth of the source contacts. (Courtesy of M. Denison.)

carriers and consequently leads to a failure of the device. This could be the failure mode observed in case of the device with 440 cells under 8 A stress, although it was not completely heated (c.f. Fig. 4.11(i)).

In conclusion, the filament movement limits heat dissipation in a single position and thus improve the current handling capability of the devices. This is favourable for the ESD robustness, which is indeed experimentally proved to be very good (e.g. for DMOS device with 440 cells the TLP failure threshold is in some cases as high as 8.5 A).

4.1.6 Failure analysis

Failure of the investigated devices was detected as an increase in the drain leakage current. This is the reverse drain-to-source current measured with the grounded gate. It reaches order of several tens of *pA* in a virgin device and it is attributed to the generation-recombination current of the reverse biased p-body/n-epi junction. When the device failed, either an abrupt increase of the leakage current into the *mA* region was observed (referred as *hard failure*), or the leakage current increased progressively, starting with a rise to the *μA* level (referred as *soft failure*). The probability of occurrence of either failure mode did not seem to be dependent on the stress pulse duration or stress current level (see also [Heer05]).

Fig. 4.17 shows the progressive evolution of the leakage current I_{leak} of the device with 440 cells stressed by the 300 ns long pulse of amplitude 2 A generated by the SV-4000 pulser. A kink in the reverse DC I-V characteristics was found, when the first stress pulse was applied (curve ① in Fig. 4.17). It suggests that the damage is located away from the p-body/n-epi space charge region at V_{DS} = 0 V, because certain voltage has to be applied to extend the space charge region of the p-body/n-epi junction towards it [Poga00]. Additionally, a black spot was found in the device active area (Fig. 4.18). When focusing on the top metal, the black spot is not sharp (Fig. 4.18(a)). One had to go into the depth of the structure to focus on the black spot (Fig. 4.18(b)). This means that the black spot is localised in the bulk. It was estimated that the damage is approximately in the depth of 5 μm, which is approximately the depth, where the n-epi/n^+-buried layer junction is realised. This is consistent with localisation of the avalanching region after the base push-out. It was the excess heating at this place, which caused the damage. When few additional stress pulses were applied, another black spot was found (Fig. 4.19), but no change in the leakage current was observed. In case of this new black spot it was not possible to exactly localise its depth – it seemed like it is

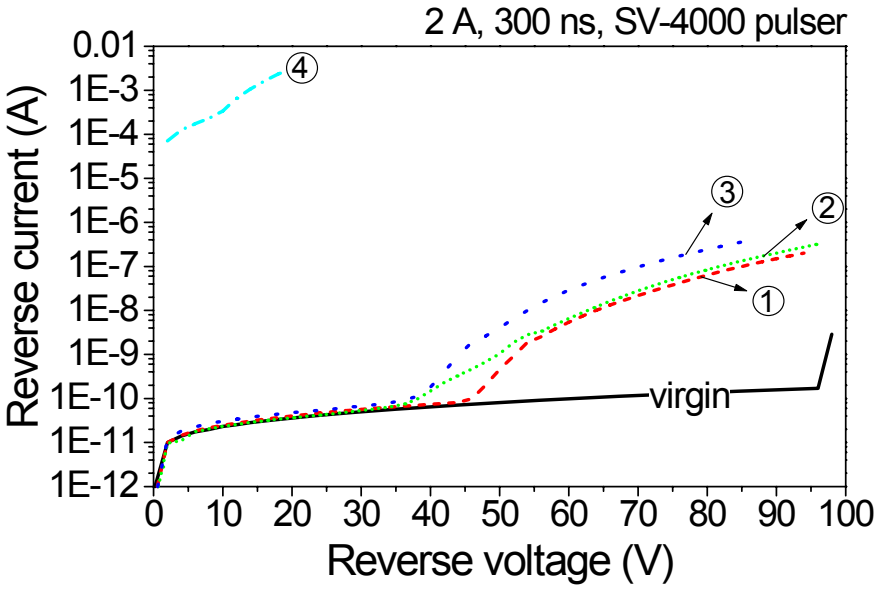


Fig. 4.17: Leakage current evolution in the DMOS device with 440 cells exposed to destructive stress pulses.

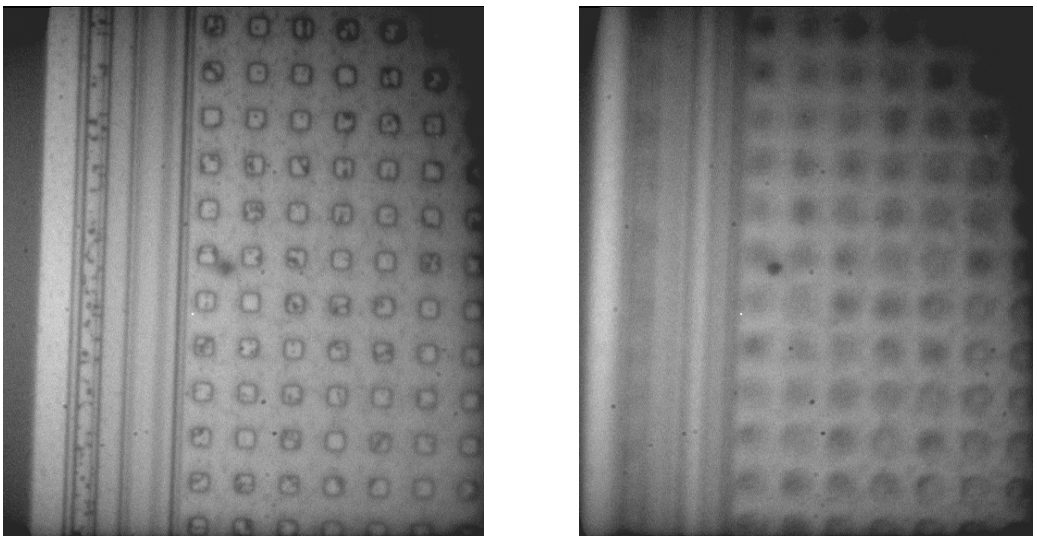


Fig. 4.18: Black spot found in the DMOS device with 440 cells after application of the stress pulse of 2 A amplitude and 300 ns time duration generated by the SV-4000 pulser. (a) focus on the top metal; (b) focus on the black spot.

spread over a larger distance. Two additional stress pulses caused a shift of the kink in the DC I-V characteristics to lower voltages (curve ② in Fig. 4.17) and a small increase of the leakage current at higher voltages (curve ③ in Fig. 4.17), respectively. Following stress pulse led to a catastrophic failure and the leakage current exceeded 1 mA (curve ④ in Fig. 4.17). No change in already found black spots was detected and no additional black spots were observed after this event.

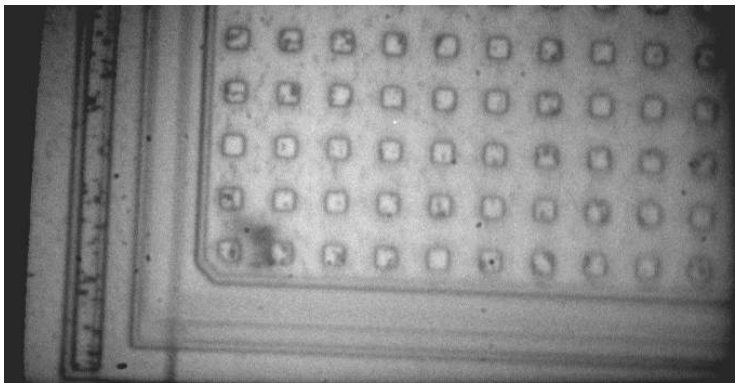


Fig. 4.19: The second black spot found in the DMOS device with 440 cells after several stress pulses of 2 A amplitude and 300 ns time duration generated by the SV-4000 pulser.

The process of device degradation was also captured during the investigation of the device with 440 cells by means of the *2*-time instant *2D* holographic set-up. The studied device was stressed by the 250 ns long pulse of amplitude 3 A generated by the SV-4000 pulser. Fig. 4.20 shows the phase shift profiles saved during consecutive stress pulses at time instances of 60 ns and 200 ns. When the first few stress pulses were applied, a typical picture of randomly arranged hot spots is observed (Fig. 4.20(a) to (d)). But from certain moment a collapse of the current into single filament can be followed (Fig. 4.20(e) to (l)). Afterwards a hard failure of the device was detected (the leakage current exceeded 1 mA level), and a black spot was found at the place of this current filament (marked by circle in Fig. 4.21). Unfortunately, the leakage current was not measured after each stress pulse, so the phase shift profiles cannot be related to its evolution, which would be beneficial for understanding of the failure mode.

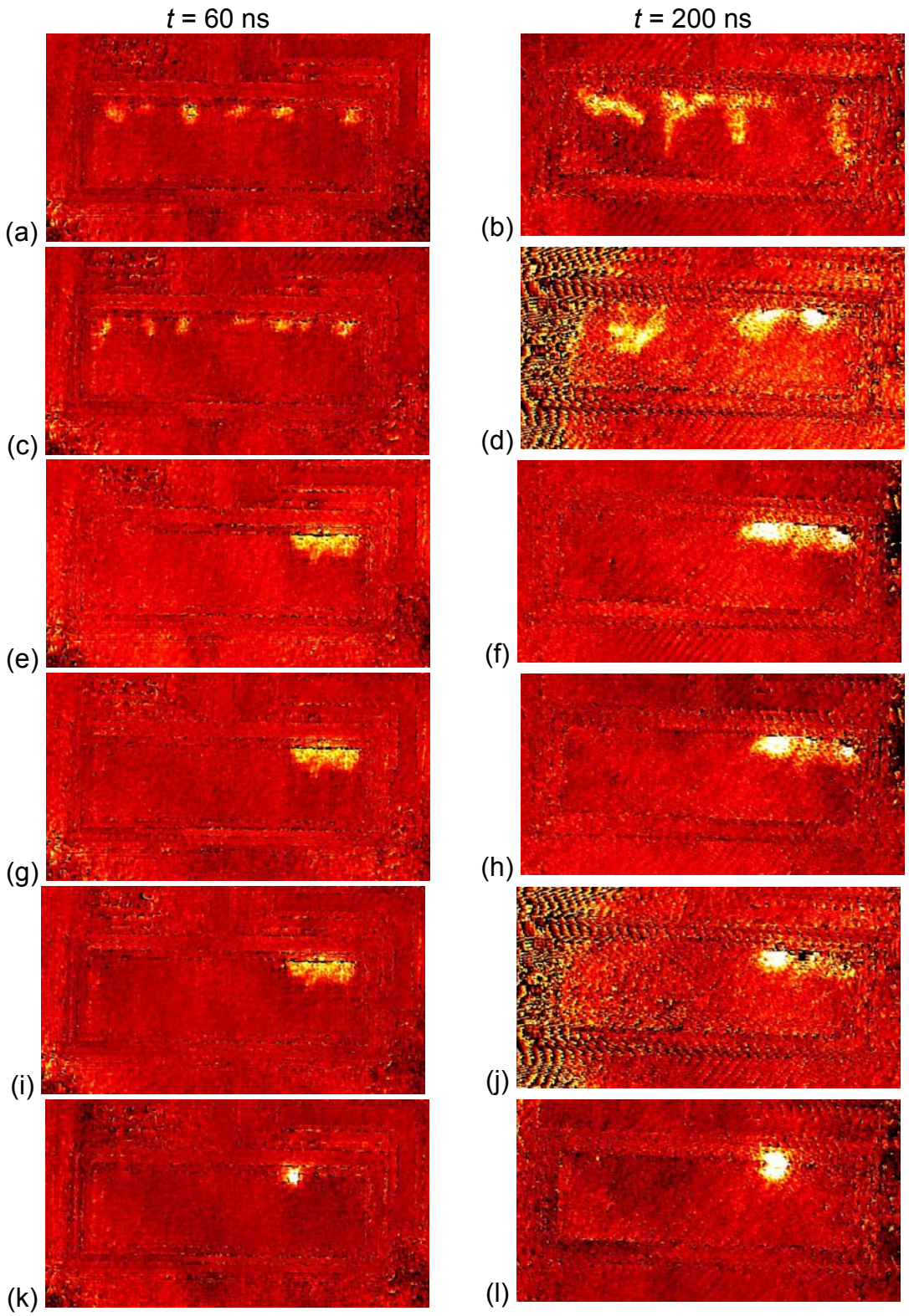


Fig. 4.20: Process of device degradation. During consecutive stress pulses the current collapsed into a single filament. The device was stressed by the 250 ns long pulses of amplitude 3 A (SV-4000 pulser).

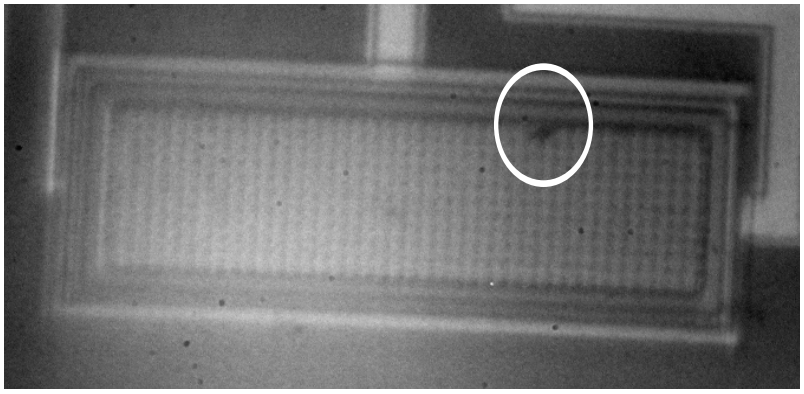


Fig. 4.21: Black spot found after sequence of destructive pulses presented in Fig. 4.20.

If the failure threshold data accumulated during the investigations are put together, they can be related to the device size and stress pulse length. Fig. 4.22 shows the dependence of the failure threshold on the device size (number of cells) for the *GG-ESD* operating condition measured using the 100 ns TLP. The data spreading is not negligible, but it can be in general summarised that the failure threshold increases with the size of the device.

The failure threshold dependence on the stress pulse length in the device with 440 cells is shown in Fig. 4.23. These data are collected from the optical characterisation experiments, when the devices were stressed by the SV-4000 pulser, which allows an easy adjustment of the stress pulse length. It can be seen from the dependence that the failure threshold decreases with increasing stress pulse length. This is indeed interesting, because the device with 440 cells is far away from being completely hot even at the longest stress pulses (cf. Fig. 4.11 and Fig. 4.20). One would expect that if there were a cool region in the device, the filament would move there, preventing in such way the device failure. However, the experiments showed that it is not like that. When the pulse length increases, the thermal diffusion length increases. The heat diffused from the distant n-epi/n^+-buried layer starts to influence the source/body junction (thermal diffusion length is about 4 μm for 250 ns) with the consequence of motionless filament, as mentioned at the end of the section 4.1.5. Contrary to the device with 440 cells, the device with 25 cells is rather small and the speed of filament was high enough to heat up the whole device active area before the above-described effect can take place.

Finally an extensive investigation was performed to find out whether a long-term cumulative degradation takes place in the studied DMOS devices. The expression “long-term cumulative degradation” means in this case a *slowly* progressing damage in the device exposed to high number of stress pulses. Several thousands of stress pulses with amplitude close to the expected failure threshold were applied. However, no evidence of such degradation phenomenon was found (see also [Heer05]).

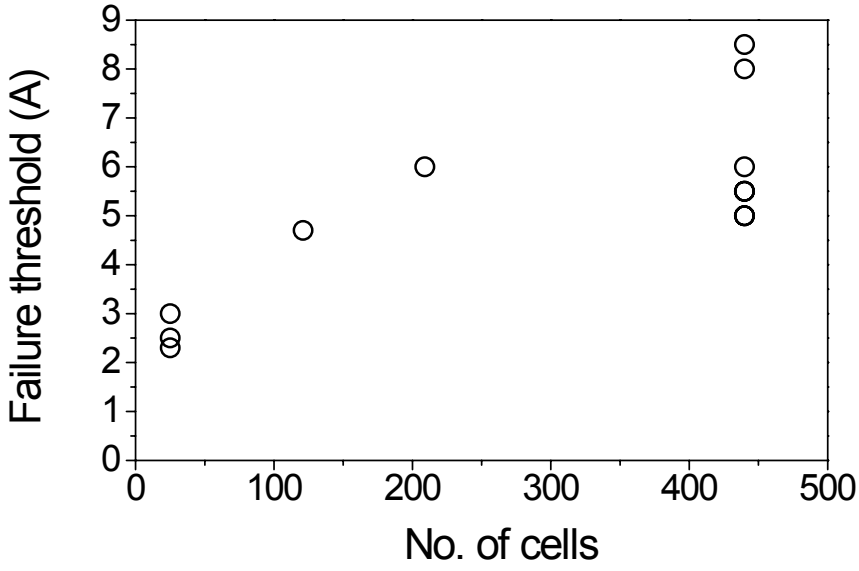
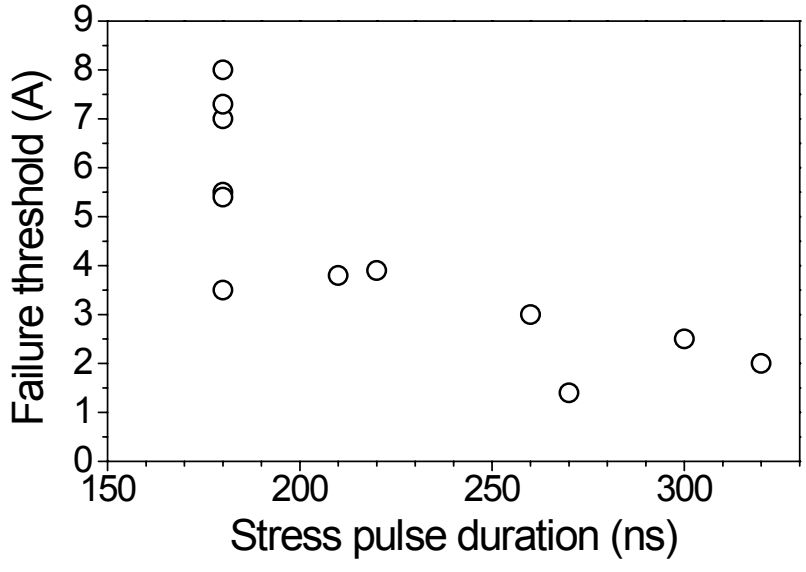


Fig. 4.22: Dependence of the failure threshold on the device size for *GG-ESD* operating condition measured using the 100 ns TLP.



4.23: Dependence of the failure threshold on the stress pulse duration in the device with 440 cells operating under the *GG-ESD* condition and stressed by the SV-4000 pulser.

4.1.7 Summary

Detailed experimental investigation of the vertical DMOS transistor exposed to ESD-like pulses were presented.

At small current levels, when the parasitic BJT was not turned-on, the current flow in the studied devices was found homogeneous. Thanks to spatial resolution of the scanning heterodyne interferometric set-up, it was possible to distinguish activity of individual cells in the studied devices.

With the turn-on of the parasitic BJT the current flow became strongly inhomogeneous: the current filaments appeared. They were formed randomly along the device termination, which is attributed to the lower breakdown voltage in this region. During the stress pulse the filaments were moving in the active region of the devices. The speed of this movement was found dependent on the stress current level. It has been also experimentally proved that several moving current filaments can coexist in the studied devices.

The mechanism of filament movement was understood thanks to the *2D* and *3D* device simulation. It was shown that it is a thermally driven process originating in the shift of impact ionisation region along an individual cell or from one cell to a neighbour one. The dominant factor, which allowed the movement, is the layout of studied devices, namely spatial separation of the avalanching region and forward biased n^+-source/p-body junction, discrete cell structure and continuous buried layer. The filament movement was found beneficial for ESD robustness, because it limited local overheating.

4.2 Investigation of the DMOS devices in the thermal SOA region

This chapter presents exploratory results of the experimental investigation of thermal behaviour of large DMOS devices exposed to long pulses of *ms* time duration using the TIM technique. This investigation was motivated by need to experimentally examine the device behaviour operating close to the border of thermal SOA. The chapter discusses possibilities of the TIM technique to be used for such type of investigation and it provides perspective ways of its further development.

4.2.1 Experimental results

The studied device was a large VDMOS transistor of size nearly 1 mm^2, which was composed of 6 parallel fingers. It was built within an SPT process of *Infineon Technologies*. During experiments the device was connected in the same way as depicted in Fig. 4.2(a) (*FB-PG* operating condition). The operating point was set in the region where $V_{GS} < V_{TCP}$ (the temperature coefficient of drain current is positive); in the region where $V_{GS} > V_{TCP}$ (the temperature coefficient of drain current is negative); and to the temperature compensation point TCP ($V_{GS} = V_{TCP}$) where the drain current is temperature independent (cf. Fig. 1.11). The scanning heterodyne interferometric set-up and the *2D* holographic set-up were employed for thermal mapping.

Figs. 4.24(a) and (b) show typical drain current evolutions[1] during 1 ms long power pulse, when the device operated with the gate bias below and above TCP, respectively. The drain current tends to increase (Fig. 4.24(a)) or decrease (Fig. 4.24(b)) with time, depending on the working point. As shown in [Deni04a] by simulation, the current is distributed inhomogeneously in the device during these operating conditions. It tends to focus in the central part of the device when $V_{GS} < V_{TCP}$, while it is redistributed toward the device periphery when $V_{GS} > V_{TCP}$. In order to investigate this behaviour experimentally, the TIM method was employed.

[1] For the sake of confidentiality the drain current values are not shown in this chapter.

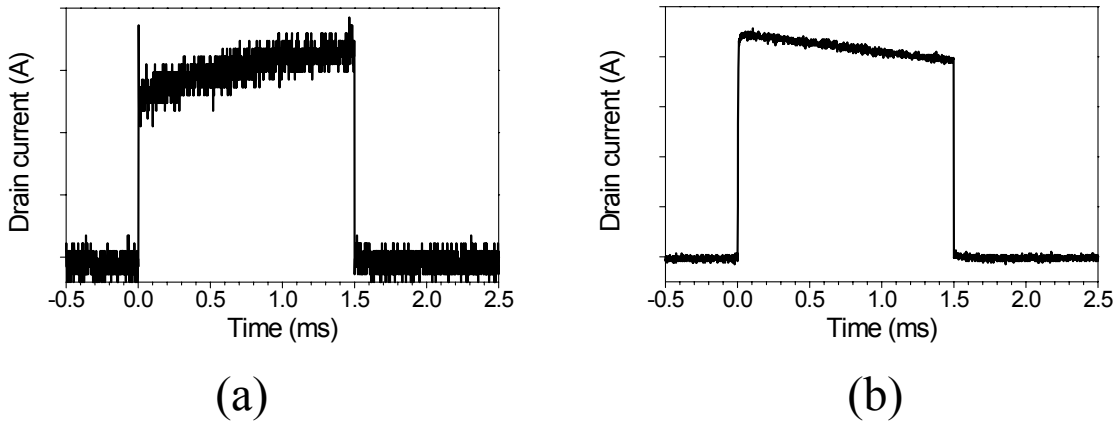


Fig. 4.24: Evolution of the drain current, when (a) $V_{GS} < V_{TCP}$ and (b) $V_{GS} > V_{TCP}$.

Fig. 4.25 shows the phase shift distributions obtained by the *2D* holographic set-up and taken in the time instants of 500 μs, 1 ms and 1.5 ms. The averaged power applied to the device was 0.063 mW.μm^{-2} and 0.024 mW.μm^{-2} for $V_{GS} < V_{TCP}$ and $V_{GS} > V_{TCP}$, respectively. The phase shift rises to extremely high values (several tens of rads) during this type of stress. In case of 1.5 ms pulse applied to the device operating with $V_{GS} < V_{TCP}$ (Fig. 4.25, t = 1500 μs) even the maximum phase shift measurable by the set-up, which is about 80 rad, is exceeded. This is caused by limited pixel resolution of used IR camera, which did not allow increasing of fringe spatial frequency to resolve the high gradient of the phase shift profile. This consequently resulted in a distortion of the measured phase shift spatial distribution.

These figures provide only very rough qualitative picture about the distribution of heat-generating sources. Six fingers of the device can be recognised, at least at time instances of 500 μs and 1 ms, but any traces of the heat dissipation dynamics is vanishing in the smeared thermal map. One way how to obtain more information is to compare normalised phase shift distributions. These are shown in Fig. 4.26 for all three time instances and for both operating points. These curves correspond to the cross sections of the phase shift profiles shown in Fig. 4.25 taken across the fingers through the central part of the device. After 500 μs the width of normalised phase shift profile obtained when the device operated with $V_{GS} < V_{TCP}$ is roughly the same as the one obtained in the regime with $V_{GS} > V_{TCP}$. However, the former becomes slightly smaller after 1 ms, and much smaller after 1.5 ms. This observation suggests that the power dissipation in the central part of the device operating with $V_{GS} < V_{TCP}$ is higher than the one of the device operating with the $V_{GS} > V_{TCP}$. It therefore confirms the assumed current redistribution in the investigated devices.

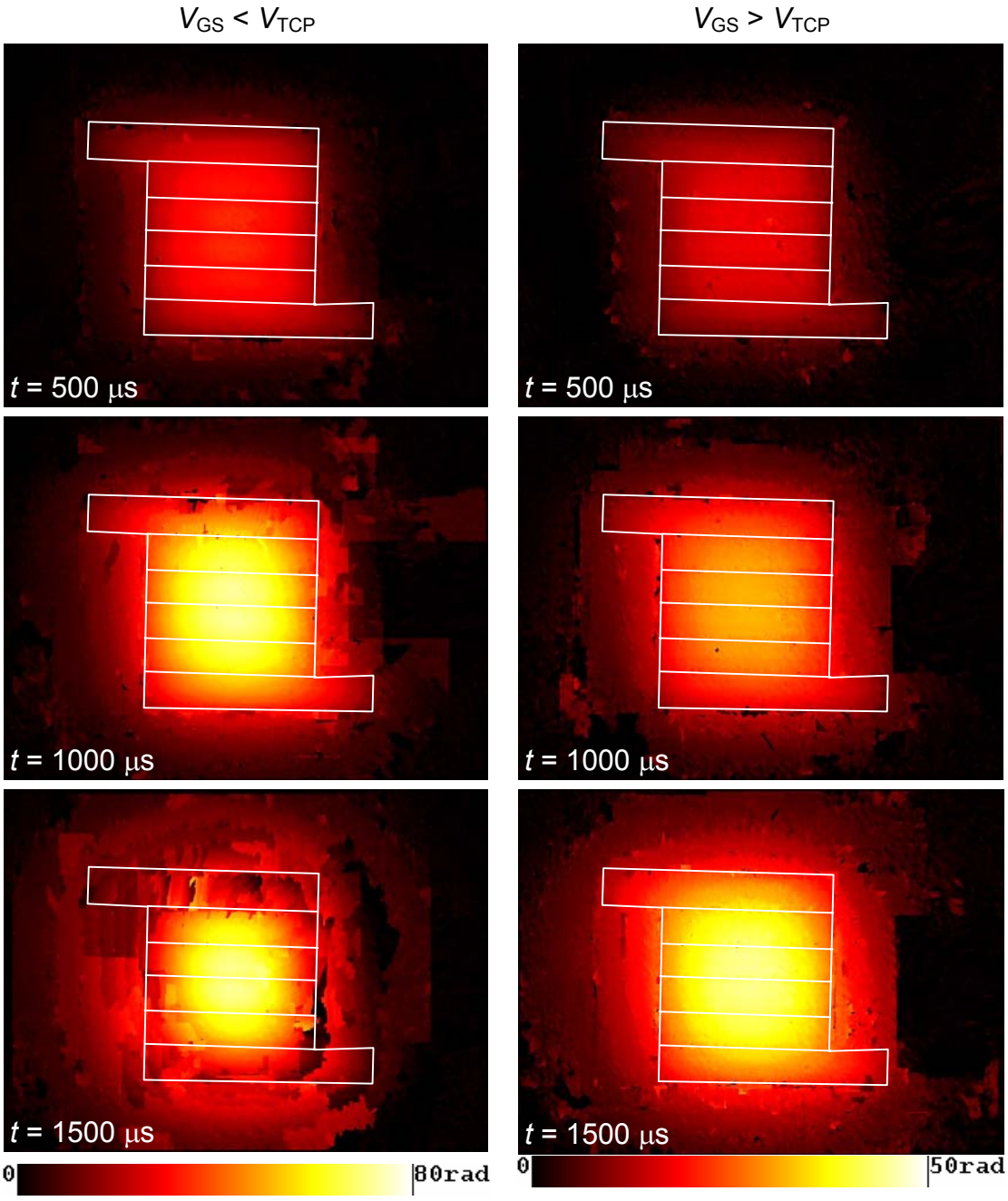


Fig. 4.25: Phase shift profiles taken in several time instances in the investigated DMOS device operating in the region of $V_{GS} < V_{TCP}$ (left column) and $V_{GS} > V_{TCP}$ (right column). The borders of device active area are depicted by solid white line.

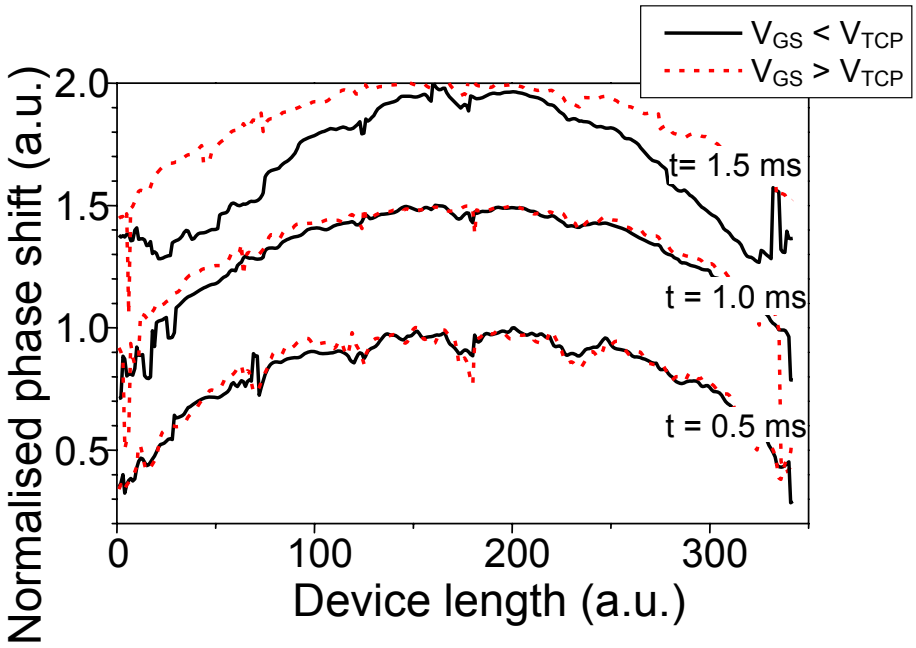
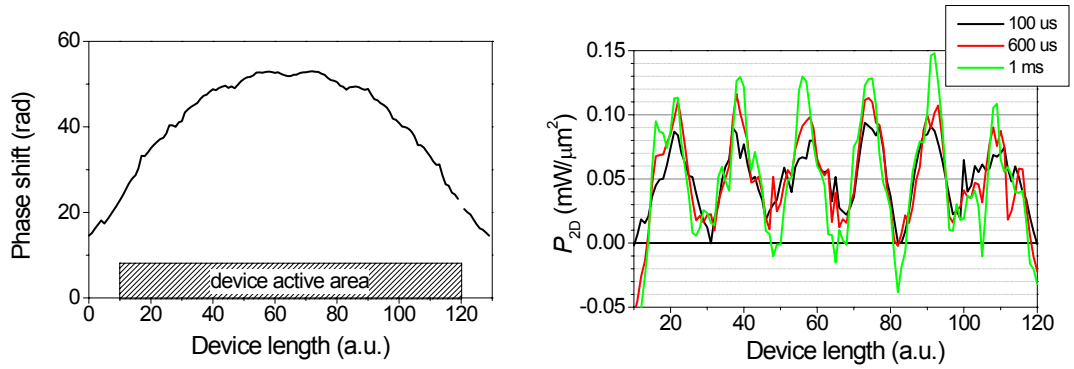


Fig. 4.26: Distribution of the normalised phase shift in the investigated device operating with $V_{GS} < V_{TCP}$ and $V_{GS} > V_{TCP}$ in several time instances.

4.2.2 Extraction of the heat-dissipating sources

As stated in the section 2.1.2, activity of the heat generation sources is much easier to unveil, if the *2*-dimensional power dissipation density P_{2D} is extracted from the measured phase shift. However, this procedure was never before applied in the *ms* -time scale. It was therefore foremost necessary to verify its applicability. For this reason limited number of line scans was performed through the central part of device using scanning heterodyne set-up. Afterwards the P_{2D} was extracted from the measured phase shift. The parameters used in the P_{2D} extraction process (cf. Eq. (2.7)) were κ = 150 W/Km, dn/dT = 1.9×10^{-4} K^{-1}, c_v = 1.63×10^{6} $JK^{1}m^{-3}$, which are values valid for T = 300 K. The spatial derivation along the direction perpendicular to the scanning one was neglected (i.e. for *x*-scan $\partial/\partial y = 0$ and vice versa).

Fig. 4.27(a) shows measured phase shift distribution across the fingers of the device operating with the $V_{GS} < V_{TCP}$. The average dissipated power during 1 ms long pulse was



(a) (b)

Fig. 4.27: (a) Phase shift distribution and (b) P_{2D} distribution in the DMOS device operating with $V_{GS} < V_{TH}$ and stressed by 1 ms long pulse. Averaged dissipated power was 0.06 mW.μm^{-2}.

0.06 mW.μm^{-2}. One can identify 4 faint peaks in the phase shift distribution. They correspond to the heat dissipation in four central fingers of the device. However, there is almost no trace about the rest two side fingers in the figure. The P_{2D} is extracted from the phase shift data is shown in Fig. 4.27(b).The heat dissipation in 6 fingers of the device is now clearly observable as 6 peaks in the P_{2D} distribution. This result demonstrates that the P_{2D}-extraction procedure is beneficial for identification of heat dissipation sources in the actual time scale. It was therefore tentatively used for comparison of device behaviour under various operating conditions.

Figs. 4.28 (a), (b) and (c) show the P_{2D} distributions along the width of a device finger during operating conditions $V_{GS} < V_{TCP}$, $V_{GS} > V_{TCP}$, and $V_{GS} = V_{TCP}$, respectively. The averaged dissipated power for each operating condition is noticed in the figure caption. The extracted P_{2D} distribution is again helpful in identification of the heat-dissipating source dimension, but it exhibits undulations, which complicate the qualitative analysis of heat dissipation dynamics (the undulations come from the derivation process). Moreover, one has to take into account also possible inaccuracies of the extraction procedure (cf. also Appendix A).

The first simplification used in the extraction procedure is the neglected spatial derivative along the direction perpendicular to the scan. The contribution of this neglected derivative should be added to the extracted P_{2D}, because it represents the amount of heat diffused to neighbour regions. It is basically possible to minimise this error by performing the *2*-dimensional scan and calculation of the spatial derivatives along both directions, but this is a time consuming procedure. Available data of the line scans allowed to perform this calculation at least in one point, and that is the cross-point of two perpendicular line-scans. This point is localised exactly in the centre of one of two middle fingers. Fig. 4.29 shows the time evolution of the P_{2D} calculated in this way for operating conditions of $V_{GS} < V_{TCP}$ (black curve in Fig. 4.29) and $V_{GS} > V_{TCP}$ (red curve in Fig. 4.29). In both cases the undulations coming

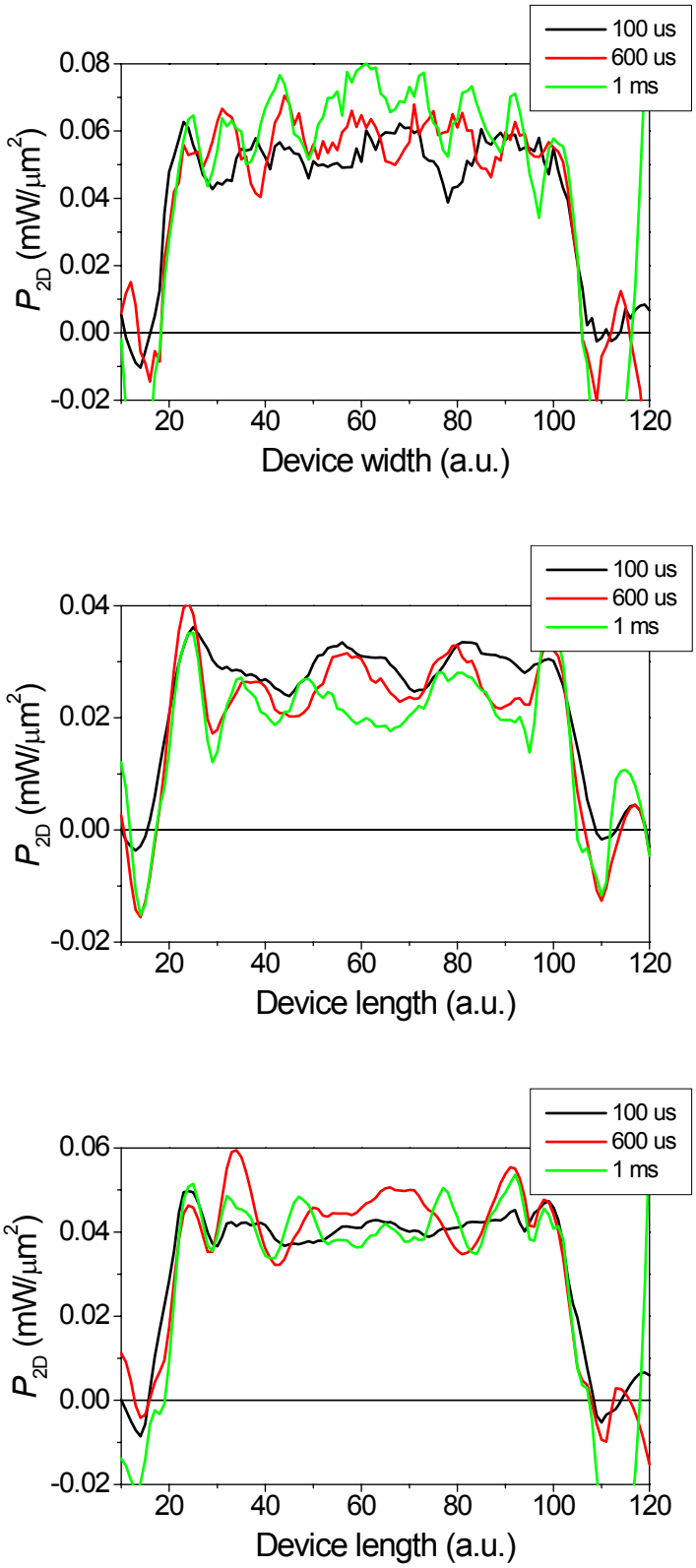


Fig. 4.28: P_{2D} distribution along a finger of the investigated device operating with (a) $V_{GS} < V_{TCP}$ (P_{diss} = 0.06 mW.μm^{-2}); (b) $V_{GS} > V_{TCP}$ (P_{diss} = 0.02 mW.μm^{-2}); and (c) $V_{GS} = V_{TCP}$ (P_{diss} = 0.04 mW.μm^{-2}).

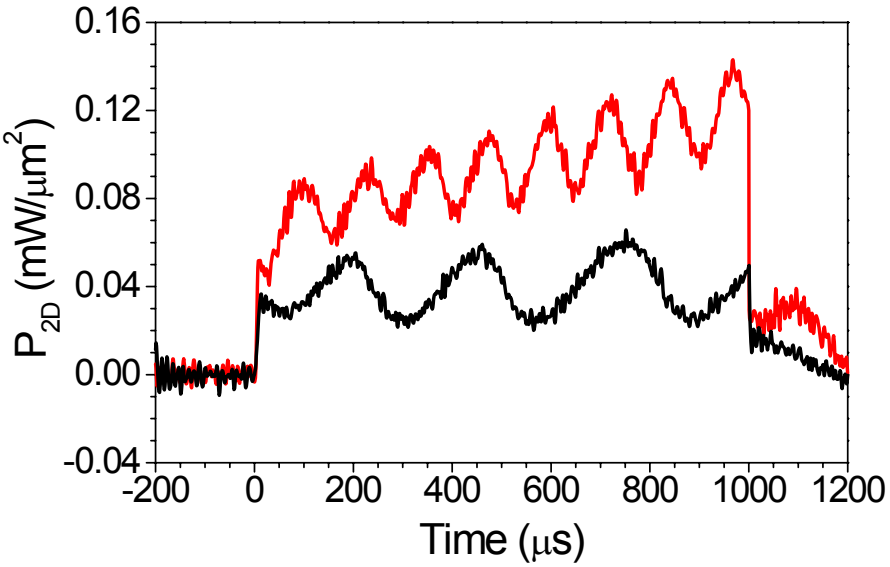


Fig. 4.29: P_{2D} time evolution in a single point in the centre of the device, which operates in regime with $V_{GS} < V_{TCP}$ and $V_{GS} > V_{TCP}$. The spatial derivation along both, *x*- and *y*-directions were taken into account.

from the derivation process are again present. However, for $V_{GS} < V_{TCP}$ the tendency of P_{2D} increasing with time is visible. In case of $V_{GS} > V_{TCP}$ it seems that the mean value of P_{2D} is constant during the energy pulse. Nevertheless, before one makes any conclusion from these results, another two sources of possible inaccuracies should be considered.

The next source of errors of the P_{2D}-extraction procedure in the actual time scale is the temperature dependence of the heat conductivity $\kappa(T)$. In case of short pulses (e.g. ESD-like stress) the heat diffusion is small and this can be neglected. But for longer pulses, when the heat spreading is considerable, κ becomes an important parameter, which has an impact on the spatial derivative terms of Eq. (2.7), and consequently on the total P_{2D}. In the presented results, κ value at $T = 300$ K is used. As the device gets hot during the pulse and κ decreases with increasing temperature, this represents the upper limit for the P_{2D}. In other words, much stronger heat diffusion is assumed in the extraction procedure than occurs in reality. This means that the extracted P_{2D} overestimates the real heat dissipation, and the discrepancy grows with time. Moreover, the P_{2D} profile is deformed if compared to the real one (cf. Appendix A). However, to determine an appropriate value of κ for the P_{2D}-extraction procedure is rather complicated, and the knowledge of the temperature distribution in the investigated device is a necessary condition for such task.

The last source of inaccuracies is the neglected temperature dependence of the thermo-optical coefficient *dn/dT*. Its influence on the P_{2D} extraction process is qualitatively very similar to the influence of heat conductivity, but it is weaker, as shown in Appendix A.

It is clear from this error analysis of the P_{2D}-extraction procedure that the results presented in Fig. 4.28 and 4.29 do not provide definite information about the heat dissipation dynamics. The neglected temperature dependency of κ and *dn/dt* causes that the P_{2D} extracted from the experimental phase shift can rise, although the real power dissipated in the device decreases or stays constant.

4.2.3 Extraction of temperature from the phase shift

Besides the distribution of heat dissipation sources, knowledge of the temperature distribution during device operation is also very interesting for device designers. As can be shown from Eqs. (2.1), (2.2), and (2.3) under condition that the free-carrier change of refractive index is neglected, which is indeed reasonable assumption for the actual time scale, the phase shift is the integral of temperature change along the laser beam path:

$$\Delta\varphi = \frac{4\pi}{\lambda}\frac{dn}{dT}\int_0^l \Delta T(x,y,z,t)dz\,, \tag{4.1}$$

where meaning of the symbols is the same as in Chapter 2. However, direct relation of the phase shift to temperature is not straightforward, because the temperature distribution along the integration path is not known.

The first attempt to deduce the surface temperature from measured phase shift was presented by Thalhammer et al., who investigated IGBT device under short-circuit operating conditions in μs time scale [Thal98]. He reached a good agreement with the simulation results using simple assumptions of linear decrease of temperature towards the substrate and neglected temperature rise at the backside.

We have also tried to estimate the temperature in the studied DMOS device from the measured phase shift. For this reason a non-linear thermal simulation of a heat dissipation source emulating the investigated device was performed[1]. Power of the simulated heat dissipation source was chosen 0.066 $mW.\mu m^{-2}$, which was the same value that was applied during one of the experiments. This allowed a direct comparison of the simulation and experimental results. The output of the simulation was the *3*-dimensional temperature map,

[1] Courtesy of M. Denison

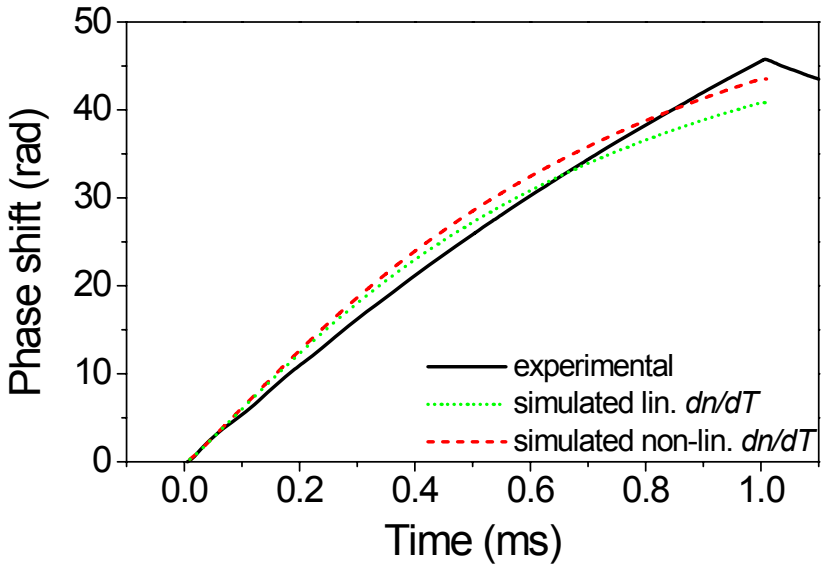


Fig. 4.30: Comparison of simulated and experimental phase shifts.

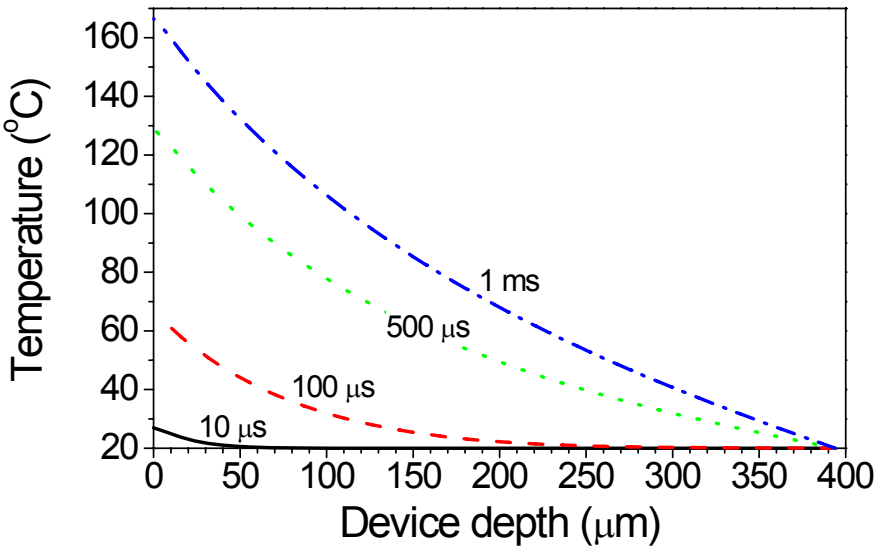


Fig. 4.31: Simulated temperature distribution along the depth of device in several time instances during the power pulse of 0.66 mW.μm^{-2}. (Courtesy of M. Denison)

from which the *2D* phase shift profile was calculated using both, temperature independent and temperature dependent thermo-optical coefficient *dn/dT*. The simulated and experimental phase shifts are compared in Fig. 4.30. Very good agreement is found for the non-linear *dn/dT(T)*, and the difference does not exceed 10%. Note that the simulated linear phase shift (*dn/dT = const*) is smaller than the non-linear one (*dn/dT(T)*). This originates from the fact that the *dn/dT* increases with increasing temperature.

The simulated temperature distribution along the *z*-axis (depth) in several time instances in currently investigated device is presented in Fig. 4.31. One can see that the simple approach of linear decrease of temperature taken from [Thal98] is still an acceptable assumption, nevertheless varying depth of the heated region has to be taken into account. This leads to a modification of the last equation of [Thal98] into form:

$$T_{\max} = \frac{\Delta\varphi \cdot \lambda}{2\pi \frac{dn}{dT} L(t)}, \tag{4.2}$$

where $L(t)$ is the depth into which the heat diffuses. This depth can be in the first approximation determined from the thermal diffusivity D [Cars59, Krie87]:

$$L(t) = \sqrt{Dt}, \tag{4.3}$$

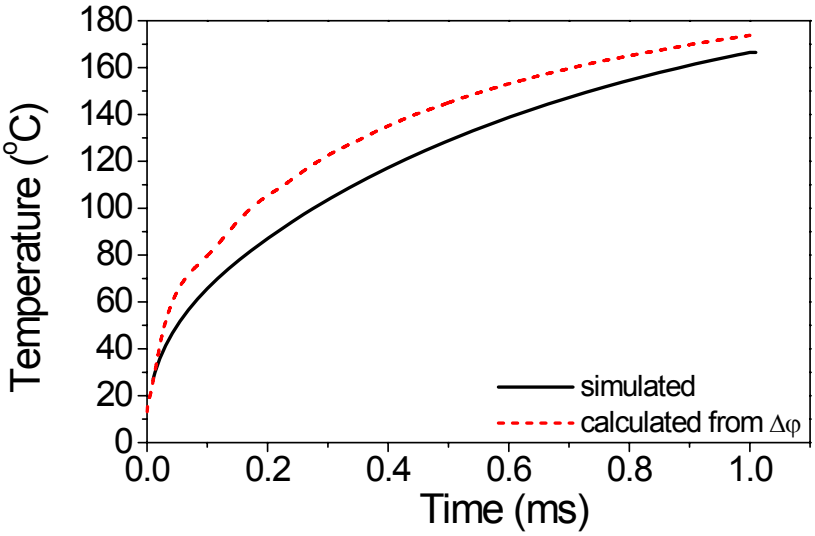


Fig. 4.32: Comparison of the simulated temperature evolution and the one calculated from the experimental phase shift using Eq. (4.2).

where t is time; and the value of D is for silicon and room temperature approximately 0.87 $cm^2.s$ [Krie87]. The T_{max} evolution calculated using Eq. (4.2) and (4.3) from the experimental phase shift is shown in Fig. 4.32. The error is about 20%, but the approximation of temperature distribution by some more complex function (e.g. Gaussian [Bych04]), together with improved determination of $L(t)$ could be a potential way how to estimate the surface temperature in investigated devices. Further improvement can be achieved by taking into account the non-linearity of the dn/dT coefficient.

4.2.4 Summary

It was shown that the TIM is applicable for the investigations in the *ms* time scale. The P_{2D} extraction procedure yielded a qualitative distribution of power dissipation sources in the device, however the present extraction methodology is not applicable for the quantitative analysis. For such purpose a more refined extraction procedure, which takes into account the temperature dependencies of heat conductivity and thermo-optical coefficient, is necessary.

A simple model was presented to roughly estimate surface temperature from the measured phase shift. The estimated temperature agreed with simulation within 20% for the studied devices. The methodology is important, because it provides an easy experimental access to temperature at silicon/metal or silicon/oxide interface at device topside. This is not possible by other techniques, like black-body radiation or liquid crystal thermometry, which give temperature at metal or SiO_2 surface and also require coating.

Chapter 5

Summary

This work presented results of experimental characterisation of semiconductor devices using transient interferometric mapping technique. Two types of devices have been studied: the devices intended for protection of smart power technology chips against electrostatic discharge, and the smart power DMOS transistors.

The detailed analysis of behaviour of BCD ESD protection devices was done by localising the heat dissipating regions and regions with increased free carrier concentration. Two current paths were identified: lateral and vertical. Although the lateral current flow was dominant, the activity along the vertical current path was also found important for the ESD robustness of the devices.

Another investigated aspect was the difference in operation of individual devices under TLP and vf-TLP stress. The observed qualitative distinctions in the measured phase shift profiles were related only to the stress pulse length. The devices were effectively triggered, and their ESD robustness was found very good in both, HBM and CDM time domains.

The experimental investigation of power VDMOS transistors was mostly focused on their ability to withstand ESD stress. Under all studied conditions the current flow in the device was homogeneous until the turn-on of parasitic bipolar transistor. Once it occurred, the current filaments appeared. They were found to move in the active region of the devices during the stress pulse. The experimental observations, which cannot be obtained by other than 2D holographic TIM method, verified the 2D and 3D device simulation results. Thanks to this the device physics was understood. It was shown that the filament movement is thermally driven process related to the negative temperature dependence of impact ionisation. The dominant factor, which allowed the movement, was the layout of studied devices. Overall the filament movement was found beneficial for ESD robustness, because it helped to avoid local overheating.

For the first time the TIM technique was applied for the study in the *ms* time scale. The effects influencing the thermal SOA of the large VDMOS transistors was investigated. It was shown by analysis of experimentally obtained data that if one wants to exploit maximum

of information from these experimental results, not the measured phase shift, but the *2D* power dissipation density extracted from the phase shift is necessary to be used. The precision of the P_{2D} extraction procedure in the *ms* time scale was also discussed. It was shown that the procedure, which does not take into account temperature dependence of involved parameters, can predict the distribution of heat generation sources. However, it was also presented that the inclusion of temperature dependent parameters is necessary for an unambiguous interpretation of the results. It will be therefore necessary to elaborate a more advanced extraction procedure.

Finally, a simple approach, which can in the future allow unique estimation of the surface temperature from measured phase shift, was proposed.

Appendix A

Effect of temperature dependent parameters on the precision of the P_{2D} extraction procedure

The extraction of *2D* power dissipation density from measured phase shift is given by formula:

$$P_{2D}(x,y,t)=\frac{\lambda}{4\pi\dfrac{dn}{dT}}\left\{c_v\frac{\partial\Delta\varphi(x,y,t)}{\partial t}-\kappa\left[\frac{\partial^2\Delta\varphi(x,y,t)}{\partial x^2}+\frac{\partial^2\Delta\varphi(x,y,t)}{\partial y^2}\right]\right\}+j_{th,z}(x,y,0,t). \quad \text{(A.1)}$$

It was derived assuming temperature independence of thermo-optical coefficient *dn/dT*, volume specific heat c_v and heat conductivity κ. However, in the time domain of μs and more, the temperature dependence of all the quantities becomes important. As a result, inaccuracies are expected to be introduced into the extracted P_{2D}.

To estimate these inaccuracies a *2*-dimensional simulation has been performed[1]. The aim of the simulation has been to figure out the influence of $\kappa(T)$ and $dn/dT(T)$ on the extracted P_{2D}. Temperature dependence of volume specific heat $c_v(T)$ is weak, and thus it was neglected. Reverse biased *pn* junction, where the thermal dependence of all electrical quantities was switched off, was simulated. The simulation can be therefore assumed as "pure thermal". The constant current pulse of 20 μs duration was applied to the structure resulting in approximately constant power dissipation. The temperature dependency of κ and *dn/dT* were switched on and off to obtain temperature map in all possible cases.

[1] Courtesy of S. Reggiani

Fig. A.1 shows the phase shift calculated from the simulated temperature distribution in the structure. This figure demonstrates how temperature dependence of thermo-optical coefficient and/or heat conductivity influences the phase shift profile if compared to the linear (temperature independent) model. The *κ(T)* affect the phase shift in an indirect way, because it influences the temperature distribution in the structure. It decreases with increasing temperature and causes an increase of the temperature in the central parts of the device ($T_{max,lin}$ ~ 180 °C vs. $T_{max,\kappa(T)}$ ~ 260 °C). On the other hand, the *dn/dT(T)* directly influences the phase shift profile. It increases with increasing temperature and thus causes a rise the phase shift at hotter areas in comparison with linear case. It is seen from the figure that the influence of the temperature dependent heat conductivity is stronger than the influence of temperature dependent *dn/dT*. In summary these two effects together lead to much higher phase shift values than in the linear case (compare black solid and blue dash-dotted lines in Fig. A.1).

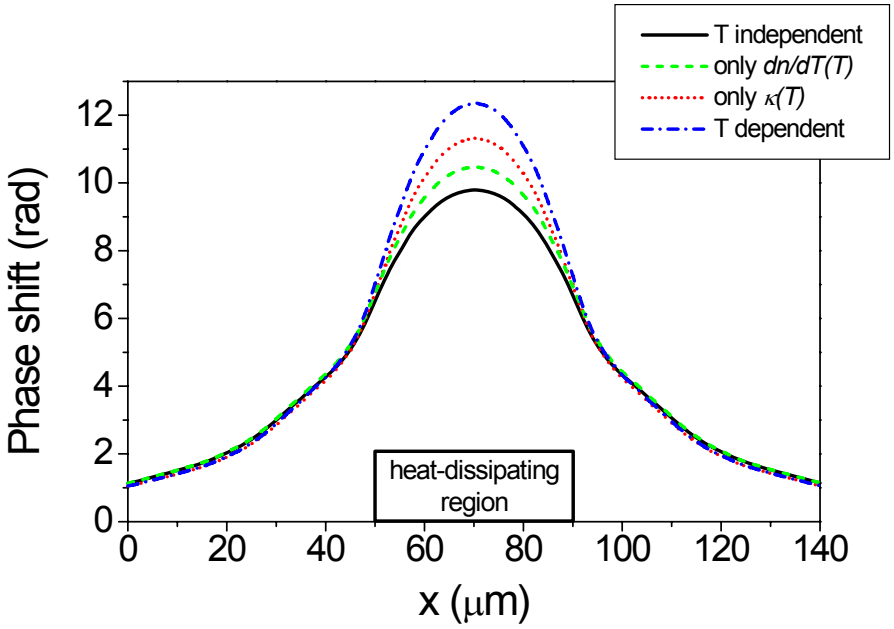


Fig. A.1: Comparison of simulated phase shift distribution at the end of 20-μs long pulse.

Fig. A.2 shows the P_{2D} extracted from the phase shift distributions shown in Fig. A.1. Note that the second spatial derivative ($\partial^2/\partial y^2$) was zero, because the simulation was *2*-dimensional and the phase shift distribution along the *y*-axis was therefore assumed to be flat. The P_{2D} distribution obtained by an integration of the simulated P_{3D} over *z*-direction is displayed as a reference (grey line in Fig. A.2).

First of all the figure confirms very good agreement between simulated and extracted P_{2D} distributions in the case of linear simulation (compare black and grey line in Fig. A.2). The size

of the heat dissipation region, as well as its shape are very well reproduced. However, the temperature dependence of both *dn/dT* and κ causes an overestimation of the P_{2D} value and deformation of its distribution. Similarly as in the case of phase shift, $\kappa(T)$ influence dominates. The *dn/dT(T)* effect on the P_{2D} is indeed negligible in this case, although it is not on the phase shift (cf. Fig. A.1). Nevertheless, the size of heat source is well reproduced. Note that the negative peaks in the P_{2D} distribution at the both sides of heat dissipating region are caused by heat removal through the contacts, which are localised at these places, and which were set to room temperature during the simulation.

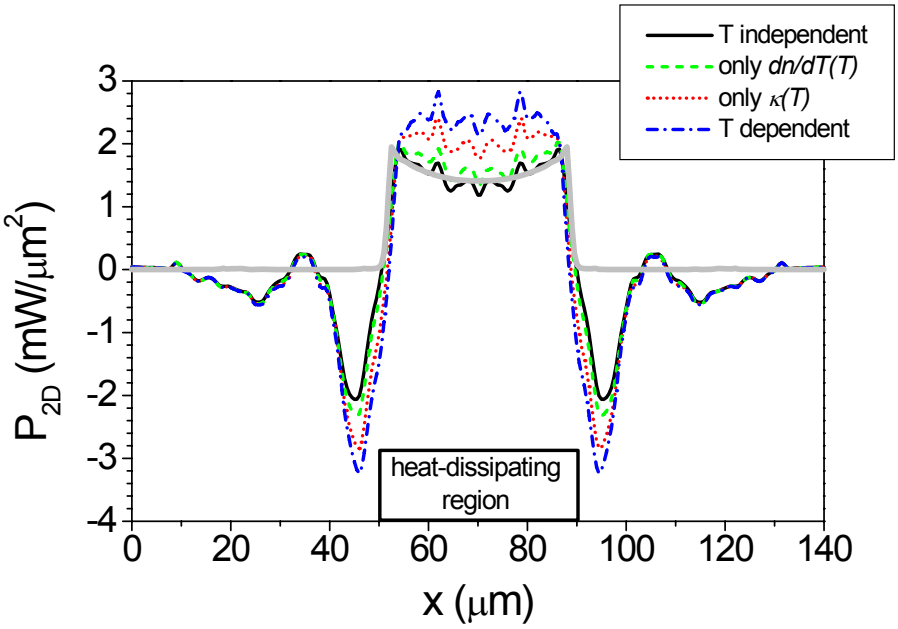


Fig. A.2: P_{2D} distribution extracted from the simulated phase shift shown in Fig. A.1. The grey line is reference obtained by integration of the simulated P_{3D} over *z*-direction.

Bibliography

[Amer95] A. Amerasekera and C. Duvvury: *ESD in silicon integrated circuits*, John Wiley and sons, Chichester, 1995

[Amer96] A. Amerasekera, S. Ramaswamy, Mi-Chang Chang and C. Duvvury: "Modelling MOS snapback and parasitic bipolar action for circuit-level ESD and high current simulations," Proc. IRPS'96, 1996, pp. 318-326

[Andr86] A. Andreini, C. Contiero and P. Galbiati: "New integrated silicon gate technology combining bipolar linear, CMOS logic, and DMOS power parts," IEEE Trans. Electron Dev., ED-33, 1986, pp. 2025-2030

[Bali91] B. J. Baliga: "An overview of smart power technology," IEEE Trans. Electron Dev., 38, 1991, pp. 1568-1575

[Bali96a] B. J. Baliga: *Power semiconductor devices*, PWS publishing company, Boston, 1996

[Bali96b] B. J. Baliga: "Trends in power semiconductor devices," IEEE Trans. Electron Dev., 43, 1996, pp. 1717-1731

[Bart00] J. Barth, K. Verhaege, L. G. Henry and J. Richter: "TLP calibration, correlation, standards, and new techniques," Proc. EOS/ESD symp.'00, 2000, pp. 85-96

[Beau02] F. Beaudoin, P. Perdu, R. Desplats, E. Doche, A. Wislez, T. Beauchene, D. Lewis, D. Carisetti, D. Tremouilles and M.Bafleur: "Laser Beam Based ESD Defect Localization In ICs," Proc. Int. Symp. for Testing and Failure Anal., 2002, pp. 543-551

[Beau03] T. Beauchêne, D. Lewis, F. Beaudoin, V. Pouget, R. Desplats, P. Fouillat, P. Perdu, M. Bafleur and D. Tremouilles: "Thermal laser stimulation and NB-OBIC techniques applied to ESD defect localization," Microel. Reliab., 43, 2003, pp 439-444

[Berg02] I. Berger: "Can You Trust Your Car?" IEEE Spectrum, 39, 2002, pp. 41-45

[Bert90] M. Bertoloti, V. Bogdanov, A. Ferrari, A. Jascow, N. Nazorova, A. Pikhtin and L. Schirone: "Temperature dependence of the refractive index in semiconductors," J. Opt. Soc. Am. B, 7, 1990, pp. 918-922

[Bess02] P. Besse, N. Nolhier, M. Bafleur, M. Zecri, and Y. Chung: "Investigation for a smart power and self-protected device under ESD stress through geometry and design considerations for automotive applications," Proc. ISPSD'02, 2002, pp. 348-353

[Blah02] M. Blaho, D. Pogany, L. Zullino, A. Andreini, and E. Gornik: “Experimental and simulation analysis of a BCD ESD protection element under the DC and TLP stress conditions,” Microel. Reliab., 42, 2002, pp. 1281-1286

[Blah03a] M. Blaho, D. Pogany, E. Gornik, L. Zullino, E. Morena, R. Stella, A. Andreini, H. Wolf and H. Gieser: “Internal behaviour of BCD ESD protection devices under very-fast TLP stress,” Proc. IRPS’03, 2003, pp. 235-240

[Blah03b] M. Blaho, D. Pogany, E. Gornik, M. Denison, G. Groos and M. Stecher: “Study of internal behavior in a vertical DMOS transistor under short high current stress by an interferometric mapping method,” Microel. Reliab., 43, 2003, pp. 545-548

[Blah04] M. Blaho, L. Zullino, H. Wolf, R. Stella, A. Andreini, H. A. Gieser, D. Pogany and E. Gornik: “Internal behavior of BCD ESD protection devices under TLP and very-fast TLP stress,” IEEE Trans. Dev. and Material Reliab., 4, 2004, pp. 535-541

[Bose01] G. Boselli, S. Meeuwsen, T. Mouthaan and F. Kuper: “Investigations on double-diffused MOS transistors under ESD zap conditions,” Microel. Reliab, 41, 2001, pp. 395-405

[Breg99] G. Breglio, F. Frisina, A. Magri and P. Spirito: “Electro-thermal instability in low voltage power MOS: experimental characterisation,” Proc. of ISPSD’99, 1999, pp. 233-236

[Bych01] S. Bychikhin, M. Litzenberger, R. Pichler, D. Pogany, E. Gornik, G. Groos and M. Stecher: “Thermal and free carrier laser interferometric mapping and failure analysis of anti-serial smart power ESD protection structures,” Microel. Reliab., 41, 2001, pp. 1501-1506

[Bych03] S. Bychikhin, V. Dubec, M. Litzenberger, D. Pogany, E. Gornik, G. Groos, K. Esmark, M. Stecher, W. Stadler, H. Gieser and H. Wolf: “Investigation of ESD protection elements under high current stress in CDM-like time domain using backside laser interferometry,” J. of Electrostatics, 59, 2003, pp. 241-255

[Bych04] S. Bychikhin, unpublished results, 2004

[Cars59] H. S. Carslaw and J. C. Jaeger: *Conduction of heat in solids - second edition*, Oxford Science Publications, Oxford, 1959

[Casi04] H. Casier, P. Moens, K. Appeltans: “Technology Considerations for Automotive,” Proc. of ESSCIRC’04, 2004, pp. 37-41

[Char96] G. Charitat, M. A. Bouanane, P. Austin and P. Rossel: “Modelling and improving the on-resistance of LDMOS RESURF devices,” Microel. Journal, 27, 1996, pp. 181-190

[Cons99] A. Consoli, F. Gennaro, A. Testa, G. Consentino, F. Frisina, R. Letor and A. Magri: “Thermal instability of low voltage power MOSFETs,” Proc. PESC’99, 1999, pp. 345-350

[Debo94] Deboy et al.: “Fundamentals of light emission from silicon devices,” Semicond. Sci. Technol., 9, 1994, pp. 1017-1032

[Deni03] M. Denison, M. Blaho, D. Silber, J. Joost, N. Jensen, M. Stecher, V. Dubec, D. Pogany and E. Gornik: “Hot spot dynamics in quasi vertical DMOS under ESD stress,” Proc. ISPSD’03, 2003, pp. 80-83

[Deni04a] M. Denison: Single stress safe operating area of DMOS transistors intergrated in smart power technologies, PhD thesis, Bremen, 2004

[Deni04b] M. Denison, M. Blaho, P. Rodin, V. Dubec, D. Pogany, D. Silber, E. Gornik and M. Stecher: “Moving current filaments in integrated DMOS transistors under short-duration current stress,” IEEE Trans. Electron Dev., 51, 2004, pp. 1695-1703

[Deni04c] M. Denison, M. Pfost, K. W. Pieper, S. Märkl, D. Metzner and M. Stecher: “Influence of inhomogeneous current distribution on the thermal SOA of integrated DMOS transistors,” Proc. ISPSD’04, 2004, pp. 409-412

[Doln92] G. M. Dolny, G. E. Nostrand and K. E. Hill: “The effect of temperature on lateral DMOS transistors in a power IC technology,” IEEE Trans. Electron Dev., 39, 1992, pp. 990-995

[Dube03] V. Dubec, S. Bychikhin, M. Blaho, D. Pogany, E. Gornik, J. Willemen, N. Qu, W. Wilkening, L. Zullino and A. Andreini: “A dual-beam Michelson interferometer for invetigation of trigger dynamics in ESD protection devices under very fast TLP stress,” Microel. Reiliab., 43, 2003, pp. 1557-1561

[Dube04a] V. Dubec, S. Bychikhin, D. Pogany, E. Gornik, N. Jensen, M. Stecher and G. Groos: “Error analysis in phase extraction in a 2D holographic imaging of semiconductor devices,” Proc. Electr. Imag. Sci. and Tech.’04, 2004, pp. 83

[Dube04b] V. Dubec, S. Bychikhin, M. Blaho, M. Heer, D. Pogany, M. Denison, N. Jensen, M. Stecher, G. Groos and E. Gornik: “Multiple-time-instant 2D thermal mapping during a single ESD event,” Microel. Reliab., 44, 2004, pp. 1793-1798

[Duvv94] C. Duvvury, J. Rodriguez, C. Jones and M. Smayling: “Device integration for ESD robustness of high voltage power MOSFETs,” Tech. Dig. IEDM’94, 1994, pp. 407-410

[Duvv97] C. Duvvury, F. Carvajal, C. Jones and D. Briggs: “Lateral DMOS design for ESD robustness,” Tech. Dig. IEDM’97, 1997, pp. 375-378

[Efla97] T. Efland, C.-Y. Tsai, J. Erdeljac, J. Mitros and L. Hutter: “A performance comparison between new reduced surface drain “RSD” LDMOS and RESURF and conventional planar power devices rated at 20V,” Proc. ISPSD’97, 1997, pp. 185-188

[Furb98] C. Fürböck, N. Seliger, D. Pogany, M. Litzenberger, E. Gornik, M. Stecher, H. Gossner and W. Werner: “Backside laserprober characterisation of thermal effects

during high current stress in smart power ESD protection devices," Tech. Dig. IEDM'98, 1998, pp. 691-694

[Furb00] C. Fürböck, D. Pogany, M. Litzenberger, E. Gornik, N. Seliger, H. Goßner, T. Müller-Lynch, M. Stecher and W. Werner: "Interferometric temperature mapping during ESD stress and failure analysis of smart power technology ESD protection devices," Journal of Electrostatics, 49, 2000, pp. 195-213

[Gies98] H. Gieser and M. Haunschild: "Very fast transmission line pulsing of integrated structures and the charged device model," IEEE Trans. Components, Packaging and Manufacturing technology-Part C, 21, 1998, pp. 278-285

[Heer05] M. Heer, V. Dubec, M. Blaho, S. Bychikhin, D. Pogany and E. Gornik: "Automated set-up for thermal imaging and electrical degradation study of power DMOS devices," accepted for ESREF'05,

[Howe01] P. Hower, S. Pendharkar, R. Steinhoff, J. Brodsky, J. Devore and W. Grose: "Using two-dimensional structures to model filamentation in semiconductor devices," Proc. ISPSD'01, 2001, pp. 385-388

[Howe02] P. Hower: "Safe operating area-a new frontier in LDMOS design," Proc. ISPSD'02, 2002, pp. 1-8

[Kawa02] K. Kawamoto, S. Takahashi, S. Fujino and I. Shirakawa: "A no-snapback LDMOSFET with automotive ESD endurance," IEEE Trans. Electron Dev., 49, 2002, pp. 2047-2053

[Kim01] J. Kim, T. M. Roh, S.-G. Kim, J. H. Lee, K.-I. Cho and Y. I. Kang: "A highly reliable trench DMOSFET employing self-align technique and hydrogen annealing," IEEE Trans. Electron Dev., 22, 2001, pp. 594-596

[Kirk62] C. T. Kirk jr.: "A theory of transistor cut-off frequency (f_T) falloff at high current densities," IRE Trans. Electron Dev., ED-9, 1962, pp. 164-174

[Krie87] G. Krieger: "Thermal response of integrated circuit input devices to an electrostatic energy pulse," Trans. Electron Dev., ED-34, 1987, pp. 877-882

[Lim97] S. L. Lim, X. Y. Zhang, Z. Yu, S. Beebe and R. W. Dutton: "Computationally stable quasi-empirical compact model for the simulation of MOS breakdown in ESD-protection circuit design," Proc. SISPAD'97, 1997, pp. 161-164

[Litz00] M. Litzenberger, C. Fürböck, D. Pogany, E. Gornik, K. Esmark and H. Gossner: "Investigation of 3D phenomena in ther triggering of gg-nMOS electrostatic discharge protection devices," Proc. of ESSDERC '00, 2000, pp. 520-523

[Litz01] M. Litzenberger, R. Pichler, S. Bychikhin, D. Pogany, E. Gornik, K. Esmark and H. Gossner: "Effect of pulse risetime on trigger homogeneity in single finger grounded gate nMOSFET electrostatic discharge protection devices," Microel. Reliab., 41, 2001, pp. 1385-1390

[Litz03] M. Litzenberger: Investigation of internal behavior in CMOS ESD protection devices under high current stress, PhD thesis, Vienna, 2003

[Malo85] T. J. Maloney and N. Khurana: "Transmission line pulsing techniques for circuit modelling of ESD phenomena," Proc. EOS/ESD Symp.'85, 1985, pp. 49-54

[Mcau94] J. A. McCaulley, V. M. Donnelly, M. Vernon and I. Taha: "Temperature dependence of the near-infrared refractive index of silicon, gallium arsenide, and indium phosphide," Phys. Rev. B, 49, 1994, pp. 7408-7417

[Mene00] G. Meneghesso, S. Santirosi, E. Novarini, C. Contiero and E. Zanoni: "ESD robustness of smart-power protection structures evaluated by means of HBM and TLP tests," Proc. IRPS'00, 2000, pp. 270-275

[Merg00] M. P. J. Mergens, W. Wilkening, S. Mettler, H. Wolf, A. Stricker and W. Fichtner: "Analysis of lateral DMOS power devices under ESD stress conditions," Trans. Electron Dev., 47, 2000, 2128-2137

[Moen04] P. Moens, S. Bychikhin, K. Reynders, D. Pogany and M. Zubeidat: "Effects of hot spot hopping and drain ballasting in integrated vertical DMOS devices under TLP stress," Proc. IRPS'04, 2004, pp. 393-398

[Mora97] F. Morancho, H. Traduc and P. Rossel: "The on-resistance limits of high cell density power MOSFET's," Proc. MIEL'97, 1997, pp. 395-398

[Mura96] B. Murari, F. Bertotti and G. A. Vignola: *Smart power ICs*, Springer, Berlin, 1996

[Mura97] B. Murari: "Reliability of smart power devices," Microel. Reliab., 37, 1997, pp. 1735-1742

[Muss96] A. Musshoff, H. Wolf, H. Gieser, P. Egger and X. Guggenmos: "Risetime effects of HBM and square pulses on the failure thresholds of ggNMOS-transistors," Microel. Reliab., 38, 1996, pp. 1743-1746

[Note98] G. Notermans, P. de Jong and F. Kuper: "Pitfalls when correlating TLP, HBM and MM testing," Proc. EOS/ESD symp.'98, 1998, pp. 170-176

[Part02] V. Parthasarathy, V. Khemka, R. Zhu, J. Whitfield, A. Bose and R. Ida: "A double RESURF LDMOS with drain profile engineering for improved ESD robustness," IEEE Trans. Electron Dev., 23, 2002, pp. 212-214

[Plik97] R. Plikat, M. Darwish, M. S. Shekar and R. K. Williams: "Impact of cell layout on the characteristics of 60V on-resistance lateral NMOS for power ICs," Proc. ISPSD'97, 1997, pp. 349-352

[Poga00] D. Pogany, K. Esmark, M. Litzenberger, C. Fürböck, H. Gossner and E. Gornik: "Bulk and surface degradation mode in 0.35µm technology gg-nMOS ESD protection devices," Microel. Reliab., 40, 2000, pp. 1467-1472

[Poga01] D. Pogany, C. Fürböck, M. Litzenberger, G. Groos, K. Esmark, P. Kamvar, H. Gossner, M. Stecher and E. Gornik: "Study of trigger instabilities in smart power

technology ESD protection devices using a laser interferometric thermal mapping technique," Proc. EOS/ESD symp.'01, 2001, pp. 216-227

[Poga02a] D. Pogany, S. Bychikhin, C. Fürböck, M. Litzenberger, E. Gornik, G. Groos, K. Esmark and M. Stecher: "Quantitative internal thermal energy mapping of semiconductor devices under short current stress using backside laser interferometry," IEEE Trans. Electron Dev., 49, 2002, pp. 2070-2079

[Poga02b] D. Pogany, S. Bychikhin, M. Litzenberger, E. Gornik, G. Groos and M. Stecher: "Extraction of spatio-temporal distribution of power dissipation in semiconductor devices using nanosecond interferometric mapping technique," Appl. Phys. Lett., 81, 2002, pp. 2881-2883

[Poga02c] D. Pogany, V. Dubec, S. Bychikhin, C. Furbock, M. Litzenberger, G. Groos, M. Stecher and E. Gornik: "Single-shot thermal energy mapping of semiconductor devices with the nanosecond resolution using holographic interferometry," IEEE Electron Dev. Lett., 23, 2002, pp. 606-608

[Poga02d] D. Pogany, J. Kuzmik, J. Darmo, M. Litzenberger, S. Bychikhin, K. Unterrainer, Z. Mozolova, S. Hascik, T. Lalinsky and E. Gornik: "Electrical field mapping in InGaP HEMTs and GaAs terahertz emitters using backside infrared OBIC technique," Microel. Reliab., 42, 2002, pp. 1673-1677

[Poga03] D. Pogany, S. Bychikhin, J. Kuzmik, V. Dubec, N. Jensen, M. Denison, G. Groos, M. Stecher and E. Gornik: "Thermal distribution during destructive pulses in ESD protection devices using a single-shot two-dimensional interferometric method," IEEE Trans. Dev. and Materials Reliab., 3, 2003, pp. 197-201

[Poga05] D. Pogany, S. Bychikhin, M. Denison, P. Rodin, J. Jensen, G. Groos, M. Stecher and E. Gornik: "Thermally-driven motion of current filaments in ESD protection devices," Solid-State Electronics, 49, 2005, pp. 421-429

[Rodi04] P. Rodin: "Theory of travelling filaments in bistable semiconductor structures," Phys. Rev. B, 69, 2004, pp. 045307-1 – 045307-11

[Russ99] C. Russ, K. Bock, M. Rasras, I. De Wolf, G. Groeseneken and H.E. Maes: "Non-uniform triggering of gg-nMOSt investigated by combined emission microscopy and transmission line pulsing," Microel. Reliab., 39, 1999, 1551-1561

[Schr78] D. K. Schroder, R. N. Thomas and J. C. Swartz: "Free carrier absorption in silicon," IEEE Trans. Electron Dev., ED-25, 1978, pp. 254-261

[Seli97] N. Seliger, P. Habas, D. Pogany and E. Gornik: "Time-resolved analysis of self-heating in power VDMOSFETs using backside laser probing," Solid State Elecron., 41, 1997, pp. 1285-1292

[Sore87] R. A. Soref and B. R. Bennett: "Electrooptical effects in silicon," IEEE. J. Quant. Electron., QE-23, 1987, pp. 123-129

[Spir02] P. Spirito, G. Breglio, V. d'Alessandro and N. Rinaldi: "Thermal instabilities in high current power MOS devices: experimental evidence, electro-thermal simulations and analytical modeling," Proc. MIEL'02, 2002, pp. 23-30

[Stad97] W. Stadler, X. Guggenmos, P. Egger, O. Gieser and C. Musshoff: "Does The ESD-failure current obtained by transmission line pulsing always correlate to human body model tests?" Proc. EOS/ESD symp.'97, 1997, pp. 366-372

[Stad03] W. Stadler, K. Esmark, K. Reynders, M. Zubeidat, M. Graf, W. Wilkening, J. Willement, N. Qu, S. Mettler, M. Etherton, D. Nuernbergk, H. Wolf, H. Gieser, W. Soppa, V. De Heyn, M. Natarajan, G. Groeseneken, E. Morena, R. Stella, A. Andreini, M. Litzenberger, D. Pogany, E. Gornik, C. Foss, A. Konrad and M. Frank: "Test circuits for fast and reliable assessment of CDM robustness of I/O stages," Proc. EOS/ESD symp.'03, 2003, pp. 327

[Stei03] R. M. Steinhoff, J.-B. Huang. P. L. Hower, J. S. Brodsky: "Current filament movement and silicon melting in an ESD-robust DENMOS transistor," Proc. EOS/ESD symp.'03, 2003, pp. 98-107

[Stur92] J. C. Sturm and C. M. Reaves: "Silicon temperature measurement by infrared absorption: fundamental processes and doping effects," IEEE Trans. Electron Dev., 39, 1992, pp. 81-88

[Sze81] S. M. Sze: Physics of semiconductor devices – 2nd edition, John Wiley and Sons, New York, 1981

[Teh97] G. L. Teh, W. K. Chim, Y. K. Swee and Y. K. Co: "Spectroscopic photon emission measurements of n-channel MOSFETs biased into snapback breakdown using a continuous-pulsing transmission line technique," Semic. Sci. and Tech., 12, 1997, 662-671

[Thal98] R. Thalhammer, C. Furbock, N. Seliger, G. Deboy, E. Gornik and G. Wachutka: "Internal characterisation of IGBTs using the backside laser probing technique-interpretation of measurement by numerical simulation," Proc. ISPSD'01, 2001, pp. 199-202

[Yilm89] H. Yilmaz, T. Tsui, I. Bencuya, T. Frontier and K. Owyang: "Safe operating area of power DMOS FETs," Proc. PESC'89, 1989, pp. 170-175

List of Symbols

Symbol	Unit	Description
a	[-]	attenuation
c_v	[$JK^{-1}m^{-3}$]	volume specific heat
C_C	[F]	pre-charged capacitance in ESD model
dn/dT	[K^{-1}]	thermo-optical coefficient
E_{2D}	[Jm^{-2}]	2-dimensional energy density
I_{aval}	[A]	avalanche current
I_C	[A]	collector current
I_{DS}	[A]	drain current
I_{DUT}	[A]	current through *DUT*
I_t	[A]	snapback triggering current
l	[m]	length
L	[H]	inductance
M	[-]	multiplication coefficient
n	[-]	refractive index
N	[m^{-3}]	concentration
P_{2D}	[Wm^{-2}]	2-dimensional power dissipation density
R	[Ω]	resistance
t	[s]	time
t_p	[s]	pulse length
T	[K]	temperature
V	[V]	voltage
V_{BD}	[V]	breakdown voltage
V_{BE}	[V]	base-emitter voltage
V_{DS}	[V]	drain-to-source voltage
V_{DUT}	[V]	voltage at *DUT*
V_{GS}	[V]	gate-to-source voltage
V_h	[V]	holding voltage

V_{inc}	[V]	amplitude of incident pulse
V_{refl}	[V]	amplitude of reflected pulse
V_t	[V]	snapback trigger voltage
V_T	[V]	thermal voltage
V_{TH}	[V]	threshold voltage
Z_0	[Ω]	characteristic impedance
$\Delta\varphi$	[rad]	phase shift
κ	$[Wm^{-1}K^{-1}]$	thermal conductivity
λ	[m]	wavelength
μ	$[cm^2V^{-1}s^{-1}]$	mobility
ω	$[rad^{-1}]$	angular frequency

List of Acronyms

AOM	Acoustic Optic Modulator
BCD	Bipolar, CMOS, DMOS
CDM	Charged Device Model
CMOS	Complementary MOS
DC	Direct Current
DMOS	Double-diffused MOS
DUT	Device Under Test
EMMI	EMission MIcroscopy
ESD	ElectroStatic Discharge
FG	Floating Gate
GG	Grounded Gate
HBM	Human Body Model
IC	Integrated Circuit
I/O	Input/Output
IR	InfraRed
LDMOS	Lateral DMOS
MOS	Metal-Oxide-Semiconductor
MM	Machine Model
OBIC	Optical Beam Induced Current
PC	Personal Computer
RESURF	REduced SURface Field
SOA	Safe Operating Area
SOI	Silicon On Insulator
SPT	Smart Power Technology
TCP	Temperature Compensation Point
TIM	Transient Interferometric Mapping
TLP	Transmission Line Pulse
VDMOS	Vertical DMOS
vf-TLP	Very Fast TLP

List of Publications

1. M. Blaho, D. Pogany, L. Zullino, A. Andreini, and E. Gornik: “Experimental and simulation analysis of a BCD ESD protection element under the DC and TLP stress conditions,” Microel. Reliab., 42, 2002, pp. 1281-1286
2. M. Blaho, D. Pogany, E. Gornik, L. Zullino, E. Morena, R. Stella, A. Andreini, H. Wolf and H. Gieser: “Internal behaviour of BCD ESD protection devices under very-fast TLP stress,” Proc. IRPS’03, 2003, pp. 235-240
3. M. Blaho, D. Pogany, E. Gornik, M. Denison, G. Groos and M. Stecher: “Study of internal behavior in a vertical DMOS transistor under short high current stress by an interferometric mapping method,” Microel. Reliab., 43, 2003, pp. 545-548
4. M. Denison, M. Blaho, D. Silber, J. Joost, N. Jensen, M. Stecher, V. Dubec, D. Pogany and E. Gornik: “Hot spot dynamics in quasi vertical DMOS under ESD stress,” Proc. ISPSD’03, 2003, pp. 80-83
5. V. Dubec, S. Bychikhin, M. Blaho, D. Pogany, E. Gornik, J. Willemen, N. Qu, W. Wilkening, L. Zullino and A. Andreini: “A dual-beam Michelson interferometer for invetigation of trigger dynamics in ESD protection devices under very fast TLP stress,” Microel. Reiliab., 43, 2003, pp. 1557-1561
6. J. Kuzmik, D. Pogany, M. Blaho, E. Gornik, P. Javorka, M. Marso and P. Kordos: “Breakdown and degradation processes in AlGaN/GaN HEMTs during electrostatic discharge,” WOCSDICE’03, 2003, pp. 5-6
7. J. Kuzmik, M. Blaho, D. Pogany, E. Gornik, A. Alam, Y. Dikme, M. Heuken, P. Javorka, M. Marso and P. Kordos: “Backgating, high-current and breakdown characterisation of AlGaN/GaN HEMTs on silicon substrates,” ESSDERC’03, 2003, pp.319-322
8. M. Blaho, L. Zullino, H. Wolf, R. Stella, A. Andreini, H. A. Gieser, D. Pogany and E. Gornik: “Internal behavior of BCD ESD protection devices under TLP and very-fast TLP stress,” IEEE Trans. Dev. and Material Reliab., 4, 2004, pp. 535-541
9. M. Denison, M. Blaho, P. Rodin, V. Dubec, D. Pogany, D. Silber, E. Gornik and M. Stecher: “Moving current filaments in integrated DMOS transistors under short-duration current stress,” IEEE Trans. Electron Dev., 51, 2004, pp. 1695-1703

10. V. Dubec, S. Bychikhin, M. Blaho, M. Heer, D. Pogany, M. Denison, N. Jensen, M. Stecher, G. Groos and E. Gornik: “Multiple-time-instant 2D thermal mapping during a single ESD event,” Microel. Reliab., 44, 2004, pp. 1793-1798
11. M. Heer, V. Dubec, M. Blaho, S. Bychikhin, D. Pogany and E. Gornik: “Automated set-up for thermal imaging and electrical degradation study of power DMOS devices,” accepted for ESREF’05
12. J. Kuzmík, S Bychikhin, V. Dubec, M. Blaho, M. Marso, P. Kordoš, T. Suski, M. Bockowski, I Grzegory and D. Pogany: “Characterization of III-Nitride Group Semiconductors and Devices Using Optical Methods,” WOCSDICE’05, 2005, pp. 61-62
13. J. Kuzmik, S. Bychikhin, M. Neuburger, A. Dadgar, M. Blaho, A. Krost, E. Kohn and D. Pogany: “Transient Self-Heating Effects in AlGaN/GaN HEMTs,” 47th TMS 2005 Electronic Materials Conference, 2005, pp.86

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Biography

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