DISSERTATION

Integrated Microwave Power Amplifiers

ausgeführt zum Zwecke der Erlangung des akademischen Grades eines Doktors der technischen Wissenschaften unter der Leitung von

ao. Univ. Prof. Dr. Arpad L. Scholtz
E389
Institut für Nachrichtentechnik und Hochfrequenztechnik

eingereicht an der Technischen Universität Wien
Fakultät für Elektrotechnik und Informationstechnik

von

Dipl.-Ing. Winfried Bakalski
Matrikelnummer 9527233
Metzstr.26
D-86316 Friedberg

Friedberg, im November 2003

Abstract

New wireless communication systems like wireless local area networks (wireless LAN, WLAN), satellite communications, wireless point to multipoint radio links, etc. lead to increasing efforts in the development of high-speed semiconductor technologies and RF circuits for these applications. Due to the demand for low-cost solutions and miniaturization, technologies enabling the complete monolithic integration of major RF building blocks on single semiconductor chips are strongly preferred. One of the key RF building blocks is the power amplifier (PA). Due to its position in front of the antenna, is has to fulfill several needs standing in contrary to each other: Low power consumption but high output power levels, or high transistor robustness and high speed efforts or high linearity and high efficiency. Another important task comes from the economic side: Expensive housing or matching networks are not wanted, but a high efficiency is required to face the market. A major limiting factor is the limited quality factor of on-chip passives. So some design techniques have to be considered to relax the limitations. All this, and accurate models for the transistors as well, are required to optimize the design.

The main results are:

- A highly integrated 2.4 GHz ISM PA with a minimum of external components [Bakalski 02,e, Bakalski 02,d, Bakalski 02,a] is presented. It shows outstanding efficiency performance of over 50% at 2 V of supply voltage [Bakalski 02,b].

- The first fully-integrated wireless 5.3 GHz LAN PA in SiGe-bipolar technology is developed. It fulfills the needs on linearity and is free of any external matching components including DC-block capacitors [Bakalski 03,b, Bakalski 03,c]. Further it shows almost perfect input and output matching. It features efficiency levels comparable with solutions requiring expensive external networks or ceramics [Bakalski 03,a, Ilkov 03,b, Simbürger 01, Bakalski 02,c].

- The first fully integrated SiGe-bipolar PA working up to 18 GHz is reported. It features as well all matching components integrated on-chip [Bakalski 03,d]. It is an example for the technological limits as it rises up to an f_T/f_{op} of only about 4.2. It is further an example for the limits in the usage of on-chip transformers.

Contents

List of Abbreviations

AC	*A*lternating *C*urrent
ADC	*A*nalog *D*igital *C*onverter
AF	*A*udio *F*requency
ACLR	*A*djacent *C*hannel *L*eakage *R*atio
ACPR	*A*djacent *C*hannel *P*ower *R*atio
B6HF	Infineon silicon bipolar technology with $f_T = 25\,\mathrm{GHz}$
B7HF	Infineon SiGe bipolar technology with $f_T = 72\,\mathrm{GHz}$
BALUN	*BAL*anced to *UN*balanced
BICMOS	*B*ipolar *C*omplementary *M*etal *O*xide *S*emiconductor
BJT	*B*ipolar *J*unction *T*ransistor
C	Capacitance in [F]
CDF	*C*umulative *D*istribution *F*unction
CCDF	*C*omplementary *C*umulative *D*istribution *F*unction
CMOS	*C*omplementary *M*etal *O*xide *S*emiconductor
CSMA/CD	*C*arrier *S*ense *M*ultiple *A*ccess with *C*ollision *D*etection
CW	*C*onstant *W*ave (= constant frequency)
DAC	*D*igital *A*nalog *C*onverter
DBPSK	*D*ifferential *B*inary *P*hase *S*hift *K*eying
DC	*D*irect *C*urrent
DQPSK	*D*ifferential *Q*uadrature *P*hase *S*hift *K*eying
DECT	*D*igital *E*nhanced *C*ordless *T*elecommunications
DSSS	*D*irect *S*equence *S*pread *S*prectrum
ϵ_r	Relative permittivity
ESD	*E*lectrostatic *S*ensitive *D*evice
EVM	*E*rror *V*ector *M*agnitude
f	Frequency [Hz]
F	Capacitance in [F]
f_{max}	Maximum oscillation frequency in [Hz]
f_{Op}	Operating frequency in [Hz]
f_T	Transit frequency in [Hz]
FET	*F*ield *E*ffect *T*ransistor
FHSS	*F*requency *H*opping *S*pread *S*prectrum
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GSM	*G*lobal *S*ystem for *M*obile Communication
H	Inductance in [H]
HBT	*H*eterojunction *B*ipolar *T*ransistor
HICUM	*H*igh-*C*urrent *M*odel
IC	*I*ntegrated *C*ircuit
ISM	*I*ndustrial *S*cientific *M*edical

IMD	*I*nter*M*odulation *D*istance
InP	Indium Phosphite
IP3	Third order intermodulation point
L	Inductance in [H]
λ	Wavelength in [m]
LDMOS	*L*aterally *D*iffused *M*etal *O*xide *S*emiconductor
LNA	*L*ow *N*oise *A*mplifier
LOCOS	*LOC*al *O*xidation of *S*ilicon
LTCC	*L*ow *T*emperature *C*ofired *C*eramics
n	Turn ratio
N	Number of turns
NPR	*N*oise *P*ower *R*atio
μ	Permeability in [Vs/Am]
MEXTRAM	*M*ost *Ex*quisite *Tra*nsistor *M*odel
MIM	*M*etal *I*solator *M*etal
MOS	*M*etal *O*xide *S*emiconductor
OFDM	*O*rthogonal *F*requency *D*ivision *M*ultiplex
PA	*P*ower *A*mplifier
PAE	*P*ower *A*dded *E*fficiency
PCB	*P*rinted *C*ircuit *B*oard
PHEMT	*P*seudomorphic *H*igh *E*electron *M*obility *T*ransistor
PWM	*P*ulse *W*idth *M*odulation
QAM	*Q*uadrature *A*mplitude *M*odulation
RF	*R*adio *F*requency
RMS	*R*oot *M*ean *S*quare
ρ	Reflection coefficient
SEG	*S*elective *E*pitaxial *G*rowth
SiGe	Silicon Germanium
SGP	*S*PICE *G*ummel *P*oon model
SMA	*SubM*iniatur *A* : Standard RF connector up to 18 GHz
SMD	*S*urface *M*ounted *D*evice
SPICE	*S*imultion *P*rogram with *I*ntegrated *C*ircuit *E*mphasis
Tranceiver	*TRANS*mitter and re*CEIVER*
VBIC	*V*ertical *B*ipolar *I*nter-*C*ompany model
VSWR	*V*oltage *S*tanding *W*ave *R*atio
WLAN	*W*ireless *L*ocal *A*rea *N*etwork
ω	angular frequency
Z	complex impedance in [Ω]

Chapter 1

Introduction

Every wireless communication system consists of different radio frequency (RF) and base band building blocks describing in sum a transceiver (*trans*mitter re*ceiver*). The RF building blocks are shown in fig. 1.1. The digital part containing the base band circuit of a modern communication system ends with its Analog/Digital converters. Due to the fact that the design of A/D converters is limited in speed, accuracy (e.g. quantization errors, noise..) [Schweinzer 96], a certain range in its resolution and the power consumption for fast converters, it is only possible to design "software radio" for a certain frequency range. Today, there only exist a small amount of real "software radios", such as shortwave receivers for frequencies up to 30 MHz [Cuno 03]. As today's mobile applications all can be found in the frequency range from 430 MHz to several GHz, it is obvious that there must be analog RF circuits outside the base band.

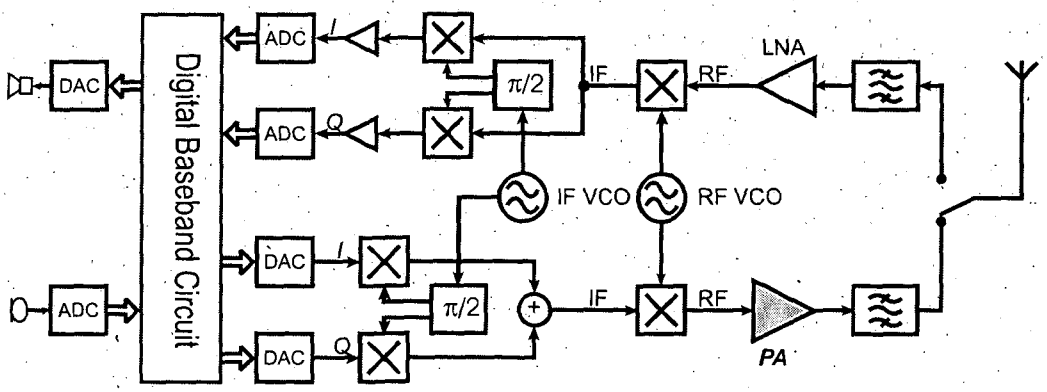


Figure 1.1: Block Diagram of a typical wireless digital communications tranceiver.

The power amplifier (PA) is one of the main building blocks of a radio frequency (RF) wireless communication system. Different to other amplifiers types, it has the focus on delivering high output power, as it usually has to drive the antenna.

The PA can be found in front of the antenna switch. As well as other building blocks there are several aims in the design of the PA, caused by the needs for its applications. Besides the necessary output power level, which can be limited by technology as well as specifications and law reglementations, it usually has to meet linearity specifications and/or efficiency specifications. Due to the fact, that the PA together with processor are mainly responsible for the system power consumption it is quite obvious, that efficiency means battery life time. Figure 1.2 shows the power consumption statistics of a DECT wireless telephone headset chipset. In this example, three battery cell operation is estimated, as lower supply voltage causes the use of DC/DC converters lowering the efficiencies for certain building blocks such as the transceiver chip. It shows, that even for a wireless communication system like DECT with low output power levels, the PA requires about up to half of the whole RF circuitry power supply.

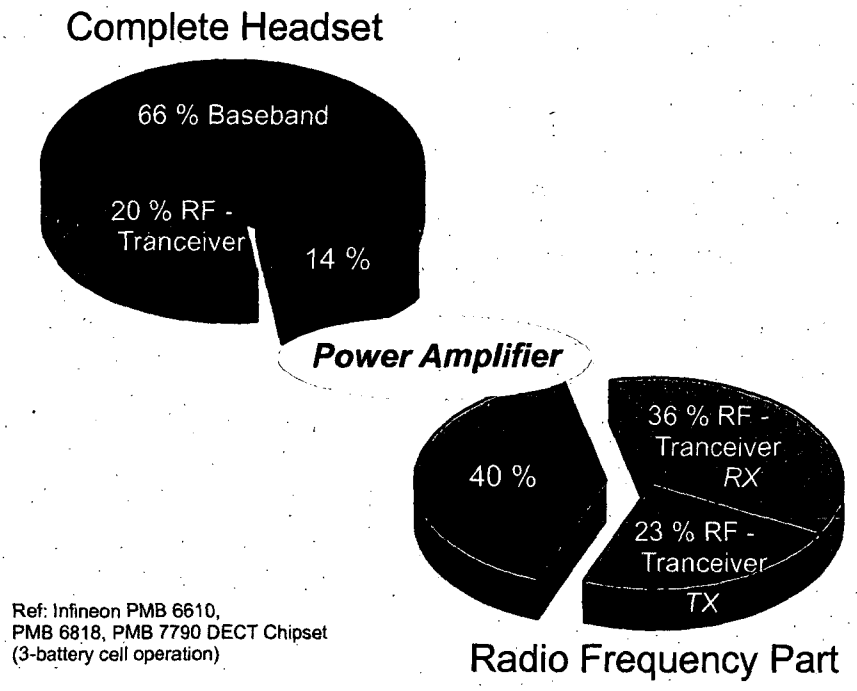


Figure 1.2: Power consumption statistics for a DECT headset chipset. (Infineon PMB 6610 tranceiver, PMB 6818 PA and PMB 7790 DECT Controller). The average power consumption values represent the normal operation mode with the PA being half time at low power and half time in high power mode.

As the PA is one of the main keys to reduce power consumption, it is necessary to improve the efficiency as much as possible. This includes also the use of efficient matching networks, switches and antennas [Krischke 95, Cripps 99, Gonzales 84, Vizmuller 95, Johnson 84, Bonek 00, Ilkov 03,b, Ilkov 03,a, Bakalski 02,e, Bakalski 02,d, Bakalski 02,a]. Another task is the linearity: New OFDM systems require highly linear PAs to guarantee the system performance. The more frequency carrier or

symbols [Agilent 02,a] are used, the tougher the linearity efforts become.

In the past years, a lot of design philosophies for power amplifiers have become feasible. Basically there exist three topologies and a lot of amplifier classes delivering a rough description of the used design. Chapter 2 gives an overview of PA characteriziation, the topologies and different classes used to categorize the design. However all these rely on the used semiconductor technology. An overview of the Si-based bipolar processes used for this thesis will be given in Chapter 3. Of course, the reason for the wide range of different technologies is not only for circuit design or technological reasons: The cheaper the building blocks can be produced, the easier a wireless system can be accepted by the market, as the products become affordable. The economic side cannot be neglected.

Currently, the market of PAs for mobile wireless applications is dominated mainly by GaAs or InP derivate technologies [Raab 03], the so-called III-V technologies[1]. It is a difficult task to compare the cost of different technologies per chip, as they depend on a lot of factors such as wafer size, mask resolution, amount of pieces to be produced and so on. Typically the cost of InP based chips is about 8 times higher than for standard Si-bipolar and GaAs based chips about 4 times higher. Typical III-V transistors are the HEMT (High Electron Mobility Transistor) and the HBT (Heterojunction Bipolar Transistor). III-V compound devices have typically lower packing densities and lower yields, increasing their per piece prices. The calculation for CMOS based circuits is much more difficult, as the circuits are more and more a mixture between baseband and RF circuits. While digital circuits can be scaled down very well by decreasing the structure size, this is not really possible for RF circuits, as components like inductors or capacitors cannot be scaled down, because of the fixed operating frequency. The main cost factor on very-large scaled CMOS processes today is the price for mask sets which are typically 10-15 times higher than in Si/SiGe-bipolar processes considering today's 120 nm CMOS processes. They become efficient only for very high production volumes. It has to be mentioned that the maximum yield and the different wafer sizes make a calculation difficult. For cheaper mass production usage there exist only a small amount of solutions on standard CMOS, Si or SiGe based power amplifiers [Aoki 01, Baltus 01, Parkhurst 98, Vathulya 01, Simbürger 00,a, Simbürger 01, Bakalski 02,c, Bakalski 02,b]. Especially [Vathulya 01] shows the basic problems in the design of CMOS PAs: The gate oxide breakdown and the hot carrier effect, which is a knock-out criterion for reliability issues. Other PA technologies featuring a high ruggedness such as LDMOS (Laterally Diffused MOS) are limited to lower microwave frequencies (typically 2 GHz) due to their direct grounding in its source eliminating bondwire inductances used to produce a negative feedback. Thus the gain at high frequencies is reduced [Raab 03].

Furthermore, it is also necessary to mention, that the highest possible integration is an important task to fulfill the market needs. Chips using a sec-

[1]III-V: Description for the used elements of the chemical periodical system. The roman number tells the used material group. e.g. Ga = III , As = V, In = III, P = V

ond integrated circuit for negative bias voltages, such as in most GaAs MMIC PHEMT technology based amplifiers like [Raytheon 02], will not survive the next years, as packaging is an important cost factor as well as the used semiconductor technology. This implies that the full integration of all matching networks into the PCB [Weber 97, Simbürger 00,a, Simbürger 01, Bakalski 02,c, Bakalski 02,b], module [Yoshida 98, Bakalski 03,a, Ilkov 03,b, Ilkov 03,a] or even the die [Aoki 01, Bakalski 03,c, Bakalski 03,b, Bakalski 03,d] should be the next step in RF integration. An introduction on matching networks for the output and on-chip matching can be found in Chapter 4.

This work presents some issues in the successful integration of matching components as well as the implementation of power amplifier techniques on standard SiGe-based technologies. It starts up in Chapter 5 with a design for the 2.4 GHz ISM band [Bakalski 02,c, Bakalski 02,b], where wireless systems like Bluetooth and Wireless LAN or even wireless telephones are typical examples for its usage. In Chapter 6, a 5 GHz wireless LAN amplifier [Bakalski 03,c, Bakalski 03,b] is presented. As higher frequencies imply smaller wave lengths, the required chip area for matching networks decreases. Therefore it is an important task to include as much matching network onto the die if possible, as packaging becomes a difficult task at high frequencies. Finally Chapter 7 presents a 17.2 GHz PA or driver design for future wireless LAN applications [Bakalski 03,d]. It is also an example, in which range transformers as matching networks could be used.

Chapter 2

RF power amplifier design

2.1 RF power amplifier characterization

Power amplifiers have their usage on the most different applications. Therefore it is necessary to characterize them to fit the right design into the right system. The following sections should give a brief introduction in typical characterization methods.

2.1.1 The power transfer characteristic

The power transfer characteristic curve represents the plot of the output power over the input power. A typical example for such a curve can be found in fig. 2.1.

This plot is one of the most often found in all application notes and datasheets. It is possible to get the information on small signal gain, the 1 dB compression point (P1dB) and the saturated output power (P_{SAT}). In some cases oscillation problems at the operation frequency are as well obtained (when the output power does not converge to 0 if no input power is supplied).

The small signal gain can be read out of the curve in the linear region (fig. 2.1). The linear region is found for an input power range beginning above the noise floor and ending up into the compression. In this area, the small signal gain is obtained by the difference between output power and input power:

$$G[\text{dB}] = P_{OUT,LIN}[\text{dBm}] - P_{IN,LIN}[\text{dBm}] \tag{2.1}$$

In addition, there exists also the saturated gain:

$$G_{SAT}[\text{dB}] = P_{OUT,SAT}\,[\text{dBm}] - P_{IN,SAT}\,[\text{dBm}] \tag{2.2}$$

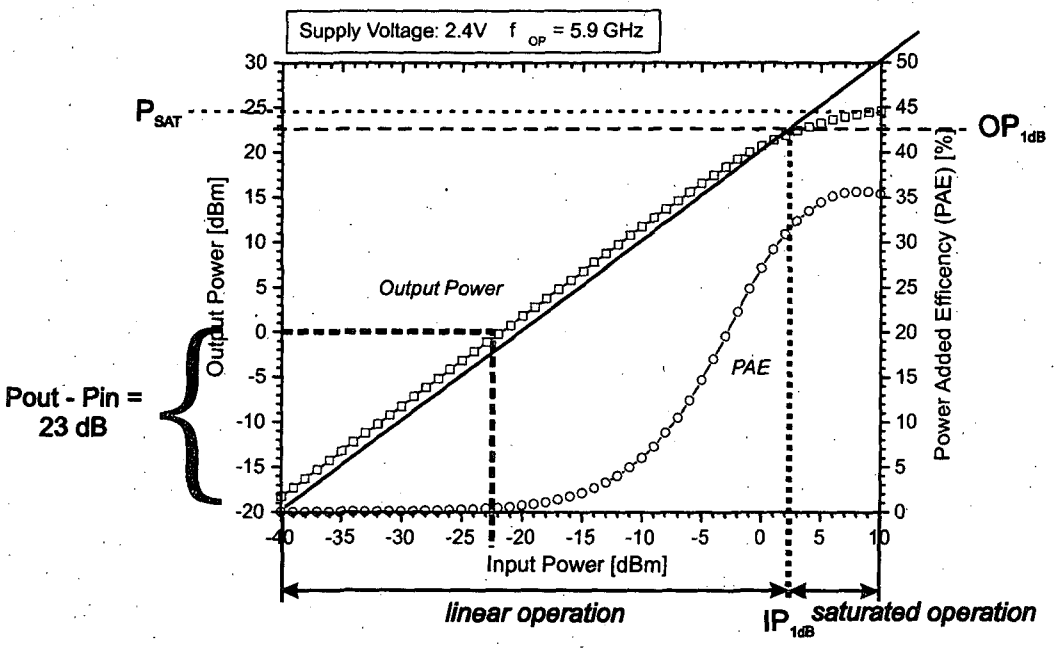


Figure 2.1: A typical PA power transfer characteristic plot [Bakalski 03,a].

Usually this definition is often used for systems operating with a saturated power amplifier (PA), such as GSM.

The point where the PA is driven into the compression is named the 1 dB compression point: It describes, for which power level the small signal gain is reduced by 1 dB. Concerning the output power it is the 1 dB output compression point (OP1dB) and for the input power the 1 dB input compression point (IP1dB):

$$OP1dB\ [\text{dBm}] = IP1dB\,[\text{dBm}] + G\,[\text{dB}] - 1\,\text{dB} \tag{2.3}$$

Using the power transfer characteristic plot, the 1 dB compression point can be observed by adding a linear help line with the slope of 1 representing a small signal gain (G) lowered by 1 dB (offset of the help line): The cross of this line with the power transfer characteristic curve gives the 1 dB compression point (P1dB) (fig. 2.1). Finally, the saturated output power can be found as well: The absolute maximum output power level the PA is able to deliver. This information is usually necessary for the dimensioning of the PA output stage. Chapter 2.2 shows some issues on it based on the selected PA topology.

Figure 2.1 also shows the Power Added Efficiency (PAE) curve. This curve represents the overall efficiency of a PA. It is defined by the quotient of the output power divided by all input power the circuit is feeded with [Raab 03]:

$$PAE = \frac{P_{OUT}}{P_{DC} + P_{IN}} \tag{2.4}$$

where P_{DC} stands for the DC supply from the power supply, P_{IN} for the input power and P_{OUT} for the output power. In the case of high gain, the power added efficiency can also be simplified to

$$PAE \approx \frac{P_{OUT}}{P_{DC}} \tag{2.5}$$

which is the definition for the *DC-to-RF Efficiency* or often only called *Efficiency*. If the PA has a gain over 20 dB so that the RF input power can be neglected, the PAE is the same as the DC-to-RF efficiency. It has theoretical limits, and each amplifier class implies the maximum efficiency for the case that all components being assumed to work ideal. The amplifier classes are described in section 2.3.

Another term often found in PA circuits is the collector efficiency CE for circuits using bipolar junction transistors (BJT) and the drain efficiency DE for field effect transistors (FET). It is defined by the output power divided by the power supply of the transistor without bias-currents:

$$CE = \frac{P_{OUT}}{P_{DC,Transistor}} = \frac{P_{OUT}}{V_{CC} \cdot I_C} \tag{2.6}$$

for BJTs with I_C representing the collector current and V_{CC} for the supply voltage.

$$DE = \frac{P_{OUT}}{P_{DC,Transistor}} = \frac{P_{OUT}}{V_{DD} \cdot I_D} \tag{2.7}$$

for FETs with I_D representing the drain current and V_{DD} for the supply voltage.

Furthermore there exist efficiency definitions considering the average efficiency, as PAs are often used for a certain range of different input power levels. The average efficiency is defined by

$$\eta_{AVG} = \frac{P_{OUT,AVG}}{P_{IN,AVG}} \tag{2.8}$$

The average power levels are usually determined by probability functions based on the used modulation scheme.

2.1.2 The frequency response

Every RF PA has a certain operating frequency range, for which it is designed. Depending on the used matching and the center operation frequency the bandwidth can vary quite much. Figure 2.2 shows a typical frequency response plot for a narrow-band PA [Simbürger 01].

In this example the 3 dB bandwidth can be read out quite simple: Just examine the frequency where the output power is going down about 3 dB (the half output

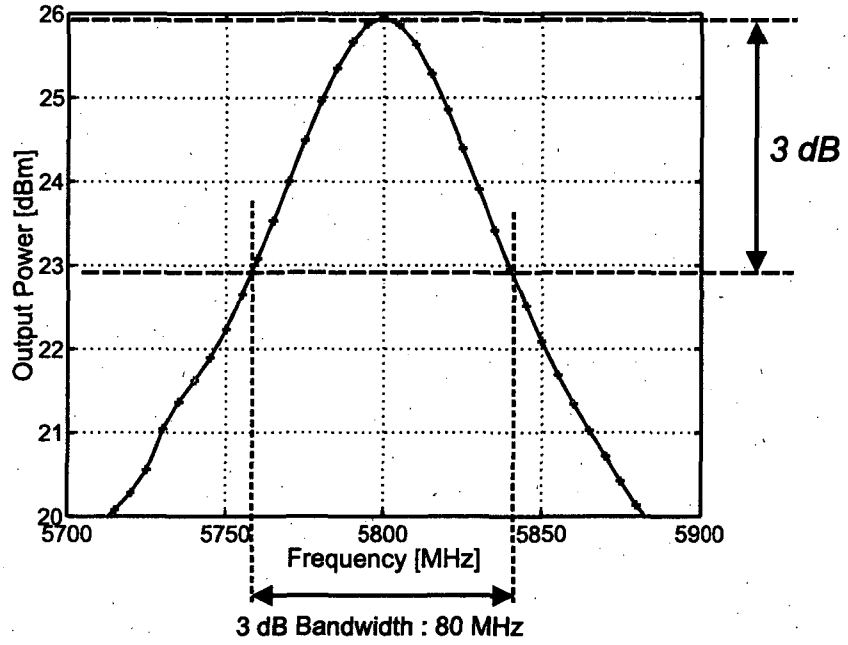


Figure 2.2: A typical PA frequency response plot.

power). The resulting frequency range gives the 3 dB bandwidth. Usually the range of operation depends on the application: For linear multicarrier systems the output power deviation has to be much smaller to satisfy conditions like *E*rror *V*ector *M*agnitude (EVM) (described in 2.1.4 or [Agilent 02,b]). Hereby the usable bandwidth is narrowed much more, so that the bandwidth is for example a 1 dB-bandwidth.

2.1.3 The third order intercept point (IP3)

Linear PAs gain more and more importance, as new communications systems like Wireless LAN require a high linearity to ensure proper operation. The most popular linearity measurement is the intermodulation measurement on third order interception (IP3). It gives the output power level (OIP3), when the third order intermodulation product reaches the fundamental frequency output power level (fig. 2.5). This level usually cannot be reached, as the amplifier saturates much earlier. It is observed by considering a nonlinear amplifier, or in the simplest case, a nonlinear transistor: The nonlinear transistor curve or PA curve can be formally written as

$$I_C = A_1 U_{BE} + A_2 U_{BE}^2 + A_3 U_{BE}^3 + ... \tag{2.9}$$

with I_C for the Collector current of a bipolar transistor and U_{BE} for the input voltage between Base and Emitter.

Applying two signals with a different frequency [1] on the input of the PA,

$$U_{BE} = U_1 \cos(\omega_1 t) + U_2 \cos(\omega_2 t) \tag{2.10}$$

with $\omega_1 - \omega_2 \ll \omega_1, \omega_2$, the output current of the transistor is

$$\begin{aligned}
&I_C = \\
&= A_1[U_1 \cos(\omega_1 t) + U_2 \cos(\omega_2 t)] + \\
&+A_2[U_1^2 cos^2(\omega_1 t) + U_2^2 cos^2(\omega_2 t)^2 + 2U_1 U_2 \cos(\omega_1 t) U_2 \cos(\omega_2 t)] + \\
&+A_3[U_1^3 cos^3(\omega_1 t) + U_2^3 cos^3(\omega_2 t) + 3U_1^2 U_2 cos^2(\omega_1 t) \cos(\omega_2 t) + \\
&+ \quad 3U_1 U_2^2 cos(\omega_1 t) cos^2(\omega_2 t)] + \\
&\qquad\qquad + \quad ...
\end{aligned} \tag{2.11}$$

Using the additional theorems [Bartsch 99] on eqn. 2.11, the spectral parts of the output signal are easy to obtain with the dependence on linear, quadratic, cubic and other parts:

$$\begin{aligned}
&I_C = \\
&\begin{array}{ll}
\text{linear term:} & A_1[U_1 \cos(\omega_1 t) + U_2 \cos(\omega_2 t)] \quad + \\
\text{quadratic term:} & \frac{1}{2} A_2[U_1^2(1 + \cos(2\omega_1 t) + \\
& +2U_1 U_2((\cos(\omega_1 - \omega_2)t + \cos(\omega_1 + \omega_2)t) + \\
& +U_2^2(1 + \cos(2\omega_2 t)] \quad + \\
\text{cubic term:} & A_3[\frac{1}{4} U_1^3((3\cos(\omega_1 t) + \cos(3\omega_1 t)) + \frac{1}{4} U_2^3((3\cos(\omega_2 t) + \cos(3\omega_2 t)) + \\
& +\frac{3}{2} U_1^2 U_2(\cos(\omega_2 t) + \frac{1}{2}\cos(2\omega_1 - \omega_2)t + \frac{1}{2}\cos(2\cos(2\omega_1 + \omega_2)t) + \\
& +\frac{3}{2} U_1^2 U_2(\cos(\omega_1 t) + \frac{1}{2}\cos(2\omega_2 - \omega_1)t + \frac{1}{2}\cos(2\cos(2\omega_2 + \omega_1)t)]
\end{array} \\
&\qquad\qquad + \quad ...
\end{aligned} \tag{2.12}$$

With this, the spectral parts that could be found in term 2.12 are:

linear term	ω_1, ω_2
quadratic term	DC, $\mid \omega_1 - \omega_2 \mid$,$\mid \omega_1 + \omega_2 \mid$, $2\omega_1$, $2\omega_2$
cubic term	ω_1, ω_2, $\mid 2\omega_1 - \omega_2 \mid$, $\mid \omega_1 - 2\omega_2 \mid$, $2\omega_1 + \omega_2$, $\omega_1 + 2\omega_2$, $3\omega_1$, $3\omega_2$

The resulting spectrum of an amplifier with a quadratic and cubic nonlinearity can be found in figure 2.3. The output power is plotted logarithmic [dBm], and some of the third order intermodulation products can be found in the operating frequency area causing errors in the output signal. The distance between the output power at the fundamental frequency and its unwanted intermodulation products is called the intermodulation distance IM3 for 3rd order and IM5 for 5th order intermodulation products.

[1] usually the same amplitude to simplify the measurements

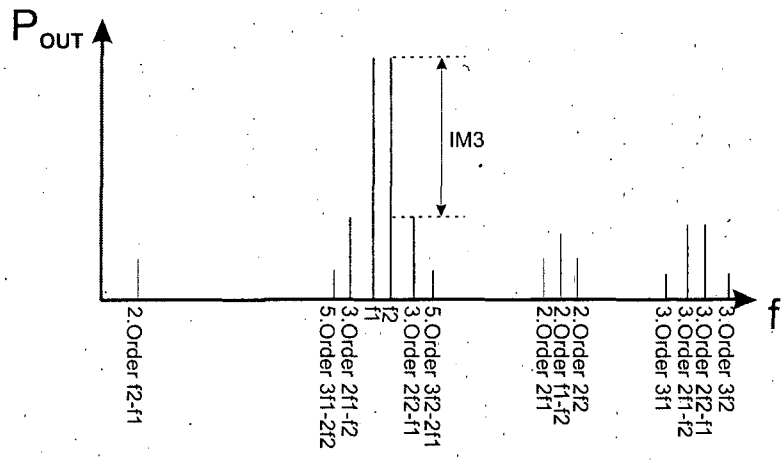


Figure 2.3: Output spectrum of a nonlinear PA: quadratic and cubic nonlinearity are shown.

There exists also another description for the intermodulation distance: The carrier to intermodulation ratio C/I. Hereby the C/I ratio describes the distance between carrier and all intermodulation products. Figure 2.4 shows a typical measurement setup for measuring the third order intermodulation point.

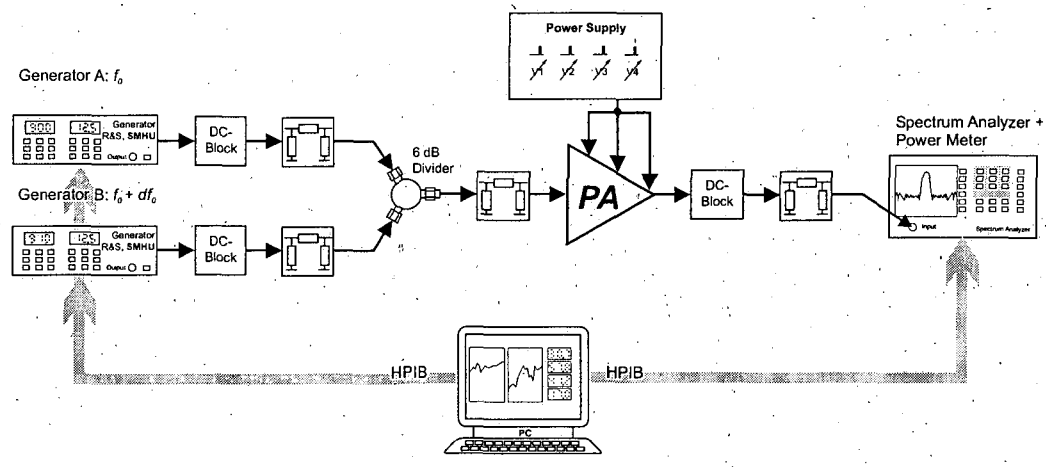


Figure 2.4: Two Tone measurement setup for the third order Intermodulation point.

In this setup two similar generators with a small frequency difference[2] are used for the IP3 measurement. To prevent any measurement errors, a lot of attenuators have to be used between the stages. This ensures that the generators and the device under test, the PA are loaded with 50 Ω loads everywhere. This is

[2]typically 10 MHz, depending on the spectrum analyzer accuracy and frequency resolution

important, as mismatched generators itself and in combination with mismatched hybrids can cause additional intermodulation not caused by the PA. Especially at the input of the PA the signal has to be checked for such effects. Figure 2.5 shows a typical IP3 plot for a 17 GHz PA [Bakalski 03,d] using this setup. Due to the limited output power of the generators and the high attenuation, the saturated region of the PA is not reached by the fundamental frequency power transfer characteristic. The 3rd order intermodulation point IP3 is defined by the crossing of the fundamental frequency and the 3rd order intermodulation curve for the linear operated region (non-saturated). It is important to mention, that the 3rd order intermodulation *must* have a slope of 3.

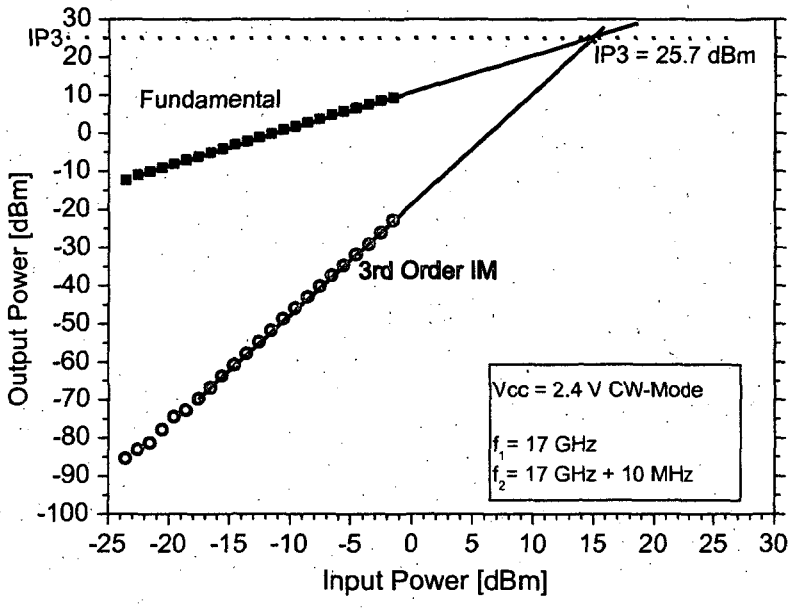


Figure 2.5: IP3 measurement of a 17 GHz PA [Bakalski 03,d].

The cross of the fundamental transfer characteristic with the 3rd order intermodulation slope implies in fig. 2.5, that the output IP3 can be easily calculated by the measurement of only two power levels using a spectrum analyser:

$$IM3[\text{dB}] = P(f_2)\,[\text{dBm}] - P(2f_2 - \omega_1)\,[\text{dBm}] \tag{2.13}$$

$$OIP3[\text{dBm}] \approx P(f_2)\,[\text{dBm}] + \frac{1}{2} \cdot IM3\,[\text{dB}] \tag{2.14}$$

Measuring just two power levels below the OP1dB compression point allows to estimate the OIP3. It has to mentioned that using eqn. 2.14 is only valid if the measured power levels fit exactly to the slopes of 1 and 3 respectively.

2.1.4 The Error Vector Magnitude (EVM) characterization

Digital communication systems use vector modulated modulation schemes. The digital bits are mapped to symbols in the constellation diagram [Hlawatsch 99]. Figure 2.6 shows a typical constellation diagram used for IEEE 802.11a wireless LAN systems.

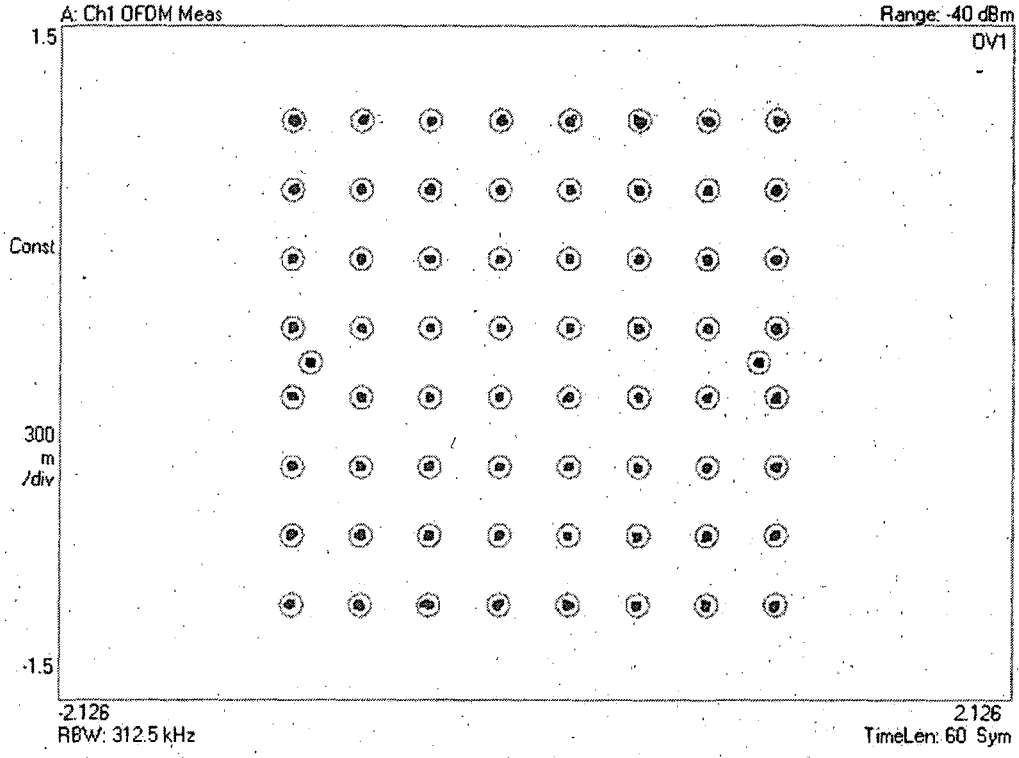


Figure 2.6: Measured 64-QAM constellation diagram. The signal was measured undistorted directly out of a generator capable to generate IEEE 802.11a test-signals (WLAN, 54Mbit/s, 64-QAM). The additional two symbols represent the tracking cursors required for the test set measurement to obtain the right amplitude and phase.

These data symbols consisting of several data bits have a certain position in this I/Q-plane represented by the carrier magnitude and the phase for a certain data clock transition. To ensure, that the signal is demodulated correctly, the exact magnitude and the exact phase at each clock transition have to be guaranteed within a certain error margin.

Figure 2.7 shows what happens, when a symbol of the I/Q-plane is shifted in its magnitude and phase. The EVM is measured for a certain modulation scheme and is defined by the scalar distance between two signal vector end points

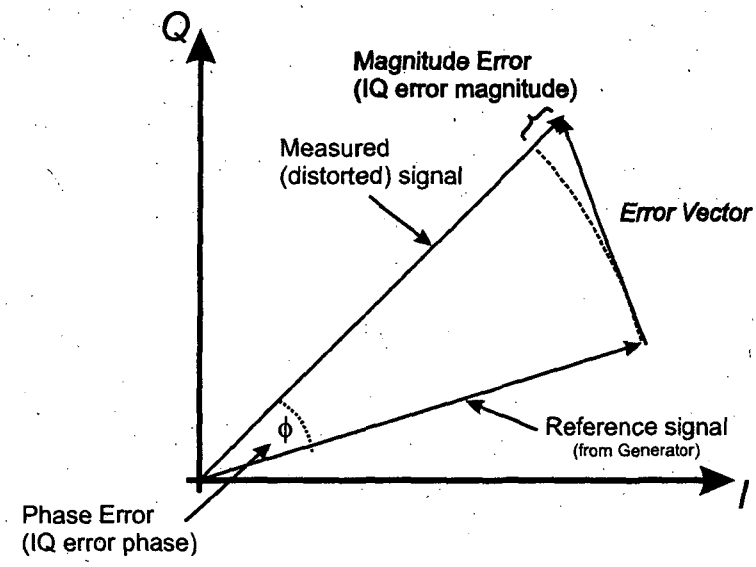


Figure 2.7: Signal vector deviation of a distorting RF building block. The blue vector represents the resulting error vector.

[Agilent 02,b, 3GPP 03]. Usually EVM can be measured for peak and RMS errors. For applications needing a high linearity the RMS value is of higher interest, as the peak (saturated) operation is not used. The relative RMS vector error is defined by

$$\text{RMS EVM} = \sqrt{\sum_{k\in K} |E(k)|^2 / \sum_{k\in K} |S(k)|^2} \tag{2.15}$$

with E(k) representing the error vector and S(k) the signal vector for each data clock transition k and K for the whole set of symbols.

The symbol vector error for a symbol k is defined by

$$\text{EVM(k)} = \sqrt{\left(\frac{|E(k)|^2}{\sum\limits_{k\in K} |S(k)|^2}\right)/N} \tag{2.16}$$

with N the total number of elements in the set K.

The EVM is usually given as percentage of the peak signal level error for the outermost symbols of the constellation diagram.

With a Vector Signal Analyzer (VSA), such vector modulation schemes can be measured. With the knowledge of the original signal, the error in the magnitude and the phase can be easily determined [Agilent 02,b]. The EVM measurement allows also further troubleshooting in RF circuits, an overview can be found in

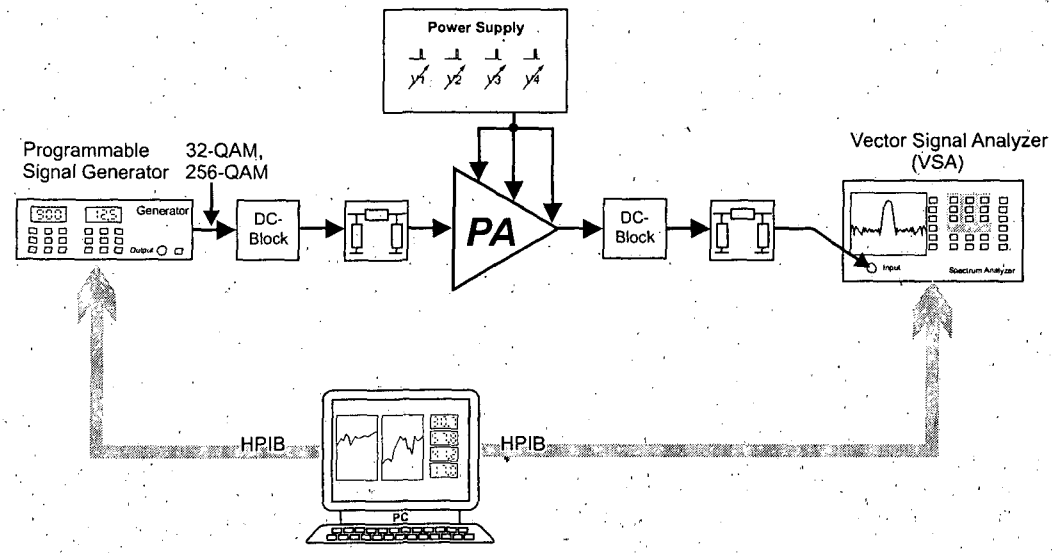


Figure 2.8: Error Vector Magnitude (EVM) measurement setup using a Vector Signal Analyzer (VSA).

[Agilent 02,b] and in the flow chart 2.9. A typical measurement setup is shown in fig. 2.8.

For PAs, a certain level of distortion could be tolerated. A common maximum value for RMS EVM is 3 % for wireless LAN applications which could usually be found in datasheets.

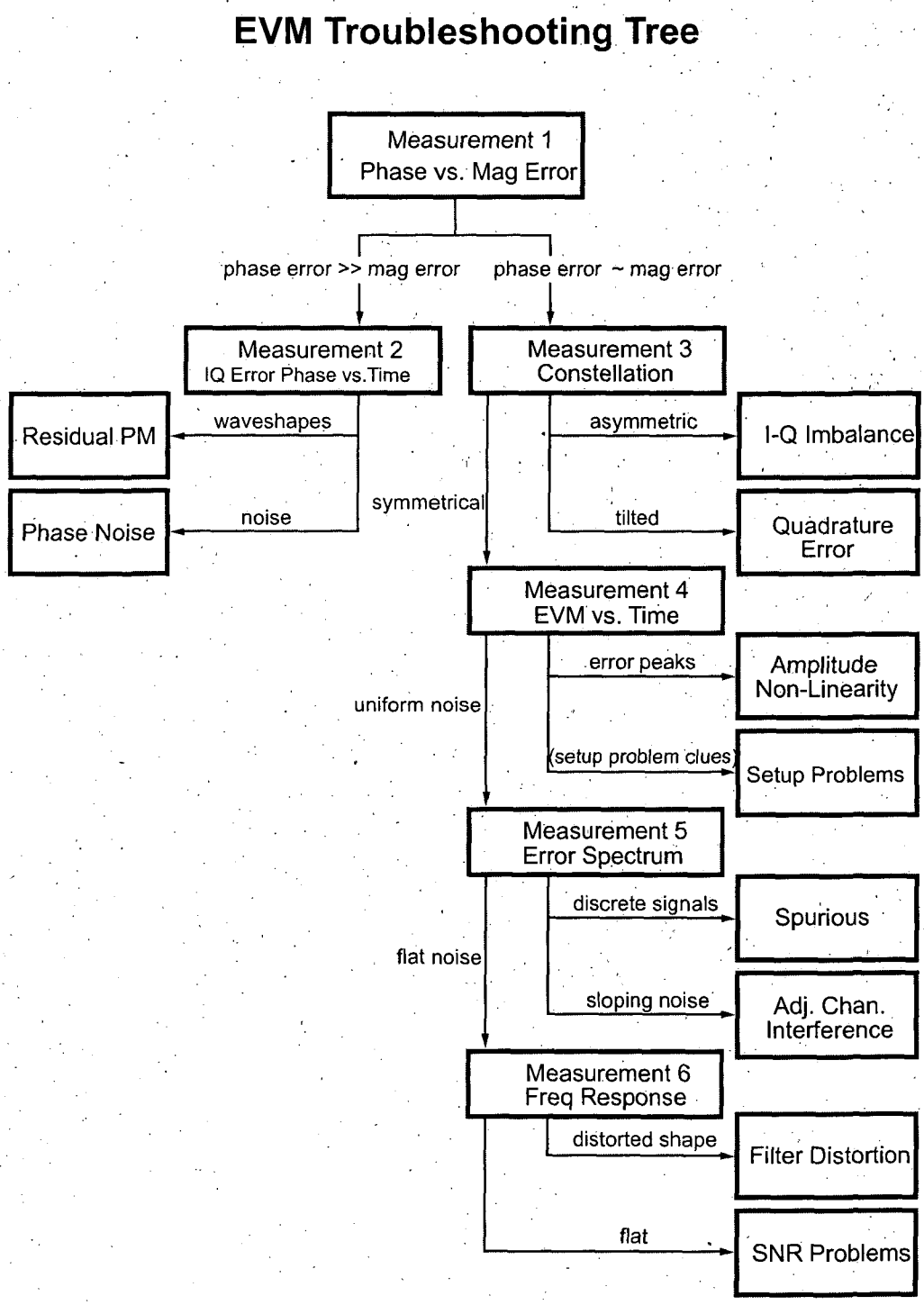


Figure 2.9: Flow chart for analyzing vector modulated signals using EVM measurements (taken from [Agilent 02,b]).

2.1.5 The Power Complementary Cumulative Distribution Function (CCDF)

As new digital modulation formats (especially with WLAN and the so called 3G Systems) feature higher peak-to-average power ratios, the power distribution function is of importance not only for the calculation of average efficiencies but also for the design of PAs, as the operation in a saturated area leads to a deformation of the outgoing power distribution function. The look on output power distribution functions was not of interest as long as modulation schemes like analog FM with a fixed output power level or AM signals with a peak to unmodulated signal ratio of 6 dB (limited by modulation index) have been the typical applications. But for coded Orthogonal Frequency Division Multiplexing (OFDM) with a large amount of symbols there exist a large amount of different magnitudes and phase values for each symbol in the I/Q-plane. This causes a wide range of output power levels. As a result, the symbols in the I/Q plane will shift due to magnitude and/or phase errors. For example, applying the undistorted 64-QAM signal in fig. 2.6 to a PA [Bakalski 03,b] with an average power in the region of P1dB, the signal will look like fig. 2.10.

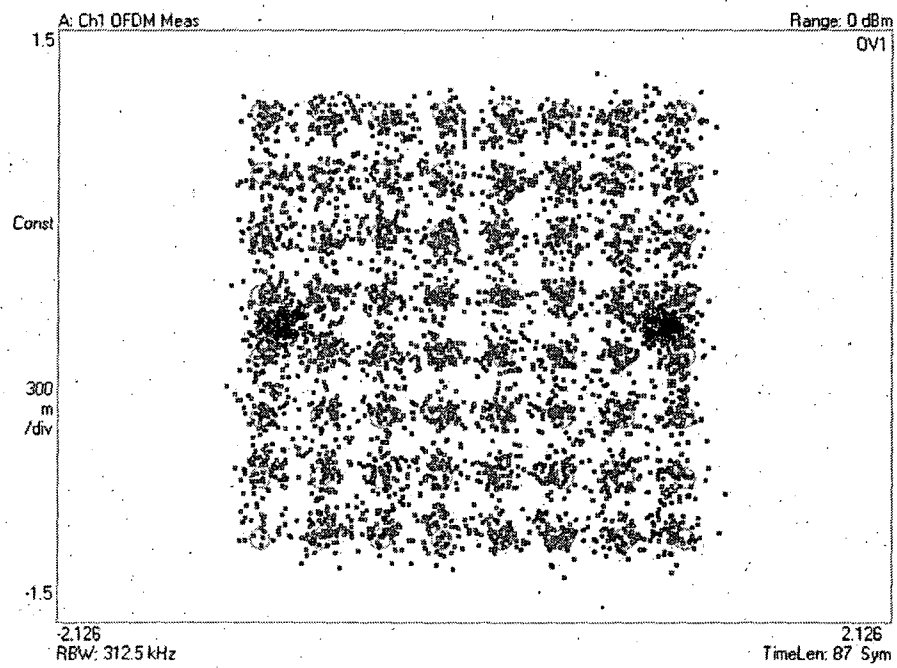


Figure 2.10: Measured 64-QAM constellation diagram of a PA working in the compression. The average power was selected to be -7 dBm at the PA presented in [Bakalski 03,b]. The additional two symbols represent the tracking cursors required for the test set measurement to obtain the right amplitude and phase.

The main idea of the power Complementary Cumulative Distribution Function

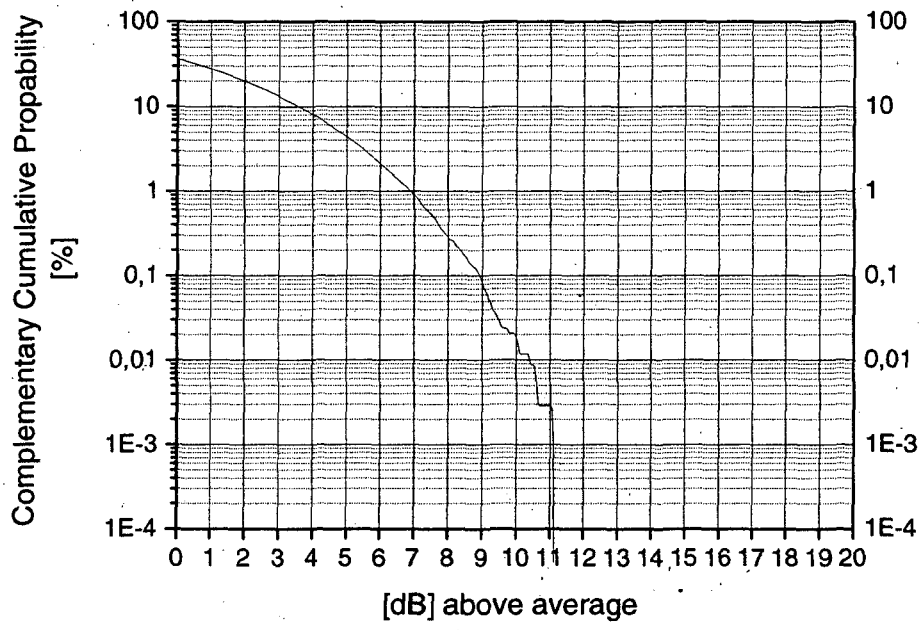


Figure 2.11: Measured undistorted IEEE 802.11a WLAN, 54 Mbit/s 64-QAM output signal CCDF curve.

(CCDF) [Agilent 02,a] is to describe the probabilities of the power levels by the signal, and how the RF building block, like the PA but also other components like low noise amplifiers (LNA), mixers will deform the curve. A CCDF curve gives the information on the probability a signal has got for a certain power level. Figure 2.11 shows the CCDF of a IEEE 802.11a 64-QAM signal. The signal varies in its maximum output power by 11 dB, so that a typical back-off from the P1dB compression of 10 dB is used. Applying higher input power to a PA will shift the output peaks into the compression and thus lead to increased errors in the I/Q constellation plane. Figure 2.12 shows the CCDF for a PA [Bakalski 03,b] driven into strong compression.

The CCDF curve bases on the probability density function (PDF) $p_x(\xi)$ given by the modulation scheme, hence by the probability of the symbols. The integration of the PDF gives the Cumulative Distribution Function (CDF) [Weinrichter 91]:

$$CDF(\xi) = \int_{-\infty}^{\xi} p_x(\alpha)d\alpha. \tag{2.17}$$

Inverting it, by subtracting the CDF from 1 (CCDF = 1 - CDF) gives the Com-

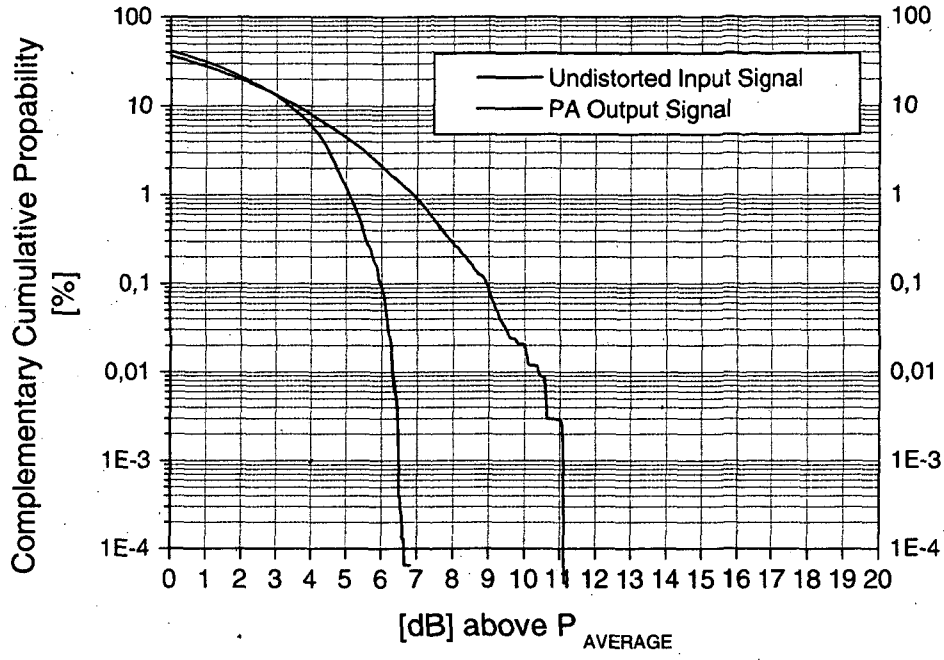


Figure 2.12: Measured undistorted input signal and a strongly compressed 64-QAM output signal CCDF curve. The PA was driven with an average input power of -4 dBm which is in the saturated area [Bakalski 03,b].

plementary Cumulative Distribution Function (CCDF):

$$CCDF(\xi) = 1 - \int_{-\infty}^{\xi} p_x(\alpha) d\alpha. \tag{2.18}$$

The difference between the CDF and CCDF curve is that the CCDF curve emphasizes peak power levels instead of minimum power levels in the CDF. The CCDF can be seen as an improvement on characterizations using the Crest Factor, as single peak levels are stressed much more. The Crest Factor itself is defined as the ratio of the peak voltage to RMS voltage level, but for the whole signal. Using only the crest factor would ignore single peak levels like parasitic effects, and the peak value measurement would strongly depend on the measurement time, and thus lead to problems in repeated measurements [Agilent 02,a].

2.1.6 Noise Power Ratio (NPR)

The Noise Power Ratio (NPR) is a less common linearity characterization method as it is now replaced more or less by CCDF or EVM characterization. Herby it is used to characterize the PA behavior used for multi-carrier signals (>10 carriers). Idea of this test procedure is to feed the PA with a white noise signal containing a notch in its spectrum. A nonlinear PA will cause the notch to disappear [Katz 03, Raab 03].

The white noise simulates many carriers of random amplitude and phase. A multi-carrier system is therefore well-covered and it is easier to feed the device-under-test with a noise than with multiple well defined carriers that even do not interfere with each other. Usually the signal is generated with a noise-source [3] [Flecker 84] that is connected to a band-pass filter and a notch filter in series (fig. 2.13).

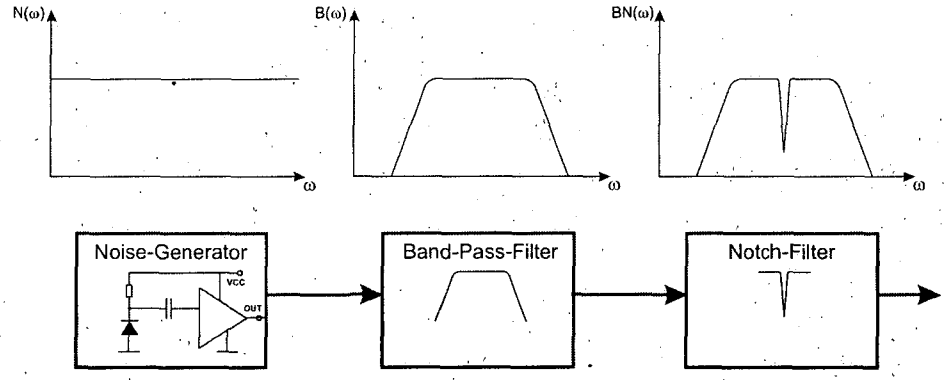


Figure 2.13: Generation of a test-noise for NPR analysis.

The notch depth can easily be measured by the use of a spectrum analyzer. Applying the signal to a PA with its intermodulation products will cause the notch to be filled up. The NPR is defined by ratio of the notch power to the average signal power (fig. 2.14):

$$\mathrm{NPR}\,[\mathrm{dBc}] = \frac{P_{OUT}(\omega_{Notch})}{P_{OUT;AVG}} \tag{2.19}$$

2.1.7 Adjacent Channel Power Ratio (ACPR)

The Adjacent Channel Power Ratio (ACPR) is another very common linearity characterization. Especially in applications working with frequency multiplex, ACPR is often used. The ACPR is the ratio of the out of band power (of a specified range) to the RMS signal power. It characterizes the affection to adjacent

[3] It is typically realised using an avalanche diode.

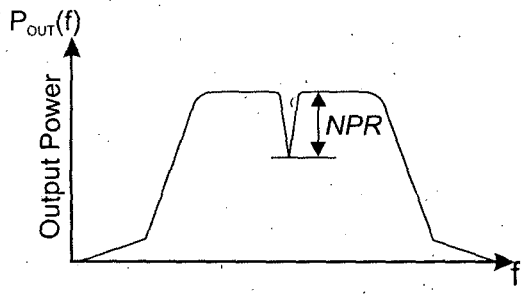


Figure 2.14: NPR measurement definition.

channels due to nonlinearity. Inverting the ACPR definition gives the Adjacent Channel Leakage Ratio (ACLR), which is not very common, but used in some R&S[4] measurement enviroments [Banerjee 02].

As introduced before, the ACPR can be defined by [Raab 03, Kenington 00]:

$$\mathrm{ACPR}_L\,[\mathrm{dBc}] = \frac{\int_{f_c - f_0 - \frac{BW_L}{2}}^{f_c - f_0 + \frac{BW_L}{2}} |H(f)|^2 S(f) df}{\int_{f_L}^{f_U} |H(f)|^2 S(f) df} \tag{2.20}$$

with S(f) representing the power spectrum, H(f) a pulse-shaping filter (CDMA applications) f_c the center frequency, BW the bandwidth, f_0 the offset, and f_L and f_U lower and upper band edge, respectively.

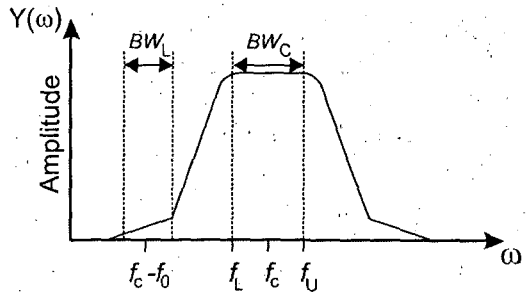


Figure 2.15: ACPR_L measurement definition.

Eqn. (2.20) specifies the lower sideband, but it is possible to specify the upper side band as well. Furthermore, sometimes the ACPR is defined for two different frequency offsets, and the outer band ACPR is often called Alternate Channel Power Ratio.

[4]R&S stands for Rohde&Schwarz, a measurement equipment manufacturer.

2.1.8 PA ruggedness: Operation into mismatch loads

Mobile wireless communication systems such as GSM have the problem that the antenna finds itself in the most different conditions. Thus the offered load to the PA will not be in the optimum area as desired. In fact high VSWR peaks can occur, which may damage the PA. To test the ruggedness of the PA, fig. 2.16 shows a measurement setup for testing the PA with mismatched loads. The sliding short together with the attenuator provides a variable load to the PA, thereby emulating a mismatched antenna. Harmonics and spurii can be measured under different mismatch conditions using the spectrum analyser.

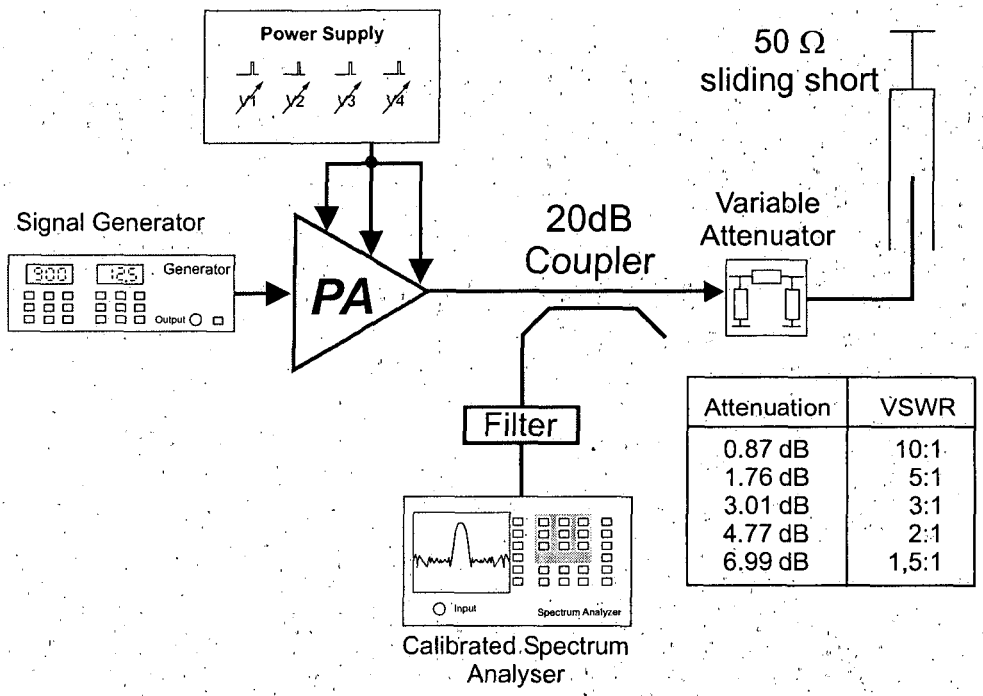


Figure 2.16: Test setup for the operation into mismatched loads.

2.2 RF power amplifiers topologies

RF power amplifiers have been constructed in three major topologies, each having different advantages and disadvantages [Shumaker 02, Walker 03]. However these rely mainly on the features of the used technology as well as the application the PA should be designed for.

2.2.1 Single-Ended PAs

The most simple and therefore most often found topology is the Single-ended power amplifier. Figure 2.17 shows the block diagram of such an amplifier.

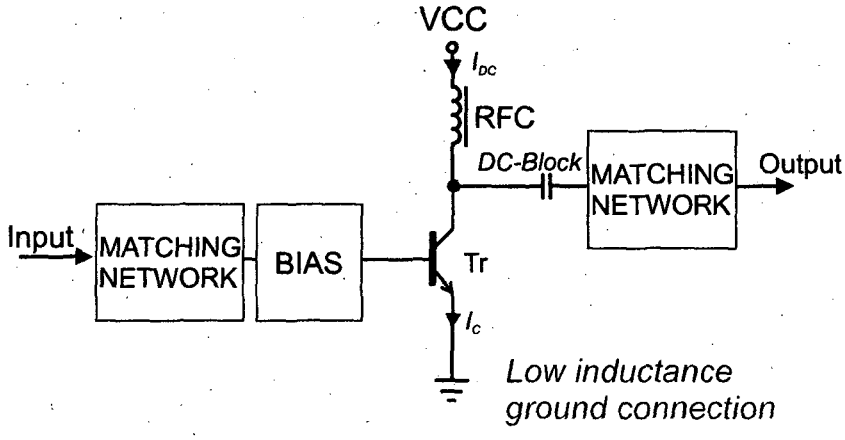


Figure 2.17: A single-ended 1-stage power amplifier block diagram.

This amplifier topology is specified by the emitter or source (FET) connection to ground, while the input is feeding the base or the gate. Another configuration uses the base or gate contact connected to ground. Both have the operation with unbalanced in- and output signals in common. This shows the first major problem in all single-ended designs: The ground connection. Considering DC voltages and currents, the ground connection is only a problem of conductivity. With the typical Al-metalization in Si-based semiconductor technologies and the connection with bond wires, the DC resistance is typically in the range of some mΩ up to 1-2 Ω. The real problem comes up considering RF signals: The longer the layout connection to ground, the higher the inductance of the connection will be. Additionally, bond wires behave like inductors with a high quality factor Q. In a typical RF chip package, the inductance from the outer connection pin to the emitter of the transistors is about 1-1.5 nH. Calculation formulas are presented in [March 91, Wadell 91]. For high frequencies, this problem becomes so dominant, that every amplifier gain will be reduced up to non-operation by the impedance of the emitter connection:

$$\lim_{\omega\to\infty} Z_{Connection}(j\omega) = \lim_{\omega\to\infty} j\omega L_{Connection} + R_{Connection} = \infty \tag{2.21}$$

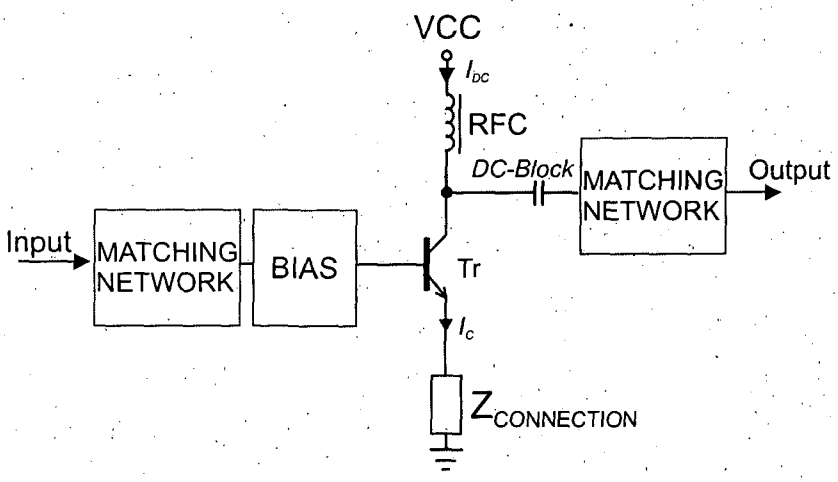


Figure 2.18: A single-ended 1-stage power amplifier with an emitter connection impedance.

It is easy to see, that the impedance $Z_{Connection}$ will lead to reduced currents through the transistor and thus to reduced output power and gain (emitter degeneration).

However, there exist several possibilities to weaken the problem:

- The use of several bond-wires in parallel. This reduces the inductance, but only up to a certain level, as bond wires close to each other have mutual inductance. Calculations on bond-wires and coupling between bond-wires could be found in [March 91].
- The chip could be housed using flip-chip packaging technologies [Nicolics 97]. Hereby the die is soldered directly onto a PCB or ceramic carrier. However, the problem of heat dissipation could become relevant, as different thermal expansion coefficients may lead to reliability problems.
- Some semiconductor technologies feature a kind of VIA connection through the chip towards a ground plane. This is typically called a Sinker, and is usually available in III-V technologies. There exist two derivates: First, the real metalized VIA and the VIA using a highly doped substrate contact on a high conductive substrate. The second option suffers from a limited conductivity and thus matching components such as coils have a reduced Q-factor. It is easier to realise in Si-based technologies.

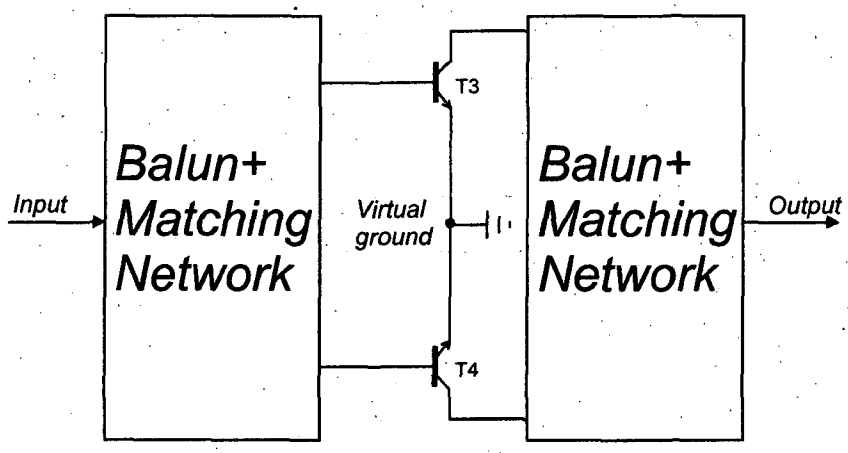


Figure 2.19: A push-pull type 1-stage PA block diagram.

The main advantage of single-ended designs is the easy in- and output matching [Gonzales 84]. Usually only a certain combination of an inductor and a capacitor is enough for a narrow-band matching network. The problems come up regarding the load impedance area and the bandwidth where transistors have to be matched. For example, single-ended GSM PAs need an output load impedance R_L of typically less than $1\,\Omega$. In dependence of the package, between output transistor and the load exists a series inductance, hence the load presented to the transistor is:

$$Z_{Tr} = Z_{L,Bondwire} + R_L = j\omega L_{Bondwire} + R_L \tag{2.22}$$

It is obvious, that even low inductances will lead to high losses in the inductor. Furthermore, if we consider, that the bondwire inductance shifts due to manufacturing inaccuracies, the matching will have deviations in a certain range. As transistors are never unilateral, this shows up the next problem: The input matching. RF BJTs have a low input impedance [5]. If such an output transistor is fed by a small driver, the matching requires high Q-factors, to have an efficient design. It should be mentioned that most switched-mode amplifiers are based on single-ended topologies. Although they allow the highest possible efficiencies, it is not possible to implement them for highest frequencies (above 20 GHz), due to the limited switching speed of the transistors.

2.2.2 Push-Pull PAs

Using two single-ended PAs supplied by an input signal shifted by 180° brings up the so-called push-pull power amplifier. Figure 2.19 shows the block diagram of this topology. The 180° phase shift is typically generated by a so called BALUN

[5] It depends on emitter area, output matching and operation point

(*BA*Lanced to *UN*balanced). There exist several methods of generating such signals, the LC-BALUN discussed in section 4.18 is one of them ($\pm 90^o$ phase shift). While push-pull amplifiers for audio frequency (AF) applications today consist of a matched pair of npn and pnp transistors (or their equivalent FET types), this is usually not possible for RF amplifiers, due to the fact that the pnp transistors are much slower and operate with lower current densities. Figure 2.20 shows an AF complementary output stage.

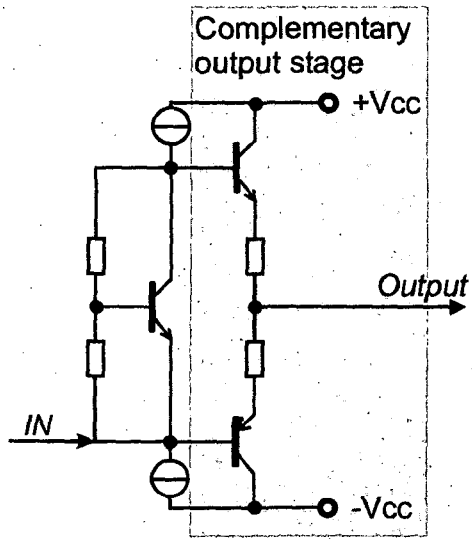


Figure 2.20: An audio frequency (AF) PA output stage. It uses two complementary transistors: The npn for the positive, the pnp for the negative input signals.

Push-pull or also called differential amplifiers have several advantages compared to the single-ended solutions:

- Easy realisation of class-B or class-AB amplifiers, due to the fact that the circuit can be dimensioned in that way that each transistor is conductive for a current conducting angle of 180^o.
- The circuit offers a virtual ground. Though, the ground connection is only required for the DC supply. For RF signals, the ground is exactly where both emitters connect to each other. Thus, the virtual ground of the input matching network can be used for the transistor biasing. No extra quarter wavelength transmission line or RF choke inductor is necessary.
- Transformer [Johnson 84] or Marchand [Marchand 44] based BALUNs have the feature that any DC potential can be applied without affecting the circuit at in- or output. Thus no DC blocks are required in this case.
- The load-line impedance for equal output power is four times higher than for single-ended designs. Thus losses in bond-wires are reduced. Further,

the necessary transistor areas are reduced as well, which improves linear design at higher efficiency and relaxes the need on high Q-factors for the interstage matching.

Of course push-pull PAs have one major disadvantage: They require a BALUN. The design of a low-loss, well-matched BALUN is not a simple task. Especially at the output side, a BALUN requires several efforts in one:

- The impedance of each input port of the differential input must be equal.
- The phase between the two ports of the differential input must be as near to 180^o as possible.
- For high efficiencies it is also advantageous to match the second and third harmonic loads to the transistors [El-Hamamsy 94]. Especially for the second harmonic frequency a low impedance and for the third harmonic frequency a high-valued impedance is desired. Typically this task is best met by Marchand-BALUN [Marchand 44, Mongia 99] derivates.
- The BALUN losses should be as low as possible. For BALUNs constructed with lumped elements this requires high Q-factors.

Today, there exist a lot of very efficient BALUN proposals [Bakalski 02,a, Ilkov 03,b, Johnson 84, Mongia 99], fitting to a lot of applications. However their design suffer from higher complexity than that of single-ended matching networks.

2.2.3 Balanced PAs

The balanced PAs differ basically in their 90^o phase shift between its parallel driven stages. It is important to mention, that usually the definition of "balanced" in RF circuits implies 180^o of phase shift. Unlike to RF circuits for power amplifiers the nomenclature "Balanced Power Amplifier" exists for 90^o phase shift between the stages [Shumaker 02]. For RF PAs, power combining is a very common method to increase output power, especially when a single stage won't fit the necessary specifications. Therefore not only Wilkinson power dividers [Wilkinson 60, Howe 74, Magerl 98] are used, also branch couplers like the Lange coupler [Lange 69] are in common for power combining. Especially for very high frequencies (>50 GHz), the combining with a 90^o coupler makes sense, as the wavelength is very short, and can be integrated on-chip [Chang 03]. Furthermore such couplers typically offer a good input matching, as a $50\,\Omega$ load is used. This is necessary especially for very high frequencies, as the input matching needs to be as good as possible, as gain is low and matching with external components is very lossy and difficult. The use of a $50\,\Omega$ load implies a big disadvantage as well: This resistor is an additional part, and it will require die-size or an area on the

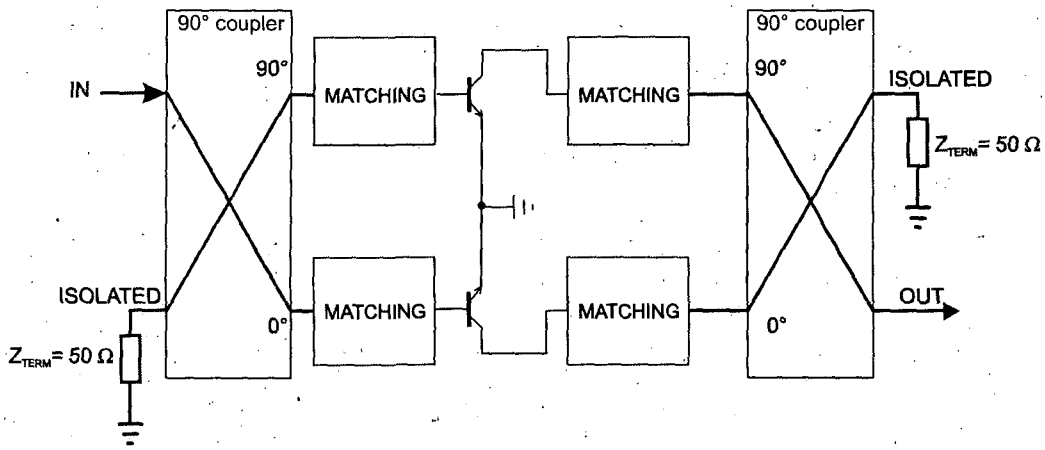


Figure 2.21: A balanced 1-stage power amplifier block diagram.

PCB. Further such loads have a certain power dissipation, worsening the thermal problems in the PA. The most important disadvantage from balanced PAs to push-pull typed amplifiers is the missing virtual ground. This causes similar problems with ground connections as known in single-ended designs. This implies that the resulting load impedances are two times lower than in push-pull designs, as it is in fact a single-ended design using a power divider. Furthermore, a class-B or class-AB operation is very difficult, as now both transistors are not used complementary anymore. Both, balanced and push-pull configuration, have the advantage, that intermodulation products are cancelled: For balanced the third order products, for push-pull the even products.

2.3 Power amplifier classes

PAs are categorized into classes dependent on the waveform of the voltages and currents observed at the transistors. The first major group are the class-A, B and AB. They are often described as the linear PA classes. The classes C, D, E, F, G, H and S are the so-called nonlinear amplifier classes. While a class-C PA uses the same topology as a class-A PA but with different biasing, the other classes have all in common that they use the transistor as a on/off switch. Most of them are based on proposals by Raab [Raab 75, Raab 78,b, Raab 78,a, Raab 77] and Sokal [Sokal 75, Sokal 77].

2.3.1 Class-A power amplifier

The most simple class is the class-A PA as it is quite similar to its small-signal amplifier counterpart. In this configuration the bias und thus the operating point is chosen in that way, as there is always a current flowing through the transistor. The transistor should therefore work in its linear area without any distortions. Typically it is realised in a single-ended configuration as discussed before. A typical schematic can be seen in fig. 2.22.

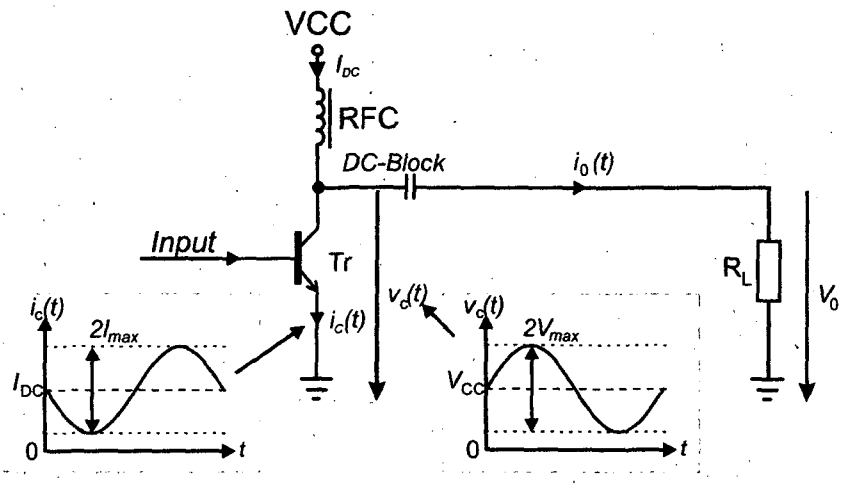


Figure 2.22: A class-A single-ended PA. The collector current i_c and the RF output voltage V_c are plotted with their ideal waveforms.

Neglecting the matching circuitry and its parasitics, the bias is assumed to be chosen that the operating point is in the mid of the linear region. With $I_{C,quiet}$ describing the bias current, the collector current can be written as:

$$i_c(t) = I_{C,quiet} - I_{MAX}\cos(\omega t) \tag{2.23}$$

with I_{MAX} being the peak value of the collector current. While $I_{C,quiet}$ flows via the RF choke coil RFC, the non-DC part passes the DC-Block capacitor causing an output voltage at the load impedance attached to the output:

$$v_0(t) = R_L \cdot I_{MAX} \cos(\omega t) = V_{MAX} \cos(\omega t) \tag{2.24}$$

Analogous to AF amplifiers using transformers, the peak output signal can reach up to V_{CC} instead of $\frac{V_{CC}}{2}$ peak output voltages. This is due to energy stored in the RF choke coil (fig. 2.23) :

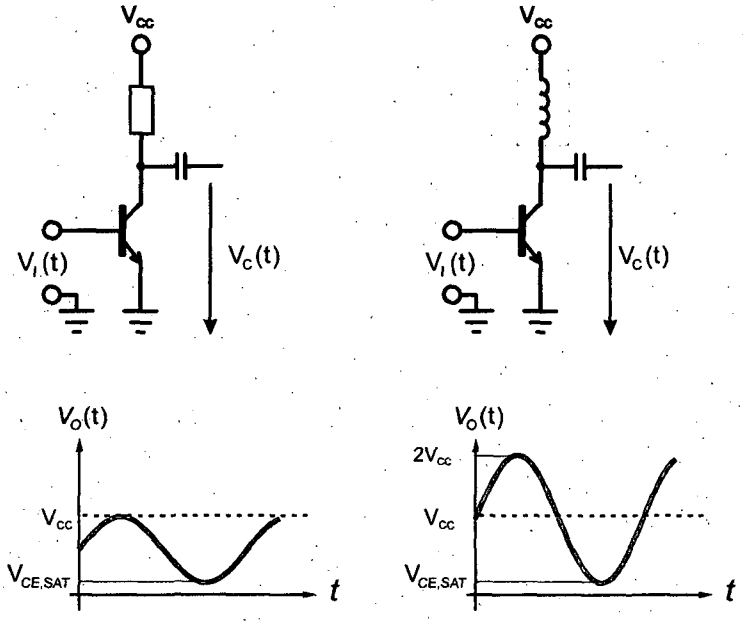


Figure 2.23: Improvement of the maximum output voltage with the use of an inductor instead of a resistor.

The maximum output power can therefore be as high as

$$P_L(t) = \frac{V_{MAX}^2}{2R_L} \leq \frac{V_{CC}^2}{2R_L} \tag{2.25}$$

using the factor $\frac{1}{\sqrt{2}}$ for the RMS voltage of a sinusoidal signal.

Considering the maximum efficiency of a class-A amplifier, additionally the power consumption has to be calculated:

$$P_{Supply} = V_{CC} \cdot I_{C,quiet} = \frac{V_{CC}^2}{R_L} \tag{2.26}$$

under the assumption, that the PA is biased to have the average output voltage V_{CC}.

The maximum overall efficiency is

$$\eta = \frac{P_L}{P_S} = \frac{V_{max}^2}{2V_{CC}^2} \leq 0.5 \tag{2.27}$$

It is important to mention that the heat dissipation has to be considered, as class-A amplifier suffer from high quiescent currents beside the low theoretic efficiency maximum. This is an important point for PA designs with high peak to average power ratios (crest factors).

2.3.2 Class-B and AB power amplifier

While the transistor in a class-A PA is always conducting, this is totally different for the other linear classes as well as for class-C. Hereby the conduction angle decides in which PA class the circuit is operated:

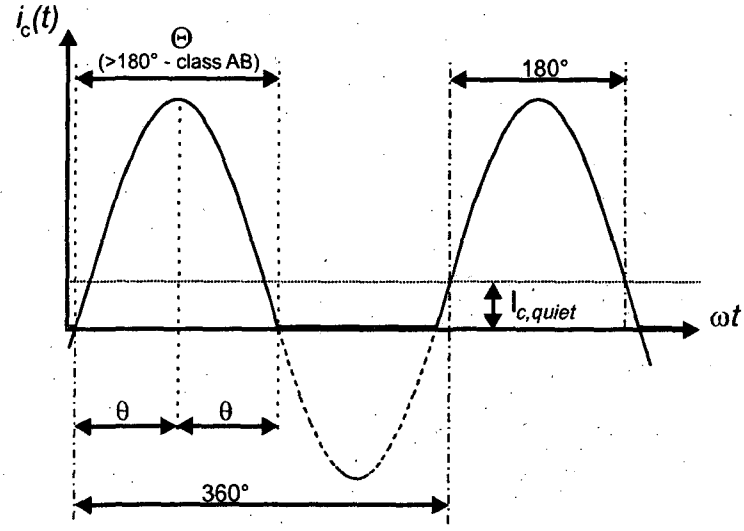


Figure 2.24: The conducting angle for a class AB amplifier

The conduction angle Θ is the fraction of a full cycle where the transistor is operated to be conductive. Thus fig. 2.24 shows that a sinusoidal signal is cut off for negative currents, and thus the amplifier transistor must have a conduction angle Θ of less then 360^o, the conduction angle for class-A amplifiers. If Θ is between 360^o and 180^o we have a class AB amplifier. For $\Theta = 180\ ^o$ it is a class-B design. Less than 180^o of conducting angle is a class-nC amplifier. For calculations on efficiency and power there is also the half conduction angle θ in common (fig. 2.24). It is used for calculations of output power an efficiencies.

The conducting angle also implies the information on the achievable output power and maximum efficiency. Expressing the collector current for $i_c(t) > 0$ with

$$i_c(t) = I_{MAX}\cos(\omega t) - I_{c,quiet} \tag{2.28}$$

with the quiescent current $I_{c,quiet} = I_{MAX} \cdot \cos\theta$ with $-\theta < \omega t < \theta$ and $\Theta = 2\theta$ gives:

$$i_c(t) = I_{MAX}(\cos(\omega t) - \cos\theta) \tag{2.29}$$

The calculation of the efficiency requires the knowledge of the DC component and the fundamental frequency component which both are determined by a Fourier series. Hence, the DC component is

$$I_{DC} = \frac{1}{2\pi}\int_{-\theta}^{\theta}[I_{MAX}(\cos\omega t - \cos\theta)]\,d\omega t = \frac{1}{\pi}\int_{0}^{\theta}[I_{MAX}(\cos\omega t - \cos\theta)]\,d\omega t =$$

$$= \frac{I_{MAX}}{\pi}[\sin\theta - \theta\cos\theta] \tag{2.30}$$

Using eqn. 2.30, the DC-power provided from the power supply is :

$$P_{DC} = V_{CC} \cdot I_{DC} = \frac{V_{CC}I_{MAX}}{\pi}(\sin\theta - \theta\cos\theta) \tag{2.31}$$

The fundamental frequency current is given by

$$i_1 = \frac{4}{2\pi}\int_{0}^{\theta}[I_{MAX}(\cos\omega t - I_{c,quiet})\cos\omega t]\,d\omega t = \frac{I_{MAX}}{2\pi}(2\theta - \sin 2\theta) \tag{2.32}$$

Hence we get the maximum output power for the fundamental frequency by

$$P_{OUT,max} = \frac{i_1^2 \cdot R_L}{2} = \frac{u_{peak}}{\sqrt{2}}\cdot\frac{i_{peak}}{\sqrt{2}} = \frac{V_{CC}}{\sqrt{2}}\cdot\frac{i_{peak}}{\sqrt{2}} = \frac{V_{CC} \cdot I_{MAX}}{4\pi}(2\theta - \sin 2\theta) \tag{2.33}$$

Thus, the theoretical maximum efficiency is determined by

$$\eta_{max} = \frac{P_{OUT,max}}{P_{DC}} = \frac{2\theta - \sin 2\theta}{4(\sin\theta - \theta\cos\theta)} \tag{2.34}$$

Figure 2.25 shows the maximum efficiency vs. the conduction angle. It can be determined that the maximum efficiency for class AB PAs is between 50 % and 78.5 % (class-B). Hence the class A PA with a conduction angle of 360° is limited in its efficiency by 50 % (eqn. 2.27). This represents a rather theoretical curve, as it implies an optimum loaded amplifier which has got its peak output voltage up to the supply voltage V_{CC}. Further the saturation voltage is simplified to 0 V. If the output peak voltage is limited to $V_{out,peak}$, eqn. 2.33 can be written as

$$P_{OUT} = \frac{V_{out,peak} \cdot I_{MAX}}{4\pi}(2\theta - \sin 2\theta) \tag{2.35}$$

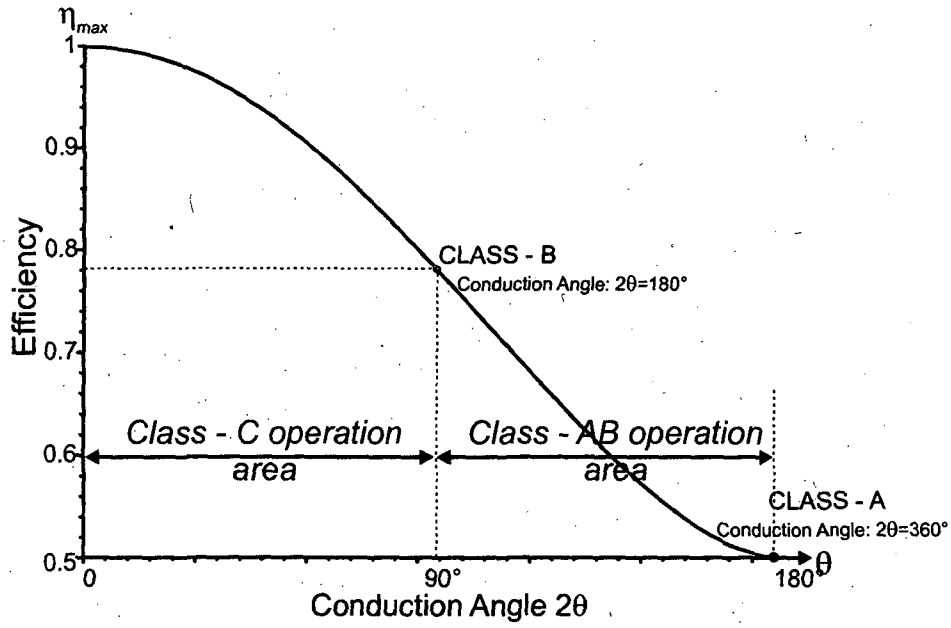


Figure 2.25: The maximum efficiency vs. the conduction angle.

2.3.3 Class-C power amplifier

Class-C type PAs are rarely found today. Even as they offer higher efficiencies than class-B, they suffer from high distortions and thus high nonlinearities. The conduction angle Θ for a class-C type PA is lower than 180^o, being the reason for the nonlinear behavior. Figure 2.25 demonstrates that the efficiency rises up to 100 %, but this implies extremely low conduction angles which must result in reduced output power levels. The degradation of output power with the reduction of the conduction angle can be found in [Rodgers 03] (fig. 2.26).

$$P_{0,max,norm} = \frac{P_{0,max}}{P_{0,norm}} = \frac{1}{\pi}\frac{(2\theta - \sin 2\theta)}{1 - \cos\theta} \tag{2.36}$$

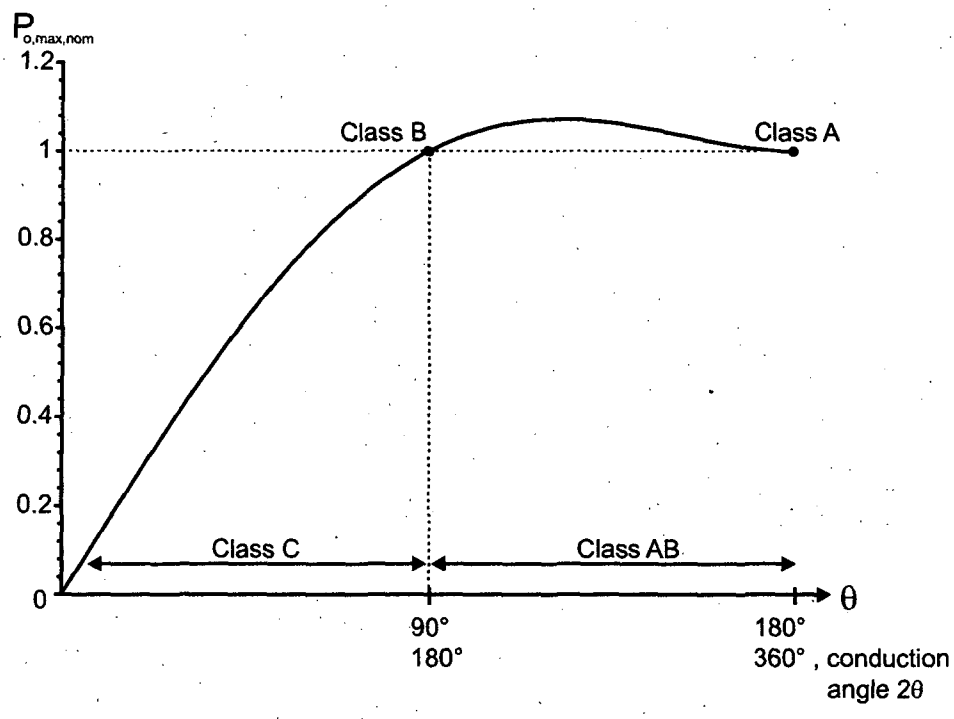


Figure 2.26: The maximum normalized output power vs. the conduction angle.

2.3.4 Class-D power amplifier

The class-D power amplifiers are switched-mode PAs. All these amplifiers see the transistor as a controlled switch (fig. 2.27). An ideal switch would behave as an ideal conductor for the 'on'-resistance and having an infinite resistance for the 'off'-resistance. Assuming that there is no loss, the output signal will be the power supply switched on and off, just depending on the rate of the input carrier signal. For this assumption the efficiency will be 100 %, as no losses due to finite switching time and internal parasitic resistances can occur.

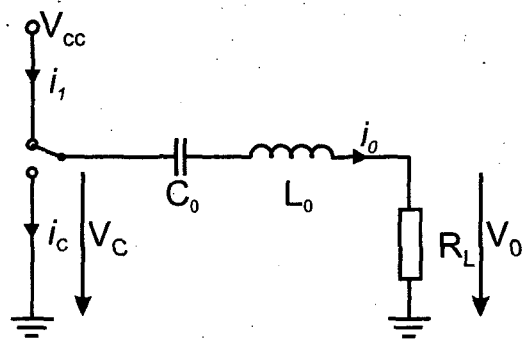


Figure 2.27: Transistor used as a switch in a PA configuration.

Class-D amplifiers typically base on a push-pull topology. Out of this there exist three types of class-D stages:

1. The complementary voltage switch PA

   Figure 2.28 shows a simplified schematic of a class-D complementary voltage switch PA stage. This design uses a transformer to drive the transistors T1 and T2 with a phase difference of 180°. This concept known is a classic push-pull type configuration where T1 is turned on if T2 is turned off and vice versa. As a result, the capacitor is switched between the supply voltage V_{CC} and ground. The voltage found between emitter and collector of T2 has therefore a square waveform (fig. 2.28) with a 50 % duty cycle.

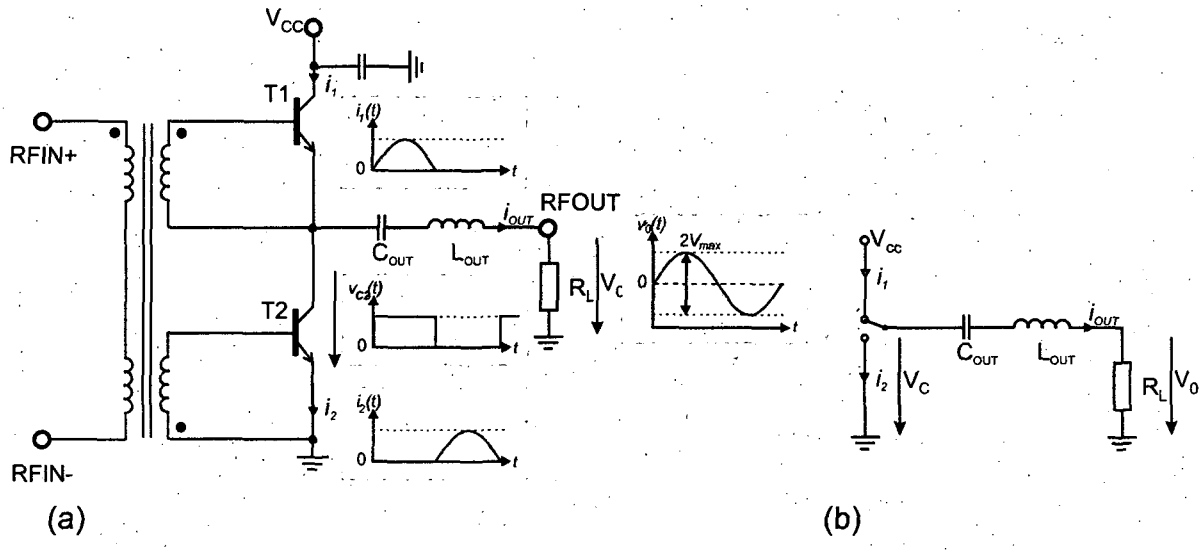


Figure 2.28: a) Complementary voltage switch class-D PA (b) equivalent circuit

The emitter-collector voltage as sketched in (fig. 2.28) is:

$$V_{C2} = V_{CC}[\frac{1}{2} + \frac{1}{2}\,\mathrm{sgn}(\omega t)] \tag{2.37}$$

with $\mathrm{sgn}(\omega t)$ as the signum function:

$$\mathrm{sgn}(\omega t) = \left\{ \begin{array}{rcl} +1 & , & \sin(\omega t) > 0 \\ 0 & , & \sin(\omega t) = 0 \\ -1 & , & \sin(\omega t) < 0 \end{array} \right\} \tag{2.38}$$

Applying the Fourier analysis on the squarewave voltage gives:

$$\mathrm{sgn}(\omega t) = \frac{4}{\pi}\left\{\sin(\omega t) + \frac{1}{3}\sin(3\omega t) + \frac{1}{5}\sin(5\omega t) + \cdots\right\} \tag{2.39}$$

and hence

$$V_{C2}(\omega t) = V_{CC}\left\{\frac{1}{2} + \frac{2}{\pi}\sin(\omega t) + \frac{2}{3\pi}\sin(3\omega t) + \frac{2}{5\pi}\sin(5\omega t) + \cdots\right\} \quad (2.40)$$

If the output network consisting of C_{OUT} and L_{OUT} is tuned to the fundamental frequency of the squarewave signal, we should see a sinusoidal current and voltage on the load Z_L as sketched in fig. 2.28:

$$i_{out}(\omega t) = \frac{2V_{CC}\sin(\omega t)}{\pi R_L} \quad (2.41)$$

with the peak value

$$i_{out,peak} = \frac{2V_{CC}}{\pi R_L} \quad (2.42)$$

for the output current and

$$V_{MAX} = \frac{2V_{CC}}{\pi} \quad (2.43)$$

for the output voltage. Hence, the output power is calculated by

$$P_{out} = \frac{2V_{MAX}^2}{2R_L} = \frac{2V_{CC}^2}{\pi^2 \cdot R_L} \quad (2.44)$$

For the efficiency calculation, the DC consumption has to be calculated. The DC peak current is the same as in eqn. 2.41 due to the whole current flowing through T1 (or T2 half a cycle later). This implies that the power gathered from the power supply equals the RF power. Thus the theoretically efficiency is 1 (100 %). However the efficiency will be reduced by finite switching speed and the non-ideal switching behavior (finite conductivity, and remaining resistance when switched off).

2. The transformer coupled voltage switching PA

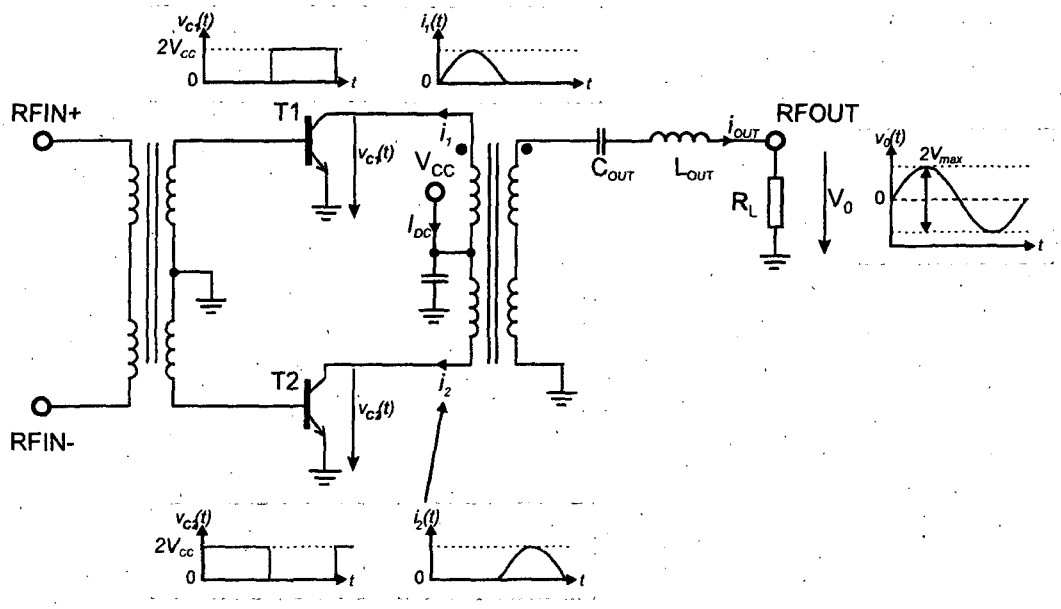


Figure 2.29: Transformer coupled voltage switch class-D PA

The transformer coupled voltage switching amplifier has the same topology as a push-pull type amplifier. It is different to the complementary voltage switch PA as it needs a second transformer as a BALUN. Though it does not need the input transformer to feature inversely arranged windings. Its efficiency is theoretical 100 %, the same as in the complementary voltage switch PA.

3. The transformer coupled current switching PA

   Referring the schematics 2.29 and 2.30, both amplifier types differ only in their power supply feeding, which is now done by a RF choke, and their output filter. The RF choke is hereby used to force the circuit to gather constant current from the power supply, which is switched by the transistors. In this configuration, the collector currents and voltages change, but the efficiency remains at the theoretical 100 %. Using the amplifier as a current switch improves device speed behavior, as BJTs for example can be tuned to operate in their optimum working point and furthermore, the problem of avalanche breakdown due to high voltage switching is reduced.

Further topics on class D amplifiers can be found in [Albulet 01, El-Hamamsy 94].

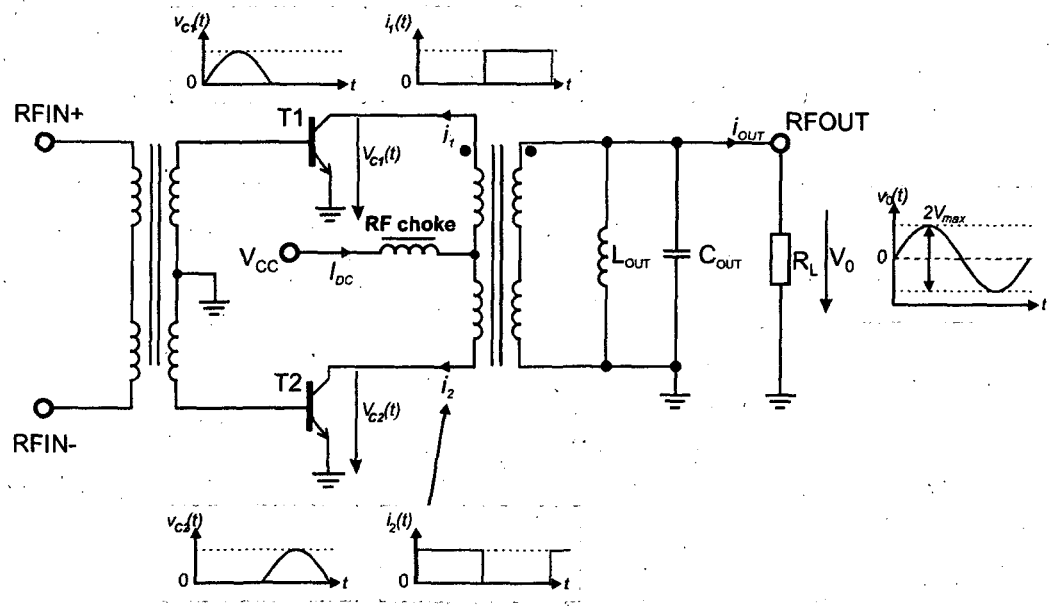


Figure 2.30: Transformer coupled current switch class-D PA

2.3.5 Class-E power amplifier

Class E power amplifiers are single-ended switch-mode configurations. Like in class D, the transistor is seen as an ideal switch. Figure 2.31 shows a simplified schematic and the equivalent circuit with a switch as an ideal transistor substitute.

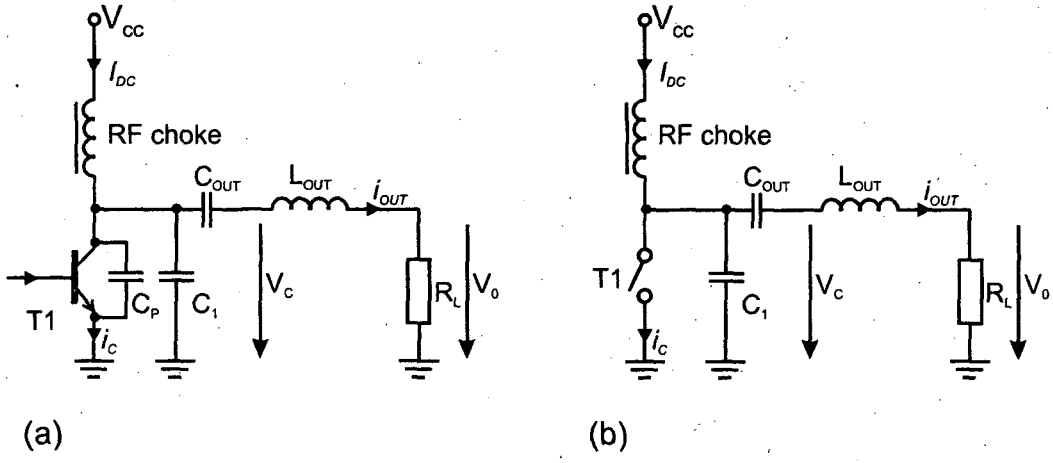


Figure 2.31: (a) Class E PA configuration (b) equivalent circuit

In this schematic C_P represents the transistors parasitic capacitance and thus a part of the passive load network sketched by C_1, C_{OUT} and L_{OUT}. Class E

amplifiers have the theoretic maximum efficiency of 100 %, but however rely on the same limitations as their class-D counterparts: Limited switching time, limitations in the Q-factor for the passive components (especially in lossy Si-substrates a big problem), and their saturation voltages.

2.3.6 Class-F power amplifier

The class F power amplifiers are usually single-ended configurations but use a load network consisting of harmonic resonator circuits. Figure 2.32 shows an example for such a configuration. The voltage waveform consists of one or more odd harmonics to approximate a squarewave signal, while the current includes even harmonics to approximate a half sine wave signal. In inverse class F called designs this is vice versa. A class-F design equals class A for the number of harmonics set as 1. For ∞ harmonics the efficiency converges to 100 % [Raab 03]. To get required harmonics the output is loaded with several C_2/L_2 tanks and the transistor operated in saturated mode similar to class-C. It is important to mention, that class-F designs require the most complex output filters, whose component values must be correct for specific frequency points.

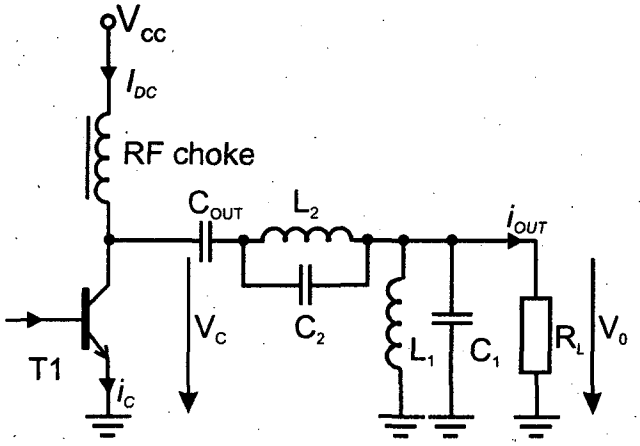


Figure 2.32: The Class F PA configuration.

2.3.7 Class-G/H/S power amplifier

Class G and H amplifiers are further PA classes improving the class B efficiency especially with a focus on low input power signals. Today they can be found only in audio amplifiers and require several supply voltages and active devices. Figure 2.33 shows a class G audio power amplifier output stage for two supply voltages.

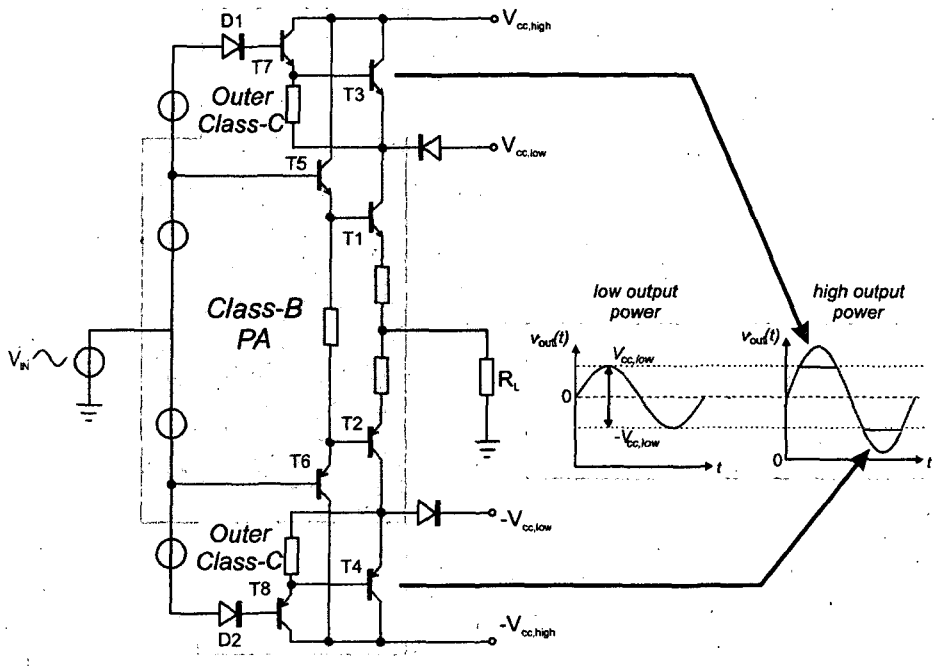


Figure 2.33: A Class G audio amplifier output stage.

The main idea in class G is to overcome the poor efficiency on low output power levels by designing an efficient class B or AB amplifier for small output power levels, so that the efficiency is high for the average power level. For the high output power levels an additional stage is stacked, operating in class-C mode. Hereby the low power amplifier transistors are cut off at their supply voltage and the stacked class-C transistor stage adds the necessary cut signals (fig. 2.33).

As a result, a class G amplifier has a higher average efficiency than a usual class B or AB amplifier. Furthermore the heat dissipation is also spread over two transistors. These designs are found mainly in audio applications due to the wide bandwidth necessary for the active components and the much slower pnp transistors.

Class H is an extension to class G and modulates the higher power supply by the input or output signal (fig. 2.34). By this, the optimum supply voltage is tracked with the input signal to achieve better average efficiencies than in class G. Examples for class H PA could be found in [Higashiyama 95, Gottlieb 87] and a commercial example is the TDA 8574 line driver IC [Philips 98]. Another PA class is the class S. It includes all PA operating with pulse width modulation. Hereby the signal is brought to a rectangular waveform with variable duty-cycles in dependence of the input signal. Figure 2.35 sketches the possible waveform resulting of half a sinusoidal input signal. With such a configuration, an amplifier stage can be operated very efficient, but requires additional filtering, hence a low-pass at the output. The major disadvantage of such configurations is, that

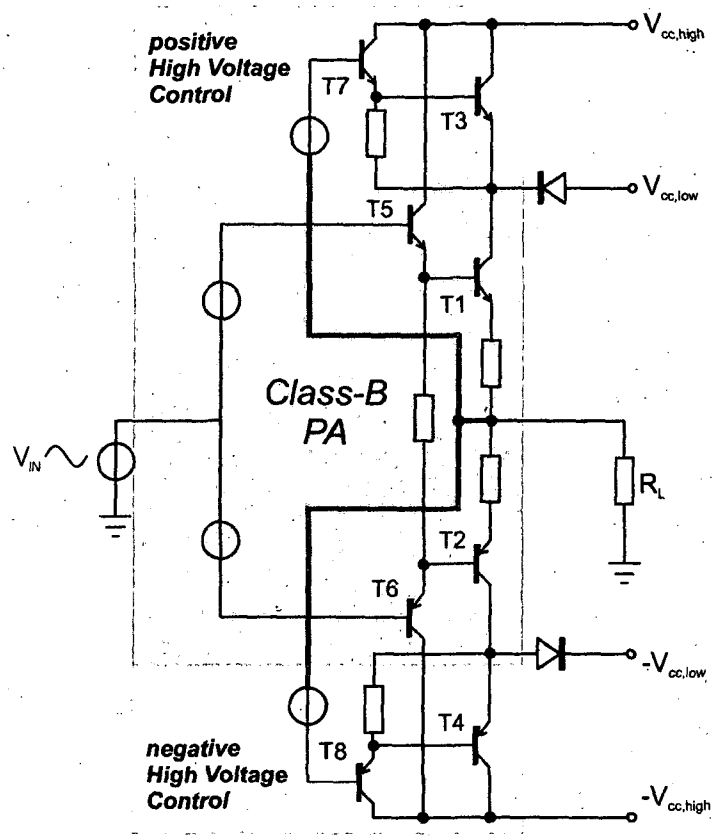


Figure 2.34: A Class H audio amplifier output stage.

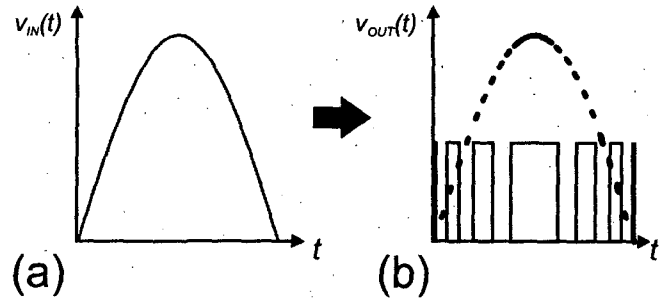


Figure 2.35: Pulse Width Modulation: Creation of a PWM waveform (b) out of an input sigal (a).

the transistors have to be much faster than in any before presented class as it must switch with a much higher switching frequency than the operating frequency to generate the accurate waveform with rectangular pulses and a low pass filter (comparable with 1-bit DACs using oversampling). This limits its RF ability, as the transistor speed is limited for every technology.

Chapter 3

SiGe bipolar transistors

3.1 Introduction

Today there exist several semiconductor technologies with the most different advantages and problems as well. A major group used for PA designs are the so called III-V-technologies. They include all InP, GaAs, and GaN technologies. III and V stand for the group in the chemical periodic system, respectively. As mentioned in the introduction, these technologies basically provide the best performance for PAs, wide band amplifiers and fast digital circuits, but suffer from high cost. The reason for the higher cost is originated in the smaller wafer sizes for III-V-technologies and the higher material cost implying higher wafer cost as well. The higher performance of III/V-technologies is based on the higher maximum carrier velocity, being up to 3 times higher than for Si.

The next major group are the silicon (Si) based semiconductor technologies. There exist the Si Bipolar Junction Transistor (BJT) and the SiGe Heterojunction Bipolar Transistor (HBT). Furthermore also Complementary Metal Oxide (CMOS) processes exits featuring complementary n- and p-FET transistors. Theoretically CMOS power amplifiers are feasible but suffer from reliability problems due to very low maximum supply voltage and hot carrier effects. Today no commercial CMOS-PAs are available. Further, there exist also mixed technologies called BiCMOS processes. These combine the excellent high integration possibilities with the better RF performance of bipolar transistors. The next sections will give a brief discussion on the construction and the modeling of Si-BJTs and SiGe-HBTs used for the PAs in this thesis. A very good source on physics and modeling of bipolar transistors is found in [Reisch 03] and [Schrenk 78].

3.2 Self-aligned Silicon Bipolar Junction Transistors (BJT) and Silicon Germanium Heterojunction Bipolar Transistors (HBT)

The PA designs described in this thesis use SiGe bipolar HBTs. As this transistor type is mainly based on its Si bipolar BJT predecessor, this should give an introduction how such transistors are constructed and how the SiGe HBT differs from the Si BJT. In the past decades a lot of literature has been published describing the functional principles of bipolar transistors. The first publications originate from [Shockley 50], but more modern presentations can be found in [Ashburn 88] and other literature.

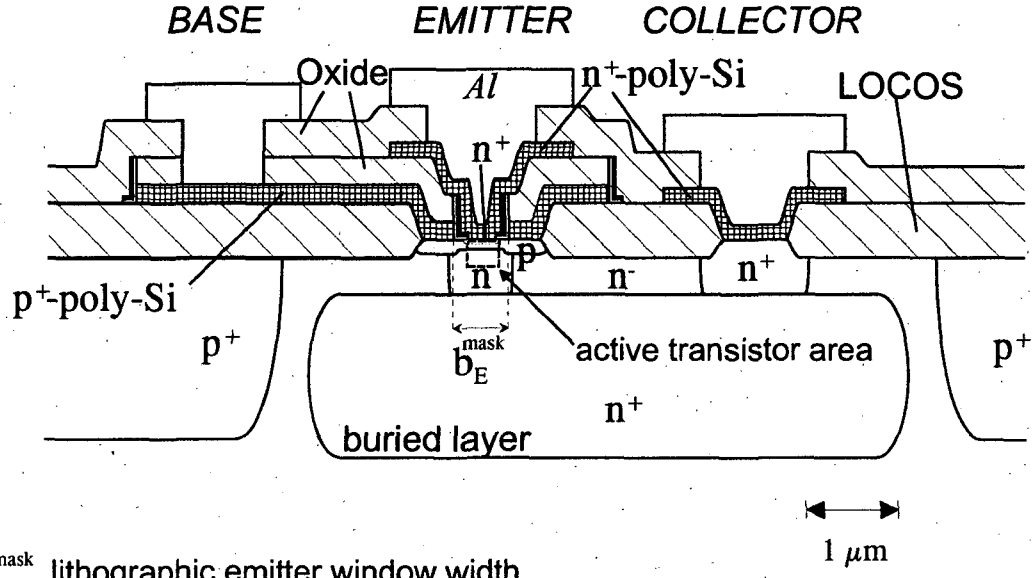


Figure 3.1: Schematic cross-section of an integrated npn Si bipolar transistor using polysilicon contacts and a self-aligned emitter-base-complex. The active transistor lies within the dashed region. The other area is used for contacting to the metalization and for the isolation from other components [Aufinger 01].

A schematic cross-section of an integrated npn BJT for RF applications is shown in fig. 3.1. The dashed lines outline the active area of the transistor with its three crystal regions, consisting of two n-doped domains for the emitter and the collector and the p-doped domain for the base. The connection to the outer metalized emitter contact is done using a highly n-doped polysilicon while the base is connected using highly p-doped polysilicon. The high doping is necessary to keep the contact resistances as low as possible. To isolate the polysilicon layers from each other a thin oxide-nitride double-layer is used. This so-called spacer is manufactured using anisotropic plasma etching and allows the construction of

structures below the lithographic limits [Nakashiba 80, Ning 81]. This is known as the principle of self-alignment. The minimum mask width of the used lithography of the transistor in fig. 3.2 is $b_E^{mask} = 0.6\mu m$. The width of the spacer is typically $\sim$ 0.1-0.2μm, so that the effective emitter width is typically $b_{eff} = 0.3\mu m$. The relatively low n-doped collector is connected to the right side in fig. 3.1 via a layer with a good conductivity called the buried layer. Figure 3.2 shows a REM micrograph of the transistor.

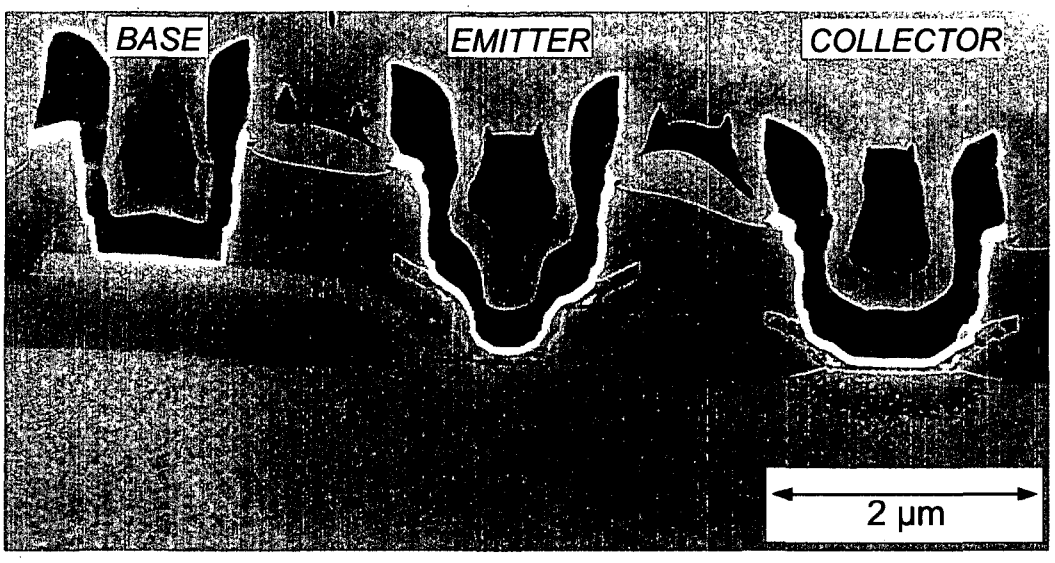


Figure 3.2: Cross-section of an integrated bipolar transistor (REM photograph) [Klose 93].

The transistor characteristics depend on the concentration of the doping materials, hence the doping profile. A typical doping profile from emitter to collector of the active transistor area in fig. 3.1, is shown in fig. 3.3 [Klose 93]. Donator materials are typically Arsenide (As) or Phosphor (P) for the emitter and collector and as acceptor material for the base usually Boron (B) is used.

Important for the further development of Si bipolar technologies for high-speed applications is the lateral and vertical down-scaling: In the first sight, the lateral down-scaling increases the packing integration density, but - more important - it reduces the transistor parasitics, as parasitic capacitances and resistances are decreasing. Thus, higher transistor switching speeds can be obtained, as the charging and discharging times are reduced by the lower resistances and capacitances of the transistor. The vertical down-scaling yields to very small base layers helping to reduce the transit time in the transistor. All this requires improvements in the process technology, as presented for example in [Ruge 84]. [Böck 96,a, Böck 96,b] show that using lateral and vertical down-scaling the transit frequency f_T (described a section 3.4) can be doubled. Further improvements are obtained by

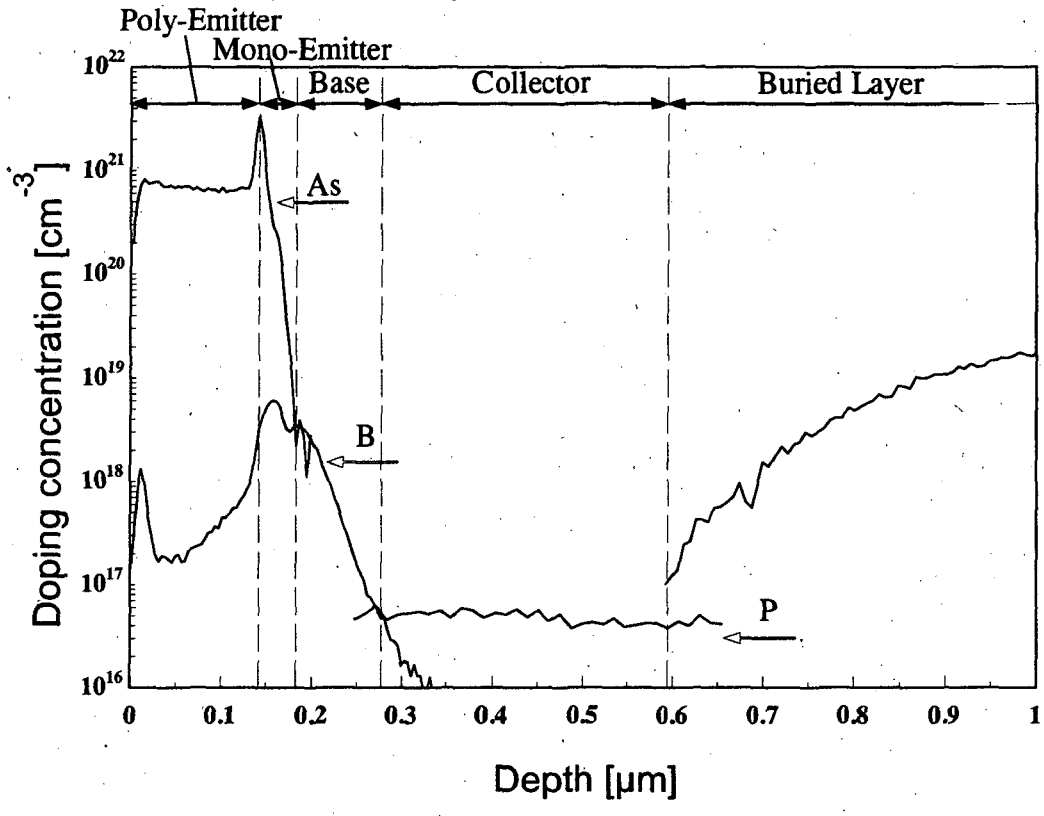


Figure 3.3: Typical doping profile for a transistor corresponding fig. 3.2 [Klose 93]

selective epitaxial growth (SEG) [Meister 95]. The SEG of doping materials has several advantages compared to implanted and diffused bases [Aufinger 01]:

- The form of the doping profile has much less limitations than in processes using implantation and diffusion.
- The epitaxial growth allows including of Germanium (Ge) into the base. Thus a heterostructure is feasible keeping all advantages of standard Si-bipolar technologies.
- The doping profile is steeper. The base can be realised much thinner without increasing base resistance. For the same lateral size, the stored electron charge in the base is reduced implying a shorter switching time.
- Due to the steeper doping profile, which controls several important transistor parameters, the base charge $Q_B = \int_{base} p(\vec{x})dv$ are better adjustable (p represents the hole density).
- Selective growth enables a quasi-self alignment of base and collector [Meister 92], reducing the base collector capacitance C_{BC}.

- Selective epitaxy allows the usage of improved isolation techniques compared to local oxidation of silicon (LOCOS) [Endo 84].

The cross-section of an integrated SiGe HBT is found in fig. 3.4. The main difference is the isolation of the base-collector complex. The basic structure of fig. 3.1 remains the same, an important advantage, as available production technologies can be used. Figure 3.5 and 3.6 show corresponding REM photographs for Infineon's production process B7HF [Klein 99, Wolf 01].

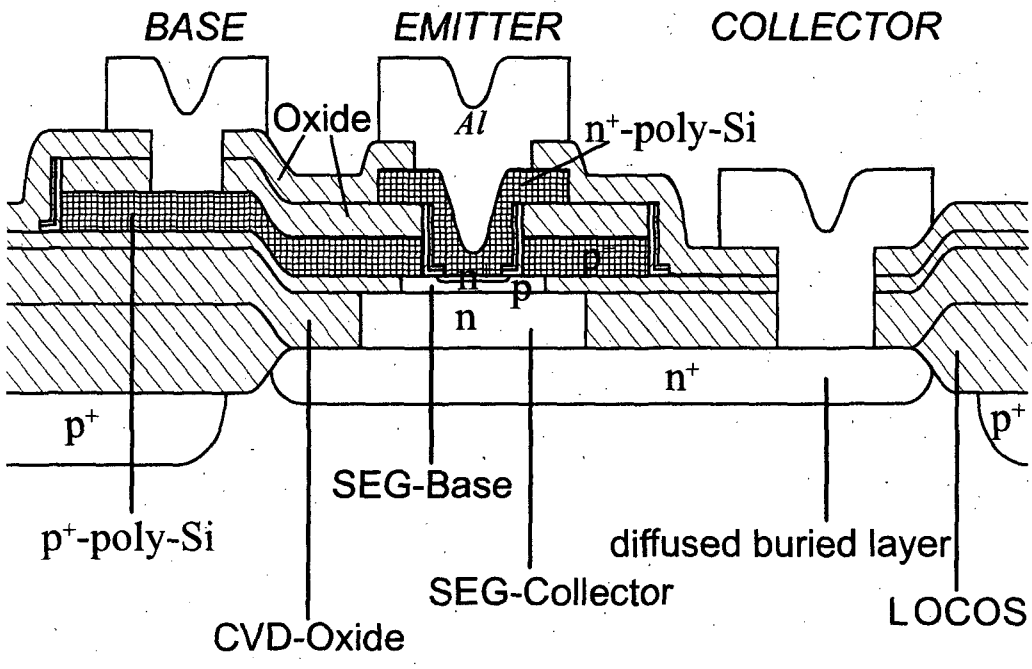


Figure 3.4: Schematic cross-section of an integrated $Si/Si_{1-y}Ge_y$ heterojunction bipolar transistor (HBT) in comparison to fig. 3.1.

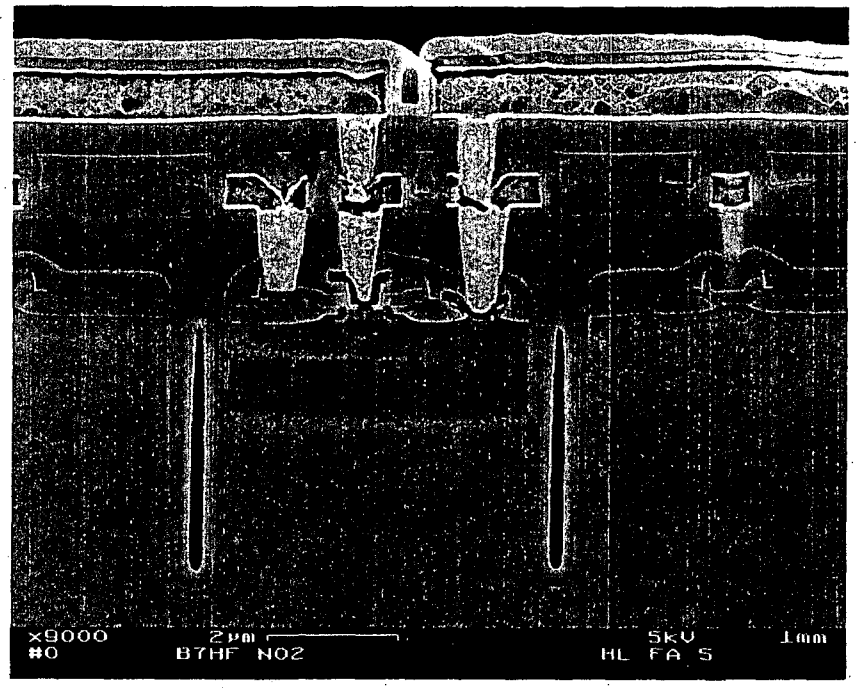


Figure 3.5: Cross-section of an integrated bipolar transistor of Infineon's SiGe production technology B7HF [Klein 99, Wolf 01].

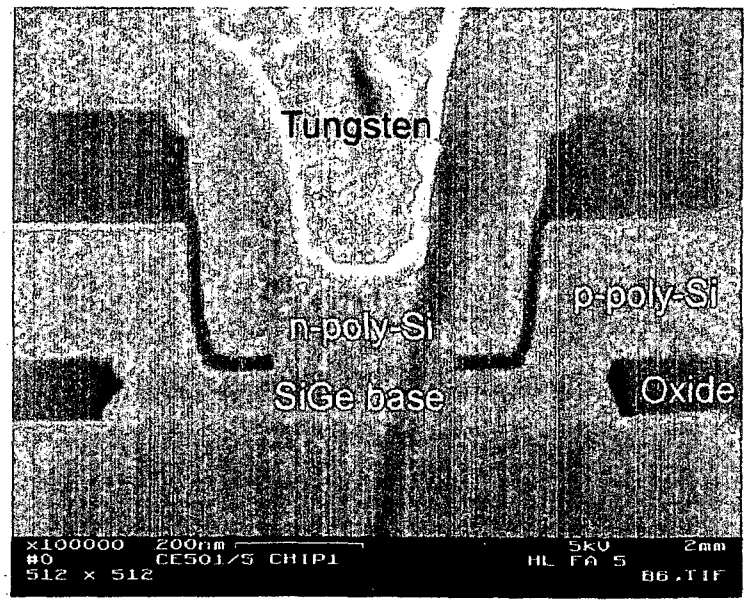


Figure 3.6: Enlargement of the emitter-base complex of the transistor cross-section in fig. 3.5.

3.3 Compact transistor models

Compact transistor models are a more or less complex set of equations used to describe the electrical behavior of a transistor. Simulation programs like SPICE[1], SPECTRE[2] and ADS[3] use these equations for their network calculations. The first compact model for bipolar transistors originates from the early 1950s by Ebers and Moll [Ebers 54]. By solving a one-dimensional static transport equation for electrons in the neutral base of a npn bipolar transistor and neglection of recombination the collector current I_C and the base current I_B are given by a function of the base emitter voltage U_{BE} and the base collector voltage U_{BC}:

$$I_C = I_S \left\{ \left[e^{U_{BE}/U_T} - 1 \right] - \left(1 + \frac{1}{\beta_R} \right) \left[e^{U_{BC}/U_T} - 1 \right] \right\}, \tag{3.1a}$$

$$I_B = I_S \left\{ \frac{1}{\beta} \left[e^{U_{BE}/U_T} - 1 \right] + \frac{1}{\beta_R} \left[e^{U_{BC}/U_T} - 1 \right] \right\}. \tag{3.1b}$$

I_S represents the saturation current, β the current gain, and β_R the reverse current gain. For base widths smaller than the diffusion length of the electrons in the base given by $I_S = -qA\frac{D_n n_i^2}{N_{AB} w_B}$, $\beta = \frac{D_n N_{DE} w_E}{D_p N_{AB} w_B}$ and $\beta_R = \frac{D_n N_{DC} w_C}{D_p N_{AB} w_B}$. Here N_{AB} is the base acceptor concentration, N_{DE} the emitter donator concentration, N_{DC} the collector donator concentration, $U_T = k_B T/q$ the thermal voltage, D_n and D_p the diffusion constants for electrons and holes, A the cross-sectional area, n_i the intrinsic charge concentration, w_B the base width, w_e the emitter width and w_c the collector width.

Most newer bipolar compact models base on the model of Gummel and Poon [Gummel 70]. It is found in a modified version in software products as SPICE GUMMEL POON (SGP)-Model in practically all modern circuit simulators. The Gummel Poon model is not limited to low injection, it allows the throughout description up to high injection with $n \approx N_A$ throughout the whole base. Different to eqn. 3.1 the collector current is given by

$$I_C = I_S \left\{ \frac{Q_{B0}}{Q_B} \left[e^{U_{BE}/U_T} - 1 \right] - \left(\frac{Q_{B0}}{Q_B} + \frac{1}{\beta_R} \right) \left[e^{U_{BC}/U_T} - 1 \right] \right\}, \tag{3.2}$$

with Q_B as the majority charge at the neutral base

$$Q_B = q \int_{base} p(\vec{x}) dv, \tag{3.3}$$

[1] *S*imultion *P*rogram with *I*ntegrated *C*ircuit *E*mphasis was developed 1975 at the University of California, Berkeley

[2] A circuit simulator from Cadence Design Systems, it is embedded in the most different Cadence chip design environments

[3] ADS is for Advanced Design System from Agilent, an RF and Microwave Simulation Suite consisting of several tools under a graphic environment.

at the operation point of the transistor. Q_{B0} is the majority charge at $U_{BE} = U_{BC} = 0\text{V}$. This concept allows a consideration of the change in the width of the space charge region in dependence of the operating point, the Early effect, and the consideration of high base majority injection, as mentioned before. In the Gummel Poon model the normalized base charge is approximated by

$$\frac{Q_B}{Q_{B0}} = \frac{1}{2}\frac{1+\sqrt{1+4I_S(\frac{e^{U_{BE}/U_T}-1}{I_{KF}}+\frac{e^{U_{BC}/U_T}-1}{I_{KR}})}}{1-\frac{U_{BC}}{V_{AF}}-\frac{U_{BE}}{V_{AR}}}. \tag{3.4}$$

V_{AF} represents the forward Early voltage, V_{AR} the reverse Early voltage, I_{KF} the forward knee current and I_{KR} the reverse knee current.

Figure 3.7 shows the equivalent circuit used for the modeling of a bipolar transistor in SPICE. The diodes D_C and D_E represent the base-collector and the base-emitter diode of the transistor, respectively. The carrier recombination in the space charge region is modeled by D_{LC} and D_{LE}. The diode D_S is used for the description of the pn-junction between collector and the substrate. The depletion layer capacitances are represented by q_{JE} for the base-emitter junction, q_{JC} and $q_{BC'}$ for the internal and external base-collector depletion layer capacitance, respectively. q_{TE} and q_{TC} describe the diffusion charges. The connection resistances are considered by $R_{EE'}$, $R_{CC'}$ and $R_{BB'}$.

Usually externally added components are used in the model files in addition to the equivalent circuit in fig. 3.7 to consider the 'outer' transistor. The outer transistor represents the structure outside the npn complex. Figure 3.8 shows the model for the complete transistor with T representing the transistor model in fig. 3.7.

Compact models are visualized as in fig. 3.8 by their equivalent circuits. This is done for several reasons:

1. Circuit simulators like SPICE need an equivalent circuit described by a netlist. The prevention of simulation errors due to misused or misplaced network elements can be improved by visualizing the equivalent circuit.

2. Parasitic elements like series resistances and capacitances outside of the inner transistor can be included easily.

3. The exact knowledge of parasitics helps to improve the selection of the transistor geometry.

4. Avalanche breakdown can be included using an additional current source as described in section 3.6.

Figure 3.9 shows the visualization of a simple compact model for the transistor in fig. 3.1. It consists of an inner transistor and the outer elements representing the connection parasitics.

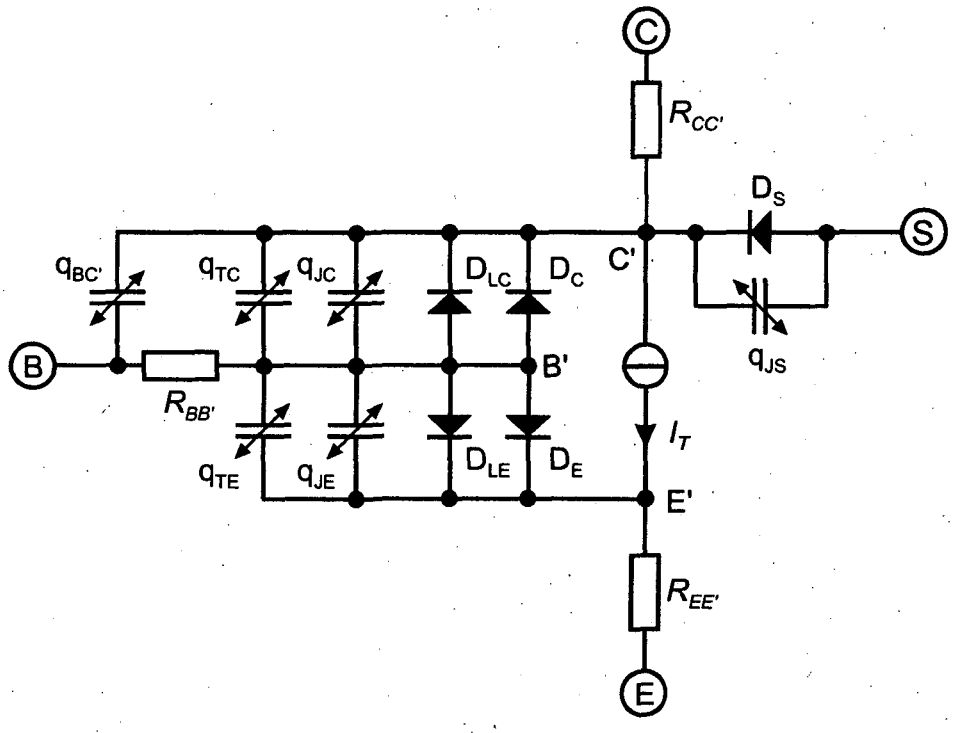


Figure 3.7: The equivalent circuit used for the modeling of a bipolar transistor in SPICE.

The model parameters are usually not calculated from their doping profile and geometry, but are determined from the measurement of characteristic curves and fit procedure minimizing the error between measurement data and the equations. In the past years several transistor models have been developed. Additional to the most common SGP model there exist the *V*ertical *B*ipolar *I*nter-*C*ompany model (VBIC), the Philips MEXTRAM (Most Exquisite Transistor Model) and the HICUM (High-Current Model). These models improve the description in the high current and saturation region. A very good overview of the compact transistor models can be found in [Graaf 90, Berkner 02].

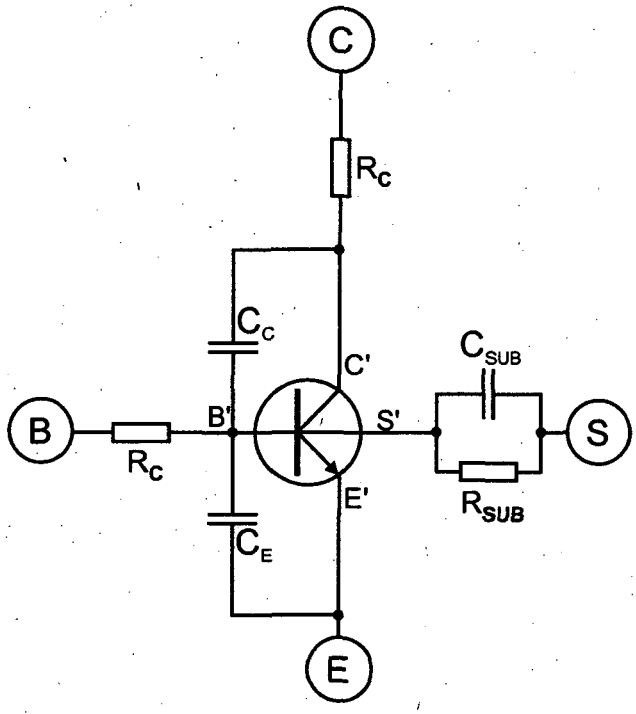


Figure 3.8: Extended model for the complete transistor. T represents the inner transistor.

3.4 Process technology characteristics

Just as circuits are benchmarked for their suitability for certain applications, this is done for technologies as well. For RF circuits there exist two major groups:

1. The transistor characteristics: They arrange the frequency region the transistor be used and the limitations considering supply voltages, optimum currents, etc.

2. The passives in the technology. RF circuits require typical matching elements like inductances and capacitances. It is important to know, which capacitors are available and their limitations in capacitance and the breakthrough voltages. Furthermore inductances need to have a certain level of quality depending on the metal layer stack and the substrate.

The following text will consider the major transistor characteristics for PA applications [Cooke 71, Allison 79]. Usually they are important for other applications as well, so this can be considered to have a certain generality.

The main transistor characteristics relevant for PAs are [Rein 80, Allison 79, Johansson 97]

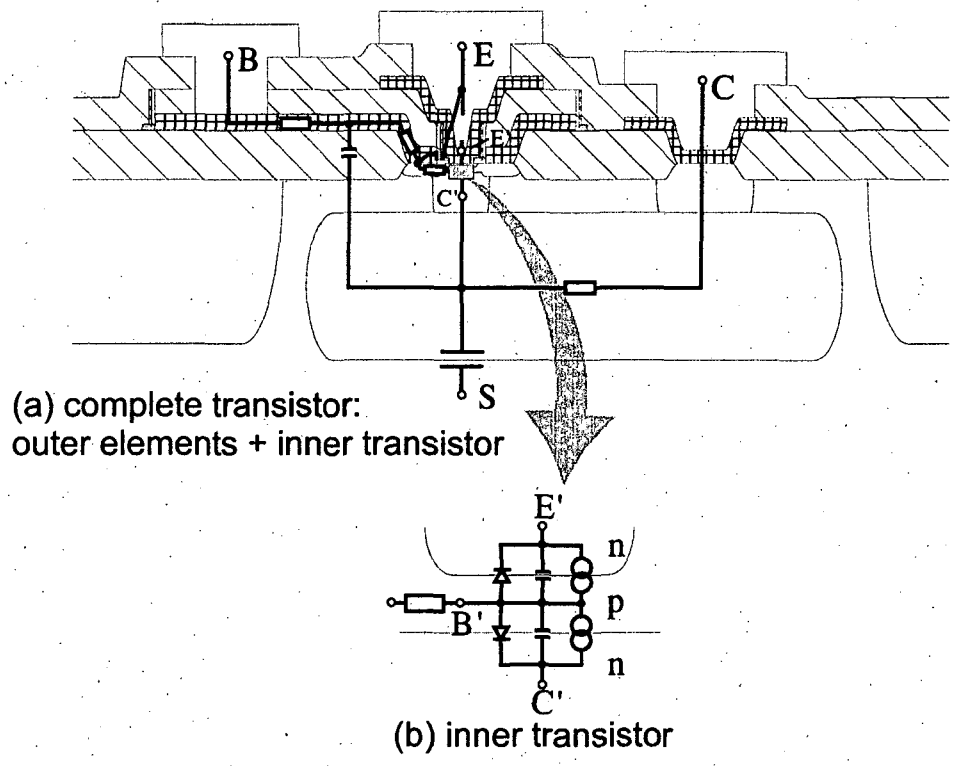


Figure 3.9: Visualization of a compact model for to the transistor in fig. 3.1. The inner transistor is represented by the connection points B',C' and E'. Parasitic resistances and capacitances (poly-Si and substrate capacitances) are modeled by the outer elements analogous to fig. 3.8.

- The current amplification β,
- the transit frequency f_T,
- the maximum oscillation frequency f_{max},
- the breakdown voltages U_{CE0} and U_{CB0},
- the parasitic capacitances C_{BC} and C_{BE},
- the series resistances R_E, R_C and R_B.

For the following explanations a transistor configured as a two port in common emitter configuration is considered (fig. 3.10).

The operating point is given by the input voltage U_{BE} and the output voltage U_{CE} and the resulting currents I_C and I_B. For a small change in the input voltage (small compared to the thermal voltage $U_T = k_B T/q$ so that a small signal analysis can be assumed) corresponding changes in I_C and I_B are obtained. For

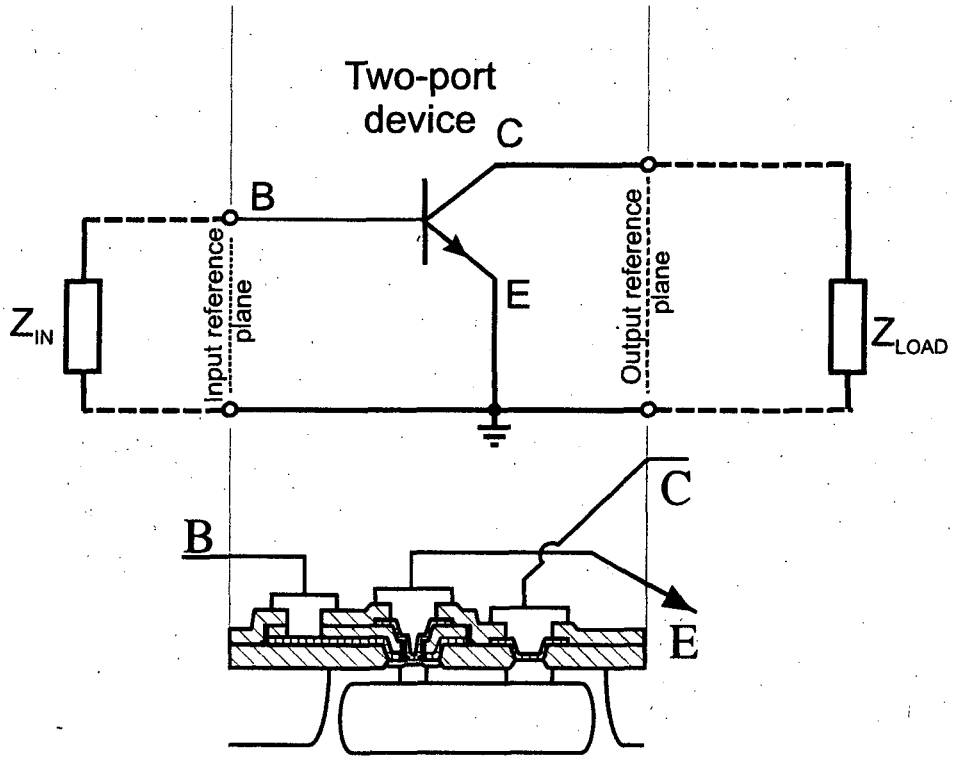


Figure 3.10: NPN transistor in a two-port configuration.

low operating frequencies f the small signal current amplification β_{AC} with output AC shorted is given by

$$\beta_0 = \lim_{f \to 0} \beta_{AC} = \left. \frac{\partial I_C}{\partial I_B} \right|_{U_{CE}=const} . \tag{3.5}$$

It is related to the static current amplification $\beta = I_C/I_B$ by

$$\beta_0 = \beta + I_B \left. \frac{\partial \beta}{\partial I_B} \right|_{U_{CE}=const} . \tag{3.6}$$

For amplifier applications, the factor β should show only a weak dependence on the base current. This implies β being about the same as β_0, typically from 100-200 for integrated transistors. For high frequencies the current amplification β_{AC} decreases, as changes in the collector current I_C follow the base current I_B after a characteristic relocation charge time in the transistor. If I_B changes too fast, β_{AC} decreases. The frequency where $\beta_{AC}=1$ is called the transit frequency f_T. Figure 3.11 shows β_{AC} vs. frequency.

The next major transistor speed benchmark is the maximum oscillation frequency f_{max}. It describes the frequency where the power amplification G = 1 under the

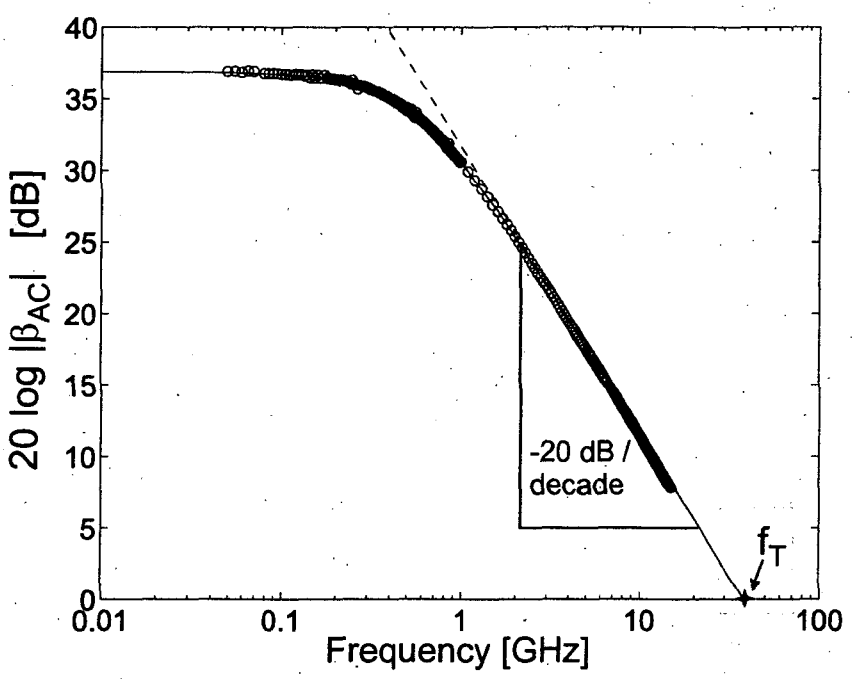


Figure 3.11: Small-signal current gain β_{AC} vs. frequency.

assumption that in- and output are perfectly impedance matched. If the matching is perfect, the maximum available gain G_{MAG} is reached. Unfortunately an amplifier typically shows instabilities like oscillation, especially at low frequencies, so that the maximum power gain is limited by the stable region (G_{MSG}). The area of stable operation can be calculated for example by the Rollet stability factor [Gonzales 84] and other methods like stability circles in the Smith-chart. Figure 3.12 shows a plot with two different power gain areas. Below 5 GHz the transistor would become instable, so that the optimum matching is not possible. The maximum available gain is observed at optimum in- and output matching. It should be mentioned, that f_{MAX} is sometimes defined by the unilateral power gain going down to 1. This definition requires the suppression of positive feedback between in- and output. Therefore, it is necessary to consider the exact definition used. In a simple approximation f_T and f_{MAX} relate to each other by [Allison 79, Gonzales 84]

$$f_{max} \approx \sqrt{\frac{f_t}{8\pi r_B C_{BC}}}. \tag{3.7}$$

with C_{BC} representing the parasitic collector base capacitance and r_B the parasitic base resistance. f_{MAX} includes the base resistance and the parasitic base collector capacitance. It is of more practical use than f_T, but the definition has to be considered carefully.

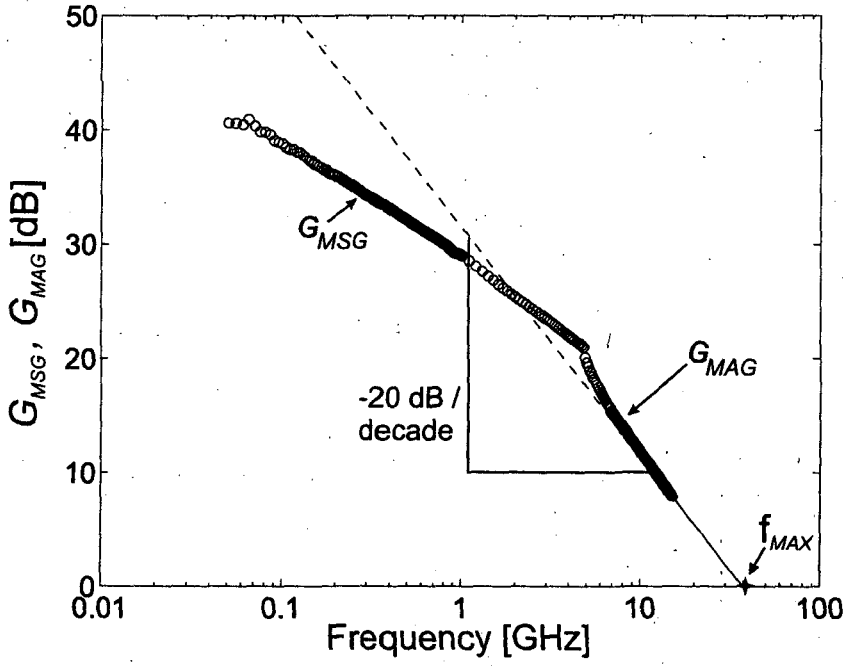


Figure 3.12: The maximum stable power gain G_{MSG} and the maximum available power gain G_{MAG}.

Another important characteristic of bipolar transistors is the avalanche breakdown. It limits the operation of the transistor especially when operated for large signal applications like PAs and wide-band driver circuits such as laser drivers. The voltage applied between two terminals of the transistor is limited by a breakdown voltage (e.g. U_{CE0}) of the junction or the maximum allowed current under forward bias [Reisch 03]. Two parameters of the three possible breakdown types are especially important: The collector emitter breakdown U_{CE0} and the base collector breakdown voltage U_{CB0}. The breakdown behavior of a transistor itself is also dependent on the circuitry around it. This will be shown in section 3.5.

Finally, there exist the parasitic elements of a transistor: The parasitic capacitances C_{BC} and C_{BE} and the series resistances R_E, R_C and R_B. The capacitances C_{BC} and C_{BE} depend mainly on the transistor layout and the physical dimensions of the transistor. While C_{BE} acts as input capacitance, C_{BC} is one of the major reasons for the limited unilateral behavior of the transistor. The series resistances also depend on the physical layout. Thus for example the base resistance can be significantly lowered by the use of multi-base transistor contacts such as in the transistor layouts of fig. 6.4 and fig. 7.4.

3.5 Breakdown effects in bipolar transistors

In a bipolar transistor several types of breakdown effects can occur [Tholl 76, Reisch 03]:

- *Collector-base breakdown:* The maximum reverse voltage allowed between collector and base (U_{CB0} or BV_{CB0}) with the emitter left open is defined by the avalanche breakdown of the base collector diode. U_{CB0} decreases for high collector doping. Typical values for RF suited SiGe processes are about 10 V (Infineon B7HF).

- *Emitter-base breakdown:*

  The breakdown of the emitter base diode occurs generally at the sidewalls between the n-doped emitter being embedded into the left and right p-doped area of the base where the maximum electric-field strength is found. The corresponding breakdown voltage U_{EB0} or BV_{EB0} decreases with increased base doping values. U_{EB0} is typically a few volts. In practical circuits, reverse biased emitter base junctions should be avoided.

- *Collector-emitter breakdown*

  The collector-emitter breakdown voltage U_{CE0} or BV_{CE0} defines the maximum allowed collector emitter voltage for a constant current driven base. For $U_{CE} > U_{CE0}$ the output current is no longer controlled by the base current. It is defined as open-base breakdown voltage with a constant driver base current. Two effects may cause it: The punchthrough effect or the carrier multiplication due to impact ionisation [Reisch 03].

  The avalanche induced breakdown is the result of a positive feedback of leakage currents. These are relatively small ($I_{CEO} \approx (\beta+1)I_{CB0}$), but with increasing U_{CE} values, the electric field strength in the base collector diode increases and causes a multiplication growth by the multiplication factor M. In the avalanche process, holes are generated acting as base current. [Reisch 03] gives a collector current of

$$I_C = M[\frac{\beta'}{1-\beta'(M-1)} + 1]I_{CB0} \tag{3.8}$$

  with $\beta' = I_{BE}/I_T$ being the current amplification for the case that the breakdown is neglected. For $\beta'(M-1) = 1$ the term corresponds to the collector emitter breakdown, as the term shows a divergence. If the Miller formula

$$M = \frac{1}{1-(\frac{U_{CB}}{U_{CB0}})^n} \tag{3.9}$$

  for M is used, the breakdown condition $\beta'(M-1) = 1$ gives [Reisch 03]

$$U_{CE0} = \frac{U_{CB0}}{\sqrt[n]{(\beta' + 1)}} + U_{BE}. \tag{3.10}$$

The breakdown voltage is decreasing with increasing current gain. Furthermore, the transistor technology can be tuned for higher breakdown voltages by lowering the current amplification. Figure 3.13 shows a secondary photon spectroscopy of a PA output transistor at avalanche breakdown.

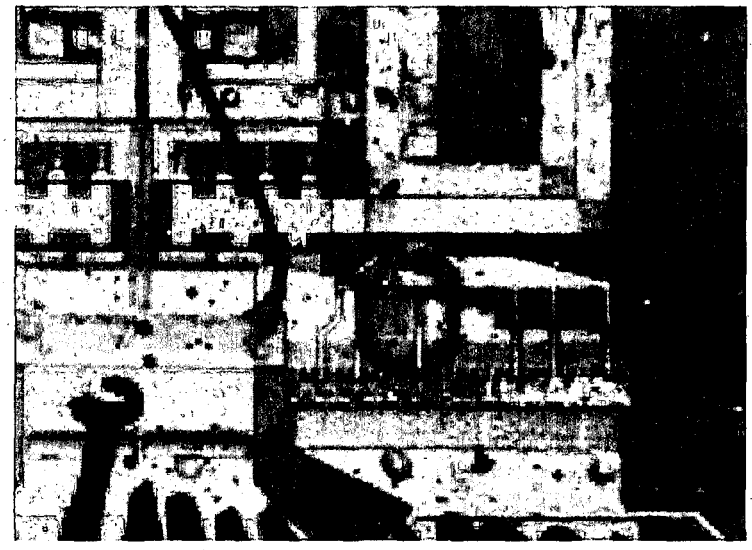


Figure 3.13: A secondary photon spectroscopy of a PA output transistor at avalanche breakdown (Infineon B6HF Si-bipolar technology [Klose 93]).

Punchthrough effects is mostly related to too thin base layers, so that the collector base space-charge layer reaches the emitter base space-charge layer. Then thermal carrier emission can cause significant current increase due to the reduced potential barrier.

3.6 Breakdown modeling

Modern Si based high speed bipolar transistors have relatively high collector doping concentrations to achieve high current densities. This is accompanied by high electric field densities in the base collector space charge layer and thus low breakdown voltages. This yields to the necessity to more accurate consideration of the breakdown effects in the design of PA, which are usually not covered by standard SGP models.

Figure 3.14 shows the output characteristics of a Si-bipolar BJT for different base resistances and emitter resistances. It shows that the avalanche breakdown

is relaxed for low base resistances. Thus, a transistor layout enabling lowest base resistances will be of advantage. Also for the circuitry, biasing networks with a low impedance will improve the breakdown behavior.

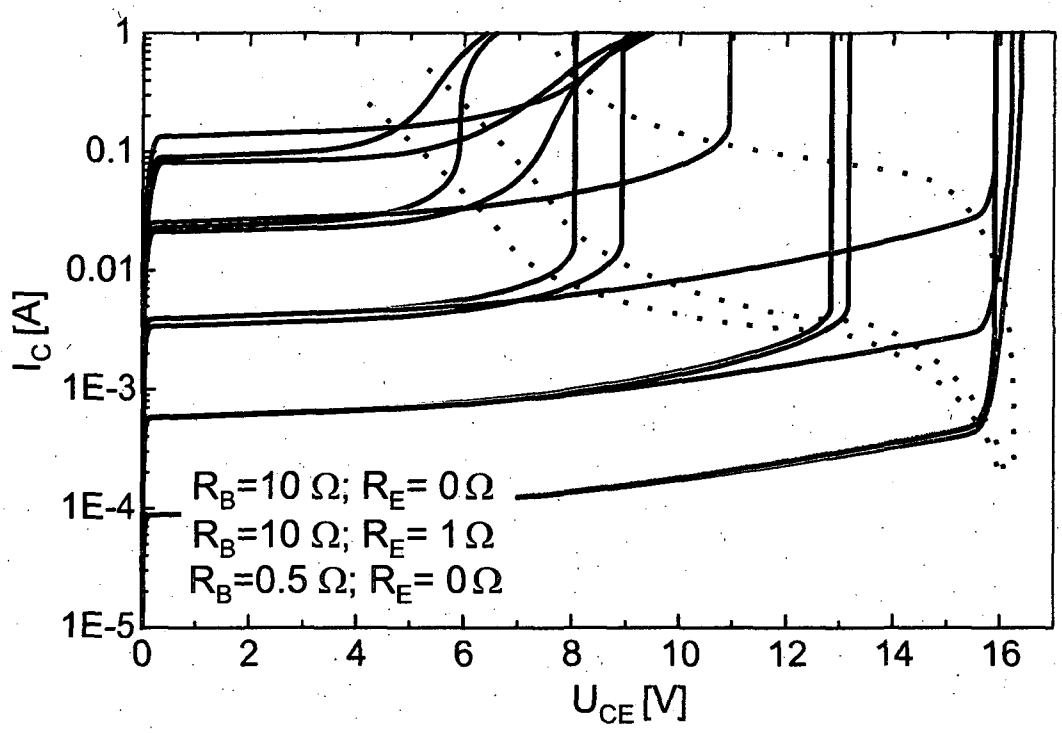


Figure 3.14: U_{CE0} Output characteristics of a Si-bipolar transistor for different base and emitter resistances (Infineon B6HF [Klose 93]).

Due to large collector base voltages significant carrier generation is found in the collector-base depletion region. This can be modeled with an additional current source as shown in fig. 3.15.

At high collector-base voltages, this source forces a significant current (e.g. 0.1 I_C) to flow out of the base, i.e. in the reverse direction. This leads to a voltage drop at the internal base resistor, resulting in a larger U_{BE} and, in turn, higher collector and base currents in the center of the transistor. Because of this positive feedback, the current finally constricts itself to the center of the transistor if the avalanche current is sufficiently high.

The modeling of the avalanche breakdown requires an accurate representation of the multiplication factor. The current source in fig. 3.15 is directly dependent on the multiplication factor. The avalanche breakdown behavior can be included can be added by this current source. Other breakdown models as presented in [Zhang 99] use such current sources as well but use additionally a current dependent capacitance $C_{BE}(I_C) = C_k I_C^2$ to include the f_T reduction resulting from the Kirk effect. A major problem in adding this current source is the knowledge

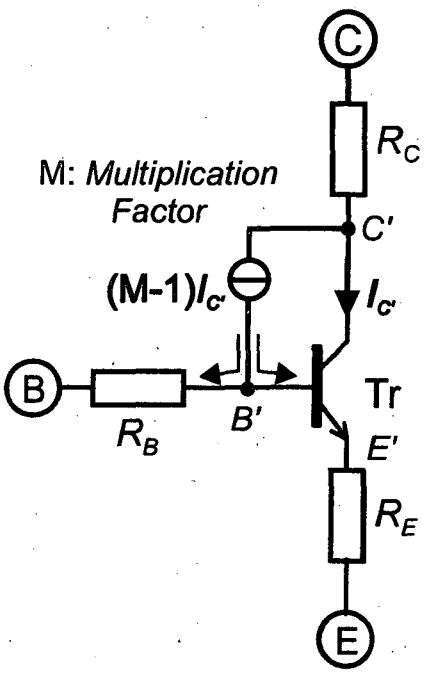
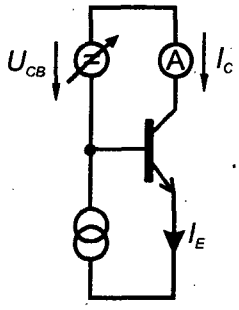


Figure 3.15: The base collector breakdown effect modeled using an additional current source describing the current generated by impact ionisation.

of the multiplication factor M. In its simplest form, the multiplication factor is expressed by Miller's empirical formula [Reisch 03, Zhang 99] eqn. 3.9.

The multiplication factor can be determined by measurements. Figure 3.16 shows the measurement setup for the multiplication factor. Typical measurement results are shown in fig. 3.17 for a B6HF Si-BJT [Klose 93].



$$\frac{dI_C}{dI_E} = \alpha \cdot M(V_{CB})$$

$\alpha = \beta/(1+\beta)$: base transport factor
M : multiplication factor

Figure 3.16: Measurement setup for the multiplication factor M.

As seen in eqn. 3.9, the empirical Miller expression for the calculation of M becomes singular for $U_{CB} = U_{CB0}$. Hence the insertion into a SGP model will cause SPICE to diverge and furthermore for high U_{CB} the term 3.9 becomes

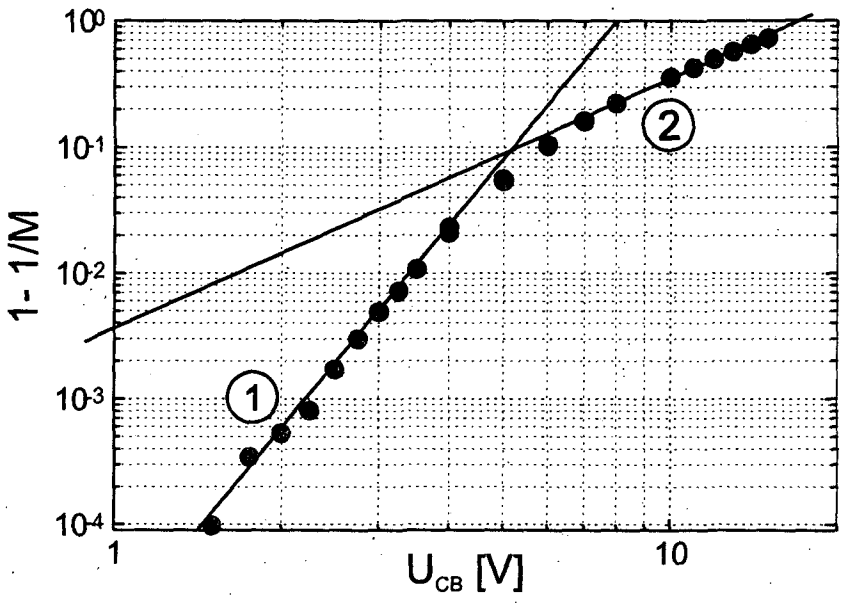


Figure 3.17: Measurement for the multiplication factor M for a B6HF transistor. The slope 1 represents the weak avalanche breakdown [Kloosterman 89], slope 2 the strong avalanche breakdown.

inaccurate. For this reason [Gabl 97] uses a modified term for the multiplication factor M term:

$$M = 1 + \underbrace{\frac{1}{1+\exp(-\frac{U_{CB}}{0.05})}}_{\text{A}} \left[\underbrace{\frac{1}{(\frac{A_1}{U_{CB}^{n_1}} + \frac{A_2}{U_{CB}^{n_2}})}}_{\text{B}} + \underbrace{A_3 \exp\Big(\frac{U_{CB} - U_{CB0}}{n_3}\Big)}_{\text{C}} \right] \tag{3.11}$$

The term A is used to get the multiplication factor M=1, for the case of $U_{CB} < 0$. Furthermore, term B must be equal to Millers equation for $U_{CB} \ll U_{CB0}$. A_1 is obtained from the slope 1 in fig. 3.17 representing the weak avalanche breakdown [Kloosterman 89] and A_3 from the slope 2. Hence, term C represents the strong breakdown in fig. 3.17. The other parameters are obtained by fitting eqn. 3.11 to the measured multiplication factor curve. For example, BJTs processed in Infineons B6HF technology [Klose 93] are fitted by the parameters A_1=1521, A_2=83357, A_3=0.5, V_{CB0}=16 V and n_1=3, n_2=5.7, n_3=0.1.

For the PA designs in [Bakalski 03,a, Bakalski 03,c] the method of adding an additional current source into an existing SGP model analogous to the proposal of [Gabl 97] was implemented successfully:

```
.SUBCKT TD12X188_C2 1 2 3 4
Q1 80 5 3 4 Q12X188_C2
RC 1 8  5.06
```

```
RB1 2 5 1.39
CE 3 5 9.7E-015
CCOX 5 8 10.9E-015
V1 8 80 0

G2 5 8 value =
{-I(V1)/(1+exp(-v(80,5)/0.01))*(v(80,5)^6.9*v(80,5)^3.5/ +
(630*v(80,5)^6.9+7500*v(80,5)^3.5)+exp((v(80,5)-8.5)/0.3))}

.ENDS TD12X188_C2
```

The current source represented in the SGP model by G2 is modeled using the parameters A_1=630, A_2=7500, A_3=1, V_{CB0}=8.5 V and n_1=6.9, n_2=3.5, n_3=0.3 (Infineon BiCMOS process B9C).

Another very accurate model splitting the intrinsic transistor area into 6 parts was proposed by [Rickelt 99, Rickelt 02]. However, this model suffers from the same problems as all complex transistor models: Long simulation time and the risk of divergence during simulations, often caused by internal limitations in simulation tools.

3.7 B7HF - A SiGe bipolar production technology

The PAs discussed in Chapters 5,6 and 7 are all based on the Infineon B7HF SiGe bipolar production technology [Klein 99, Wolf 01]. The transistor model equivalent circuit is realised as mentioned before by the use of an additional parasitic pnp transistor (fig. 3.18). The SiGe bipolar technology is a 0.35 μm, 72 GHz/ 75 GHz (f_t/f_{max}) volume production process. The key features of the technology are npn transistors with double-polysilicon self-aligned emitter-base-configuration and selective SiGe-epitaxy, a selectively implanted collector (SIC) and a trench isolation. The worst-case collector-base breakdown voltage for the npn HBT is BV_{CB0} = 8 V (typical: 10 V) and the worst-case collector-emitter breakdown voltage is BV_{CE0} = 2.3 V (typical: 2.8 V). Further usable devices are a vertical pnp transistor, poly-Si resistors, MIM capacitors and inductors. Figure 3.19 shows the metalization stack in scale. The upper metal layer has a thickness of 2.8 μm, making on-chip inductors with quality factors of up to 15 feasible.

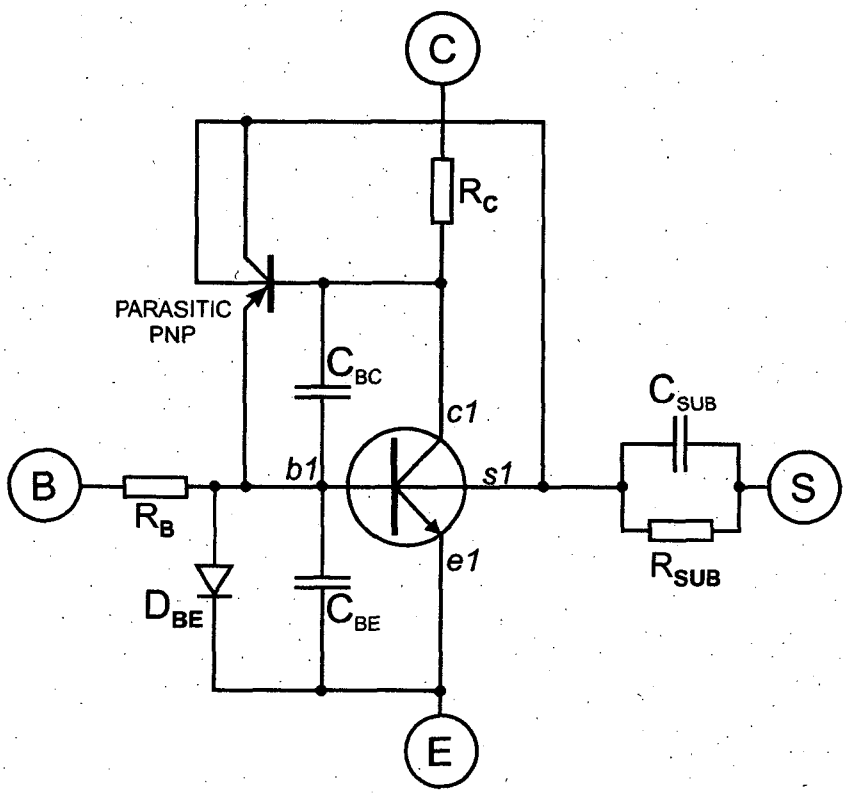


Figure 3.18: The npn transistor equivalent circuit for B7HF.

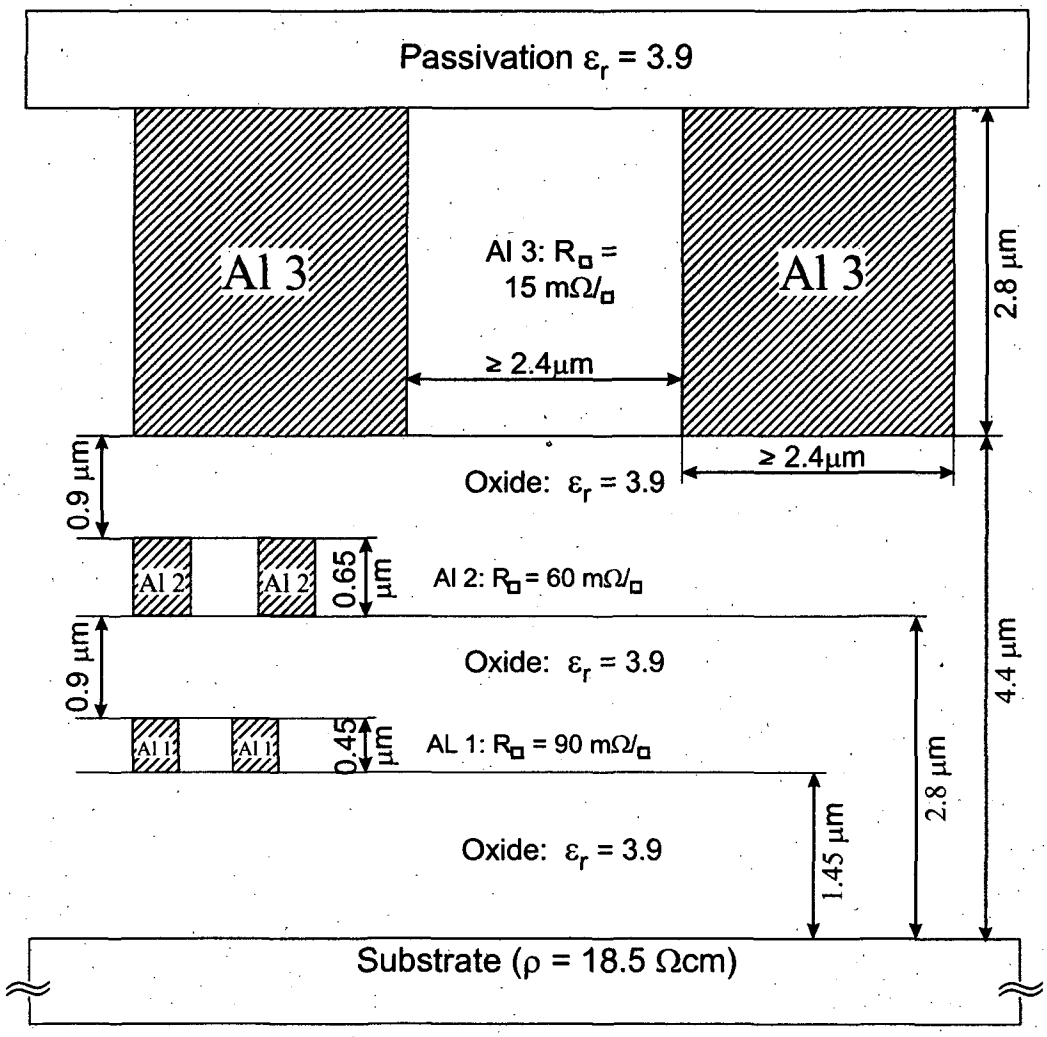


Figure 3.19: Schematic cross section of the metal layer stack.

Chapter 4

Matching Networks

4.1 Introduction

Besides the transistors, the key component in successful RF microwave circuit design is the accurate modeling and knowledge on matching circuits. Especially efficient power amplifiers basically depend on the matching network. The better they are implemented, the higher the performance will be. Furthermore there exist different targets in the design of the matching networks (e.g. noise matching, power matching). Considering the necessary bandwidth, possibility of integration and losses, there exist a large variety of matching circuits [Freyer 87, Mongia 99] in the most different way of implementation.

4.2 Matching using lumped elements

Most matching applications can be solved using the Smith chart using trajectories. Its mathematical background can be found in [Magerl 98]. Basically there exist two types of Smith-charts, the Z-Smith-chart for impedances and the Y-Smith-chart for admittances.

Figure 4.1 shows the effect of ideal lumped elements: In series connected inductances cause a clockwise shifting in the Z-Smith chart whereas a capacitance shifts counterclockwise. For parallel connected elements the same happens vice versa in the Y-Smith chart.

Regarding the resistances an important effect can be seen. If an inductor behaves non ideal, the circle will no more be exactly counterclockwise, it will be shifted to higher Z_0. This implies, that for certain matching circuits, for example a very low impedance to $50\,\Omega$ will need inductors and capacitors with a low-ohmic part. This fact is described by Constant Q arc plots in the smith chart [Vizmuller 95].

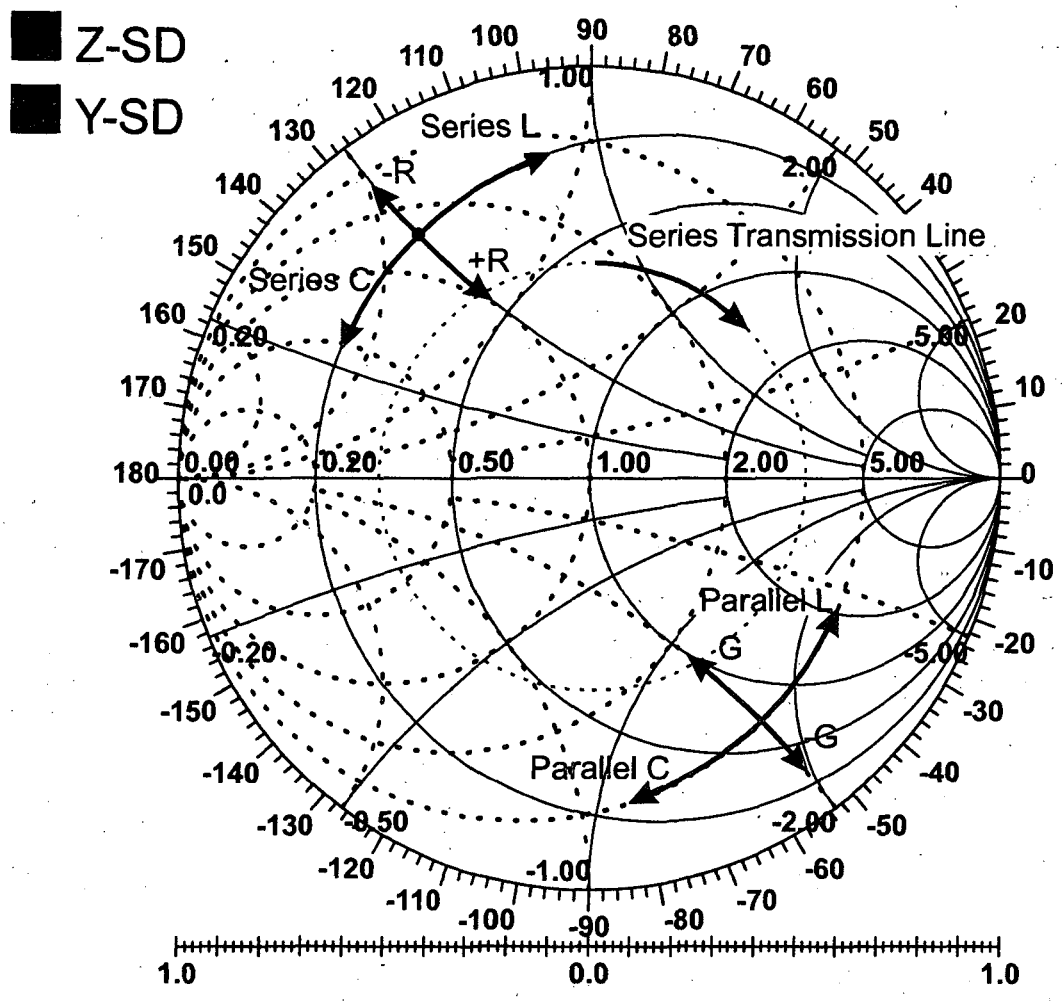


Figure 4.1: Impedance matching using ideal R,L,C lumped elements in series (Z-Smith chart) and parallel configuration (Y-Smith chart).

4.3 Transmission lines as matching components

As sketched in fig. 4.1 transmission lines could be used as matching elements. A transmission line is defined by its characteristic impedance Z_0 and its length. For microstrip transmission lines, the [Hammerstad 75] formulas are typically used. The characteristic impedance sets the radius around the Smith chart origin, while the phase shift is given by the transmission line length. If transmission line are selected carefully, they can be used to substitute lumped elements [Mongia 99]. The most important configurations are shown in fig. 4.2.

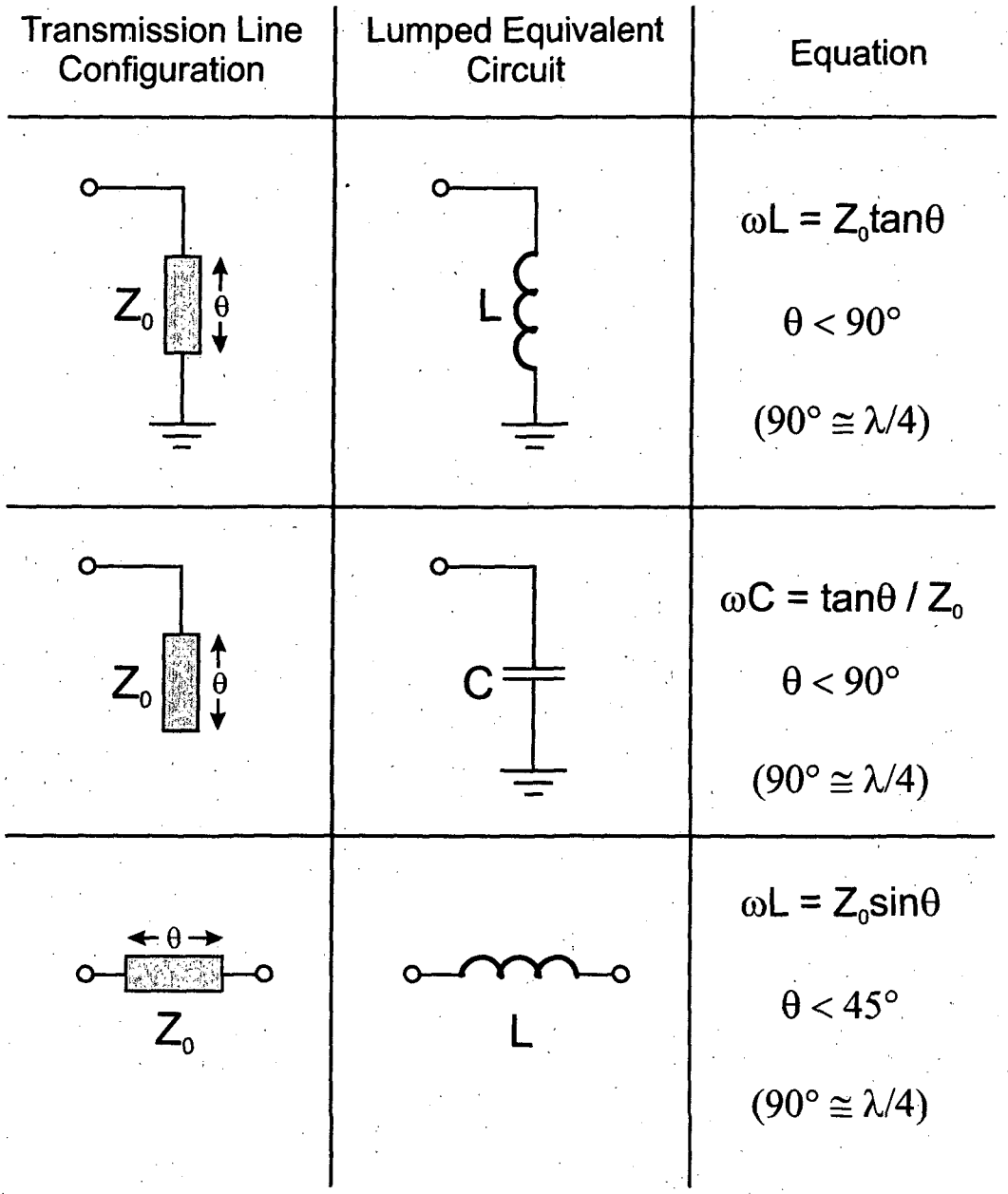


Figure 4.2: Substitution of lumped elements using transmission lines and vice versa [Mongia 99].

4.3.1 The $\lambda/4$-transformer

A very popular way of matching two real-valued impedances is the $\lambda/4$-transformer. As a transmission line can be sketched in the Smith-chart on a circle around the Z_0 point, it is easy to see that it is possible to transform a low impedance into its

180° shifted counterpart. The diameter of this circle is given for the impedance of the transmission line. For two given impedances Z_1 and Z_2, the necessary impedance of the transmission line can be determined by

$$Z_{TL}^2 = Z_1 \cdot Z_2 \tag{4.1}$$

4.3.2 Radial stubs

A stub is an open ended transmission line often used to realise an RF ground. A ground connection is usually defined by its resistance at the observed frequency toward the ground potential and should be as low as possible [Kraus 99].

Figure 4.3 shows such a radial stub with its characteristic dimensions: The angle α of the stub, the radius R_L and the inner radius R_i (Fig. 4.3).

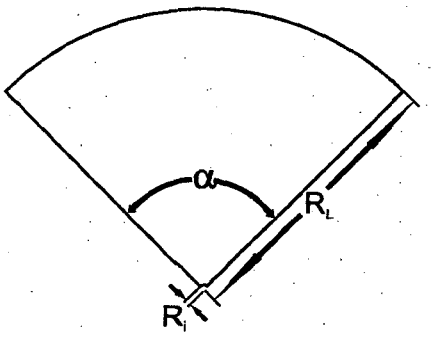


Figure 4.3: Characteristic dimensions for the equations of a radial stub.

[Agilent 88] and [Vinding 67] have shown, that the reactance X of such a stub is given by

$$X = \frac{Z_0 d}{2\pi R_i} \frac{\cos(\theta_i - \psi_L)}{\sin(\psi_i - \psi_L)} \frac{360}{\alpha} \tag{4.2}$$

The variable d is the height of the substrate dielectric and

$$Z_0 = \frac{120\pi}{\sqrt{\epsilon_r}} \sqrt{\frac{J_0^2(kR_i)+N_0^2(kR_i)}{J_1^2(kR_i)+N_1^2(kR_i)}}$$

$$k = \frac{2\pi\sqrt{\epsilon_r}}{\lambda_0} \text{ (approximate for microstrip)}$$

$$\theta_x = \tan^{-1}\left(\frac{N_0(kR_i)}{J_0(kR_i)}\right)$$

$$\psi_x = \tan^{-1}\frac{J_1(kR_{i,L})}{-N_1(kR_{i,L})}$$

$$x = i \quad or \quad L$$

with the letter J for the Bessel and N for the Hankel function. ϵ_r is taken from the microstrip expression $\epsilon_{eff} = \frac{\epsilon_r+1}{2} + \frac{\epsilon_r-1}{2}(1+10\frac{d}{w})^{-\frac{1}{2}}$ with d as the dielectric thickness and w as the line width. [Agilent 88] use for W the width corresponding to the half-splitted stub area. As these equations are not simple to use, a simulation tool has to handle them. A simpler method is described in [Kraus 99]: The radial stub is cut into a lot of transmission lines in series with the width of the lines taken as small as possible to get the original radial stub structure. The radius is about $\lambda/4$. This structure enhances calculation speed.

The way to design such a DC-stub can be seen as a two steps procedure: First, a radial stub is designed to act as a shunt. This is done by fixing R_i and the angle, and then optimizing the radius. The larger the angle is, the larger the bandwidth will be. A radial stub does a good work for angles above 45^o.

The main usage of a radial stub is the power supply feeding. In combination with a $\lambda/4$-transformer the short circuit is transformed into an open. The point the stub is meeting the choke is the port where the DC supply has to be connected. At this position, the RF signal is short circuited. On the other end of the choke an open circuit is seen, so that the RF signal is not affected from the power supply feeding.

4.4 Transformers and inductors

The usage of on-chip transformers and inductors depends mainly on a convenient way of modeling. As inductors on Si-substrates always suffer from limited metalization conductivity and a lossy substrate, an accurate and fast implementation into the simulation has to be implemented to optimize the circuitry.

4.4.1 Physical layout design and modeling

The layout of monolithic on-chip transformers and inductors is constructed using conductors wrapped in the same plane and/or overlaid on multiple stacked metal layers. Implemented by circular or rectangular shapes with different winding configurations, each of these realizations has specific performance advantages. For some semiconductor technologies, the shape is limited by mask scaling limitations, not allowing for example circular shaped windings, even if it would be preferred due to high quality factor Q requirements. There exist publications on possibilities in construction and optimization of inductors [Ashby 96, Yue 98, Niknejad 00, Wohlmuth 00] and transformers [Rabjohn 89, Long 00, Thüringer 02].

All these inductive structures show the same physical effects independent on their geometrical structures, which influence their behavior in their quantitative values. Figure 4.4 shows a three dimensional schematic cross-section of an inductor structure. It sketches a brief insight to the physical effects. The picture shows

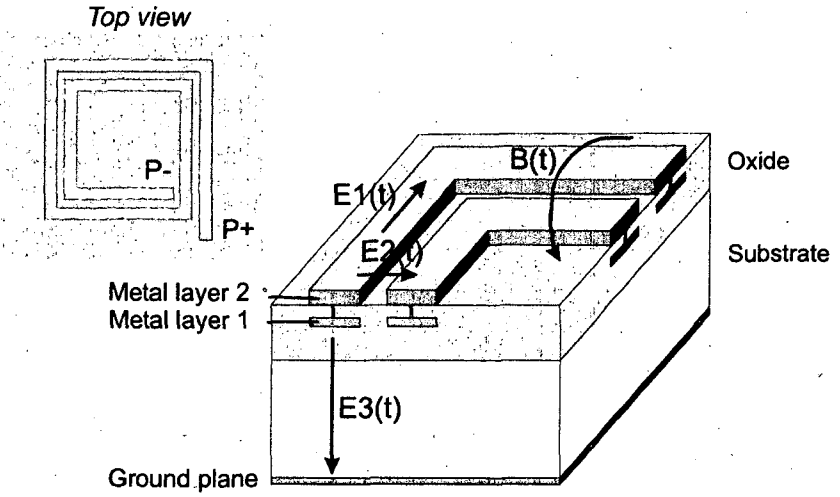


Figure 4.4: Schematic cross-section of a planar inductor.

only two adjacent turns realised on one metal layer plane embedded in oxide separated from the substrate by the oxide. Thus it is a simplified model for a real metal stack, it illustrates the different electromagnetic field components present in an integrated inductor when excited:

Around the traces exists a time varying magnetic flux density B(t), caused by the current in the metal conductor. B(t) causes stored magnetic energy and the resulting inductance. Furthermore it is the reason for coupling between the primary and secondary winding in transformers.

Unfortunately all inductors structures suffer from losses. The reason for this can be found in the existence of electric field components. Each of the electric field components E1-E3 sketched in fig.4.4 result in loss of energy. Hereby E1(t) represents the electric field along the metal trace caused by the finite conductivity. A current flowing through this metalization in association with ohmic losses causes a voltage drop. A voltage difference between each turn originates denoted by the field E2(t) being present between each turn. Furthermore the finite resistance and capacitive coupling involves a leakage current between the turns. Finally the electric field component E3(t) forces a leakage current between the metal traces and ground.

In addition to the described electromagnetic fields, many other high-order effects are present. For instance, eddy currents arise in the metal traces and force a skin effect due to penetration of time varying magnetic fields. As well, a proximity effect occurs due to the interaction between the magnetic field and currents. This results in an increased resistance and losses. Additionally currents induced in the substrate give rise to counterproductive secondary magnetic fields which interact with the primary magnetic flux density B(t).

Regarding the modeling, an alternative to a fully 3-D field analysis is the ap-

proximation with electrical lumped elements (R,L,C). It is valid because of the physical lengths of the conducting segments in the layout being typically much less than the guided wavelength at the operation frequency. Thus the analysis is reduced to electrostatic and magnetostatic calculations.

4.4.2 Low-order inductor model

Aim of the low-order models is the reduction of lumped elements in the equivalent circuit to the necessary minimum. The model in fig. 4.6 allows the characterization of an inductor up to its first self resonant frequency. Hereby the whole winding is modeled as a lumped physical element with two ports. Furthermore all parasitics are added around the inductance.

Which parasitics appear and how they have to be arranged in an equivalent electrical circuit can be seen in fig. 4.5.

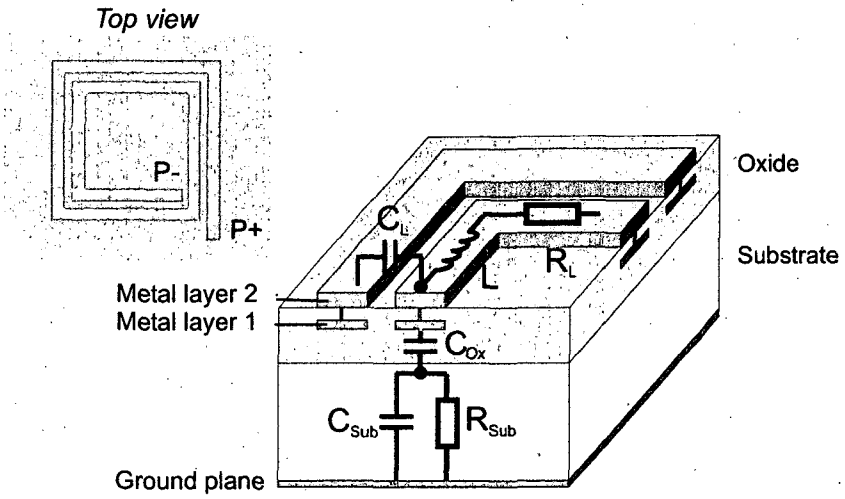


Figure 4.5: Three dimensional cross-section of a monolithic inductor

The lumped elements are identified by:

- L, Inductance.
- R_L, Ohmic loss in the conductor material due to skin effect, current crowding and finite conductivity.
- C_L, Parasitic capacitive coupling between the winding turns.
- C_{Sub}, Parasitic capacitive coupling into the substrate.
- C_{Ox}, Parasitic capacitive coupling into the oxide.
- R_{Sub}, Ohmic loss in the conductive substrate.

Figure 4.6 shows the equivalent circuit. It represents a symmetrical pi-circuit with ports on both sides. The series branch consists of the overall inductance L and serial resistance R_L for the whole winding. C_L is located between the terminals and represents the winding to winding capacitive coupling losses. Assuming a symmetry, the other static parasitic elements C_{Ox}, R_{Sub}, C_{Sub} of the winding are divided into two equal parts and placed at each port side. This is expressed by

$$C_{Ox1} = C_{Ox2} = C_{Ox}/2 \tag{4.3}$$

$$C_{Sub1} = C_{Sub2} = C_{Sub}/2 \tag{4.4}$$

$$R_{Sub1} = R_{Sub2} = 2R_{Sub} \tag{4.5}$$

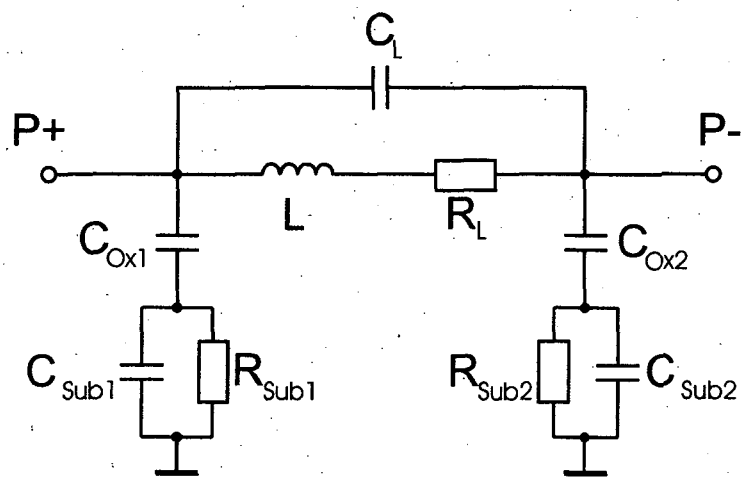


Figure 4.6: The compact inductor model

Note, that the capacitance C_L models the parasitic capacitive coupling between the input and output port of the inductor. The capacitive coupling is based on the

crosstalk between the adjacent turns. The capacitance allows the signal to flow directly from the input to the output port without passing through the inductor. The modeling of this capacitor requires the voltage profile along the winding to be taken into account. All other parameters have to be determined by statical investigations of the inductor structure.

4.4.3 Higher-order inductor model

Using additional circuit elements by creating a higher-order model results in an improved accuracy. Compared to the low-order model the lumped elements are not derived from the impact of the whole winding. Furthermore the structure is sectioned into multiple individual segments with each of them characterized by an equivalent subcircuit. The electrical behavior of the whole inductor results by joining the subcircuits related to the physical structure. For a first approximation the inductor winding can be divided into straight conductor elements and each inductance can be obtained using Greenhouse [Greenhouse 74] and Grover [Grover 46] type calculations. A large collection of inductance approximations can be found in [Wadell 91].

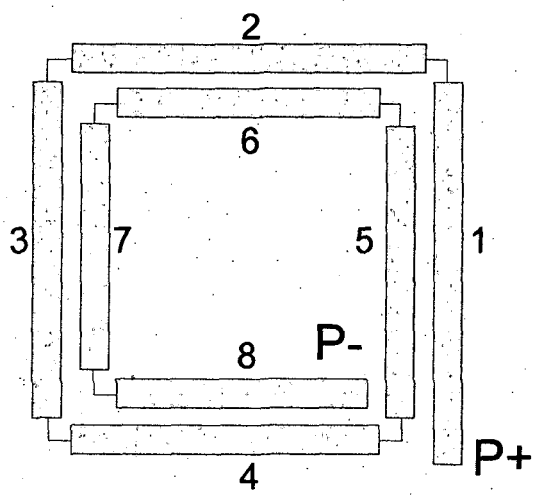


Figure 4.7: Segmentized rectangular spiral inductor.

Figure 4.7 shows such a rectangular spiral inductor divided into 8 segments. Each segment is represented by a similar pi-equivalent circuit as the inductor illustrated in fig. 4.6, except of the capacitor C_L.

All lumped pi-elements are connected in series to get the entire inductor. The capacitive and inductive coupling between the segments is considered with a capacitance between each segment and the coupling factor k between each inductance. The resulting high-order equivalent circuit for the inductor fig. 4.7 can be found in Figure 4.8. Hence this is again a simplification, as only adjacent parallel

segments are considered. Due to the low capacitive coupling to the more outer segments this simplification error can be neglected.

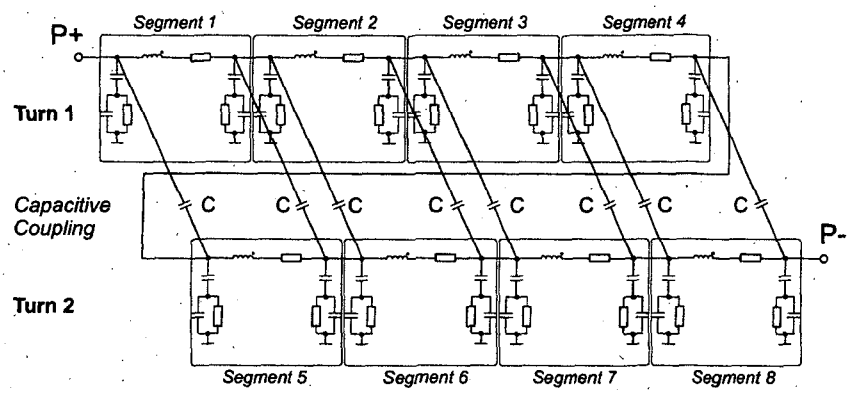


Figure 4.8: Inductor higher-order model.

4.4.4 On-chip transformer design

Transformers have a wide usage in power supply circuits due to their DC blocking and high coupling coefficients. For RF circuits, they can be used for impedance matching with optional BALUN function. The operation of transformers is based upon the magnetic coupling between two windings. Each winding, primary and secondary, has a self inductance L_P, and L_S. The magnetic coupling between the windings is expressed by the mutual-inductance M or the coupling coefficient k with

$$k = \frac{M}{\sqrt{L_P L_S}} \tag{4.6}$$

In case of an ideal transformer this information is sufficient to create an equivalent circuit, shown in Fig. 4.9.

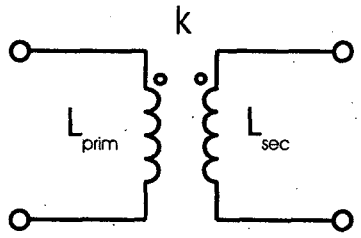


Figure 4.9: Ideal transformer equivalent circuit.

Monolithic transformers suffer from the same loss mechanisms as planar inductors as they are realised by two planar inductor windings. An equivalent low-order

transformer circuit can be determined by using the low-order inductor model fig. 4.6.

Figure 4.10 shows the resulting equivalent low order transformer circuit [Simbürger 00,b, Kehrer 00]. Two low order inductor circuits are placed symmetrically. The magnetic coupling between both windings is represented by the coupling factor k between the two inductances. Parasitic capacitive coupling between the windings is considered by four crossing capacitors C_k. As the capacitive coupling between primary and secondary winding is more dominant compared to the in-winding capacitance, the capacitance C_L has been neglected.

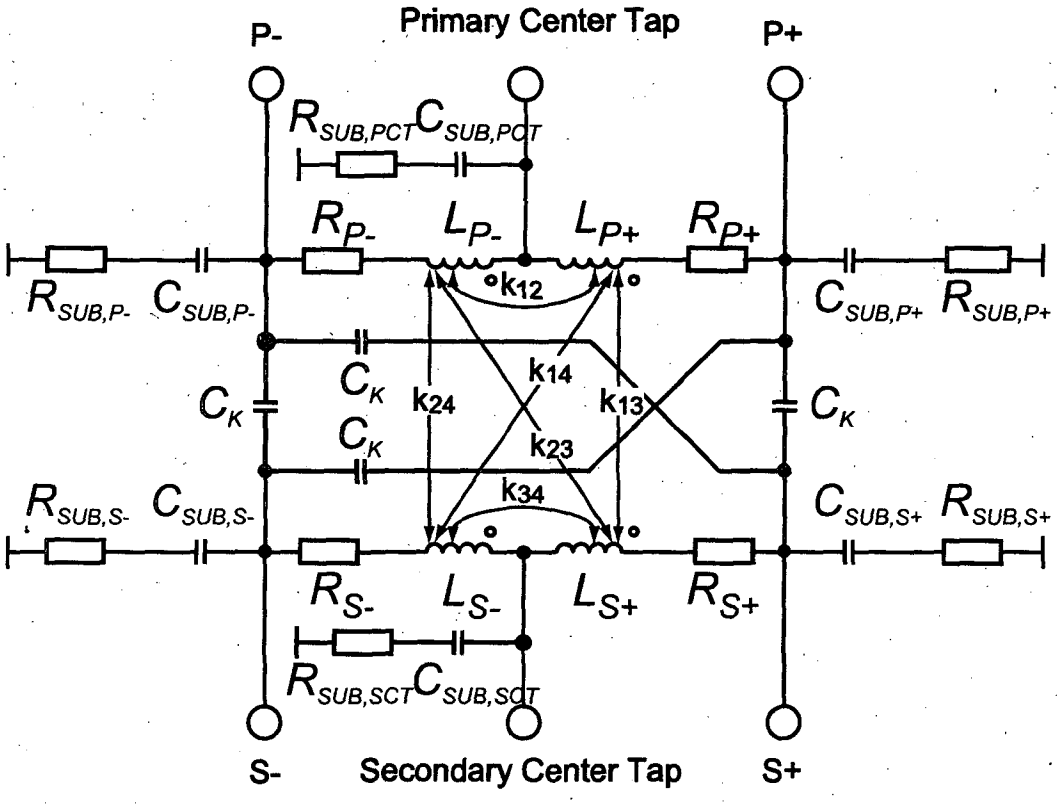


Figure 4.10: The compact transformer model.

This model is a good prediction in frequency range starting up from DC up to about 2/3 of the first self resonant frequency. A higher accuracy can only be obtained using a high order model which can be derived similar to section 4.4.3.

Inductance extraction issues can be found in [Kehrer 01, Kehrer 00, Thüringer 02]. First approximations could be done using Greenhouse [Greenhouse 74] and Grover [Grover 46] type calculations.

4.5 Capacitors

Capacitors are used in integrated circuits for LC-tank tuning, DC-blocking and impedance matching. Depending on the semiconductor technology there exist several available types of capacitors. This should only be a brief overview of the capacitor types used for matching networks, as the variety of usable dielectrics, layout forms is quite large [Hastings 01], und thus there are a lot of capacitors such as the trench capacitor, which are not useful for RF applications due to their high substrate parasitics.

4.5.1 Metal/Metal capacitors

The main idea behind the Metal/Metal capacitor or metalcap is the parallel-plate capacitor. It uses two metal layers from the standard metal stack for its realisation with the silicon oxide as dielectrics (fig. 4.11).

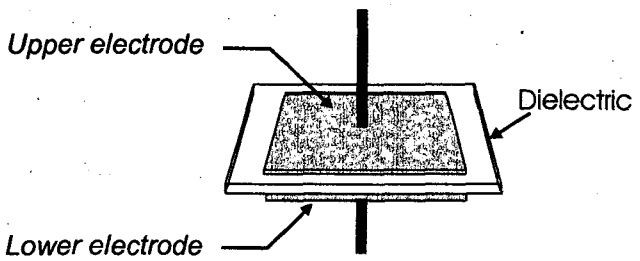


Figure 4.11: A simple parallel-plate capacitor construction.

Its capacitance can be easily determined by

$$C = \varepsilon_r \varepsilon_0 \frac{A}{d} \tag{4.7}$$

with A for the metal plate area and d for the distance between the electrodes. For SiO_2 ε_r is 3.9. Hence the capacitance depends on the technology layer stack and for large capacitors the substrate parasitics have to be considered (fig. 4.12). Hereby C_{ox} represents the silicon oxide (SiO_2) capacitance and R_{sub} and C_{sub} the substrate parasitics. Additional connection inductances have to be considered from the layout. Hence a Metalcap can be realised using two metal layers as in fig. 4.13 or even as interdigital structure using several metal layers.

4.5.2 Metal/Isolator/Metal capacitors

Parallel plated capacitors which use an extra dielectric material layer with a reduced electrode distance d and additional vias for the connection instead of the

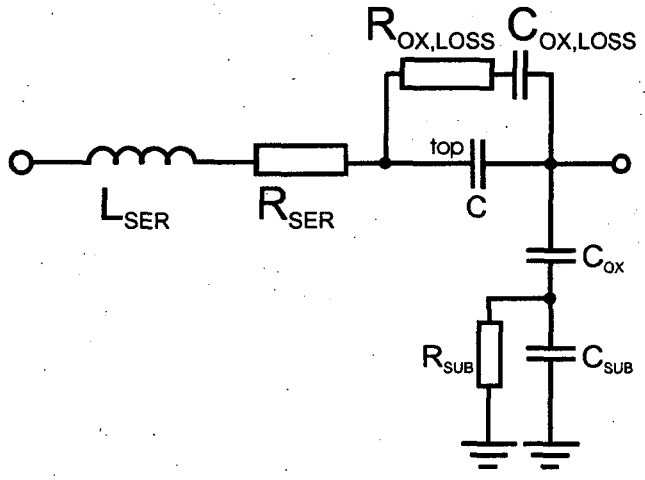


Figure 4.12: A Metalcap equivalent circuit.

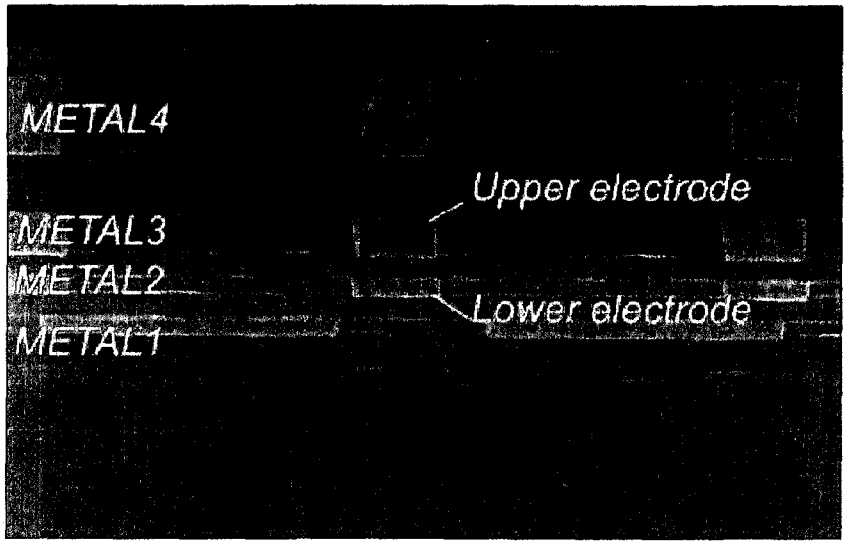


Figure 4.13: A 4 metal layer stack. Metal 2 and 3 build a Metalcap with metal 3 as the upper and metal 2 as lower electrode.

standard metalization are called MIM-caps for Metal-Isolator-Metal capacitors. The reason for doing this is the limited capacitance which can be obtained by the dielectric constant of SiO_2 ($\varepsilon_r = 3.9$) and the distance between the metal layers. Table 4.1 gives the permittivities of the most common dielectric materials used in semiconductor technologies.

MIM-caps are the most often used capacitors in Si-based semiconductor technologies due to their high Q-factors and low dielectric losses [Allers 03]. As mentioned before, MIM-caps are parallel plate capacitors using a thin dielectric material. A

Material	Material permittivity ε_r	Dielectric strength [MV/cm]
Silicon (Si)	11.8	30
Silicon oxide (SiO_2)	3.9	11
Silicon nitride (Si_3N_4)	6.5	10
Aluminia oxide (Al_2O_3)	7.9	16

Table 4.1: Relative permittivities and strengths of selected materials.

TEM micrograph of a MIM-cap with Al_2O_3 dielectric is shown in fig. 4.14. The economic disadvantage of MIM-caps is the need on additional masks for the semiconductor process.

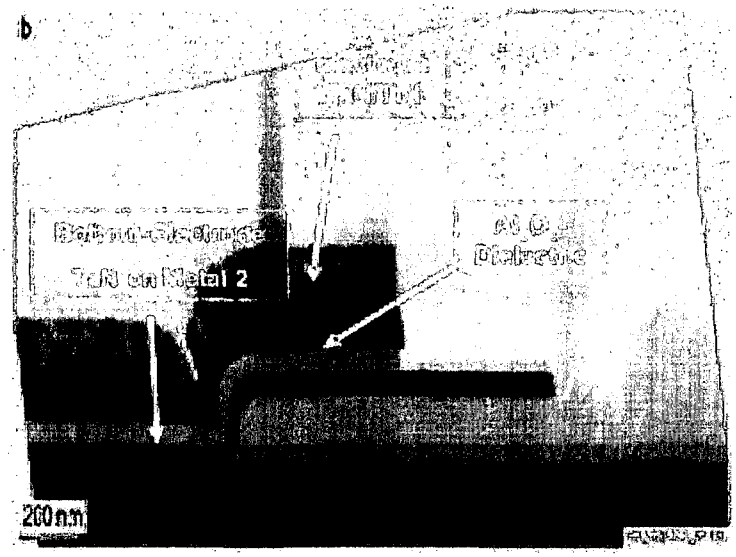


Figure 4.14: A MIM-cap TEM micrograph.

Like all passive elements, MIM-caps are not ideal. Figure 4.15 shows a schematic of the MIM-cap and its equivalent circuit. This equivalent circuit is used for very high accuracy. The most important part of it is the capacitor itself, it is modeled as a voltage dependent device. This dependence is given for the used dielectric material as well as the leakage resistor R_{LEAK}, the dielectric loss ($R_{DIEL,LOSS}$,$C_{DIEL,LOSS}$). Further parameters like the series resistances R_{SER1}, R_{SER2} and the connection inductance L_{SER1} and L_{SER2} depend on the metalization as "outer" capacitor. These parasitics are usually not implemented in simulation packages as they depend on the actual layout. Finally the substrate is considered by the network of C_{SUB}, R_{SUB} and C_{OX}. Further information and data tables can be found in [Allers 03].

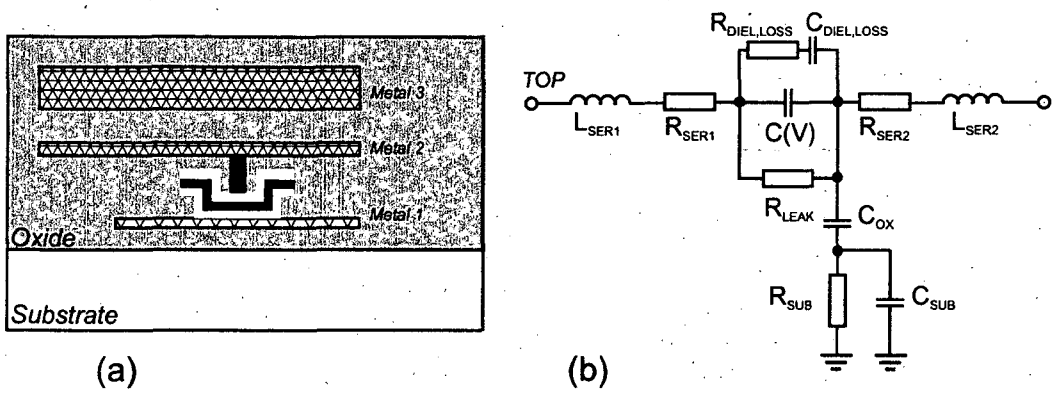


Figure 4.15: (a) The MIM-cap in the die (b) Equivalent circuit.

It has to be mentioned, that for small capacitance values most of the parasitic elements can be neglected due to their extreme small area. Especially when switched in parallel to a transformer, the substrate parasitics from the transformer will dominate, simply because of their much larger area. Hereby it is more important to consider the breakdown voltage of the dielectric material.

4.5.3 MOS capacitors

Metal Oxide Semiconductor (MOS) capacitors base on MOS transistor geometries. A MOS capacitor uses a highly doped Si layer for the lower contact. A thin silicon oxide layer is used as dielectric material. The other electrode is formed either of metal or a doped polysilicon material. Figure 4.16 shows the schematic cross-section of a MOS capacitor for a bipolar technology. Hence it shows why the MOS capacitor has lower performance than a MIM-cap:

- The capacitor is found below the first metal layer. Thus the parasitic capacitance is much higher.
- MOS caps suffer from much higher leakage due to their embedding into the substrate.
- The conductance of the contacting materials such as polysilicon are lower than metal. Thus R_{SER} will be higher.

Today, MOS-caps are more used for RF blocking applications than for matching issues. Like their MIM-cap counterparts, the breakdown voltage has to be considered, and is usually lower due to the thin gate oxide layer. The equivalent circuit can be considered like those of the MIM-cap, with the difference of higher parasitic values and varactors for modeling the voltage dependent capacitance to the substrate.

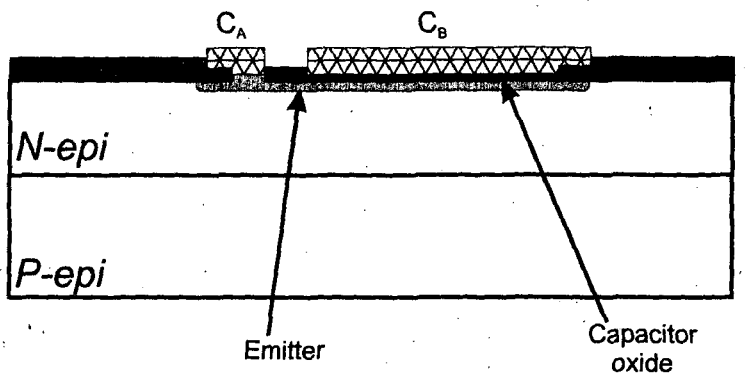


Figure 4.16: Cross-section of a MOS capacitor in a Si-bipolar process.

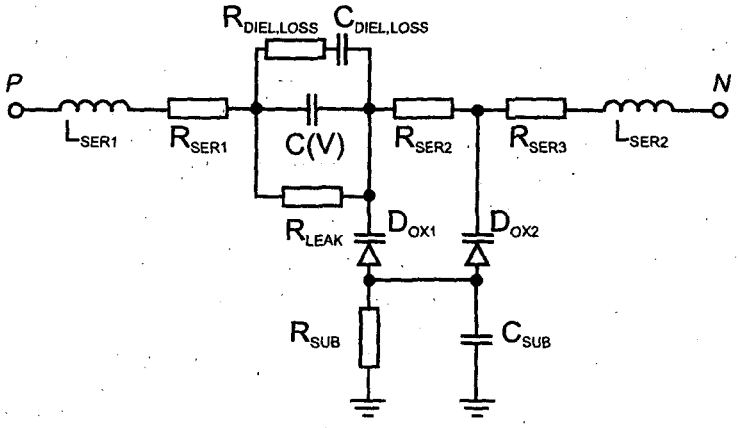


Figure 4.17: Equivalent circuit for a MOS-cap.

4.6 BALUNs

In RF technology, BALUNs (*BAL*ANCED to *UN*BALANCED) play an important role wherever a differential signal has to be connected to unsymmetrical system. They are used to guarantee a transition from coaxial line to the symmetrical two-wire system used for several antennas, such as the dipole and for RF electronics itself, e.g. mixers and push-pull PAs as discussed in section 2.2.2. A BALUN has to fulfil several characteristics:

- Precise 180^o phase shift must be maintained between the two terminals of the symmetrical port.
- In PAs, the impedance presented to the symmetrical port must be equal. If this is not the case, then there will be a decrease in the efficiency.
- The symmetrical port must be well isolated from earth. This is especially important for PAs, since parasitic oscillations can occur.

- The insertion loss should be kept as low as possible.

The basic idea behind the construction of a BALUN can easily be outlined. Two signals 180^o out of phase (symmetrical port) are "synchronised" in their phases and their outputs added. Many designs involving $\lambda/4$ phasing lines (90^o) and $\lambda/2$ phasing lines (180^o) have been developed out of this basic idea. A good overview of various types of BALUNs can be found in [Bakalski 02,d, Bakalski 02,a, Krischke 95, Johnson 84, Mongia 99]. The most important used in the PA designs are found in the following subsections.

4.6.1 The lumped LC-BALUN

Fig. 4.18 shows a lumped LC-BALUN, which was originally used as an antenna BALUN [Cripps 99, Krischke 95, Vizmuller 95]. It is also known as the Lattice-type BALUN [Johnson 84]. The bridge-type circuit consists of two inductors $L_1 = L_2$ and two capacitors $C_1 = C_2$. A RF-choke coil and a DC-block capacitor are used to feed the supply voltage.

R_1 is the balanced input impedance of the bridge. Each collector is loaded by $R_1/2$. R_L is the load resistor, $50\,\Omega$ usually.

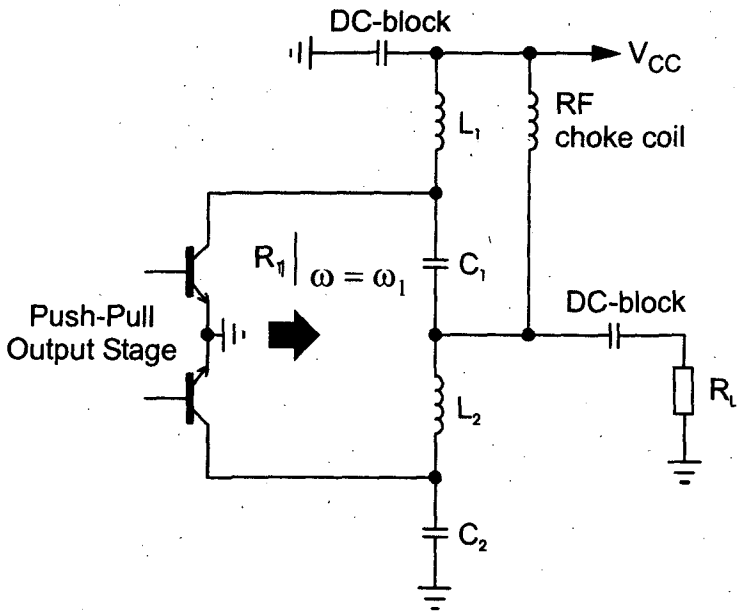


Figure 4.18: The lumped LC-BALUN.

L and C can be calculated by

$$L_1 = L_2 = \frac{Z_1}{\omega_1}, \tag{4.8a}$$

$$C_1 = C_2 = \frac{1}{\omega_1 Z_1} \tag{4.8b}$$

where $Z_1 = \sqrt{R_1 \cdot R_L}$ is the characteristic impedance of the bridge-type circuit. $\omega_1 = 2\pi f_1$ is the frequency of operation. R_1 and Z_1 are assumed to be real valued. If R_1 should be complex valued, matching is possible, but then the bridge becomes more or less imbalanced ($C_1 \neq C_2$ and $L_1 \neq L_2$). Further, at the harmonic frequencies the BALUN becomes also imbalanced.

4.6.2 The microstrip line BALUN

The four lumped elements of the LC-BALUN in fig. 4.18 can be substituted by transmission lines. L1, L2 and C2 were substituted by transmission lines while C1 remains as a lumped element. Figure 4.19 shows the BALUN layout for f = 2.4 GHz for a substrate with a thickness of 0.51 mm and an ε_r of 3.38 [Bakalski 02,e]. The radial stub is not necessary if it is replaced by a RF bypass capacitor. However, the radial stub is a good RF short-circuit [Agilent 88, Vinding 67].

The necessary equations in addition to the [Hammerstad 75] formulas are given by:

$$\omega L_1 = Z_0 \tan\theta \quad , \quad \theta \leq \frac{\pi}{2} \tag{4.9}$$

$$\omega L_2 = Z_0 \sin\theta \quad , \quad \theta \leq \frac{\pi}{2} \tag{4.10}$$

$$\omega C_2 = \frac{\tan\theta}{Z_0} \quad , \quad \theta \leq \frac{\pi}{2} \tag{4.11}$$

with $\frac{\pi}{2} \mathrel{\hat{=}} \frac{\lambda}{4}$ and λ as wavelength [Mongia 99]. Designing such a BALUN starts by calculating L and C using eqn. 4.8. Next step is the substitution of the lumped elements by transmission lines (Eqns. 4.9 - 4.11). C1 is not substituted for the reason, that a long transmission line larger than $\lambda/4$ would be necessary. This would lead to a narrow bandwidth and large outer dimension for low frequencies.

This BALUN structure shows several advantages to the standard LC-BALUN solution:

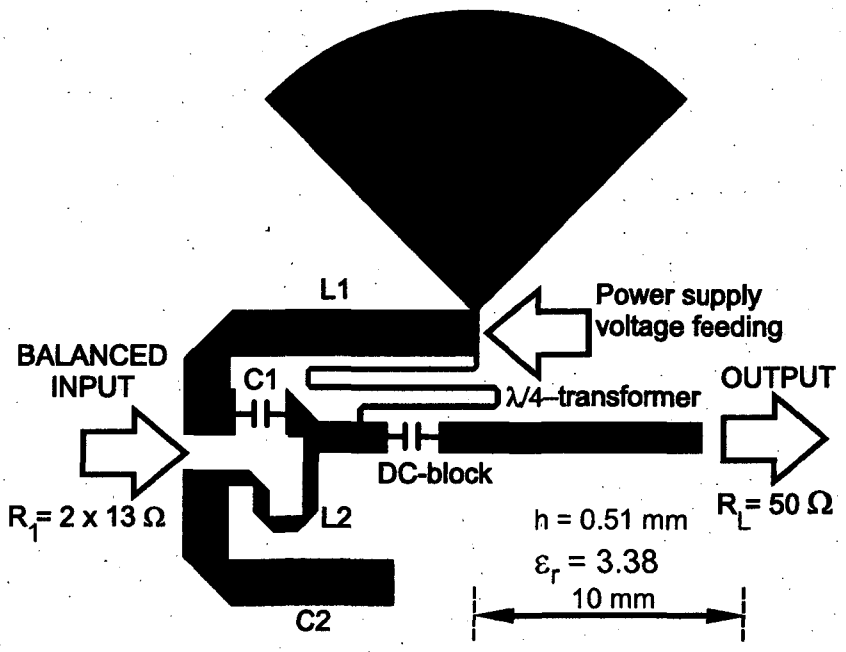


Figure 4.19: Microstrip line BALUN for 2.45 GHz and a substrate with a thickness of 0.51 mm and $\varepsilon_r = 3.38$.

- Only one lumped element is required.
- The use of transmission lines gives two variables per element to adjust the outer dimensions. However this complicates the design procedure and requires simulation tools.
- The second harmonic load impedance shows very low input impedances while the third harmonic load impedance shows very high impedances. Especially for nonlinear operation this leads to high efficient amplifiers [El-Hamamsy 94].
- The outer dimensions are significantly smaller than other microstrip based BALUNs [Raicu 98].

Fig. 4.19 shows the layout of such a BALUN. It was designed for a center frequency of 2.45 GHz and a load impedance of 26 Ω. Figure 4.20 shows the simulated results for fundamental, second and third harmonic frequency.

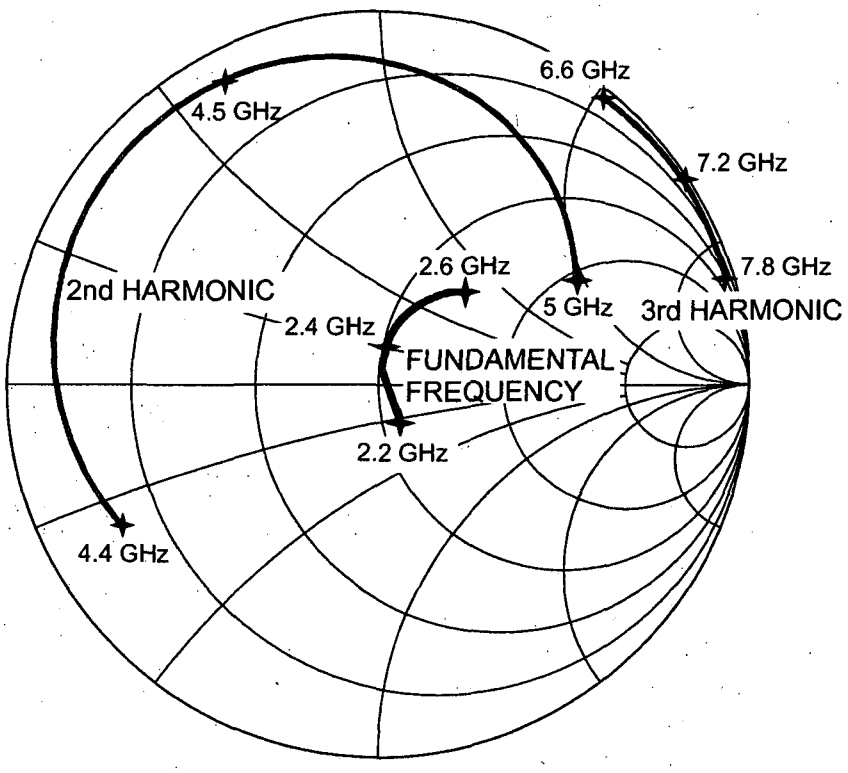


Figure 4.20: Simulated results for the load impedance at the fundamental frequency of 2.45 GHz and the second and third harmonic frequency for $Z_0 = 26\,\Omega$.

4.6.3 The lumped dual band LC-BALUN

For dual band applications an extension can be made: If the inductors are replaced by a parallel resonant circuit and the capacitors are replaced by a series resonant circuit as shown in fig. 4.21, then a lumped dual-band LC-BALUN, shown in fig. 4.22, is available.

The circuit provides a balanced input impedance R_1 at $\omega_1 = 2\pi f_1$ and R_2 at $\omega_2 = 2\pi f_2$. Independent matching and BALUN conversion at two different frequencies can be done. L_S, C_S, L_P and C_P can be calculated by

$$L_S = \frac{\omega_1 \cdot Z_1 + \omega_2 \cdot Z_2}{\omega_2^2 - \omega_1^2} \tag{4.12}$$

$$C_S = \frac{\frac{\omega_2}{\omega_1} - \frac{\omega_1}{\omega_2}}{\omega_1 \cdot Z_2 + \omega_2 \cdot Z_1} \tag{4.13}$$

$$L_P = \frac{\left(\frac{\omega_2}{\omega_1} - \frac{\omega_1}{\omega_2}\right) \cdot Z_1 \cdot Z_2}{\omega_1 \cdot Z_1 + \omega_2 \cdot Z_2} \tag{4.14}$$

$$C_P = \frac{\omega_1 \cdot Z_2 + \omega_2 \cdot Z_1}{(\omega_2^2 - \omega_1^2) \cdot Z_1 \cdot Z_2} \tag{4.15}$$

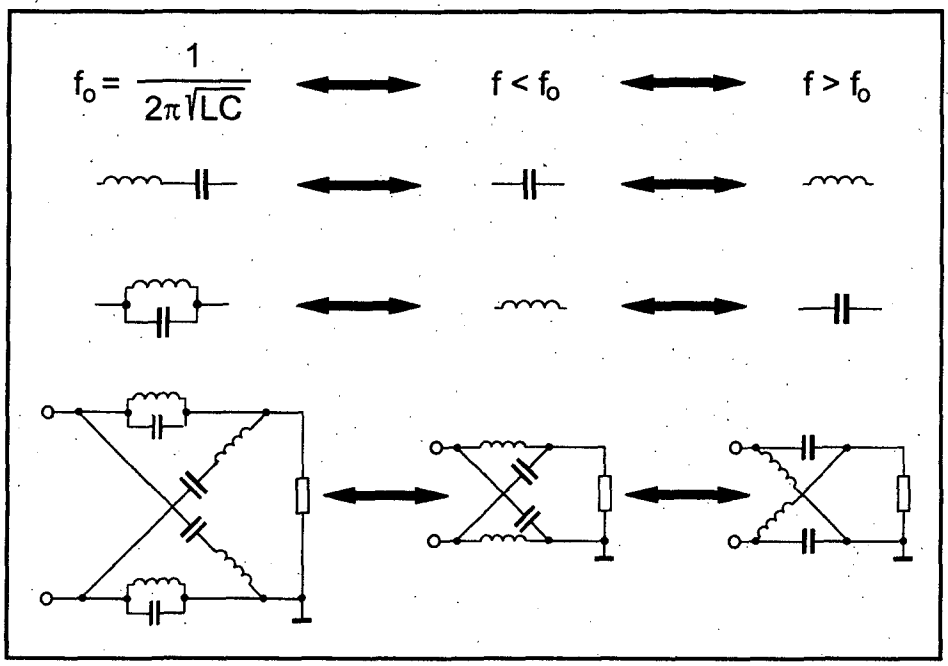


Figure 4.21: Behavior of the dual-band LC-BALUN with the frequency.

where $Z_1 = \sqrt{R_1 \cdot R_L}$ and $Z_2 = \sqrt{R_2 \cdot R_L}$ are the characteristic impedances of the bridge at ω_1 and ω_2. R_1, R_2, Z_1 and Z_2 are assumed to be real valued. Note, that

$$\omega_2 > \omega_1 \tag{4.16}$$

is a must, using the design equations above.

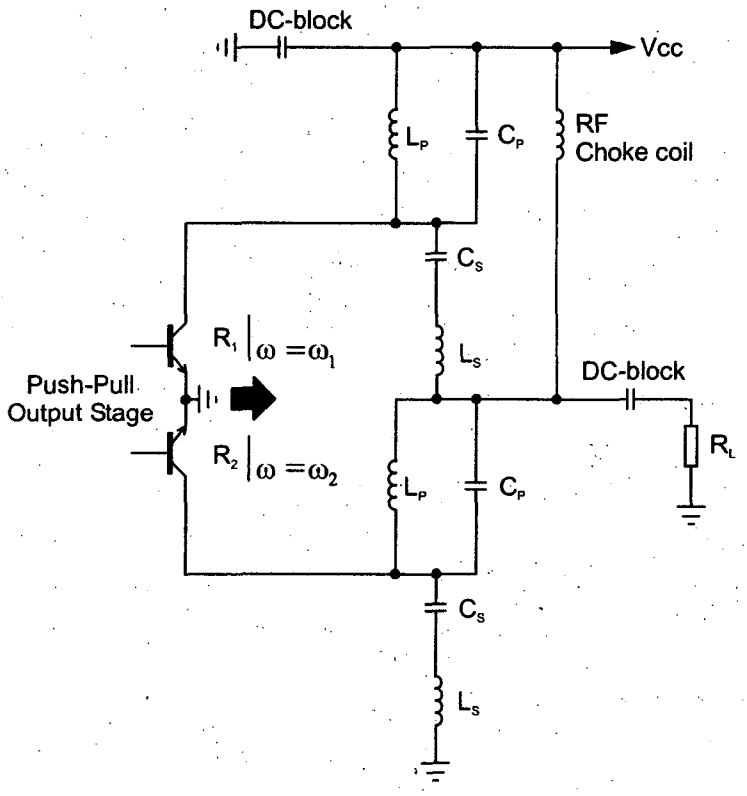


Figure 4.22: The dual-band lumped LC-BALUN.

Chapter 5

Highly efficient 2.45 GHz ISM power amplifier

The frequency band between 2.4 and 2.5 GHz is used for most different applications. Fixed for an Industrial, Scientific and Medical (ISM) use, we find here several applications in parallel:

- *Bluetooth:*[1] A standard technology for low-cost, low power short range wireless communication. First specified in 1999 (Version 1.0) several promotor companies build up the Bluetooth Special Interest Group (SIG) [BT SIG]. The actual Bluetooth specification Version 1.1 uses the frequency range location of $f = (2402 + k)MHz, k = 0, ..., 78$ for the majority of the countries around the world. Bluetooth uses frequency hopping spread spectrum (FHSS) with 1 MHz of frequency spacing. There exist three power classes for Bluetooth: Class 1 with 100 mW (20 dBm), Class 2 with 2.5 mW (4 dBm) and Class 3 with 1 mW (0 dBm) output power at the PA output. Considering any output filtering and antenna switches, the necessary output power of the PA can rise up to 23 dBm and more. Bluetooth amplifiers are operated in 625μs time slots which can be lengthened up to 5 slots. Thus the amplifier is operated in pulsed mode such as in GSM 900 MHz power amplifiers. Furthermore Bluetooth features maximum data throughput up to 1 Mbit/s.

- *Wireless LAN:* There exist several Wireless LAN standards, all starting with IEEE 802.11x. In the 2.4 GHz band, the most popular WLAN standard is IEEE 802.11b. It features a maximum throughput of 11 Mbit/s and uses a Direct Sequence Spread Spectrum (DSSS) modulation. Like coaxial cable based Ethernet IEEE 802.3 (10Base-2), it uses Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA). It is found between

[1]The name is from the 10th century Viking King Harald Bluetooth. The first feasibility studies came up at Ericsson in 1994.

2.4 and 2.483 GHz with 3 channels of each 11 Mbit/s allowing a maximum of 192 users. Dependent on the country, the allowed maximum output is 1 W (30 dBm) for the United States, 0.1 W (20 dBm) for Europe and only 0.01 W/1MHz (10 dBm) in Japan. Furthermore, the data throughput can be reduced to 5.5, 2 and 1 Mbit/s using different modulation schemes: *D*ifferential *B*inary *P*hase *S*hift *K*eying (DBPSK - 2 symbols due to 180° phase shift) for 1 Mbit/s and *D*ifferential *Q*uadrature *P*hase *S*hift *K*eying (DQPSK - 4 symbols due to 90° phase shift) for 2 Mbit/s.

- *Cordless Phones:* In the U.S. DECT-like cordless phone standards are found in the 2.4 GHz frequency band with similar requirements as in the European counterpart.
- *Wireless Audio/Video Connection Systems*
- *Movement Detection Systems*
- *Unspecified short range transmitters*
- *13cm Amateur Radio:* Testing and sporadic operation in different modulation schemes (digital as well as standard Frequency Modulation, Single-Side Band etc.)

5.1 PA design overview

Every power amplifier should behave as ideal as possible. Besides a high efficiency, also a wide bandwidth is preferable as well as small die size, high gain and depending on the modulation scheme, the linearity. The amplifier presented here, was designed with a focus on high efficiency at low supply voltages, preferably for 1-cell battery operation (1.5 V) and a frequency range as wide as possible, mainly to be able to cover all DECT standards with one die at the same time as for example Bluetooth applications. Figure 5.1 shows the chip photograph of the PA die. Its size is $1.4 \times 0.9\,\mathrm{mm}^2$.

Fig. 5.2 shows the circuit diagram of the PA. The circuit consists of a transformer X1 as input BALUN, a driver stage T1 and T2, a transformer X2 as interstage matching network and the output stage T3 and T4. The bias of the driver stage and the output stage are set by current mirrors D1 and D2, respectively.

The SiGe bipolar technology used is similar to Infineons 0.35 μm, 72 GHz/ 75 GHz (f_t/f_{max}) volume production process which is described in Chapter 3 and [Klein 99, Wolf 01]. Slight process modifications to obtain optimum power amplifier performance and robustness included a reduced SIC implantation dose and profile, improved boron and germanium profiles in the base and lower parasitic subcollector resistances. The devices have transit frequencies and maximum oscillation frequencies in the range of 30 GHz and 50 GHz, respectively. The collector-base

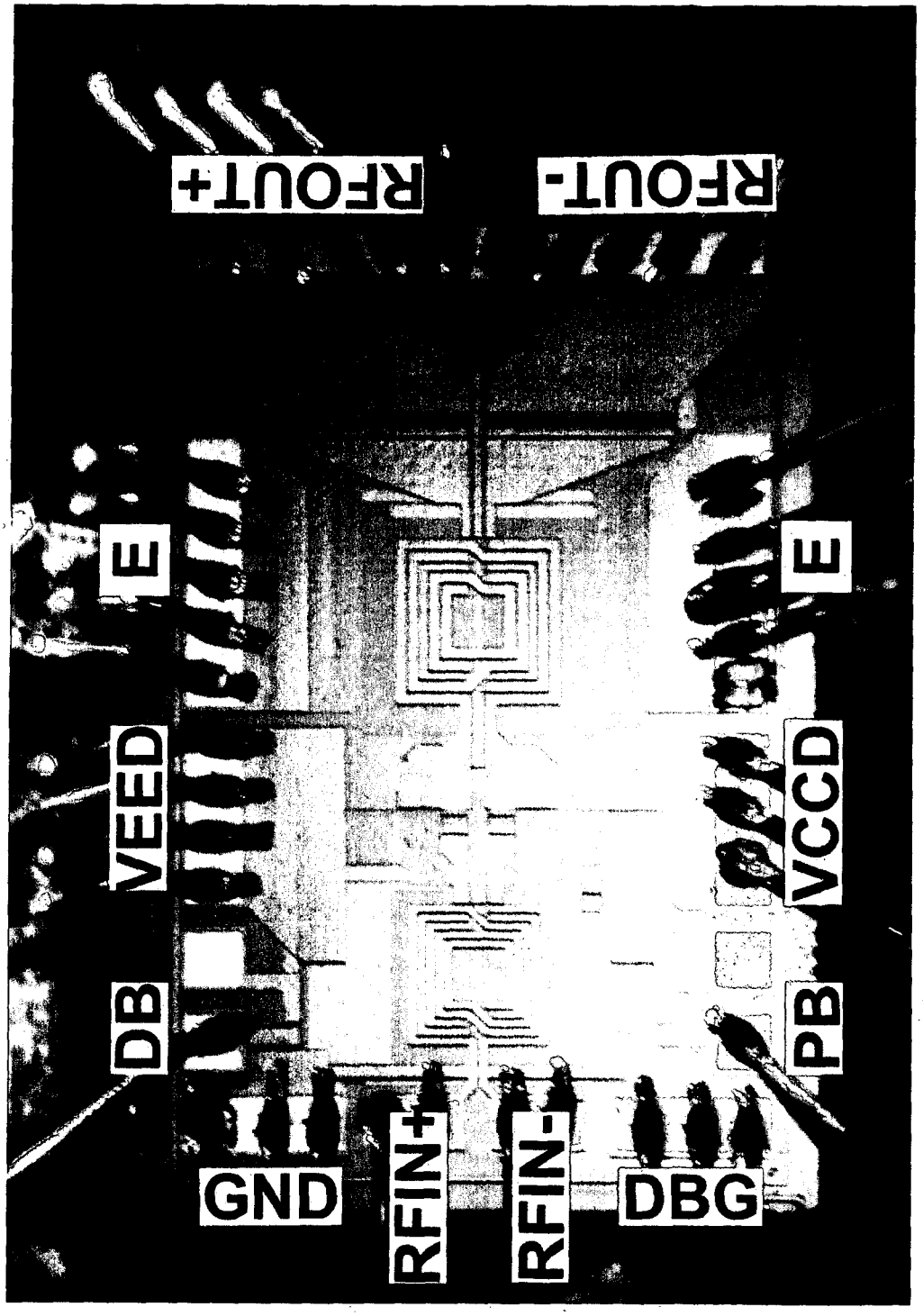


Figure 5.1: The 2.4 GHz ISM PA die (size: $0.9 \times 1.4\,\mathrm{mm}^2$)

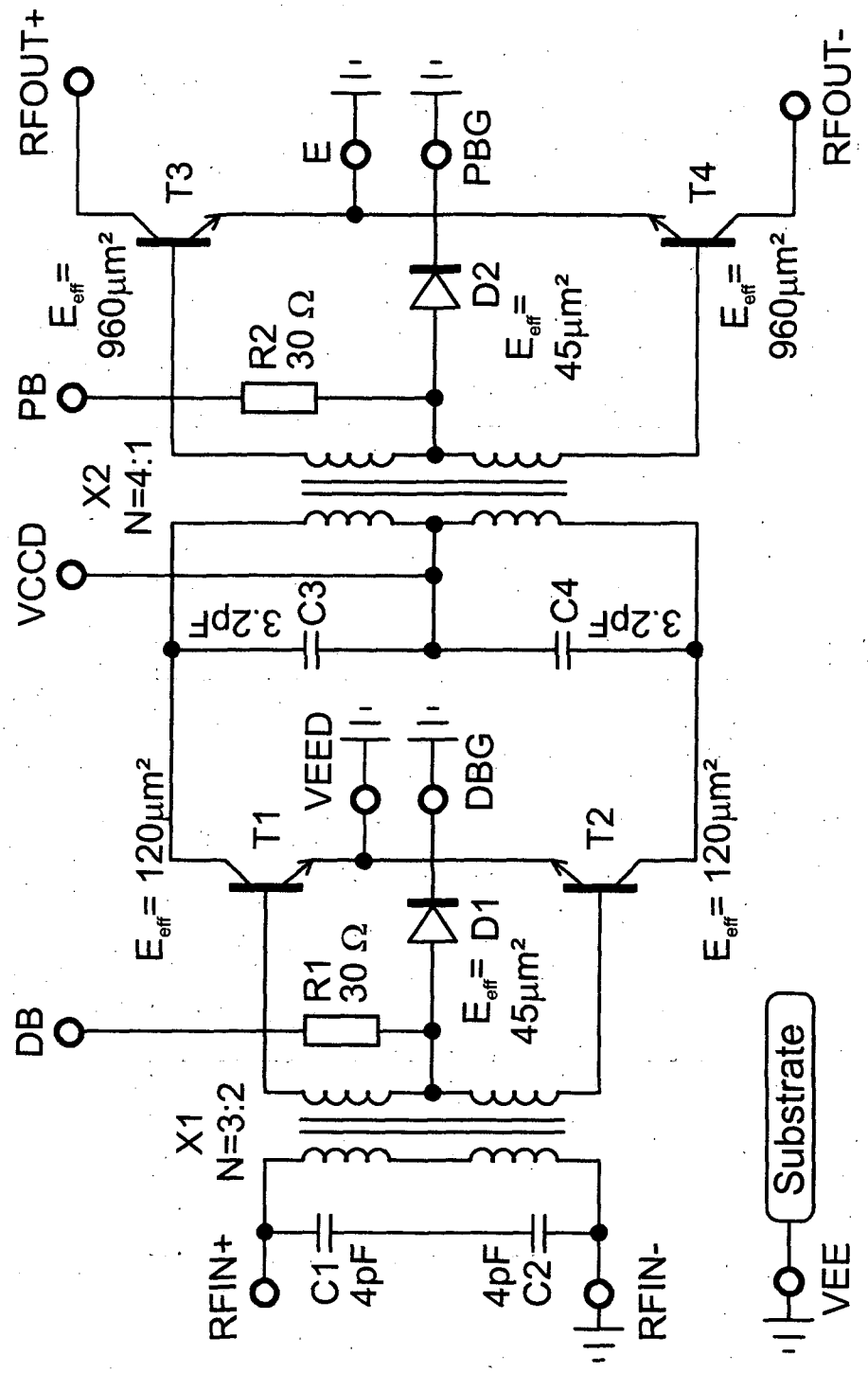


Figure 5.2: The push-pull PA circuit diagram. The used transformers operated as LC tanks are stressed in yellow.

breakdown voltage is $BV_{CB0} = 16.6\,V$ and the collector-emitter breakdown voltage is $BV_{CE0} = 5.6\,V$ being above the typical production technology values of $BV_{CB0} = 8\,V$ (typical: 10 V) and $BV_{CE0} = 2.3\,V$ (typical: 2.8 V) as presented in section 3.7.

5.2 Input stage design

Beginning with the input section we find the input transformer X1. Its 3D view is sketched in fig. 5.3 while its winding scheme is sketched simplified in fig. 5.4.

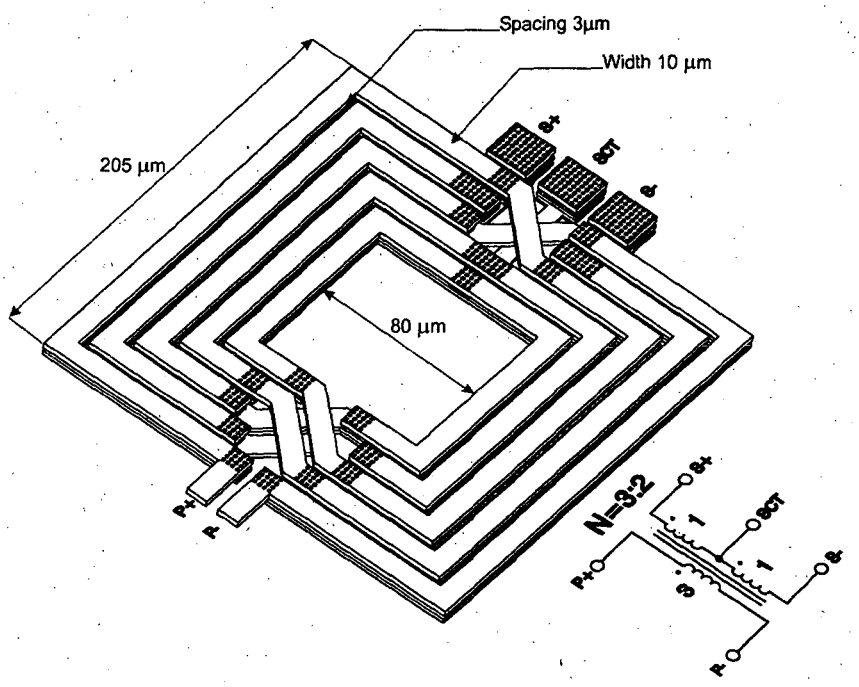


Figure 5.3: Input power transformer X1: 3D View and schematic symbol

X1 is connected as a parallel resonant device with the input MIM capacitors C1 and C2 (see section 4.5.2). The transformer acts as a BALUN as well as an input matching network. In addition there are several advantages:

- No restrictions to the external DC potential at the input terminals.
- No external DC-block capacitor required.
- The input signal can be applied balanced or unbalanced if one input terminal is grounded. Due to the fact, that most transceiver chips are based on differential-type designs, an external BALUN is no more necessary.

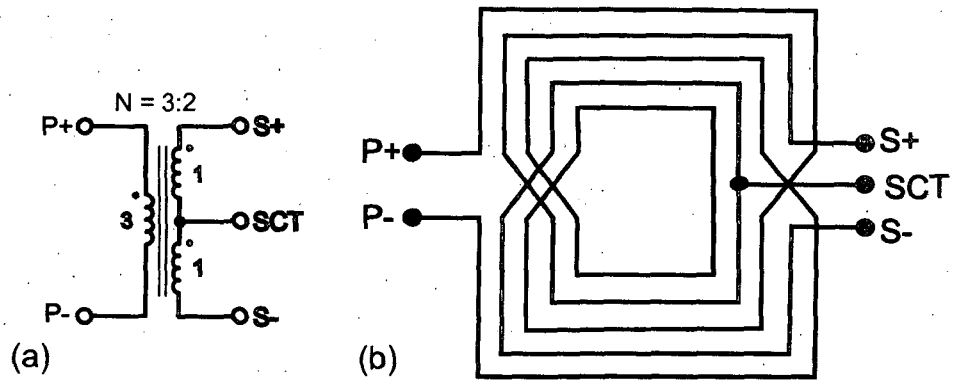


Figure 5.4: Input power transformer X1: (a)schematic symbol (b) winding scheme

- Relaxed electrostatic device requirements. If the primary winding is dimensioned thick enough, e.g. 10 μm, an average (!) DC current of typically 50 mA is allowed [2]. Thus the peak current can be applied much higher.

The dimension of the input transformer has two major targets:

- Realisation of the input matching. For this, it is important to know the necessary input impedance as well as the used packaging, as this has got a strong influence due to the bond wire length, the amount of bondwires, implying an additional input impedance. Furthermore if a differential input is wanted, the packaging has to consider this. However, the input section can be simulated using the fig. 5.5 equivalent circuit at the input. Another problem regarding the input matching are the input bond pads. They are modeled by a capacitor with a resistance in series to ground, due to the limited conductance of the substrate. Usually they do not affect the matching for low frequencies, but they become a dominating factor when reaching frequencies in the range of over several 10 GHz. Their influence can be simulated very easy by the use of a smith chart. The MIM caps in fig. 5.5 are sketched as ideal capacitors, as their parasitics can be neglected due to their small outlines compared to the transformer they are connected with.

- Feeding the driver transistors T1, T2 with the bias current and sufficient RF base current. The transformer does this by transforming the impedance from 50 Ω down to a fractional value. Furthermore the center tap is used for the biasing, with the advantage, that the necessary choke coils are now integrated in the transformer. The center tap features a low DC resistance to the base of the driver transistors, an advantage for biasing circuits, so that this influence can be mostly neglected.

[2]For 100° operation with 2.8 μm thick Al metalization (Infineon B7HF specification).

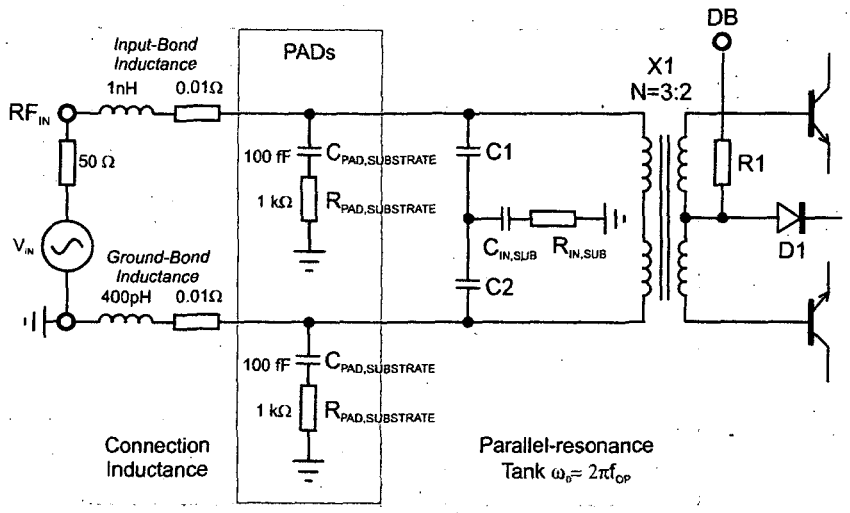


Figure 5.5: Input equivalent circuit used for simulations for the input matching, biasing and tuning of the tank resonance frequency.

With the knowledge of the necessary values for in- and output impedance, a winding type for the transformer can be selected. Furthermore, the outer dimensions of the transformer relate to the maximum current density allowed for the metalization, the substrate capacitance and the parasitic capacitances C_{BC} and C_{BE} of the driver transistor. The capacitors C1 and C2 in fig. 5.5 and fig. 5.2 are used for tuning the transformer to the operating frequency. In theory, they could be eliminated by the substrate capacitance, but this would make the complete design having a strong dependence on a certain substrate type and will lead to problems for the case of process variations. Thus the amplifier could behave unstable.

Another problem in observing the right input impedance is the often missing large-signal S-Parameter simulation. Usually most tools offer only a small signal S-Parameter extraction, which is not satisfying for amplifiers operated in saturated mode such as GSM-PAs. As transistors are in fact never unilateral, the input matching for relatively high input power, such as 10 dBm has to be considered. A simple work-around could be realised by adding a 50 Ω input resistor between signal generator and power amplifier (fig. 5.6). If the input voltage drops by the half, the optimum input matching is reached. It has to be mentioned, that some simulators feature an AC-source with integrated 50 Ω resistance.

For the design of the input transformer, the input impedance on the bases of the driver stage transistor can be simplified as a short circuit for the transformer, as the input impedance of the large BJTs and HBTs are typically very low. Fig. 5.8 shows a secondary short-circuit transformer. It consists of a primary winding L_p and a secondary winding L_s. L_p and L_s are mutually coupled, denoted by the coupling coefficient $k = M/\sqrt{L_p \cdot L_s}$, where M is the mutual inductance. The ohmic loss of the primary winding L_p, ohmic loss of the secondary winding L_s

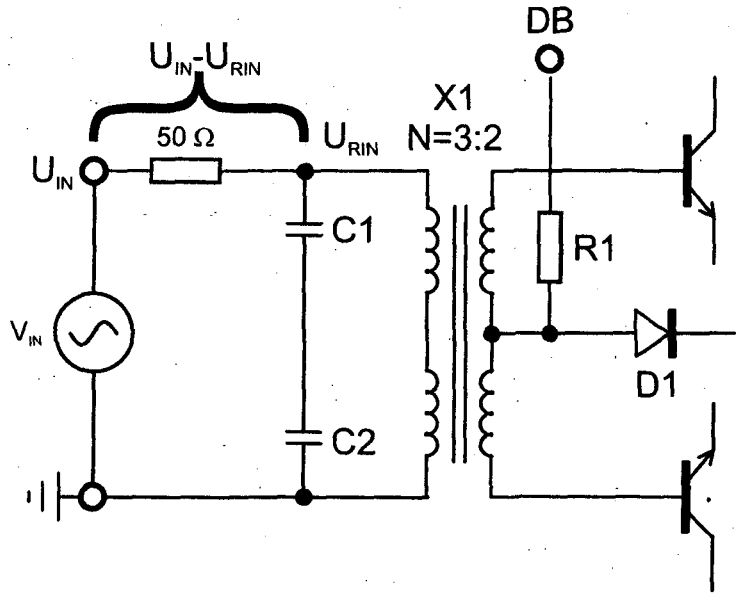


Figure 5.6: Method of simulating the correct input impédance by adding a resistor with the same value as the target Z_{IN}.

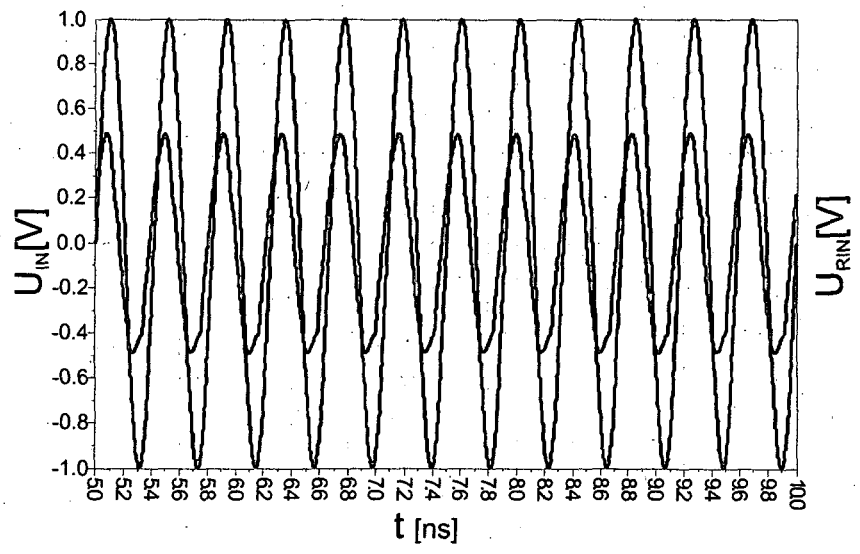


Figure 5.7: Voltage drop on a 50 Ω series resistor to determine input mismatch. For ideal 50 Ω the amplitude should be half of the input voltage, and the phase deviation as near to 0^o as possible.

and the input impedance of the transistors (assumed real valued) are considered by the admittance G. The transformer is connected as a parallel resonant device using the capacitor C.

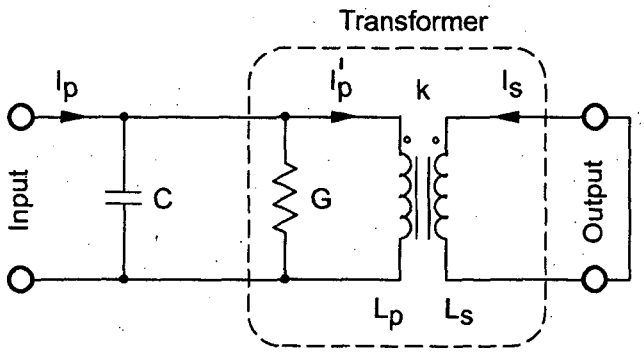


Figure 5.8: Tuned ideal transformer equivalent circuit.

Then the resonant frequency ω_{res} of the tuned transformer can be derived as

$$\omega_{res} = \frac{1}{\sqrt{(1-k^2)\cdot C\cdot L_p}} \tag{5.1}$$

The quality factor Q of the resonant circuit is

$$Q = \frac{\omega_{res}\cdot C}{G} = \frac{1}{G}\cdot\sqrt{\frac{C}{(1-k^2)\cdot L_p}} \tag{5.2}$$

The inner current transfer ratio of the ideal transformer is

$$\frac{I_s}{I'_p} = -k\cdot\sqrt{\frac{L_p}{L_s}} \tag{5.3}$$

Now the total current transfer ratio I_s/I_p of the parallel resonant transformer can be expressed by

$$\left|\frac{I_s}{I_p}\right| = k\cdot Q\cdot\sqrt{\frac{L_p}{L_s}} \tag{5.4}$$

This relation shows that in contrast to the untuned transformer, the total current transfer ratio can be increased by a quality factor of $Q > 1$. The capacitor C in fig. 5.8 corresponds to C_1/C_2 and C_3/C_4 in fig. 5.2 respectively.

Fig. 5.3 shows the input transformer X1 in a three dimensional view. Its winding scheme is found in fig. 5.4. The turn ratio X1 is N=3:2. The size is $205 \times 205\,\mu m^2$. The primary winding consists of 3 turns. Al 3 and Al 2 are connected in parallel to decrease the ohmic loss (see metal layer stack in fig. 3.19). Al 1 is not used to reduce parasitic substrate coupling of the primary winding. Both turns of the secondary winding use also Al 3 and Al 2 connected in parallel. The total coupling coefficient is k = 0.8 at 2.45 GHz. The transformer is modeled by a SPICE equivalent circuit (fig. 5.9) at f = 2.45 GHz. The modeling issues of monolithic transformers are presented in section 4.4 and in [Cheung 98, Long 00, Kehrer 01].

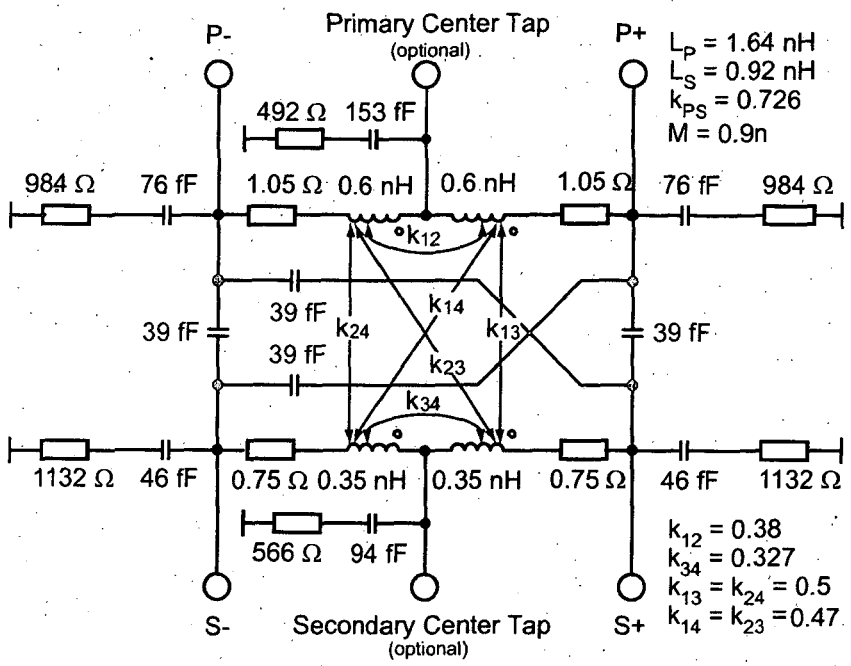


Figure 5.9: Input transformer X1: SPICE model.

The simulation results of the transformer modeling tool FastTrafo [Thüringer 02] are presented in figures 5.10, 5.11, 5.12. The resulting SPICE model is shown in fig. 5.9.

The parallel resonance is tuned by the input capacitor as well as the input matching. Figure 5.13 shows the resonance in the frequency range between 2 and 2.5 GHz, thus the wanted operating frequency range.

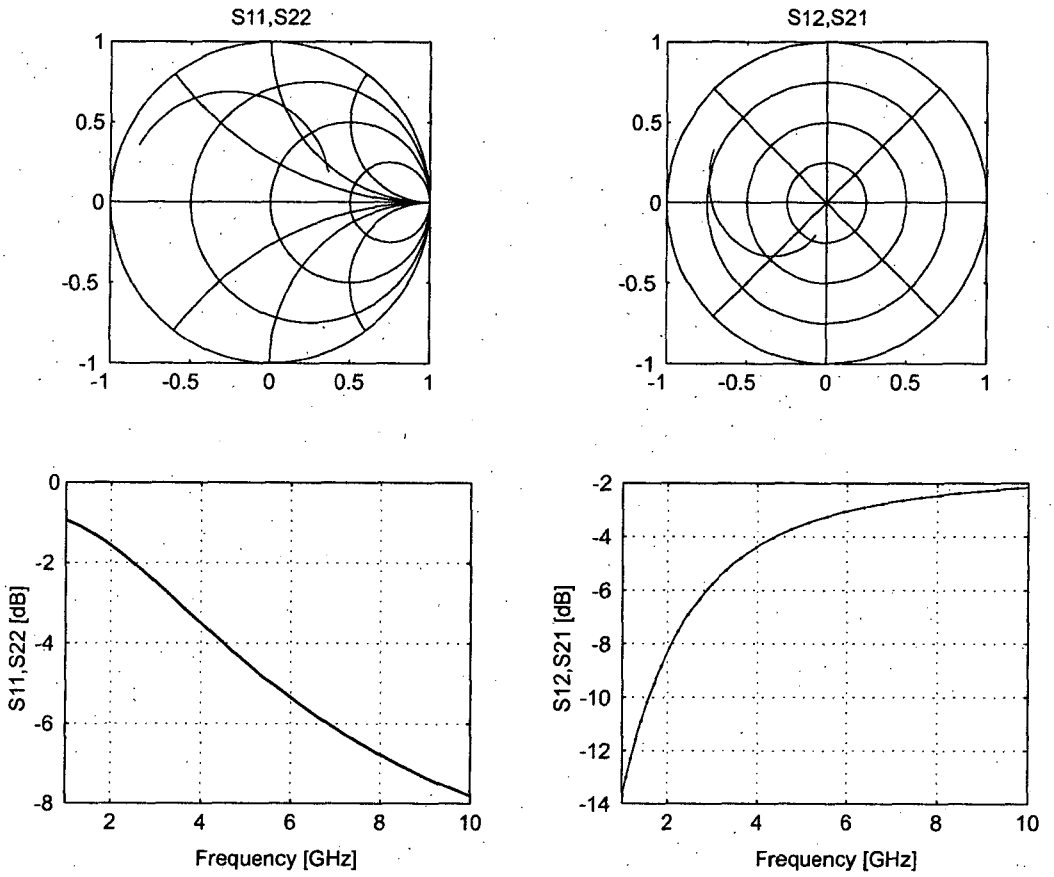


Figure 5.10: S-Parameter simulation results of the input transformer using Fast-Trafo.

5.3 Interstage section

The interstage section describes the driver stage together with the interstage transformer. The design of the interstage transformer is mainly like the input section, but with the big difference that it has a strong influence in the circuit performance. Its design depends on the following factors:

- The area of the output transistor. The output stage is usually dimensioned by the desired output power. Hence the necessary transistor area, usually characterized by the effective emitter area implies a low input impedance. This is caused by the large capacitance C_{BE} as well as C_{BC} and the needed base current due to the limited current gain β.

- The selected substrate and the transformer metalization. If the semiconductor technology features thick Al or better thick copper metalization, the

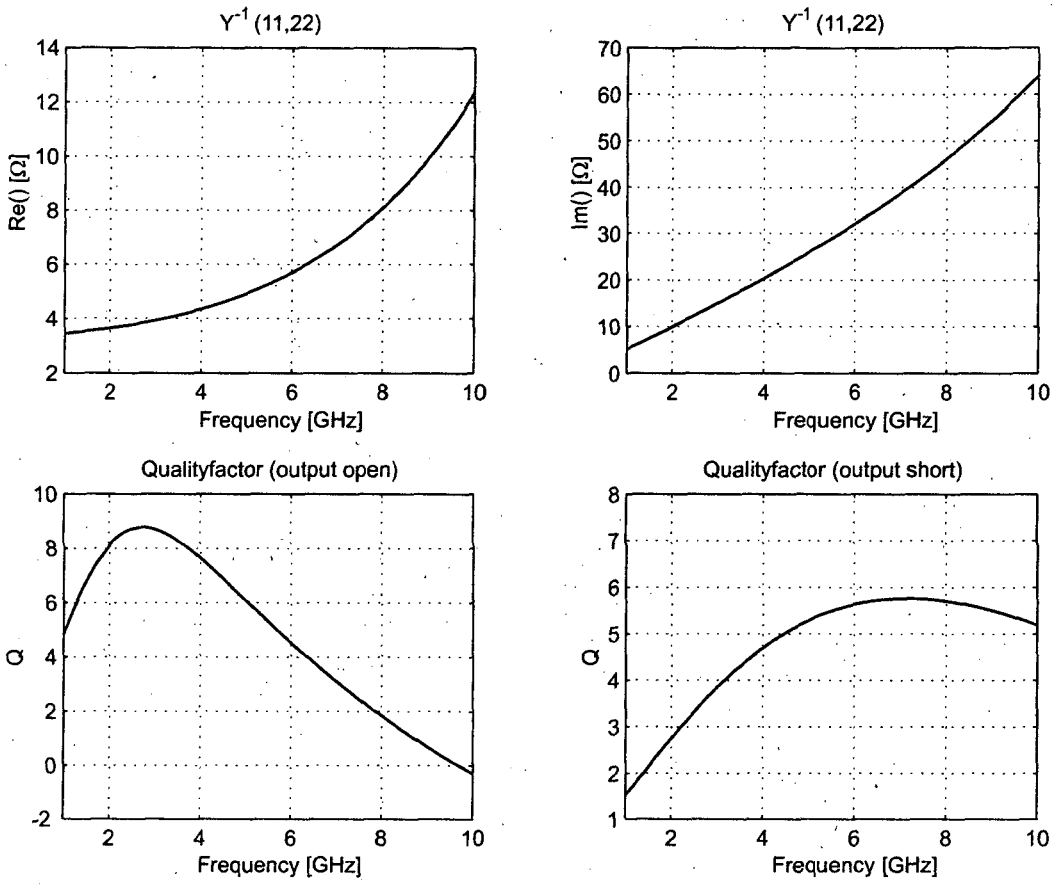


Figure 5.11: Y^{-1}-Parameter simulation results of the input transformer using FastTrafo.

substrate parasitics can be reduced as for the same current density smaller trackwidths can be selected.

- The size of the driver stage transistor area is limited, as for large driver stage transistors the C_{BE} may become too large, so that the interstage transformer tank can no more be tuned to resonance.

This shows, that the design of the amplifier requires some iterations, as there are a lot of unknown parameters for the transformer design and transistor area in addition they depend on each other. The typical way of the amplifier design is to calculate the necessary emitter area for a specified saturated output power and the given supply voltage. Let us assume the output power to be 0.4 W (26 dBm) in saturation at a supply voltage of Vcc = 2 V.

For a single ended configuration, the necessary ideal output load would be given by

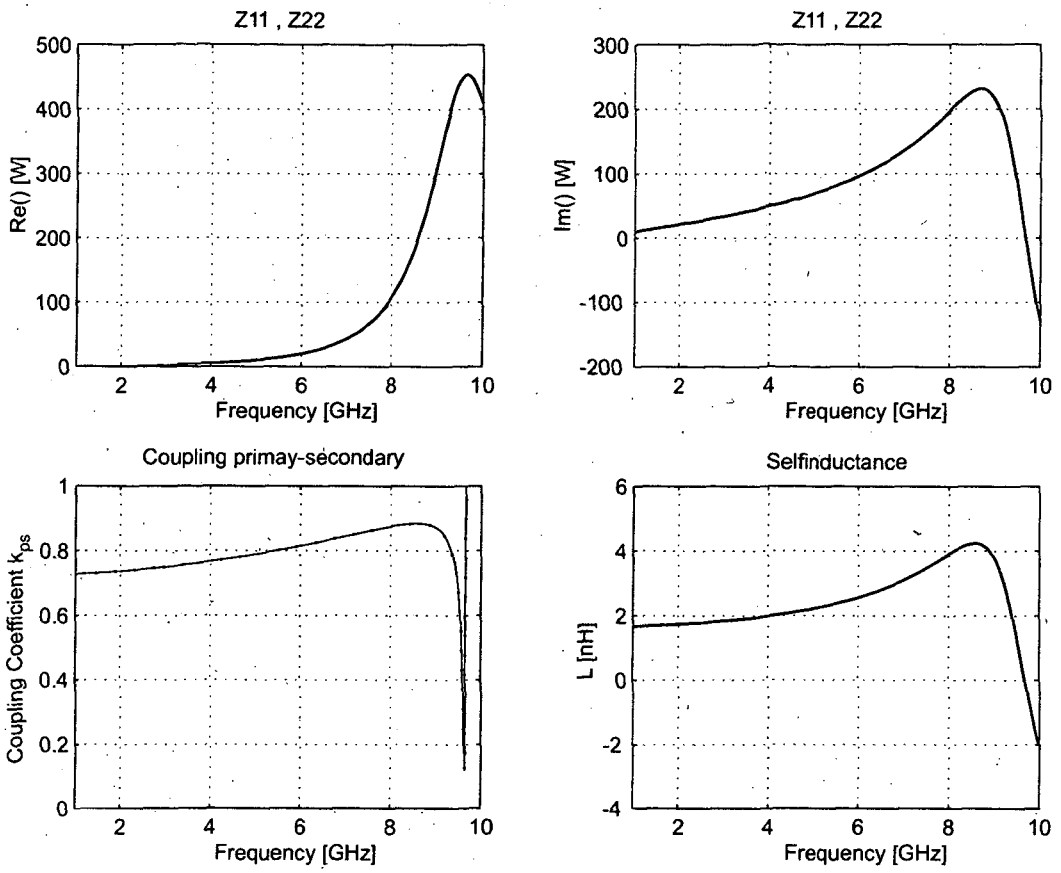


Figure 5.12: Z-Parameter simulation results of the input transformer using Fast-Trafo.

$$P = \frac{U_{eff}^2}{R_L} = \frac{U^2}{2\,R_L}. \tag{5.5}$$

Hence, the optimal load

$$R_L = \frac{U^2}{2\,P} \tag{5.6}$$

can be calculated. For a single-ended configuration with $U = Vcc$, R_L would be $5\,\Omega$ and the average collector current would be 400 mA. If the optimum current density to obtain f_T is $0.25\,\mathrm{mA}/\mu\mathrm{m}^2$ an emitter area of $1600\,\mu$m would be necessary for the output transistor.

For a push-pull configuration, Eqn. (5.5) will change to

$$P = \frac{(2 \cdot U_{eff})^2}{R_{L,diff}} = \frac{2 \cdot U^2}{R_{L,diff}} \tag{5.7}$$

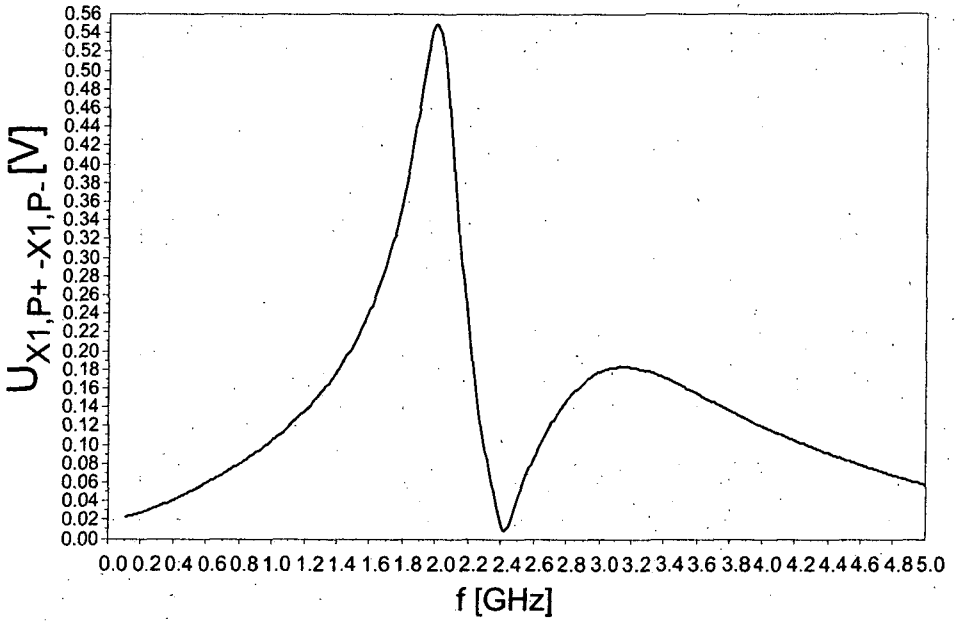


Figure 5.13: AC-Simulation of the primary winding of the input transformer X1. Between 2 and 2.5 GHz the transformer in parallel to the input capacitors C1 and C2 shows a resonance effect.

with the optimal load now being

$$R_L = \frac{2U^2}{P}. \tag{5.8}$$

For the same output power the differential load is now $R_{L,diff} = 20\,\Omega$ which implies a load $R_{L,COL} = 10\,\Omega$ per collector. Thus the average current per collector is reduced to 200 mA reducing each transistor area to the half of the single-ended configuration. The load will shift in reality in dependence on supply voltage variations, operating point (RF input current and biasing) and the parasitics originated in the die layout. So usually we will find an optimal complex valued Z_L instead of R_L which has to be matched by the output matching circuit. For this circuitry, the optimum current density for large scale operation was estimated to be about $0.25\,\mathrm{mA}/\mu\mathrm{m}^2$. For high speed SiGe technologies as presented in [Meister 03] this current density value can reach up to $8\,\mathrm{mA}/\mu\mathrm{m}^2$. With this the start value, the emitter area can be estimated to $800\,\mu m^2$. Usually the area is selected to be higher, to improve the linearity for systems with a high peak to average power levels and further to increase the robustness of the output transistors. Also thermal effects lowering f_T/f_{MAX} are better considered. In this design, the area was selected to be $960\,\mu m^2$ using 32 transistor subcells in a double-collector, double base layout configuration. Each transistor cell uses a $20.4\,\mu m$ long emitter finger and a width of $1.75\,\mu m$ including the spacer ($0.25\,\mu m$ thick).

As now the transistor area is known the input impedance of the output transistor can be calculated and simulated for its transient behavior.

As the resulting output transistor shows up a very low input impedance, due to the fact that the current gain is lowered from the ideal value (SPICE Parameter BF (here about 150)) with 20 dB per decade as shown in Chapter 3. Thus in this case the transistor with all parasitics will have a current gain of about 4 to 5. Therefore the transformer must supply the bases with a peak to peak current of $\approx$ 200 mA ($\pm$100 mA). Figure 5.14 shows the base current of one output transistor attached at the secondary winding, representing the output of the transformer and the collector current of the driver transistor into the primary winding of the transformer.

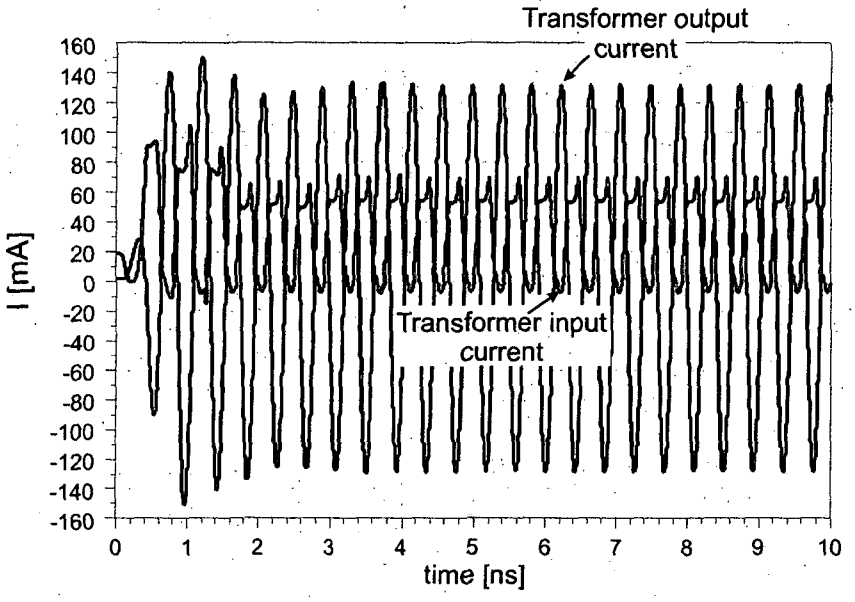


Figure 5.14: Transient simulation of the currents for transformer X2. The input represents the collector current of one transistor into the primary winding and the output the base current from the secondary winding into the transistor.

The design of the driver stage transistor follows from of the necessary current into the transformer, furthermore the transformer together with the capacitors C_3 and C_4 and the transistors should be tuned to the operating frequency. Figure 5.15 shows an AC sweep simulation. The transformer was tuned to the frequency of 2.2 GHz to have an equal performance for 1.9 GHz (DECT) and 2.45 GHz (ISM-band). This figure shows the driver and the output stage resonance using an ideal BALUN at the output tuned to the operating frequency.

Figure 5.16 shows the used interstage transformer winding scheme. X2 has a turn ratio of N=4:1. The total coupling coefficient is k = 0.65 at 2.45 GHz. The size is $250 \times 250\,\mu m^2$. The primary winding consists of 4 turns with Al 3 and Al 2

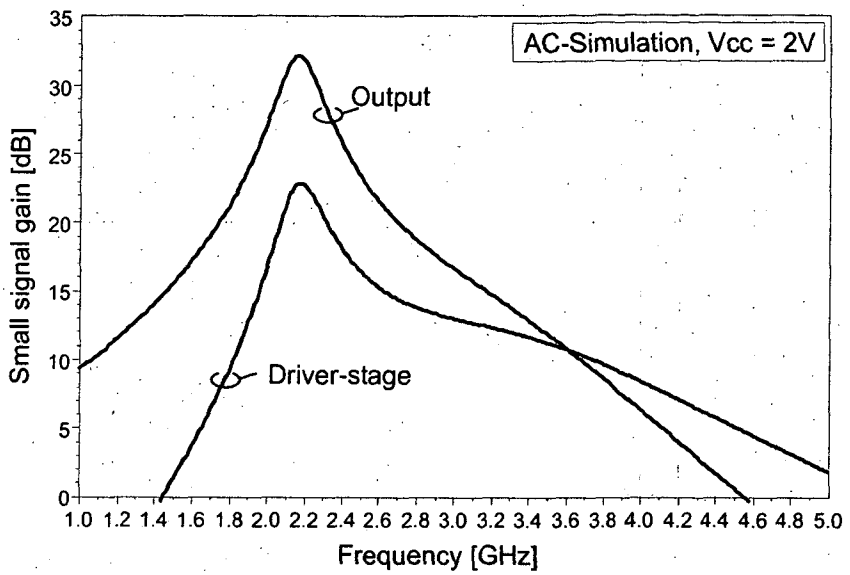


Figure 5.15: AC sweep simulation of the driver stage and the output.

connected in parallel. A primary center tap is available, connected via metal 1. The secondary winding consist of one turn with a center tap connected via Al 1. The winding itself uses Al 3 and Al2 in parallel. The equivalent circuit of the transformer X2 is found in fig. 5.17.

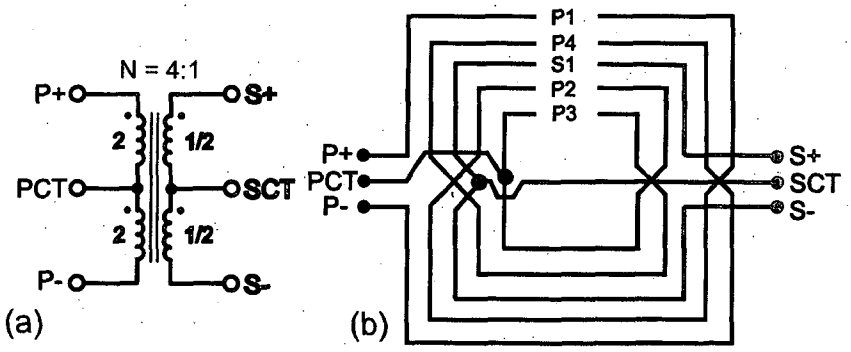


Figure 5.16: Interstage transformer X2: (a)schematic symbol (b) winding scheme

The transistors used in this circuit for the driver and the output stage have the same layout. Both feature a double base contact to reduce the transistor base resistance compared to single base configurations and a double collector, single emitter contacting. Due to the transistor symmetry a multifinger structure is easily designed, as the collectors of two neighbour transistor cells can be connected directly together. The emitter length of the transistors is 20.4 μm and the effective emitter width is 1.5 μm. Figure 5.18 shows the layout of the driver stage transistor.

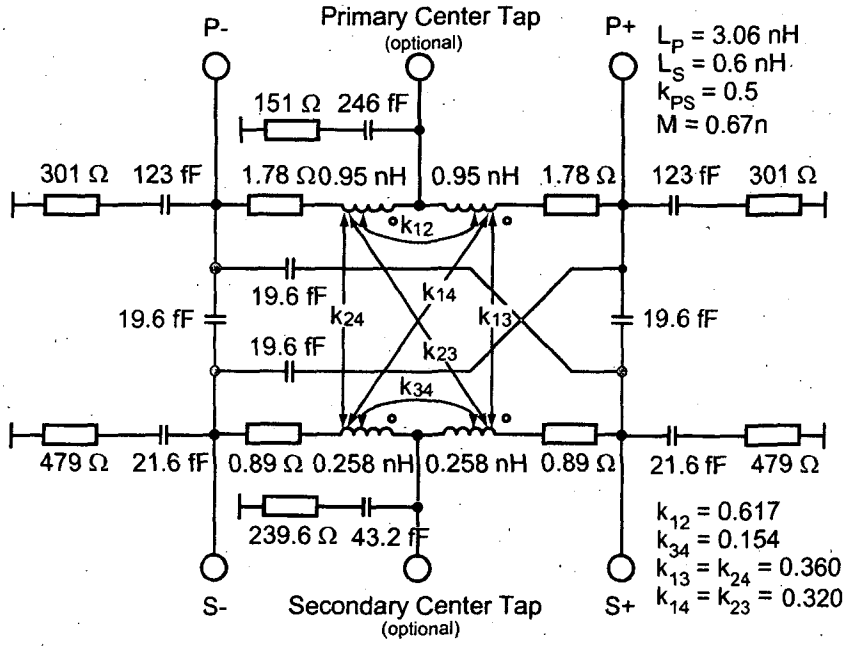


Figure 5.17: Interstage transformer X2: SPICE model.

Using 4 transistor cells in parallel gives the effective emitter area of 120 μm^2. The transistors emitter is connected on the base side to ground. The collector contacts and the emitter-contacts are connected using a trapezoid metalization becoming smaller in the mid of the finger. This is only possible for larger emitter widths due to metal layer spacing design rules and improves the current density distribution over the emitter finger. Figure 5.19 shows the output transistor. It has the same structure as the driver transistor with the difference of using 32 transistor cells.

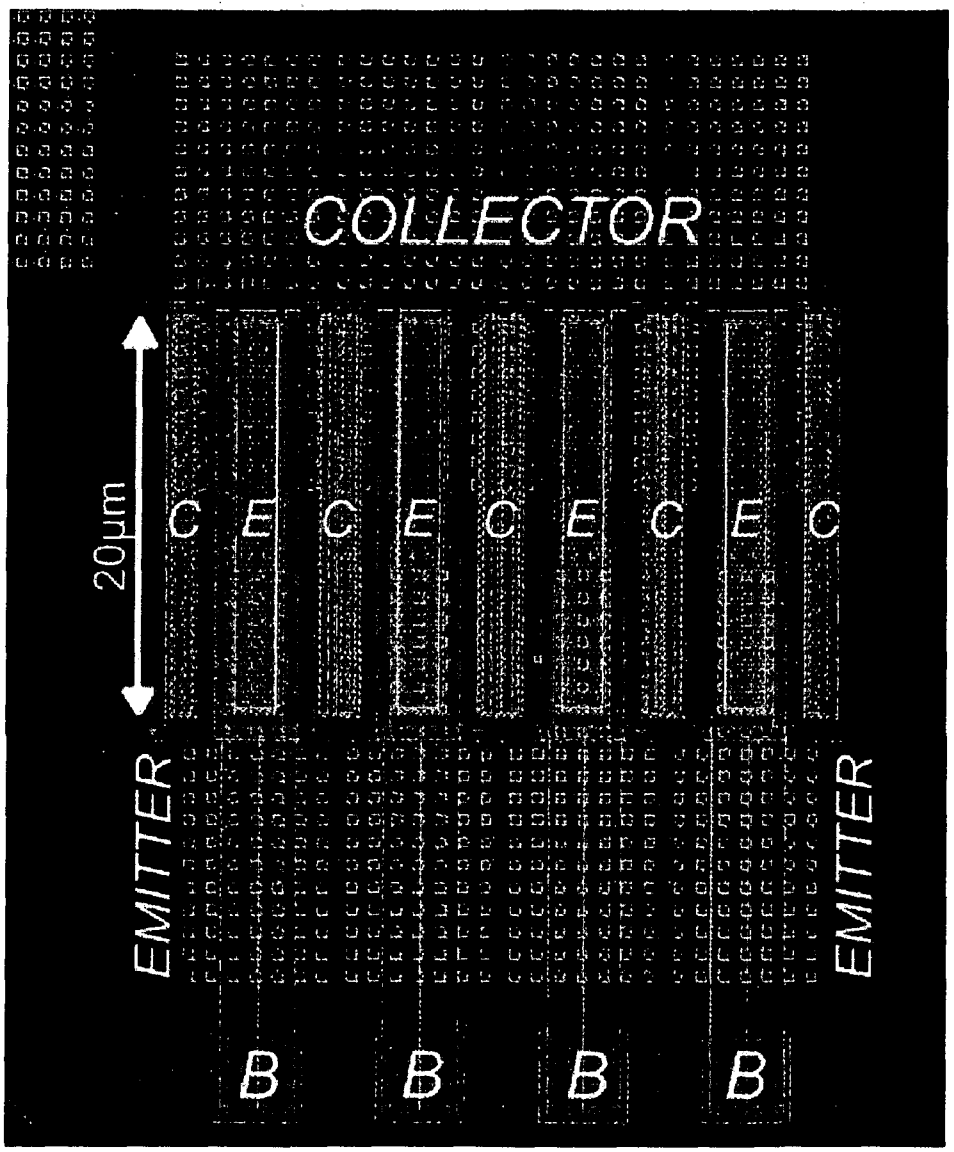


Figure 5.18: Layout of the driver transistors T1 and T2. The 4 parallel-connected transistor cells features a double base, single emitter, double collector configuration. The emitter length is 20.4 μm and the effective emitter width 0.5 μm.

5.4 Output matching

As the power amplifier is designed to work with a differential output, an efficient output BALUN with optimized matching has to be attached. There exist several solutions for this, as presented before and in [Bakalski 02,d, Bakalski 02,a, Mongia 99]. However the solution should end up in a cheap, small-sized and efficient solution. As the smallest BALUN solution, the LC-BALUN has the major

Figure 5.19: Layout of the output transistors T3 and T4. The 32 parallel-connected transistor cells features a double base, single emitter, double collector configuration. The emitter length is 20.4 μm and the effective emitter width 0.5 μm.

disadvantage of using costly RF components and depending strongly on the PCB layout, it is obvious, that using the PCB with transmission lines will help to reduce production variations due to soldering and mounting as well as the reduction of the number of RF components. Therefore a microstrip line BALUN was introduced in Chapter 4 and [Bakalski 02,e]. As the design of this BALUN requires the knowledge on the optimum output load, this was done by a load-pull setup on a predecessor chip [Bakalski 02,c]. As this setup requires high efforts for an accurate measurement [Bakalski 01] the measurement was used to estimate the load impedance for this power amplifier, as the same output power range was desired. The optimum load therefore was set to 13 Ω per collector. Attaching the resulting microstrip line BALUN to the schematic in fig. 5.2, the complete power amplifier circuit results in fig. 5.20.

5.5 Experimental results

As explained before, a microstrip line BALUN is used for output matching and power supply feeding. Figure 4.19 in section 4.6.2 shows the layout of the used microstrip line BALUN.

Figure 5.21 shows the power amplifier test-board including the microstrip line BALUN for characterization. The substrate parameters are $\varepsilon_r = 3.38$, $\tan\delta = 0.0027$ and the dielectric thickness is 0.51 mm. The metalization layers consist of 18 μm copper with a nickel diffusion barrier [Nicolics 97] and 5 μm gold on top for bonding. The die is attached with a conductive epoxy to the substrate and is bonded directly on the board.

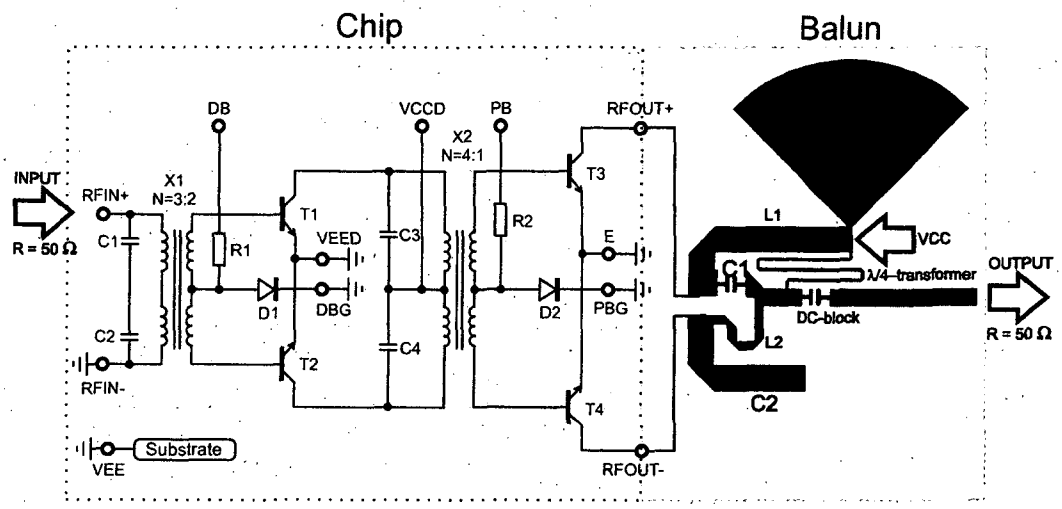


Figure 5.20: Power amplifier module schematic with microstrip line BALUN.

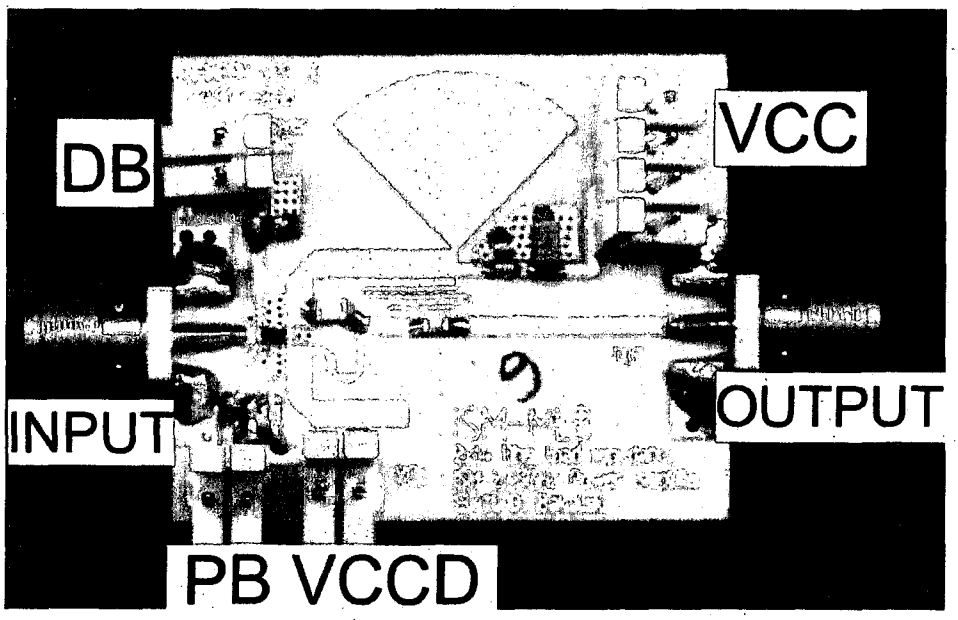


Figure 5.21: Power amplifier module PCB (size: $36 \times 29\,\mathrm{mm}^2$).

The input of the amplifier is connected directly via a bondwire to the $50\,\Omega$ microstrip transmission line. The output is bonded to the microstrip line BALUN with $13\,\Omega$ load per collector. Here, a 1.2 pF AVX ACCU-P 0805 SMD type capacitor was selected for the lumped capacitor C1. Furthermore the necessary DC-block capacitor is inserted on the test board as well. It was selected using a network analyser with the focus on a low reflection coefficient and low S21 (AVX ACCU-P 12pF 06035J120GBT). The power amplifier was characterized operat-

ing in a pulsed mode with a duty cycle of 12.5% with a pulse width of 577 ms, typical for DECT and GSM specifications.

Figure 5.22 shows the measured power transfer characteristic. The maximum output power is 26 dBm (400 mW) at the low supply voltage of only 2 V. The maximum PAE is 53% which is an excellent value, as the maximum efficiency of a class B amplifier is 78.5 % as shown in section 2.3.2.

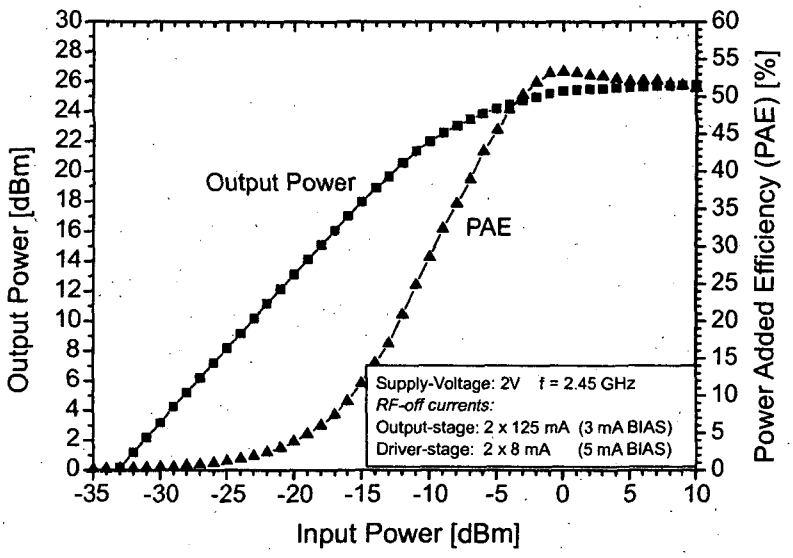


Figure 5.22: Measured power amplifier transfer characteristic.

For battery operation, the behavior for lower supply voltage is of interest as well. Figure 5.23 shows the measured power transfer characteristics for supply voltages of 1 V, 1.2 V, 1.5 V and 2 V, which include the most important single battery cell supply voltages (1.2 V for NiCd and NiMh cells and 1.5 V for a standard AAA AlMn battery cell). Thus, the PA is suited to operate down to 1 V of supply voltage with a reduced output power. Figure 5.22 shows the small signal gain of 33 dB as described in section 2.1.1.

Figure 5.23 shows the frequency response. The frequency response shows a high PAE and output power level in a frequency range from f = 1.9 GHz to 2.6 GHz. Thus the power amplifier is well suited for DECT and ISM applications without any change of the matching network. Finally, Tab. 5.1 shows the performance summary that includes the current dissipation of the PA circuit as well as the quiescent currents which are extremely low. This indicates, that the transistors are basically driven by the RF current of the transformers and thus operate very near to class B operation. This is extremely advantageous for wireless LAN applications using a low average power. As for example the PCMCIA card slot for notebooks is limited in its overall current consumption to 500 mA, Tab. 5.1 shows further its usability if the design is tuned for the necessary linearity.

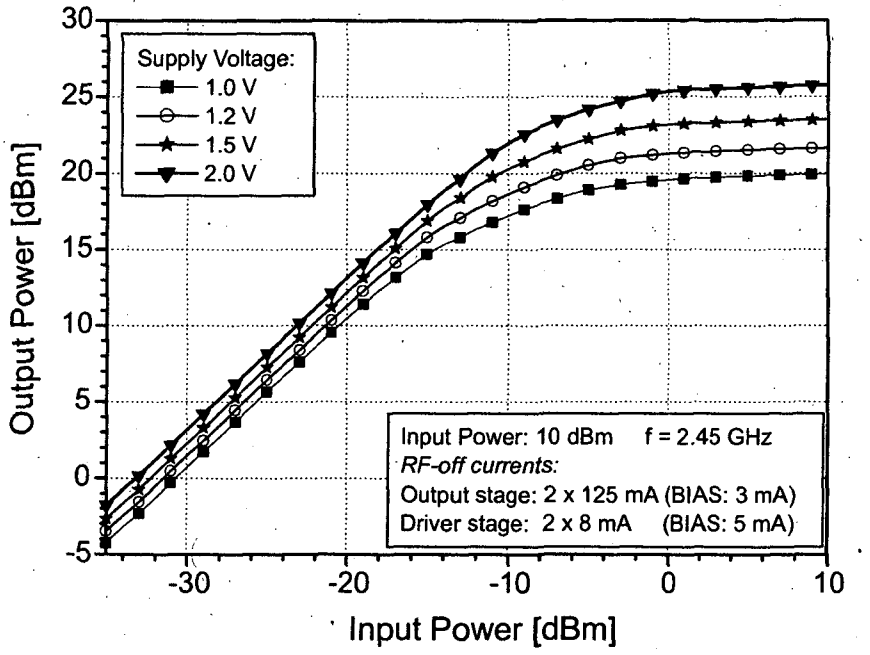


Figure 5.23: Measured power amplifier transfer characteristic.

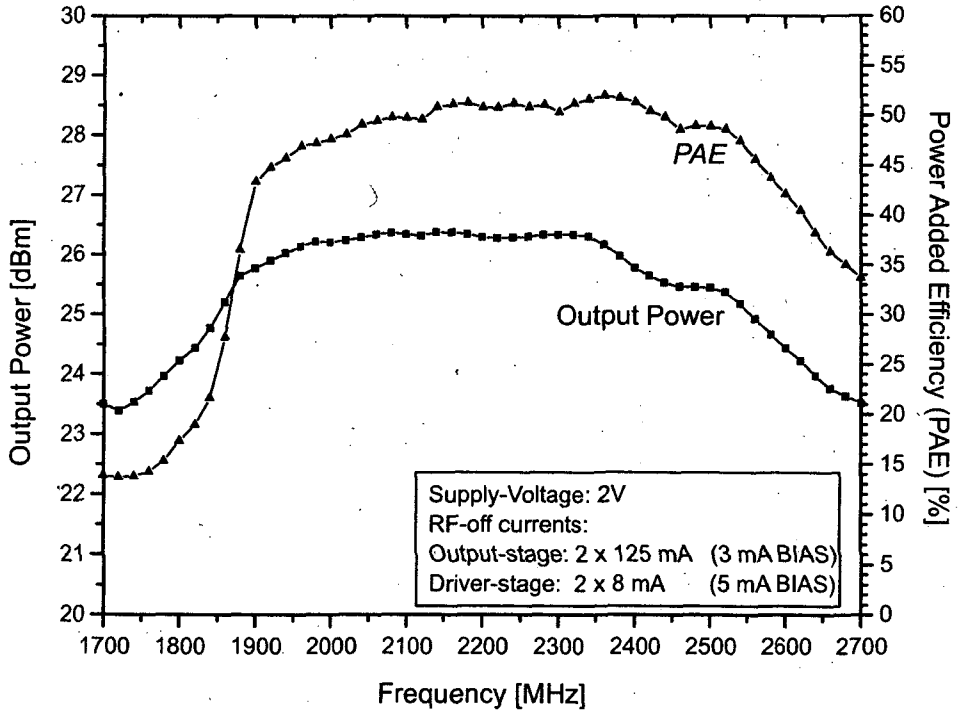


Figure 5.24: Measured power amplifier frequency characteristic.

Operating frequency	1.9 GHz – 2.6 GHz				
Small-signal gain (2.45GHz)	33 dB				
Supply voltage	1	1.2	1.5	2.0	V
Maximum output power	20	21.5	23.6	26	dBm
(2.45 GHz, Pin = 10 dBm)	100	142	230	400	mW
Power-added efficiency (2.45 GHz, Pin=10 dBm)	36	41	49.5	53	%
Output stage collector efficiency (2.45 GHz, Pin=10 dBm)	47.6	54.2	66	71.4	%
Output stage collector current (RF on) + bias	2 x 105 + 3	2 x 109 + 3	2 x 116 + 4	2 x 140 + 5	mA
Output stage collector current (RF off) + bias	2 x 125 + 3	2 x 125 + 3	2 x 125 + 3	2 x 125 + 3	mA
Driver stage current (RF on) + bias	2 x 27 + 6	2 x 30 + 7	2 x 35 + 7	2 x 41 + 7	mA
Driver stage current (RF off) + bias	2 x 8 + 5	2 x 8 + 5	2 x 8 + 5	2 x 8 + 5	mA

Table 5.1: Performance Summary (T=300 K, 12.5 % duty cycle, 0.577 ms pulse width.)

Chapter 6

A fully integrated 5.3 GHz Wireless LAN power amplifier

The 5 GHz band is another frequency area, where industrial applications can be found. While there exist some ISM applications, and a wireless telephone band at 5.8 GHz, the most important usage is wireless LAN. Unfortunately, the wireless LAN frequencies depend on the local law limitations which differ a lot as sketched in fig. 6.1. The usual specified IEEE 802.11a frequency range is 5.15 to 5.35 GHz, but there exist further wireless LAN bands, like those in Japan and some for high output power levels in the USA. A power amplifier with a large bandwidth will be advantageous for mass production efforts.

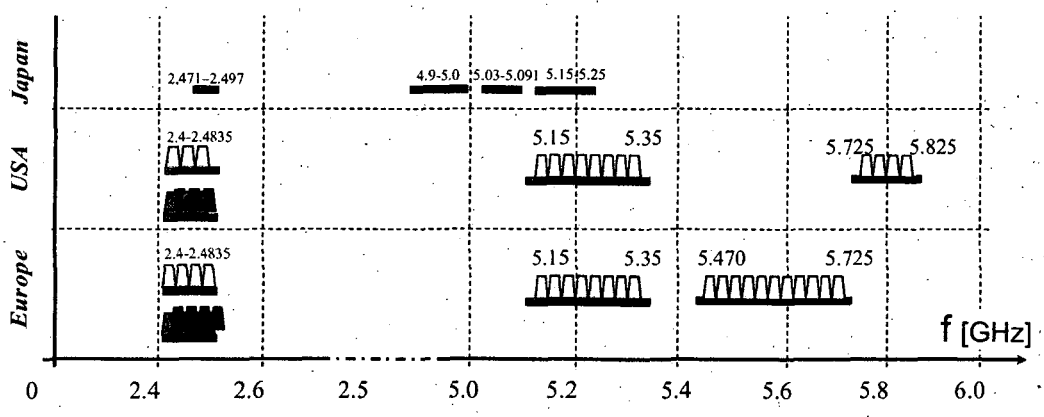


Figure 6.1: Worldwide specified wireless LAN standards and their operating frequencies.

This Chapter presents a Wireless LAN IEEE 802.11a suited PA for the 5.25 GHz band with an integrated LC-Output BALUN [Vizmuller 95, Cripps 99] and integrated RF chokes and output DC-block. It further shows (fig. 6.25) a high bandwidth, covering the japanese wireless band as well. The absence of any external

matching components is a cost advantage, especially as no costly external module structure or RF components are necessary.

The chip was manufactured in a mass-production 75 GHz-f_T SiGe-Bipolar technology [Klein 99, Wolf 01] using the metal layer stack as presented in Chapter 3 (fig. 3.19). The PA circuit core principle is a two stage differential push-pull type amplifier based on two on-chip transformers as input BALUN and for the interstage matching. Figure 6.2 shows the PA chip photograph. The die size is $1 \times 0.9\,mm^2$.

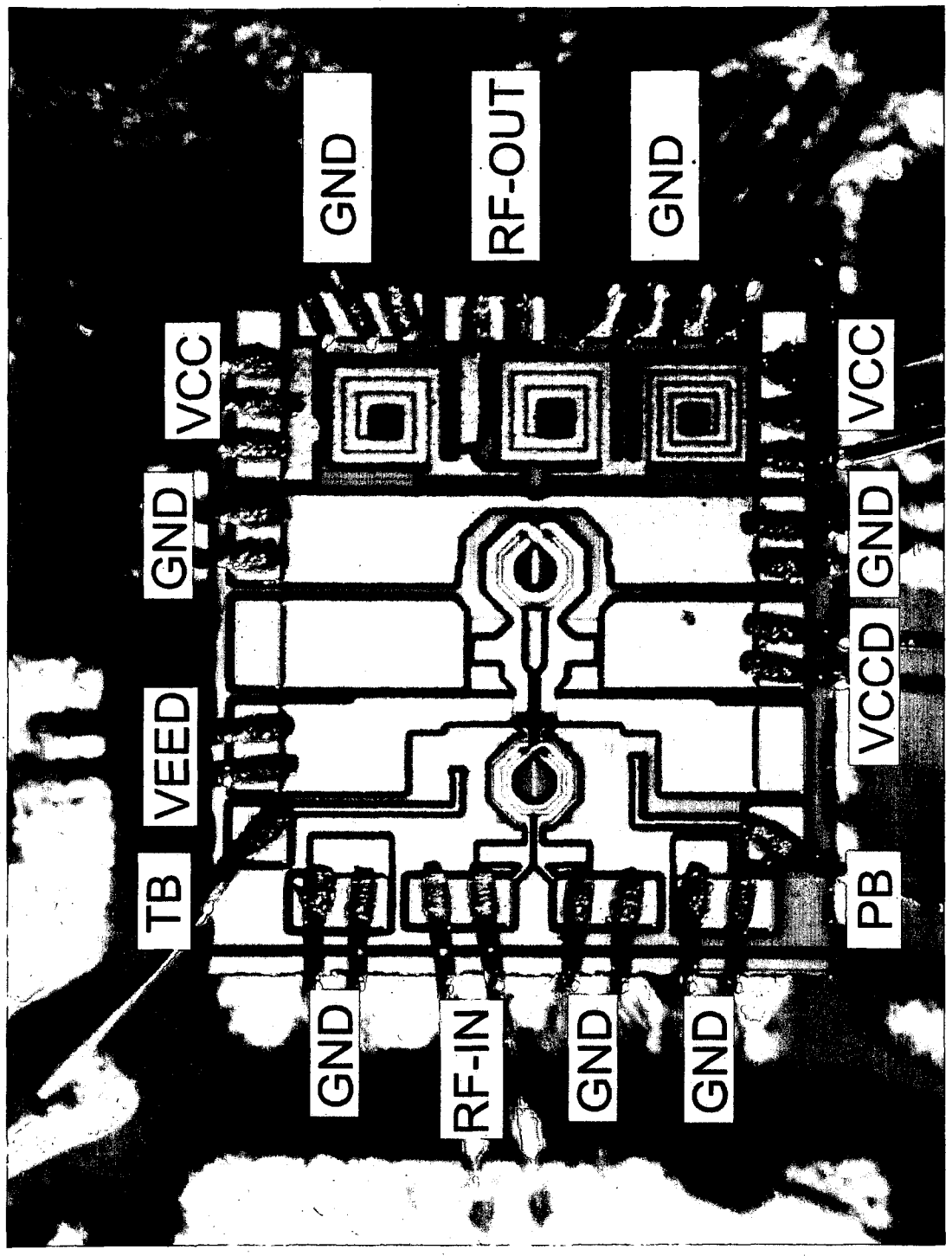


Figure 6.2: Die photograph of the power amplifier (chip size: $1 \times 0.9\,\mathrm{mm}^2$).

6.1 Circuit design

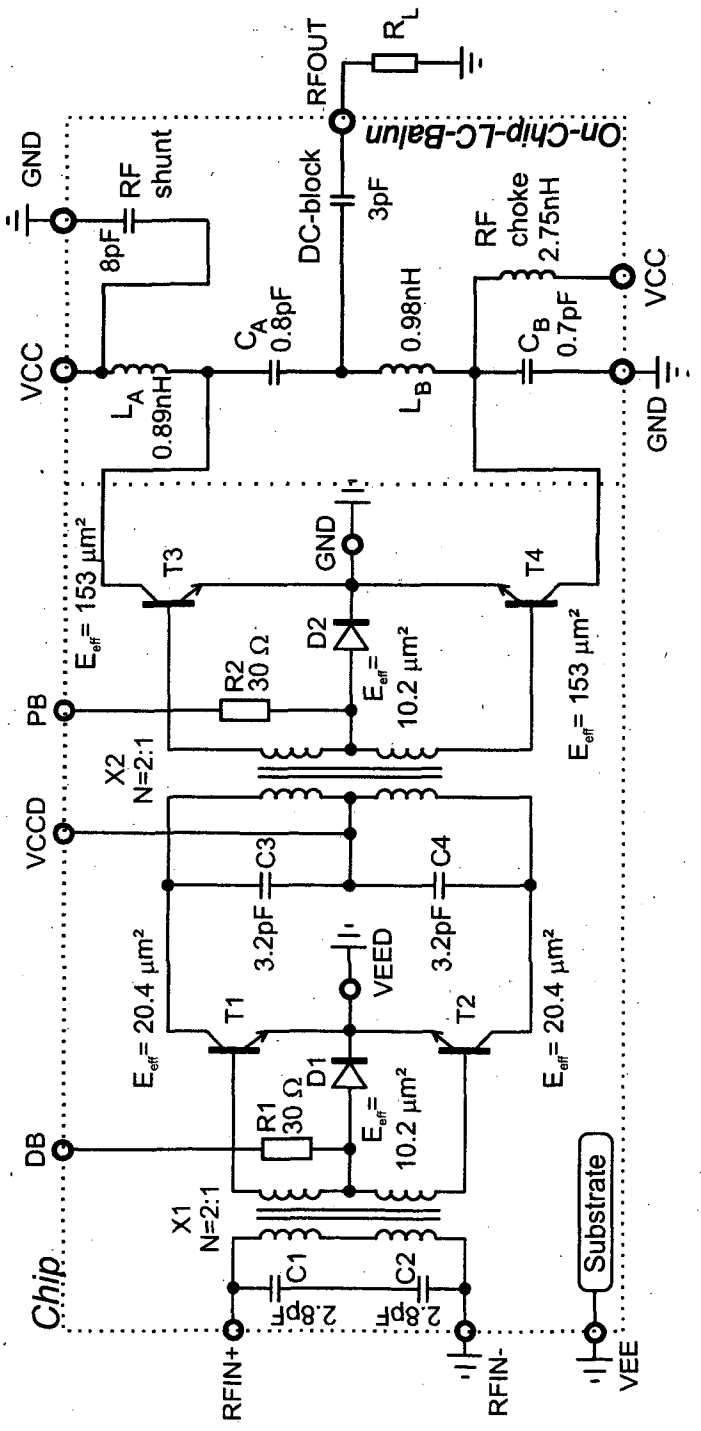


Figure 6.3: Circuit diagram of the power amplifier.

Fig. 6.3 shows the simplified circuit diagram of the power amplifier. It is a push-pull configuration using two transistor stages like the PA presented in Chapter 5. The transformer X1 acts as input BALUN or just only as an input matching network, depending on the bond configuration at the input. X2 acts as interstage matching network between the driver stage T1 and T2 and the output stage T3 and T4. The bias of the driver stage and the output stage are set by current mirrors D1 and D2, respectively, using the transformer center taps. The effective emitter area of T1, T2 is $20.4\,\mu m^2$ and of T3, T4 $153\,\mu m^2$. Figure 6.4 shows the driver stage transistor layout. $10.2\,\mu m$ long, $0.75\,\mu m$ width emitter fingers are used to get the effective emitter area of $20.4\,\mu m^2$ using two double collector transistor cells. The transistor cell uses a triple base connection, double emitter and double collector layout. The triple base connection significantly reduces the base resistance compared to single base configurations, hence the breakdown behavior is relaxed due to the low impedance base connection directly to the transformer.

Figure 6.4: Layout of the driver transistors T1 and T2. The 2 parallel connected transistor cells feature a triple base, double emitter, double collector configuration. The emitter length is $10.2\,\mu m$ and the emitter width $0.75\,\mu m$.

The output transistor in fig. 6.5 has the same configuration, but uses a doubled emitter finger length of $20.4\,\mu m$. Thus, 15 transistor cells are used to obtain an effective emitter area of $153\,\mu m^2$.

Figure 6.5: Layout of the output transistors T3 and T4. The 15 parallel connected transistor cells feature a triple base, double emitter, double collector configuration. The emitter length is 20.4 μm and the emitter width 0.75 μm.

Similar to Chapter 5 fig. 5.5 shows the used input equivalent circuit. It consists of the input bondwires, the pads, the MIM capacitors and the input transformer X1. The chip was intended to work with a single-ended input signal, so that the second bond-wire can be assumed to be shorter which implies a lower inductance. In difference to Chapter 5, the input transformer was designed as an octangular formed structure to improve the quality factor.

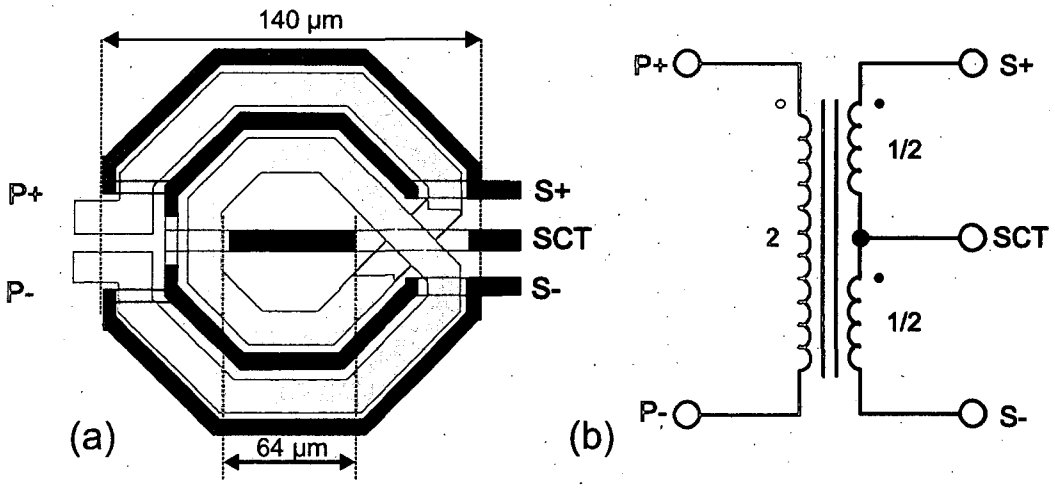


Figure 6.6: Input power transformer X1: (a) Winding scheme (b) Schematic symbol.

Figure 6.6 shows the used input transformer X1 and its winding scheme. The turn ratio of X1 is N=2:1 with the secondary winding consisting of parallel connected turns. The size is 140 $\times$ 140 μm^2. The primary winding consists of 2 turns with a width of 10μm on the top metal layer (Al 3). Al 1 and Al 2 (fig. 3.19) are not used for both windings to reduce parasitic substrate coupling. The total coupling coef-

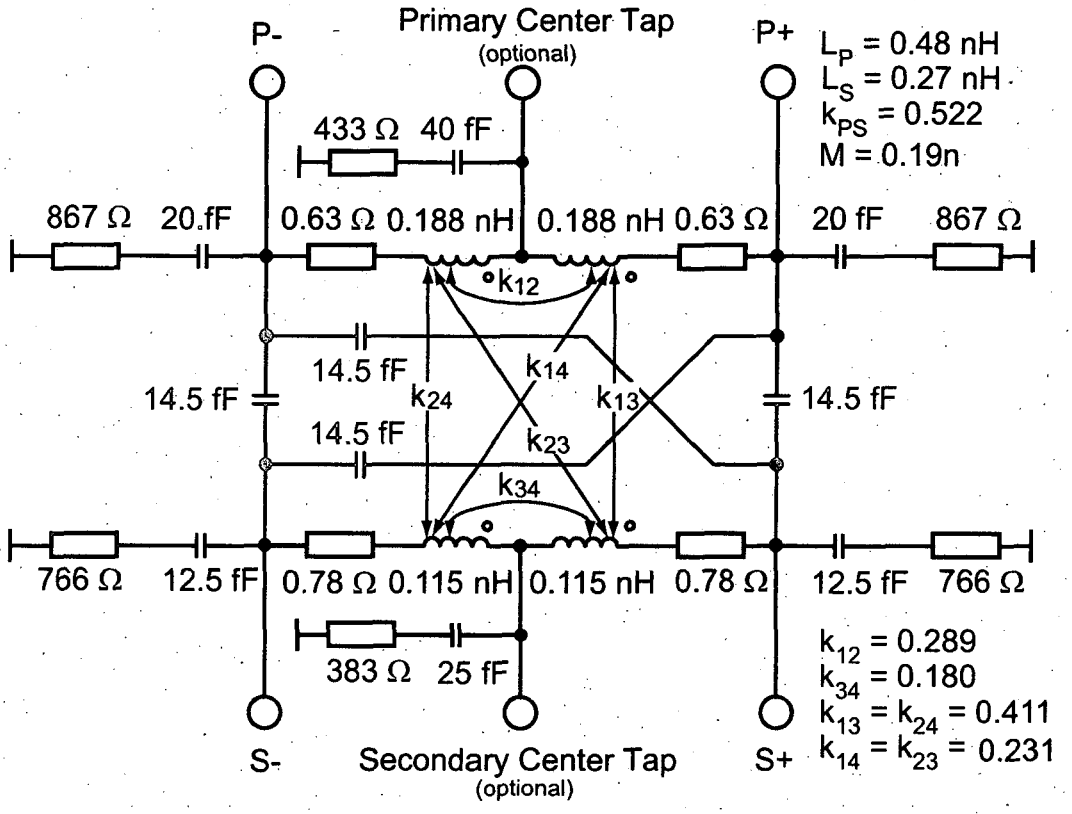


Figure 6.7: Input transformer X1 equivalent circuit.

ficient is k = 0.55 at 5.3 GHz. The simulation results of the transformer modeling tool FastTrafo are presented in figures 6.8, 6.9, 6.10. The low-order equivalent circuit can be found in fig. 6.7.

The input matching optimization method described in section 5.2 was used again to optimize the input matching. Out of the S-parameter measurements in fig. 6.22, an excellent input matching behavior is determined.

The driver stage consisting of transistor T1 and T2 together with the transformer is used to drive the output stage. The transformer is tuned with the MIM-caps C3 and C4 and the transistors T1 and T2 to a parallel resonant circuit at the operating frequency of 5.3 GHz. This can be observed by an AC-simulation and in the measurement setup by a frequency sweep for low input power levels. Figure 6.11 shows the AC simulation results and a small signal measurement for comparison. The curves show excellent match for the resonance frequency matching, but the measured bandwidth is larger than in the AC simulation. This is caused by the low-order transformer and inductor model. Another possible problem for high frequency design can be determined by AC-simulations as well: oscillation. Due to the fact, that high-speed HBTs are used, a possible oscillation has to be prevented. Oscillation problems show themselves in AC-curves as small-banded

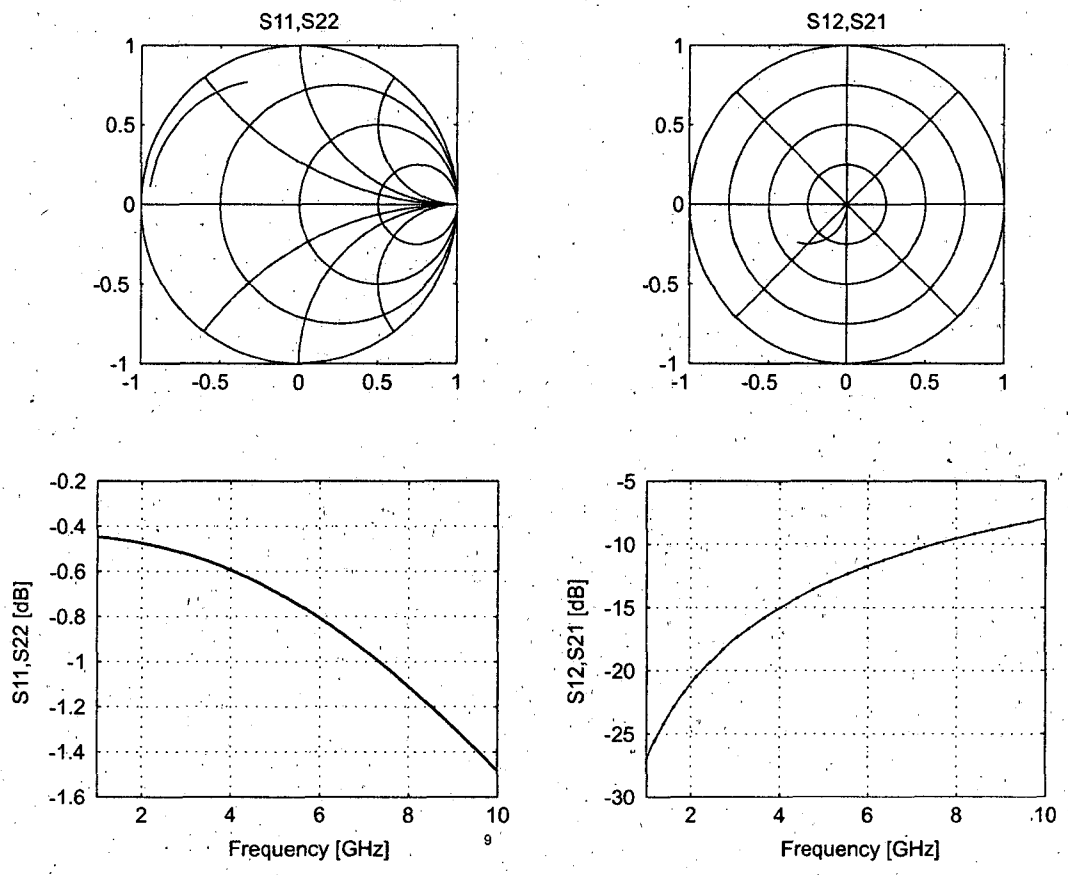


Figure 6.8: S-Parameter simulation results of the input transformer using FastTrafo.

peaks with extreme high amplitudes.

To drive the output stage, the interstage transformer thus has to fulfill a current transformation, hence an impedance transformation. As described in section 5.2, the output HBTs have a very low input impedance, and the transformer acts idealized like having its secondary side short circuited (fig. 5.8). To estimate the current transformation ratio $|I_s/I_p|$ eqn. 5.4 can be used.

In the simulation, the current transformation looks like fig. 6.12. Here a $|I_s/I_p|$ of about 3 is obtained.

Figure 6.14 shows the interstage power transformer X2. It is connected as a parallel resonant device with two capacitors C3 and C4. X2 has a turn ratio of N=2:1. The total coupling coefficient is k = 0.45 at 5.3 GHz. The size is $160 \times 160\,\mu m^2$. The primary winding consists of 2 turns with Al 3 and the secondary of 1 turn also using Al 3. The simulation results of the transformer modeling tool FastTrafo are presented in figures 6.15, 6.16, 6.17. The low-order equivalent circuit can be found in fig. 6.13.

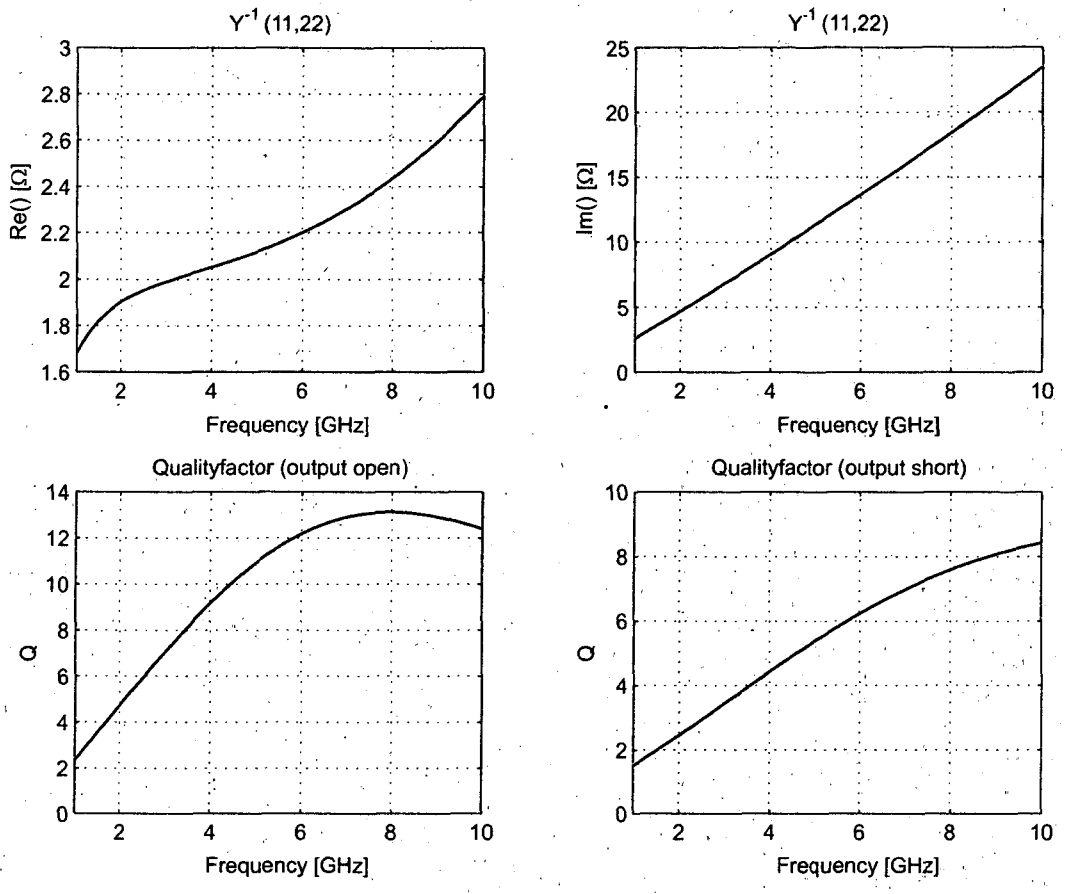


Figure 6.9: Y^{-1}-Parameter simulation results of the input transformer using FastTrafo.

The output stage transistors drive the output BALUN to provide a single-ended output. Hence as well as the transformers, this BALUN has to be designed to have its optimum matching for the operating frequency, here the 5.3 GHz WLAN band. While the input and the driver stage are tuned by the MIM-caps and the transistor areas, this cannot be done that easily for the output stage: A certain saturated output power is needed, and this requires a technology-dependent optimal transistor area and output load. So an LC-BALUN was chosen to be integrated for several reasons:

- The loads at in- and output can be calculated for any real-valued impedance. If the BALUN bridge is used to work asymmetric, or better some prematching is done, even any complex valued loads are possible.
- Due to the advantage of a push-pull type PA of having a 4:1 load-line impedance benefit, the impedance transformation ratios are relaxed, and thus relax the need on high-Q inductors.

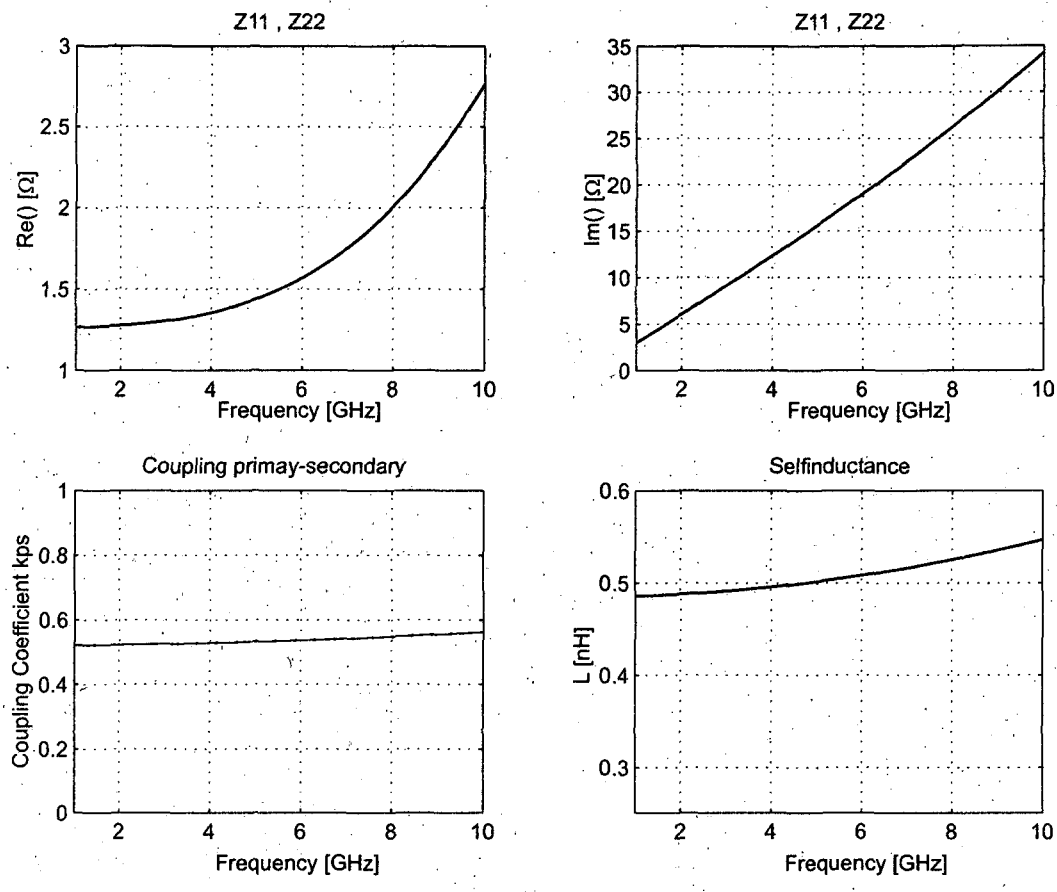


Figure 6.10: Z-Parameter simulation results of the input transformer using Fast-Trafo.

- Together with the transformer the LC-BALUN is one of the smallest solutions in realising a 180^o BALUN structure.

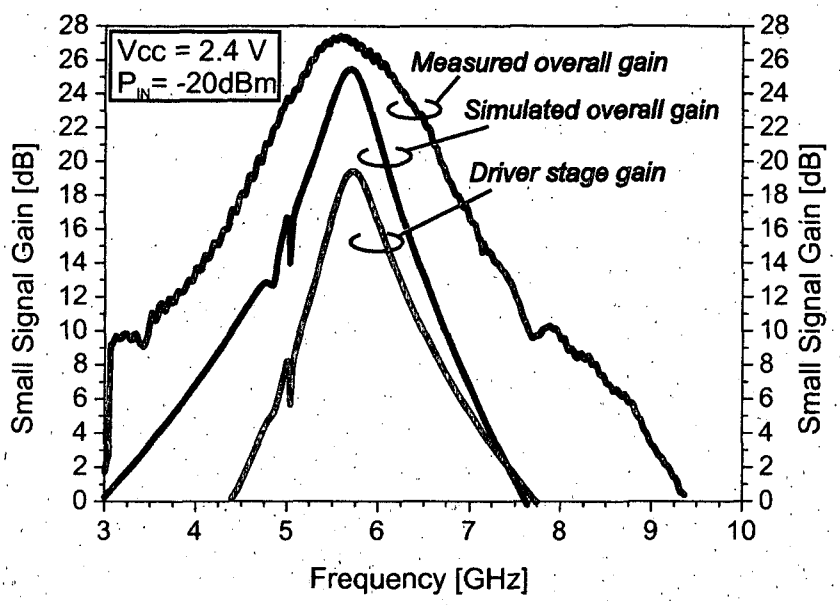


Figure 6.11: Measured and simulated gain curves for the output stage and simulated curve for the input of the interstage transformer. The simulated gain curve is valid for the whole circuitry including the lossy LC-BALUN. The measured curve was obtained using a low input power of -20 dBm.

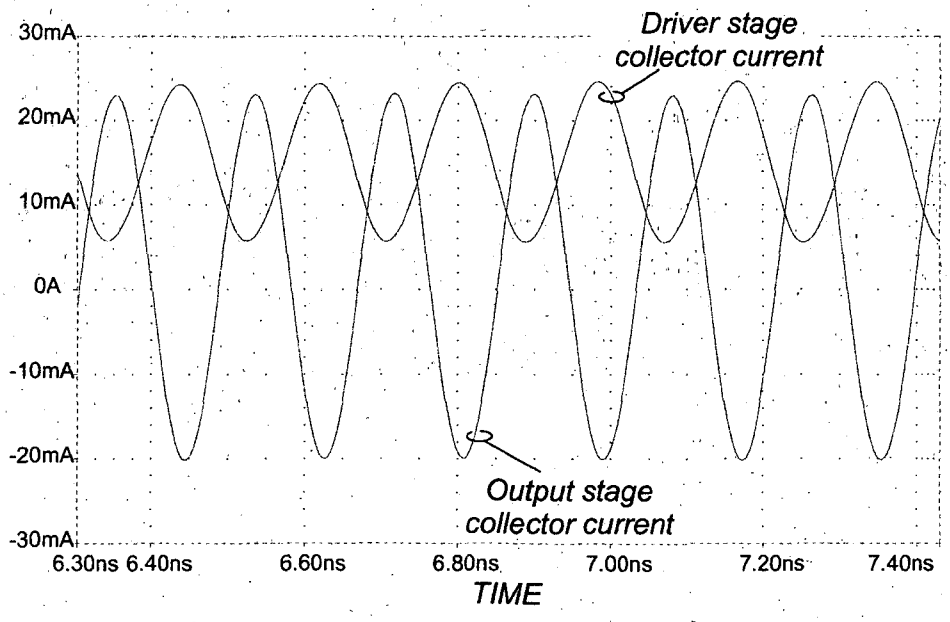


Figure 6.12: $|I_s/I_p|$ current transformation. It is a transient simulation for an input power of -13 dBm. The current curves are shifted due to overlapped bias currents.

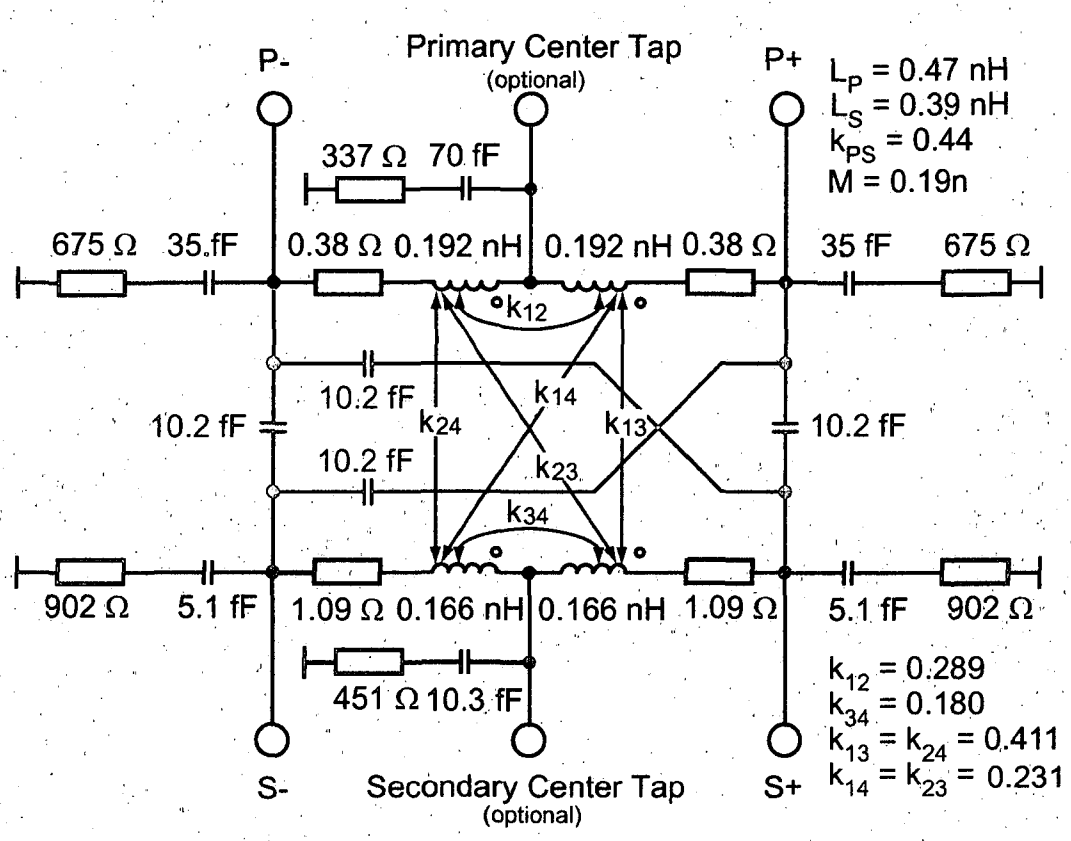


Figure 6.13: Interstage transformer X2 equivalent circuit.

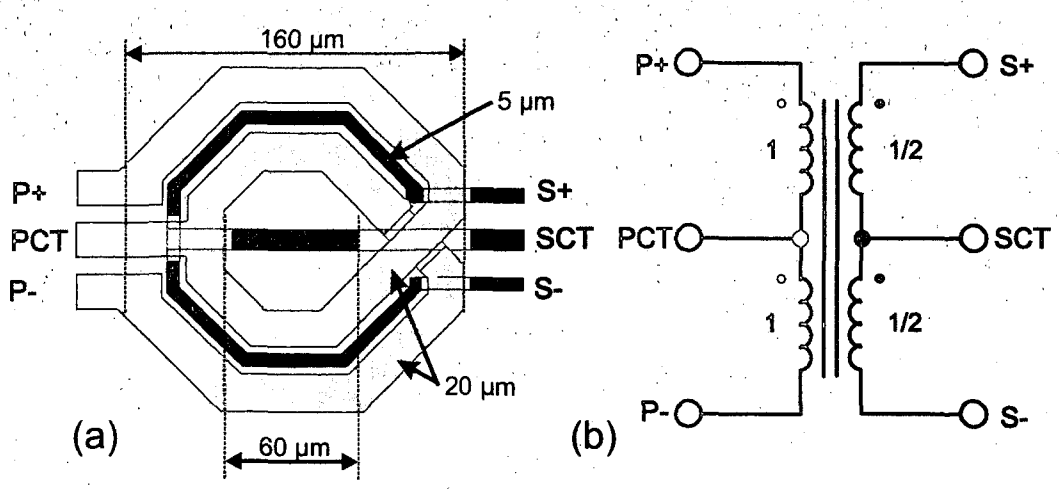


Figure 6.14: Interstage power transformer X2: (a) Winding scheme (b) Schematic symbol.

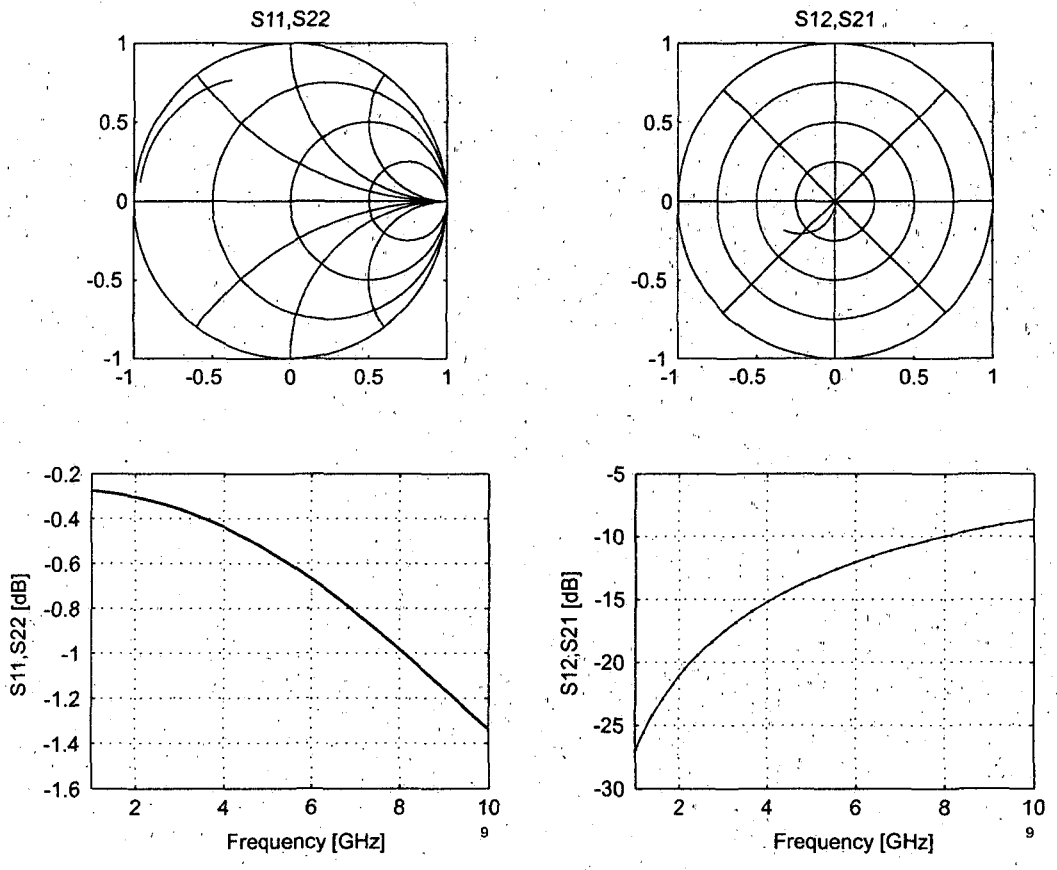


Figure 6.15: S-Parameter simulation results of the interstage transformer using FastTrafo.

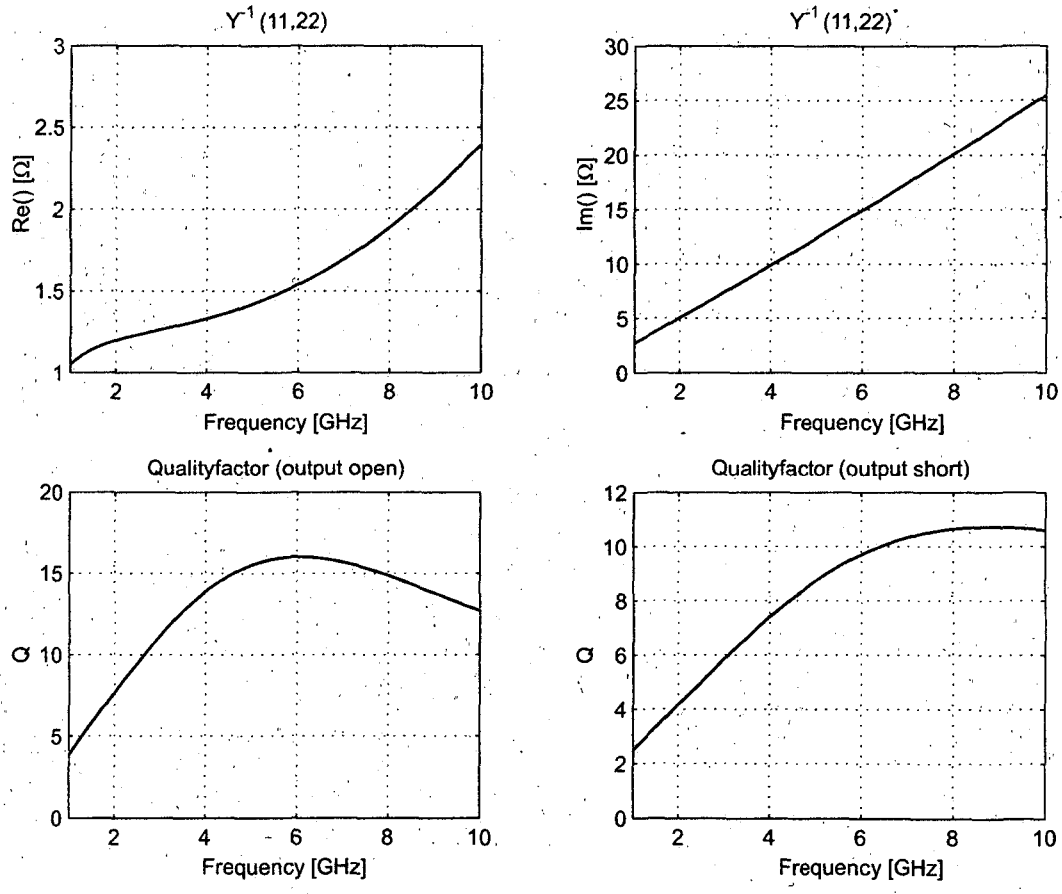


Figure 6.16: Y^{-1}-Parameter simulation results of the interstage transformer using FastTrafo.

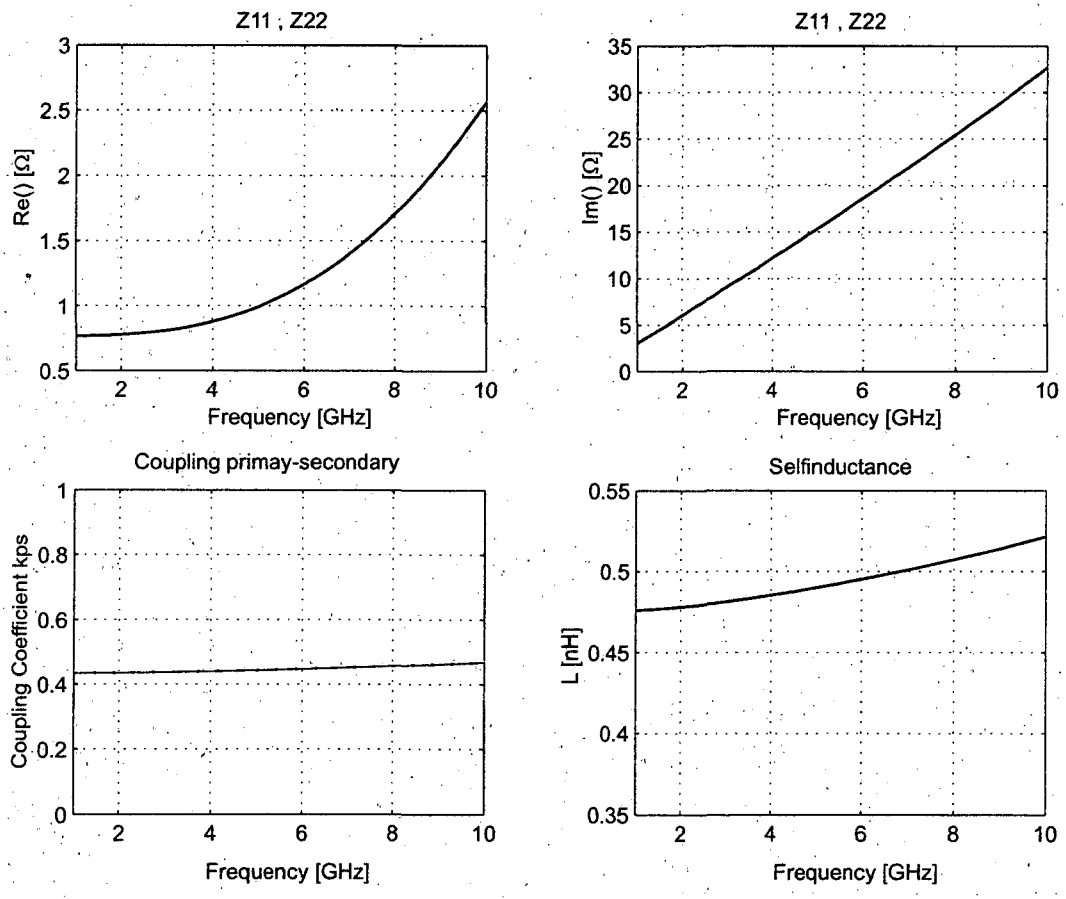


Figure 6.17: Z-Parameter simulation results of the interstage transformer using FastTrafo.

6.2 On-chip LC-BALUN design

During the recent decades several BALUN concepts have been proposed [Johnson 84, Mongia 99, Krischke 95]. One of the most often found is the Marchand [Marchand 44, Mongia 99] BALUN and its derivates. As this BALUN requires certain outer dimensions due to its dependence on the bulk wavelength and good coupling between the lines, it is well suited for LTCC or Laminate structures [Ilkov 03,b, Bakalski 03,a] and shows a good performance and a wide bandwidth. However, for on-chip integration, it is not suitable due to its typically too large layout.

The LC-BALUN described in Chapter 4.18 [Vizmuller 95, Cripps 99] is one of the most compact solutions, as it is based on lumped components. As seen before, there exist accurate models for dealing with inductors and capacitors. It is possible to design such a BALUN structure on-chip. Additionally it also allows an impedance transformation and can be realised using transmission lines [Bakalski 02,e]. Thus, it does not require any prematching. Unfortunately, the inductance of bond wires [March 91, Wadell 91] at the RF output leads to a complex-valued load impedance on the die. Furthermore we find the bond-pad having certain substrate parasitics, depending on the semiconductor technology.

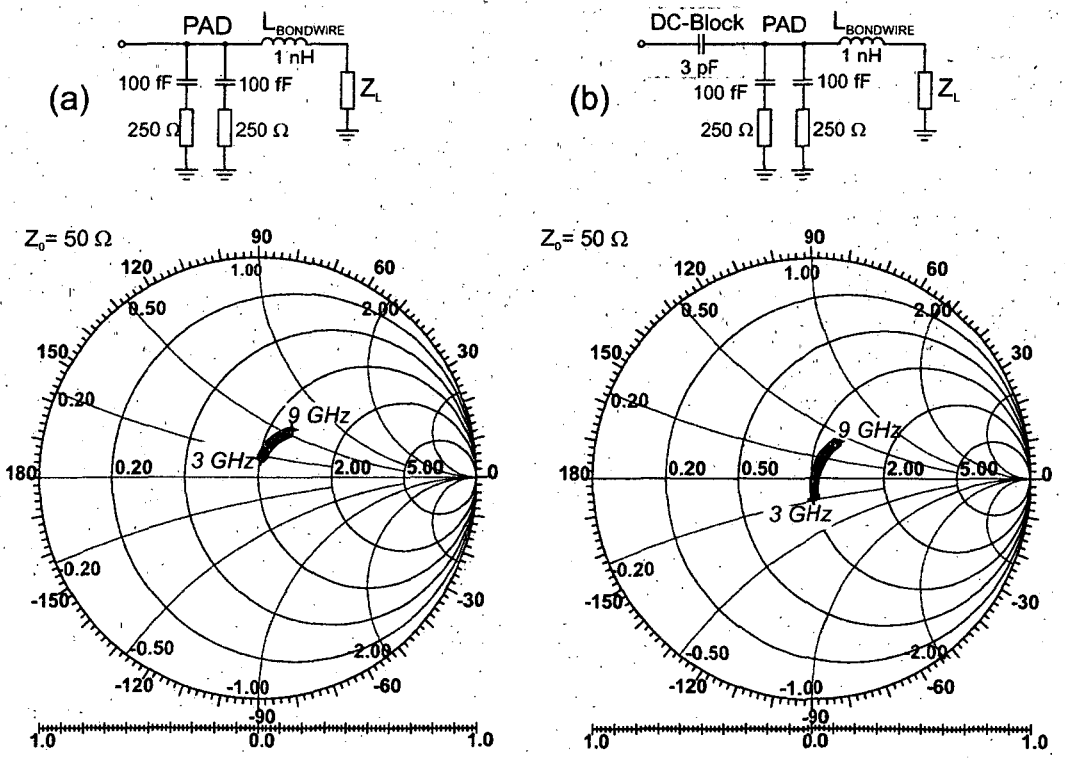


Figure 6.18: (a) Resulting load for the connection parasitics consisting of the pad and the bondwire (b) with additional DC-Block tuned to a real-valued Z_L

Figure 6.18 shows the resulting load for a circuit consisting of a pad and a bond-wire.

If the DC-block capacitor is optimized in this way, that approximately a real-valued load is found in front of the DC-block capacitor (fig. 6.18), the equations 4.8 can be used to design the BALUN. For the optimization, interconnections, inductances and parasitic capacitances shifting the calculated values for L and C have to be considered. Furthermore the RF-choke coil has to be included in the BALUN equivalent circuit, as its parasitics have an influence on the BALUN matching as well.

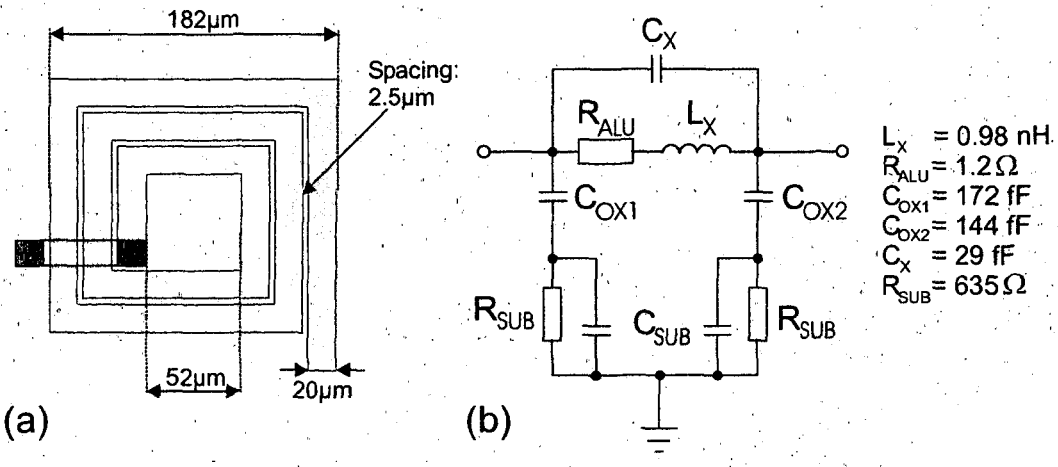


Figure 6.19: (a) 1nH Coil (b) Equivalent circuit.

For the integrated BALUN two similar inductors L_A and L_B (fig. 4.18) are used. Figure 6.19 shows the used coils L_A and L_B. The size is $182 \times 160\,\mu m^2$. The winding consists of 2.75 turns. Al 1 and Al 2 are not used to reduce parasitic substrate coupling of the winding. The interconnection uses Al 1 and 2 to have about the same maximum current density applicable. The inductors are modeled with a tool called Coilgen based on Grovers formula [Grover 46] and substrate effects presented in [Kehrer 01, Wohlmuth 00]. The equivalent circuit for the used coils L_A and L_B can be found in fig. 6.19. Capacitances and DC-block were realised as MIM-CAPs as described in section 4.5.2. Note, that the MIM-CAP parasitics are small compared to the inductors. Hence the equivalent circuit of the on-chip LC-BALUN can be simplified to the structure in fig. 6.20 for the optimization of the inductors.

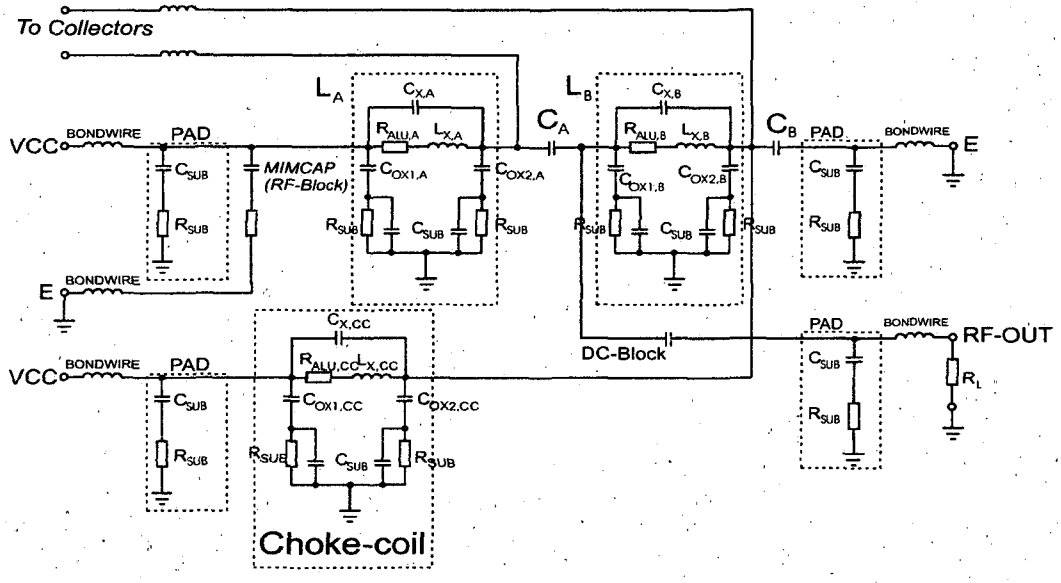


Figure 6.20: Simplified LC-BALUN equivalent circuit.

6.3 Experimental results

For the characterization, the chip was cleaved with a conductive epoxy and bonded to the test board in fig. 6.21. The PCB substrate parameters are $\varepsilon_r = 3.38$, $\tan\delta = 0.0027$ and the dielectric thickness is 0.51 mm. The metalization consists of a 18 μm copper layer with a 1 μm nickel diffusion barrier and 5 μm gold on top for bonding.

The input and the output of the amplifier is connected via a 50 Ω microstrip line. The input and output matching of the power amplifier is shown in fig. 6.22. The power amplifier was characterized operating in a pulsed mode with a duty cycle of 12.5% and a pulse width of 600 μs as well as for CW operation (Tab. I).

Figure 6.23 shows the measured power transfer characteristic at 2.4 V supply voltage. The maximum output power is 25 dBm at 5.3 GHz. The maximum PAE is 24% and the small signal gain is 26 dB.

Figure 6.24 shows the measured power transfer characteristics for supply voltages of 1.0 V, 1.5 V, 2.4 V, 3 V in pulse mode and 2.4 V in continuous wave (CW) mode without additional cooling. It is remarkable, that for 1.5 V single battery cell operation the 1dB compression point is still 20 dBm.

In the 5 GHz band several wireless LAN frequency bands have been defined with regional limitations. Thus, it is of interest if this PA is suited to cover other frequencies as well. Figure 6.25 shows the measured frequency response. The frequency response shows a high PAE and output power level in a frequency range from f = 4.5 GHz to 6 GHz. The 3 dB bandwidth in fig. 6.25 is about 900 MHz,

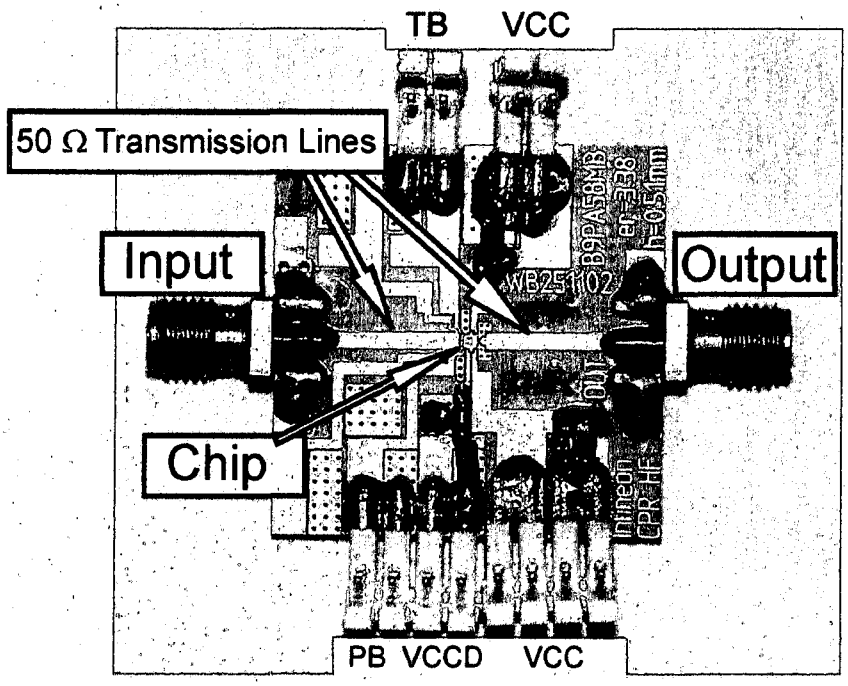


Figure 6.21: Photograph of the power amplifier test-board (size: $30 \times 30\,\mathrm{mm}^2$).

covering the range from 4.8 to 5.7 GHz.

One of the most important properties for PAs suited for wireless LAN is the linearity. Especially due to the modulation scheme, for example a 64-QAM in IEEE 802.11a, a high peak-to-average output power distribution is found. Typically all commercial available PAs are characterized by the Error Vector Magnitude (EVM) [Agilent 02,b] and the Complementary Cumulative Distribution Function (CCDF) [Agilent 02,a]. Commercial wireless LAN PAs are typically specified by a maximum EVM in the range of 3-5%, so the PA was characterized for a maximum EVM limit of 3%. The PA was supplied with an undistorted 64-QAM, 54 Mbit/s test signal and the output measured with an Agilent 89600 vector signal analyzer. The used average input power was $P_{in,avg}$=-13 dBm. The corresponding average output power was $P_{out,avg}$= 11 dBm, all measured in CW-mode. Figure 6.26 shows the corresponding symbol constellation diagram. No major distortions in the outer or inner constellation symbols can be found. The corresponding output spectrum is plotted from the test set in fig. 6.27.

Additionally to the EVM measurement, a CCDF curve [Agilent 02,a] was measured (fig. 6.28). This type of curve emphasizes compression effects very well. This plot shows the ideal CCDF curve for the used modulation scheme as well as the measurement at the output. As the probability for high output power levels is low, the measured curve shows some steps. Thus, the PA has a compression lower

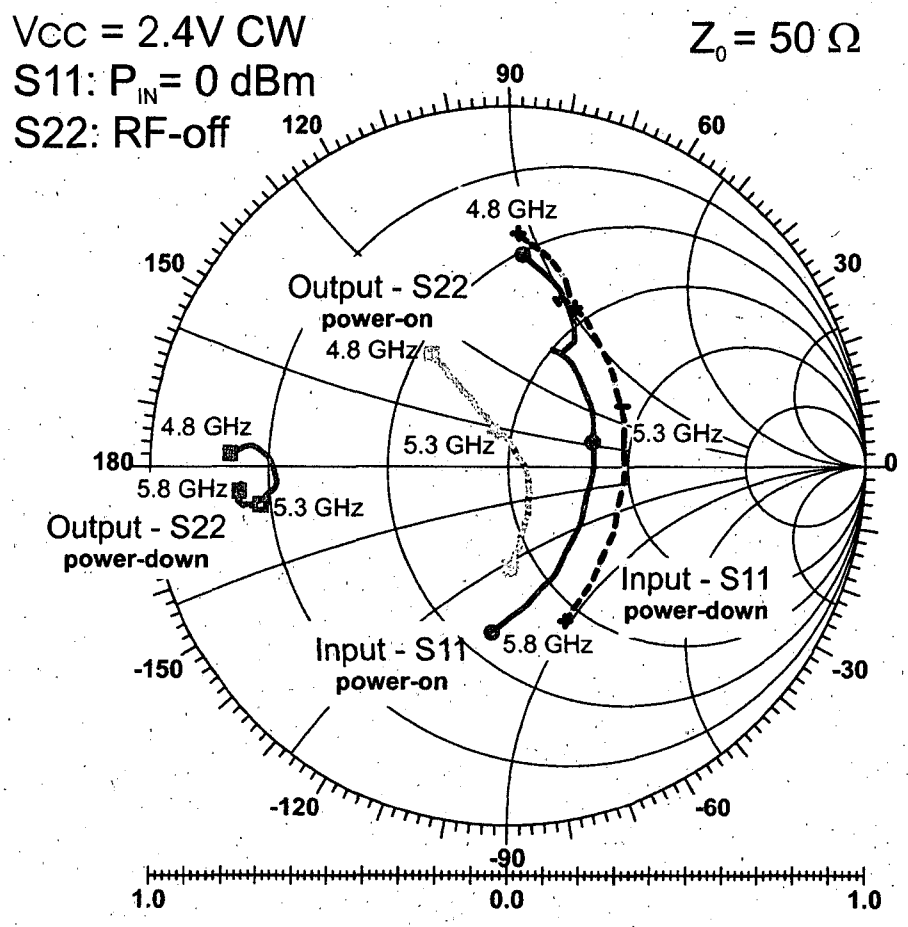


Figure 6.22: Measured S-Parameters for Input (S11) and Output (S22).

than 1 dB at the highest output level in this configuration. With this, the PA is very linear up to the 1 dB compression point showing no noticeable errors in magnitude and phase.

Tab. 6.1 shows the performance summary.

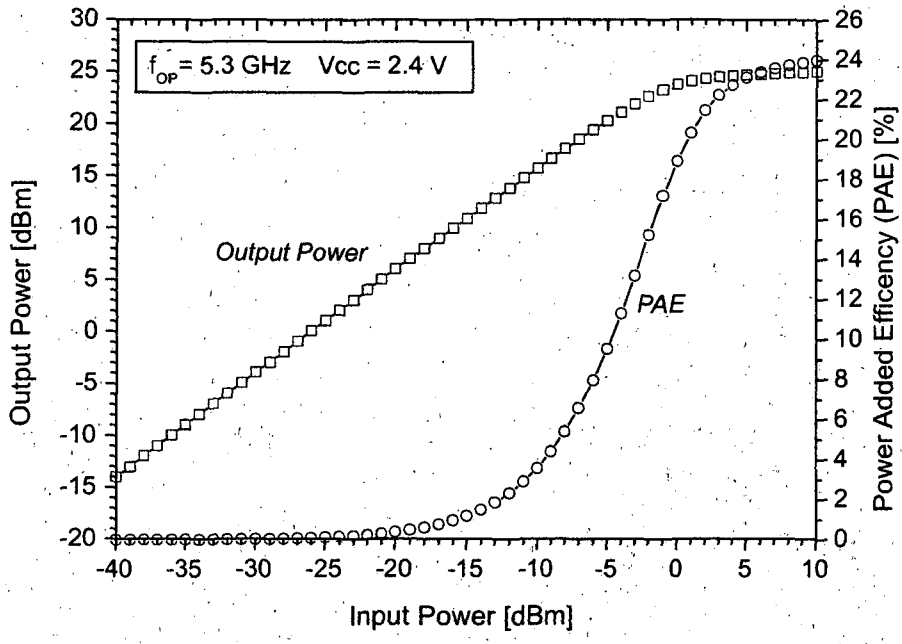


Figure 6.23: Measured power amplifier transfer characteristic.

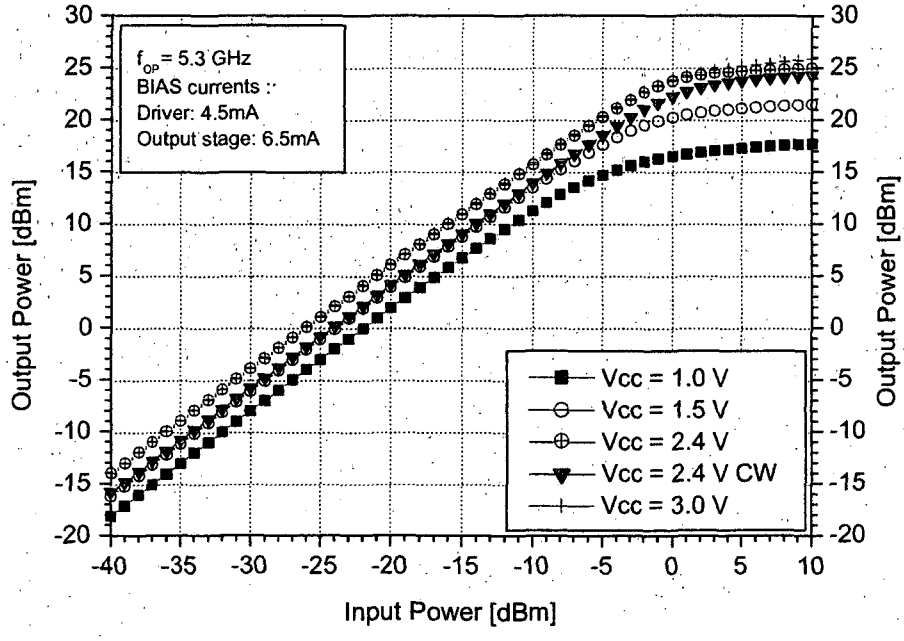


Figure 6.24: Measured power amplifier transfer characteristic versus supply voltage.

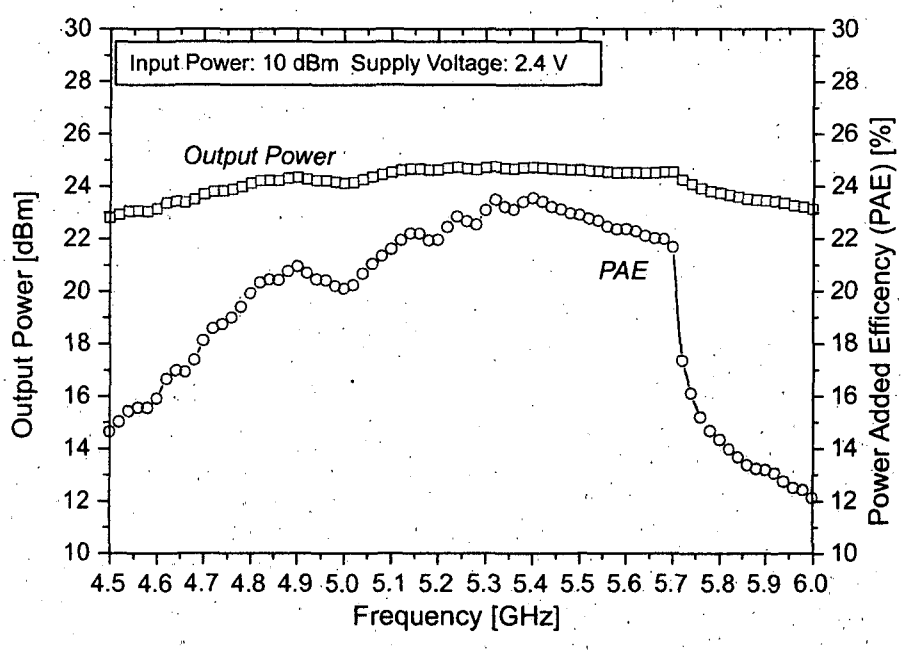


Figure 6.25: Measured power amplifier frequency characteristic.

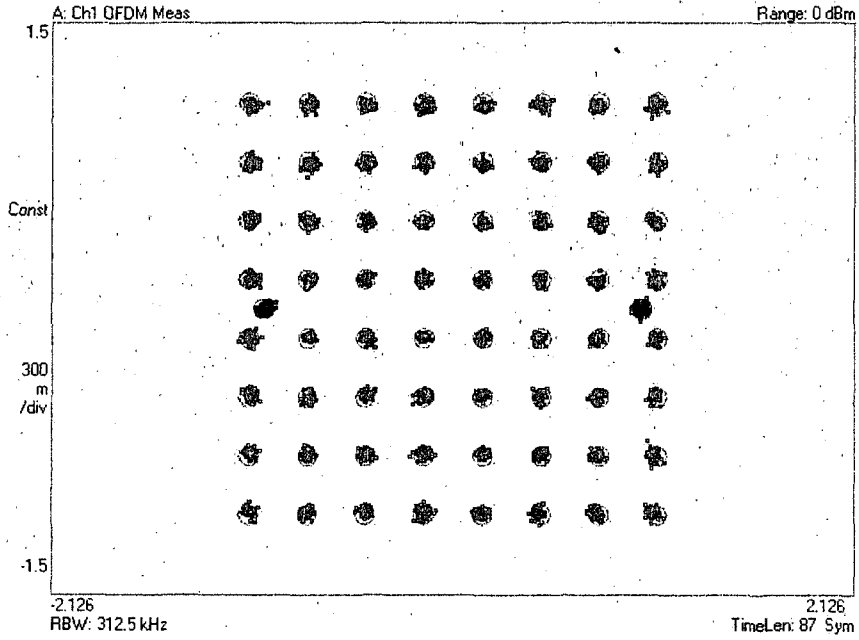


Figure 6.26: Constellation diagram corresponding to an EVM of 2.8%. The additional two points represent the tracking cursors from the test set.

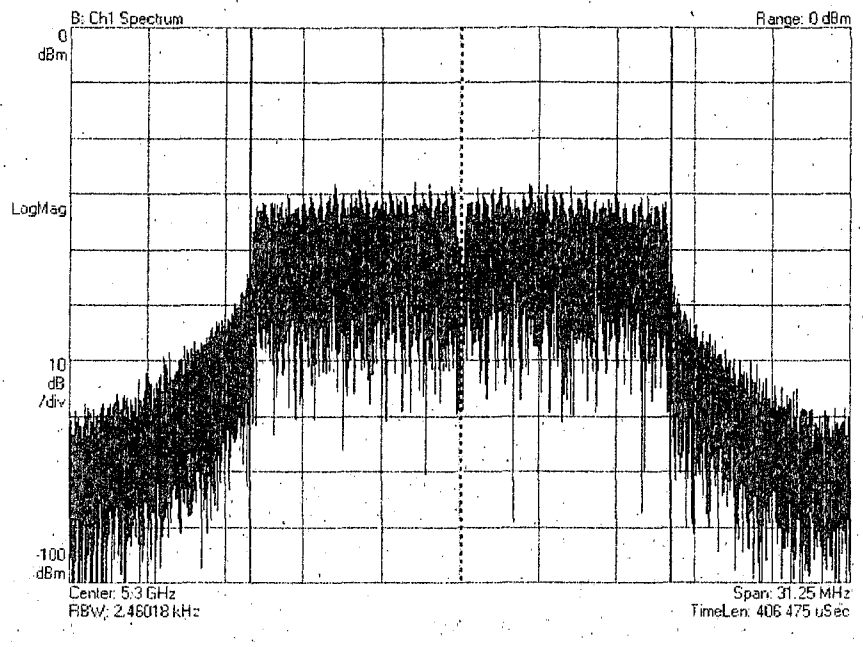


Figure 6.27: The output spectrum corresponding to an EVM of 2.8% measured at the output of the PA.

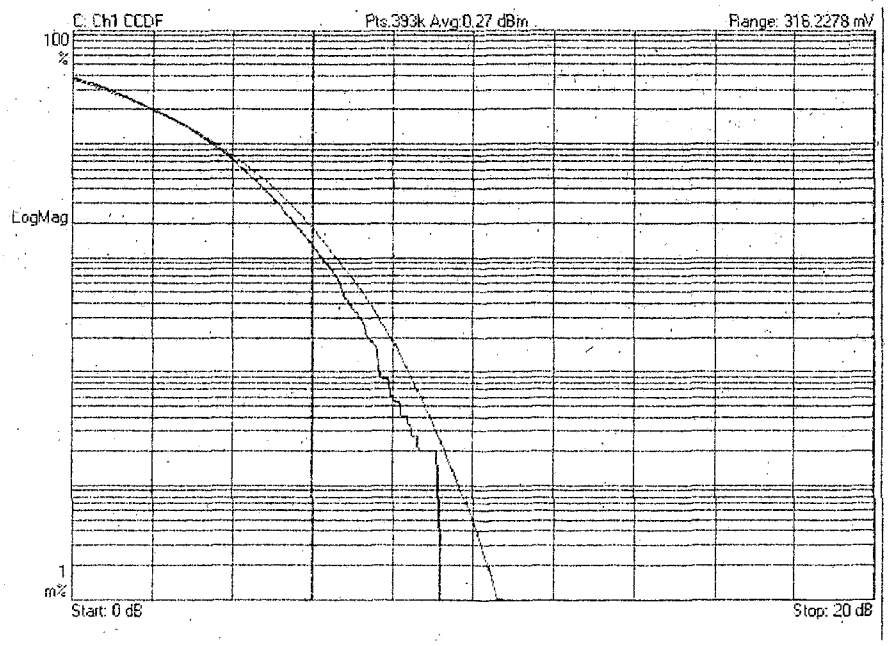


Figure 6.28: Measured PA CCDF output curve for a IEEE 802.11a 64-QAM, 54Mbit/s input signal. The corresponding EVM is 2.8%.

Operating frequency	4.8 GHz – 5.7 GHz					
Small-signal gain	26 dB					
Supply voltage	1	1.5	2.4	3.0	2.4 CW	V
Maximum output power	17.7	21.6	25	26.6	24.4	dBm
(5.3 GHz, Pin=10 dBm)	(60)	(145)	(316)	(457)	(275)	mW
Power-added efficiency (5.3 GHz, Pin=10 dBm)	15.6	22.5	24	15	22	%
Output stage collector current (RF on) + bias	288 + 6.4	327 + 6.4	443 + 6.4	800 + 6.4	422 + 6.4	mA
Output stage collector current (RF off) + bias	288 + 6.4	321 + 6.4	360 + 6.4	450 + 6.4	370 + 6.4	mA
Driver stage current (RF on) + bias	71 + 4.6	78 + 4.6	96 + 4.6	90 + 4.6	89 + 4.6	mA
Driver stage current (RF off) + bias	26 + 4.6	29 + 4.6	35 + 4.6	36 + 4.6	40 + 4.6	mA

Table 6.1: Performance Summary (T=300 K, 12.5 % duty cycle, 0.600 ms pulse width - CW: continuous wave.)

Chapter 7

A fully integrated 7-18 GHz Power Amplifier

The Chapters before have discussed some PA designs for the frequency area lower than 10 GHz. In this area lumped components like capacitors and inductors have proven to work for on-chip integration. As with higher frequencies, parasitic ca-

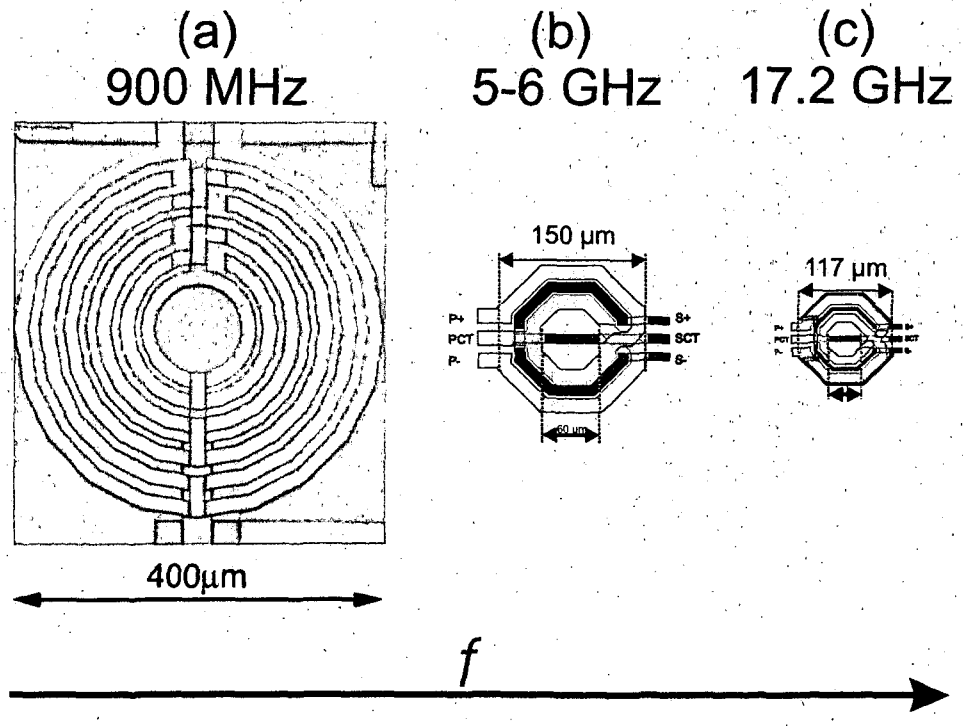


Figure 7.1: Transformer designs for increasing frequencies: (a) GSM interstage transformer [Simbürger 99] (b) 5-6 GHz Wireless LAN PAs [Bakalski 03,c, Bakalski 03,a] (c) 17 GHz PA [Bakalski 03,d]

pacitances to the substrate become more and more dominant, and required inductances are decreasing at the same time. Transformers must be smaller to achieve a parallel resonant circuit for the interstage matching at high frequencies (fig. 7.1). Additionally, fast SiGe technologies as presented in [Meister 03] operate with current densities up to 8 mA/□ which is about 8 times higher than the manufacturing process used in the design presented in Chapter 6.

Using transformers above the 20 GHz range for PA applications will not make sense, as reliability limitations for the metalization will make a successful design impossible. Further a higher accuracy for transformer models for frequencies above 20 GHz [Kehrer 01] would be necessary. But as on-chip transformers will be too small to face reliability requirements, microwave coupler structures like the Lange coupler [Lange 69] would make more sense. The PA presented here is an example for the limit in the usage of on-chip transformers.

7.1 Design overview

This section shows a design based on the same semiconductor technology (Chapter 3) as the amplifier presented in Chapter 6. Figure 7.2 shows the chip photograph of the fully integrated PA. With a die size of $0.8 \times 0.9\,\mathrm{mm}^2$ the amplifier is suited to be inserted into smallest packages. Thus, as described later, the chip was characterized by cleaving it directly onto a test PCB and direct wedge-wedge bonding [Nicolics 97].

Like the PA presented in Chapter 6 and [Bakalski 03,b] it is a PA with all matching elements integrated on-chip. The PA [Bakalski 03,d] has a maximum output power of 17.5 dBm at 2.4 V of supply voltage and has a small signal gain of 15 dB using two transistor stages. The SiGe bipolar technology used here is the Infineon B7HF process described in Chapter 3 and [Klein 99, Wolf 01].

The complete PA schematics is shown in fig. 7.3. The circuit elements on the die can be identified easily in the schematics: Two transformers at the input and in the mid of the die the interstage transformer. Further, the output BALUN with its three inductors realised as planar coils can be found.

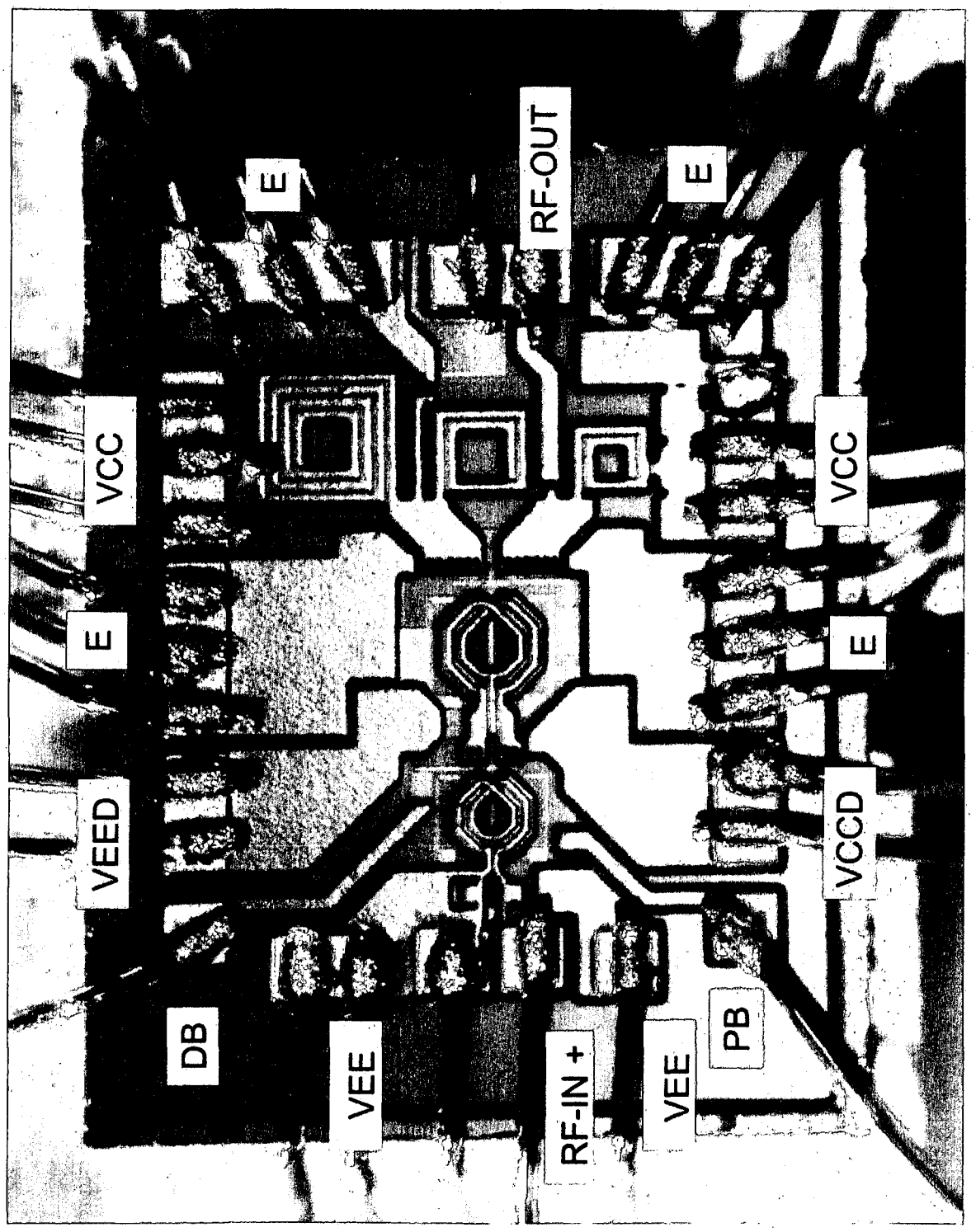


Figure 7.2: Die Photograph of the power amplifier (size: $0.8 \times 0.9\,\mathrm{mm}^2$).

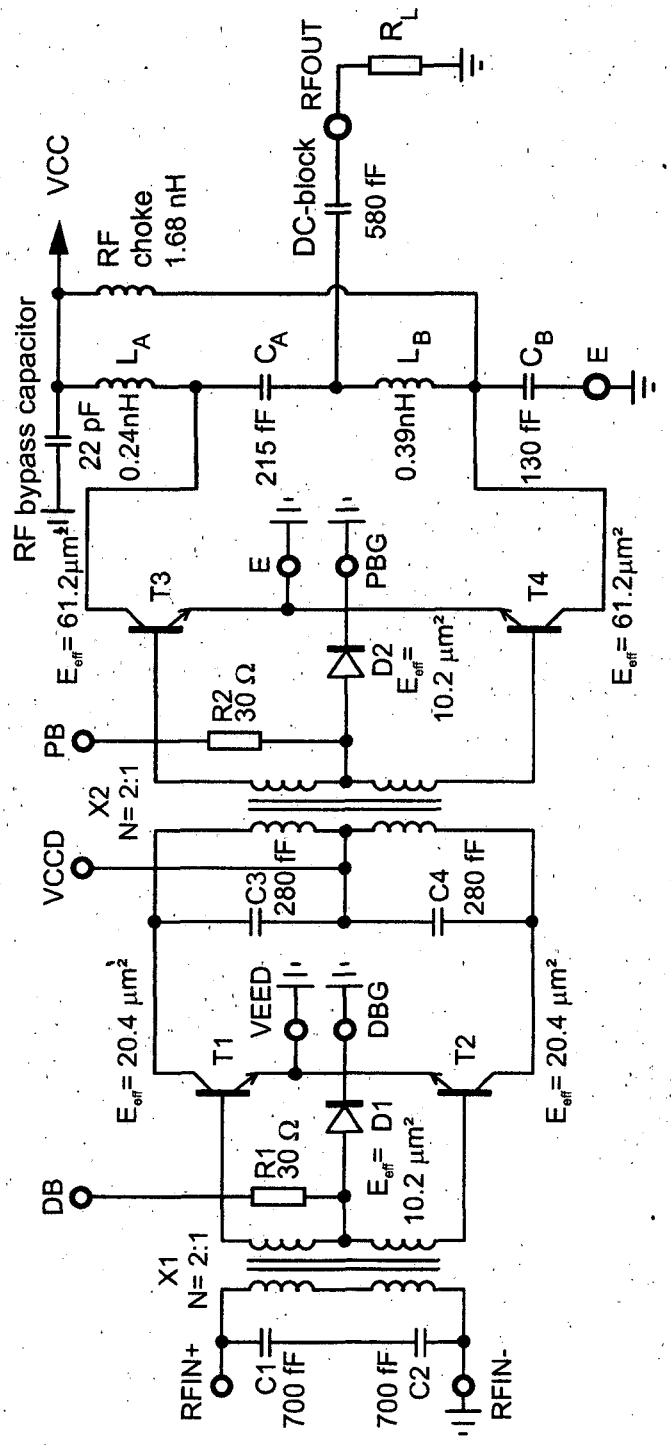


Figure 7.3: The push-pull power amplifier circuit. The PA uses an on-chip LC-BALUN as output matching network.

7.2 The PA core

Referring to fig. 7.3 the circuit consists of a transformer X1 as input BALUN, a driver stage T1 and T2, a transformer X2 as interstage matching network and the output stage T3 and T4. The bias of the driver stage and the output stage are set by current mirrors D1 and D2, respectively. The effective emitter area of T1, T2 is $20.4\,\mu m^2$ and $61.2\,\mu m^2$ for T3, T4 each.

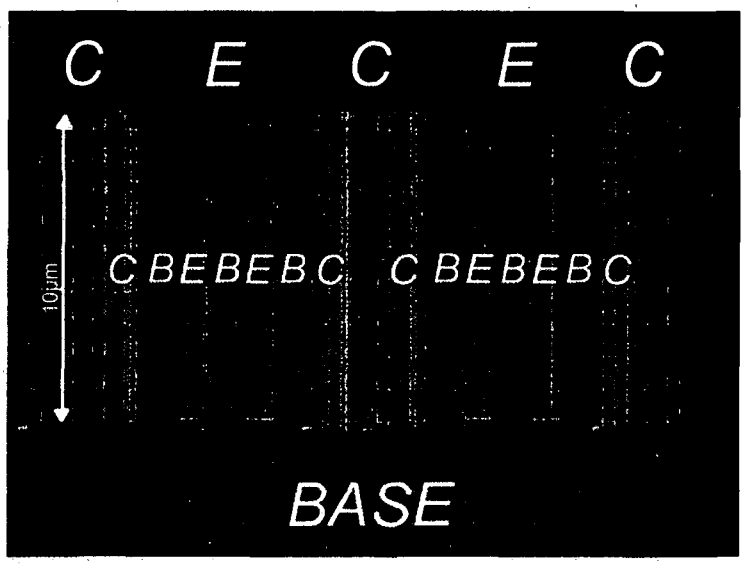


Figure 7.4: Layout of the driver stage transistors T1 and T2. The doubled transistor cell features a triple base, double emitter, double collector configuration. The emitter length is $10.2\,\mu m$ and the effective emitter width $0.5\,\mu m$.

Figure 7.4 shows the driver stage transistors T1 and T2. The transistor configuration is a triple base, double collector and double emitter layout. The triple base configuration lowers the base resistance of the transistor, while the use of the double emitter and collector reduces the parasitic capacitances compared with simple single base- collector- emitter transistors. The effective single emitter area is $0.5\,\mu m \times 10.2\,\mu m$. Two parallel transistors cells have the emitter area of $20.4\,\mu m^2$.

Figure 7.5 shows the layout of the output stage transistor. It is similar to the driver stage but with 6 transistor cells used in parallel. The resulting emitter area is $61.2\,\mu m^2$.

The function of the transformers and their tank circuits are similar to the designs presented before.

Figure 7.6 shows the input transformer used as input BALUN and input matching network. The turn ratio of X1 is N=2:1. The size is $94 \times 94\,\mu m^2$. The primary

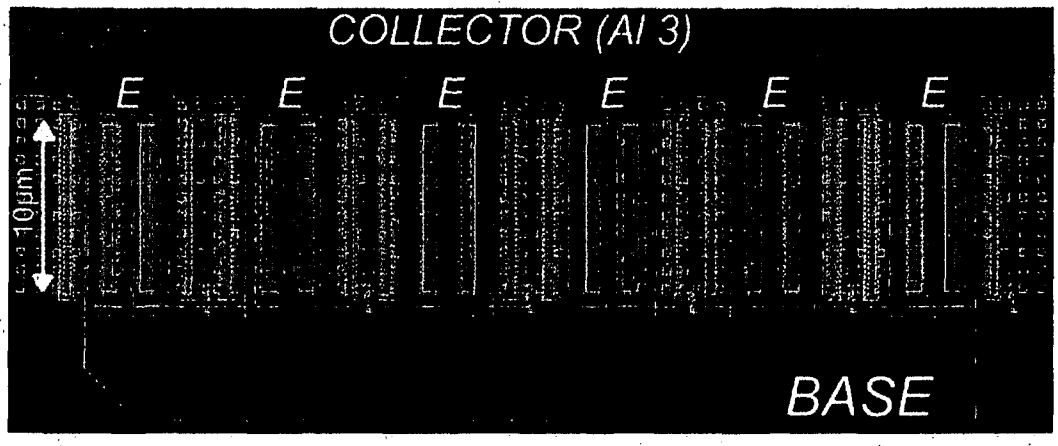


Figure 7.5: Layout of the output transistors T3 and T4. The 6 parallel connected transistor cells features a triple base, double emitter, double collector configuration. The emitter length is 10.2 μm and the effective emitter width 0.5 μm.

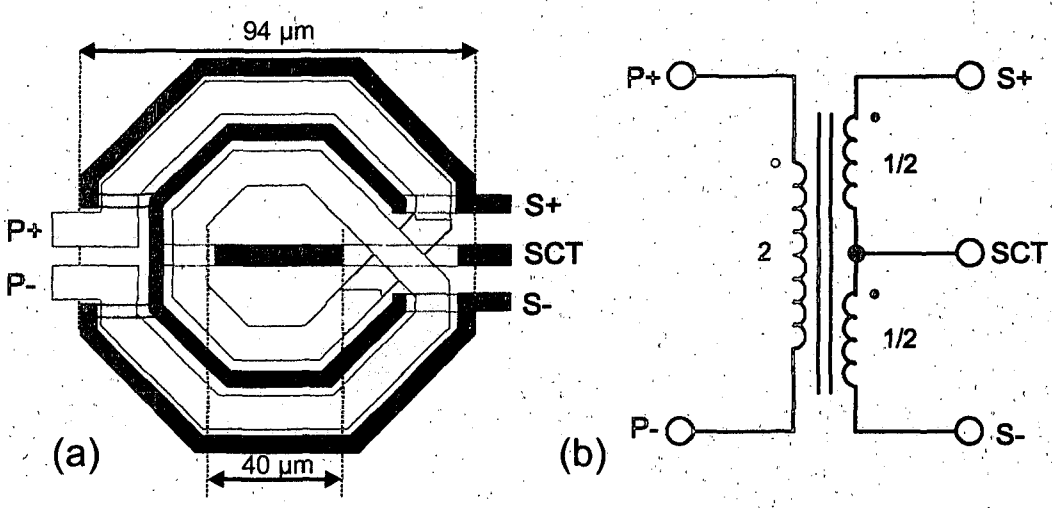


Figure 7.6: Input power transformer X1: (a) Winding scheme (b) Schematic symbol.

winding consists of 2 turns. Al 1 and Al 2 in fig. 3.19 are not used to reduce parasitic substrate coupling of the primary winding. Both turns of the secondary winding use also Al 3. The total coupling coefficient is k = 0.45 at 17.2 GHz. The low order equivalent circuit is found in fig. 7.7.

Figure 7.8 shows the interstage power transformer. X2 is connected as a parallel resonant device with two capacitors C3 and C4. C3 and C4 are connected to short the parasitic substrate capacities to the VCCD node. X2 has a turn ratio of N=2:1. The total coupling coefficient is k = 0.6 at 17.2 GHz. The size is $118 \times 118\,\mu m^2$. The primary winding consists of 2 turns with Al 3 and the secondary of 1 turn

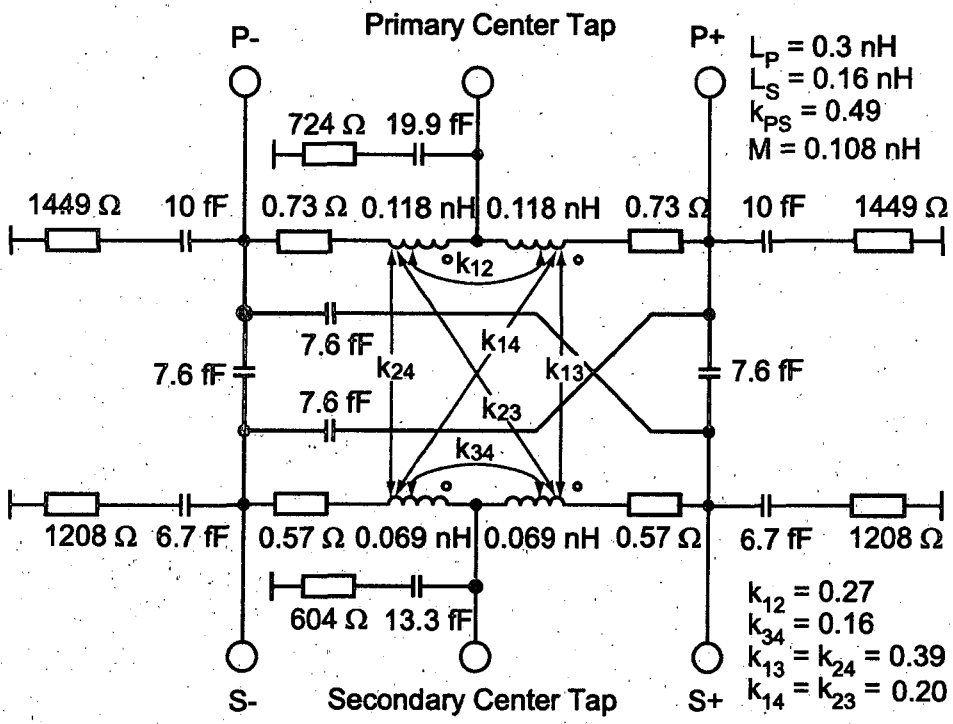


Figure 7.7: Input transformer X1 equivalent circuit.

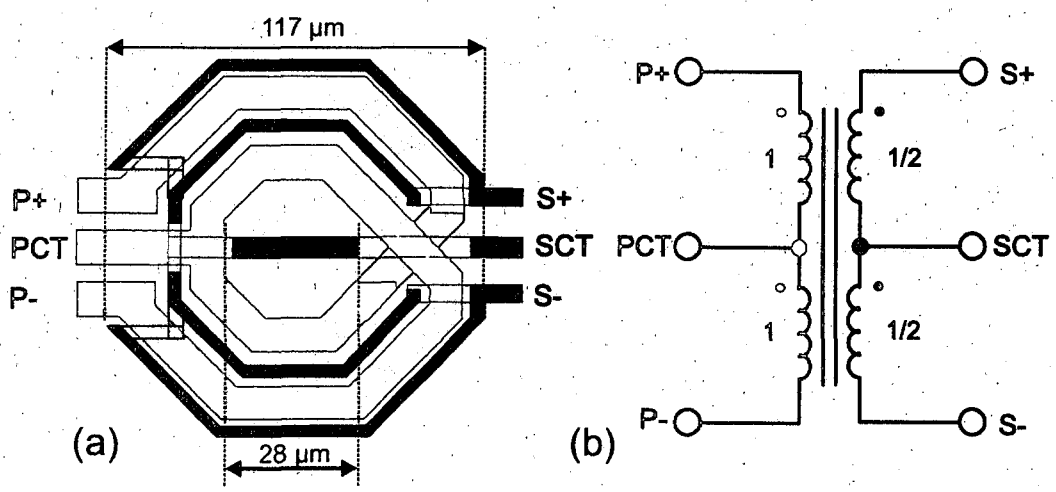


Figure 7.8: Interstage power transformer X2: (a) Winding scheme (b) Schematic symbol.

also using Al 3. Figure 7.9 shows the low order equivalent circuit.

The interstage transformer in this design suffers from a major trade-off between model accuracy and current transformation ratio:

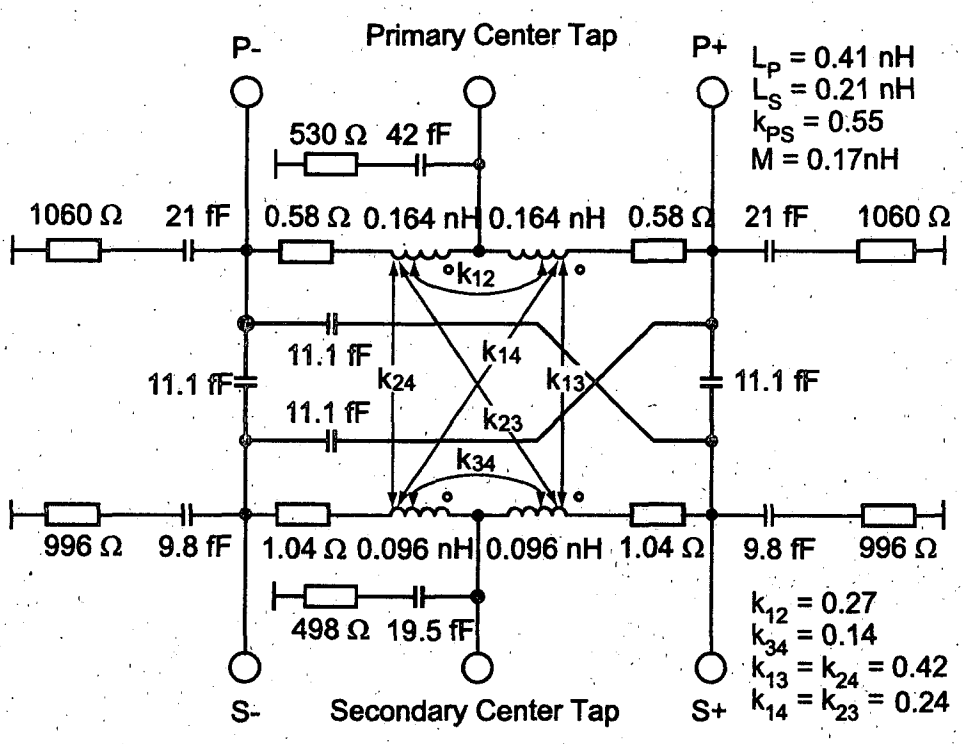


Figure 7.9: Interstage transformer X2 equivalent circuit.

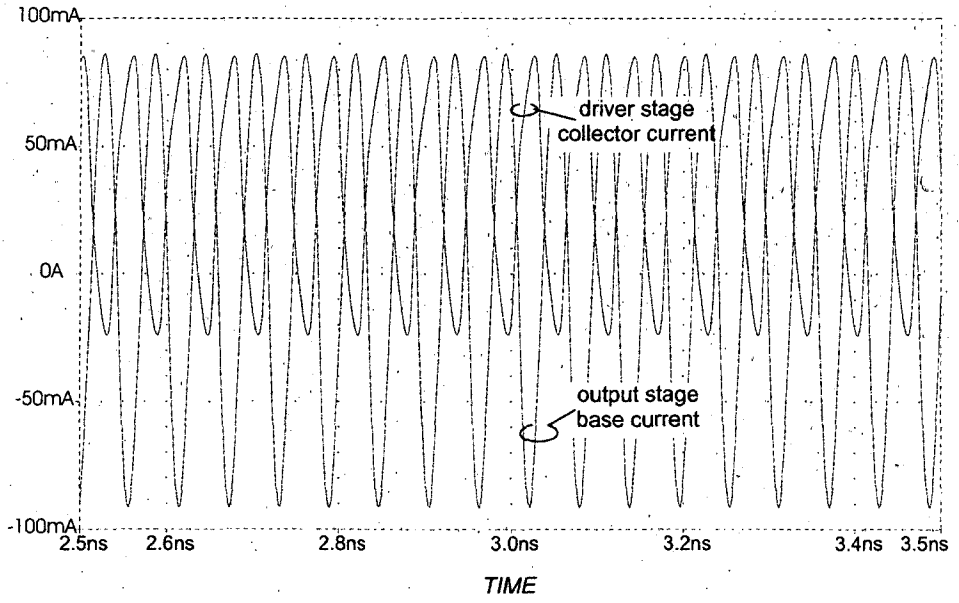


Figure 7.10: Current transformation due to transformer X2: The transformation ratio is only about 1.8.

- Tuning to the resonance frequency: As the PA is designed for an operating frequency of 17 GHz, the LC-tank has to be tuned to about 17 GHz. This implies, that the driver transistor area in combination with the transformer is limiting the transformer area (to minimize the parasitic substrate capacitance) and the transformer is limiting the transistor area.

- Due to the area limitation, the current transformation ratio is limited. If eqn. 5.2 is considered, the quality factor Q of the resonance circuit will be low, as the shunt capacitance and the coupling coefficients are low due to the limited area. Figure 7.10 shows the simulation of the currents flowing into P+ (driver stage collector) and S+ (output stage base). Even as the transformer uses a sliced structure, the current transformation ratio is only about 1.8.

7.3 The integrated LC-BALUN output matching network.

Similar to the 5.3 GHz design, an LC-BALUN was chosen for on-chip integration. As sketched in fig. 6.18 the bondwire will lead to an inductive load at the LC-BALUN output. As the frequency is now more than doubled the bondwire inductance cannot be compensated as good as in the 5 GHz case. Figure 7.11 shows the used output equivalent circuit for the frequency range of 9 to 20 GHz.

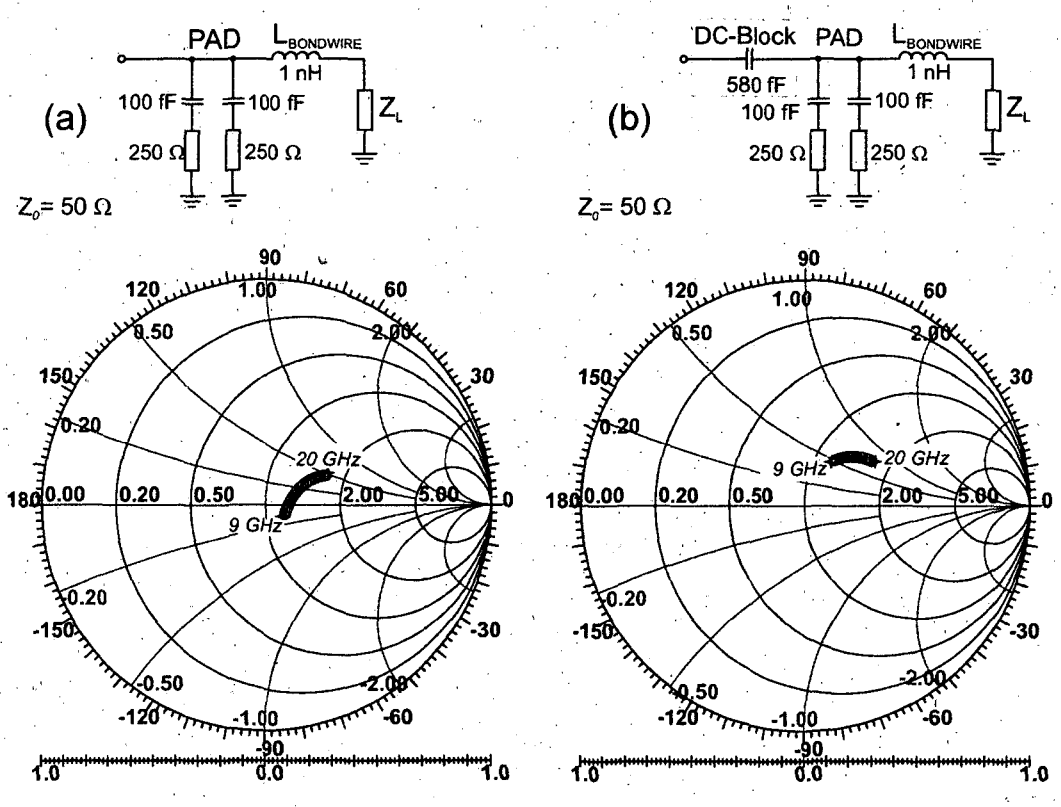


Figure 7.11: (a) Resulting load for the connection parasitics consisting of the pad and the bondwire (b) with additional DC-Block.

Additionally to the DC-block, the BALUN-bridge is operated imbalanced with two different inductances. Their layout and the equivalent circuit is shown in fig. 7.12.

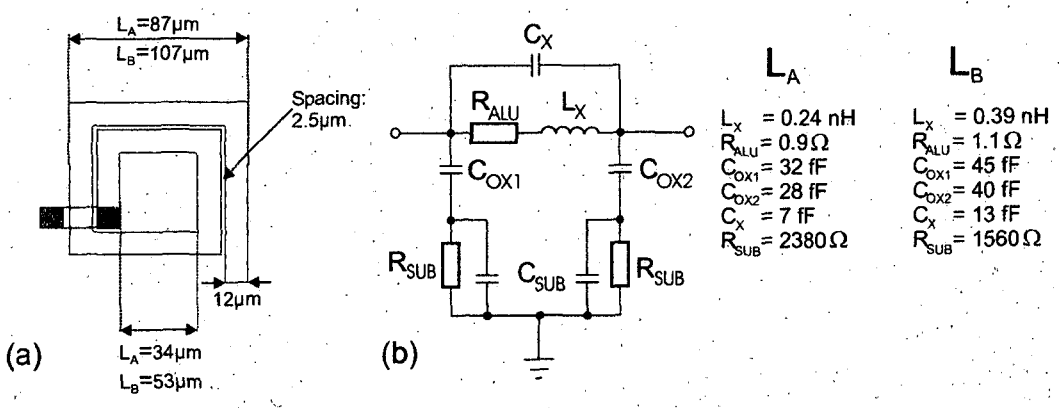


Figure 7.12: (a) Coil layout (b) Equivalent circuit.

7.4 Experimental results

For the characterization a test PCB with two 50 Ω microstrip lines for in and output was used (fig. 7.13). The die is attached with a conductive epoxy to the substrate and is bonded directly on the board. The PA in- and output are connected to 50 Ω microstrip transmission lines. The connections used here were standard SMA-connectors.

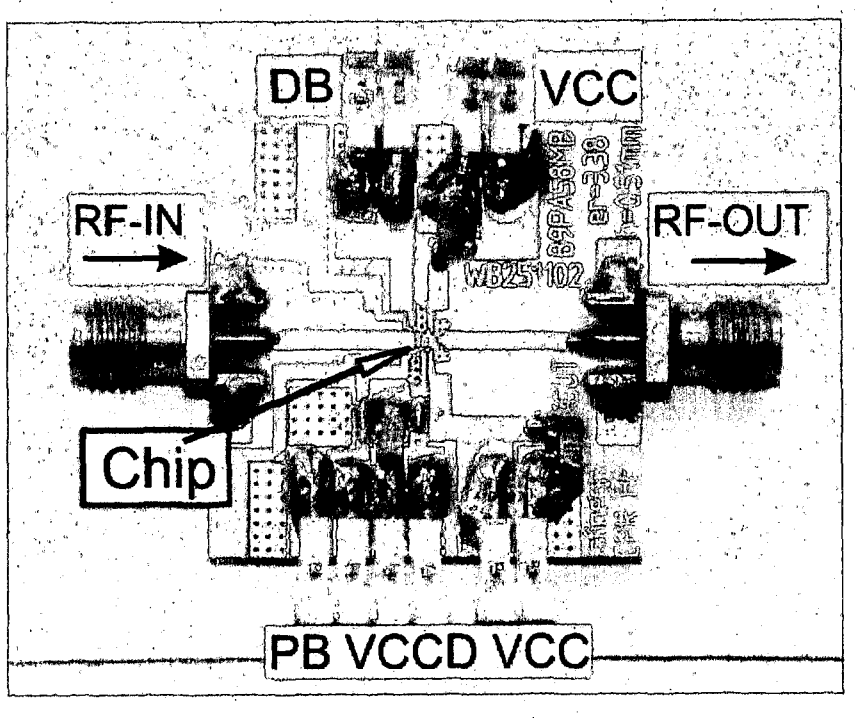


Figure 7.13: Photograph of the power amplifier test board (size: $30 \times 30\,\mathrm{mm}^2$).

The PCB substrate parameters are $\varepsilon_r = 3.38$, $\tan\delta = 0.0027$ and the dielectric thickness is 0.51 mm (Rogers RO 4003). The metalization layers consist of 18 μm copper with a nickel diffusion barrier and 5 μm gold on top for bonding.

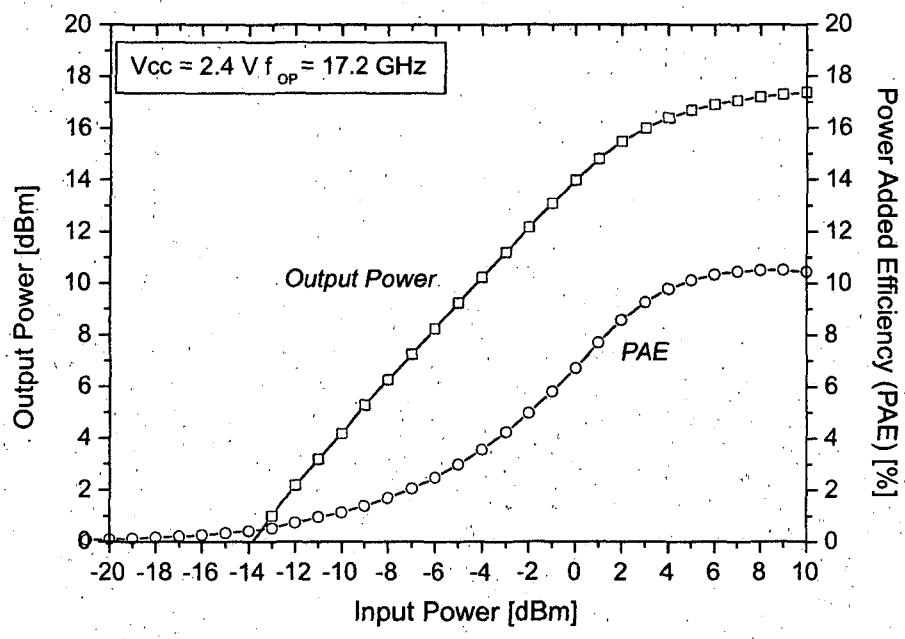


Figure 7.14: Measured power transfer characteristic (T=300 K, 12.5 % duty cycle, 0.600 ms pulse width).

The power amplifier was characterized operating in a pulsed mode with a duty cycle of 12.5% with a pulse width of 600 μs as well as for CW operation (Tab. 7.1).

Figure 7.14 shows the measured power transfer characteristic. The maximum output power is 17.5 dBm at 2.4 V supply voltage and 17.2 GHz. The maximum PAE is 11.2%. Figure 7.15 shows the characteristic vs. the supply voltage.

Figure 7.16 shows the frequency response. The frequency response shows a steady PAE and output power level in a frequency range from f = 7 GHz to 18 GHz. Considering the f_{max} of 75 GHz and the f_T of 72 GHz the results show the limit of the semiconductor technology.

The linearity was investigated using a two-tone measurement setup as described in section 2.1.3 using the test setup in fig. 2.4. Figure 7.17 shows the resulting intercept point 3rd order (IP3) of 25.7 dBm. Tab. 7.1 shows the performance summary.

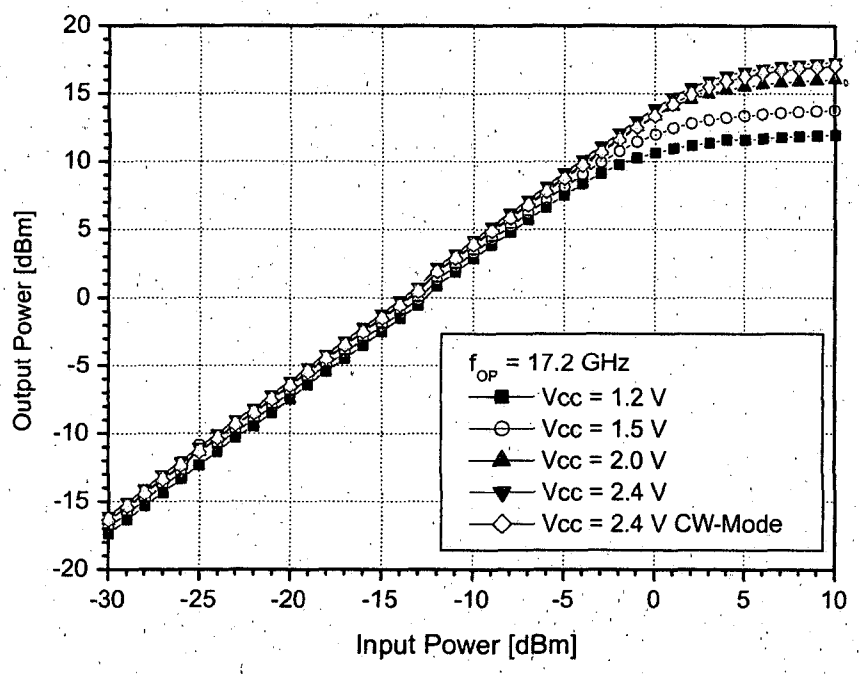


Figure 7.15: Measured power transfer characteristic vs. supply voltage.

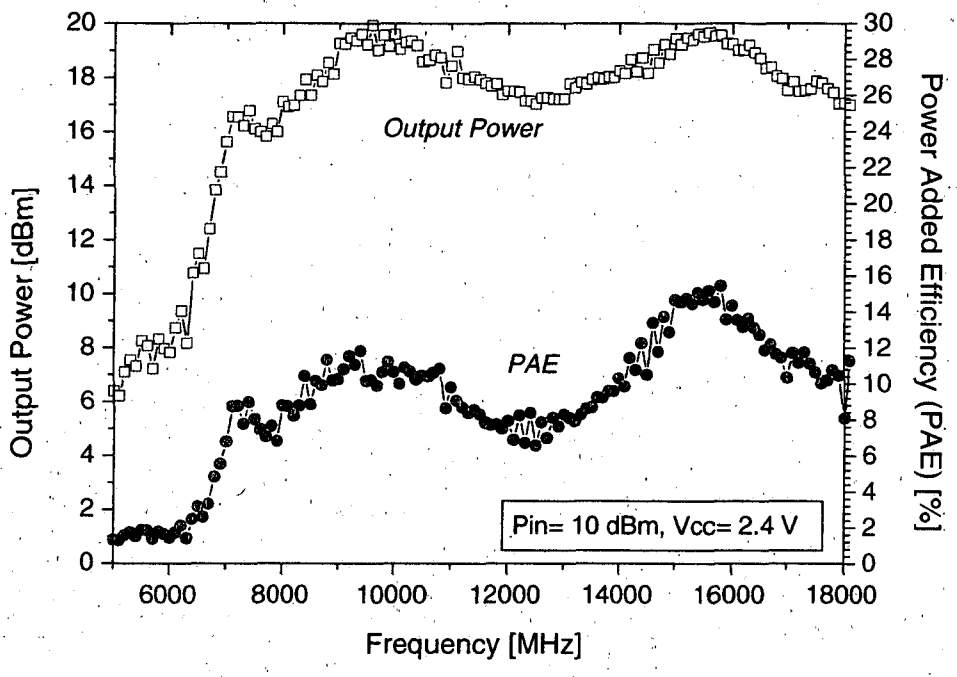


Figure 7.16: Measured power amplifier frequency characteristic.

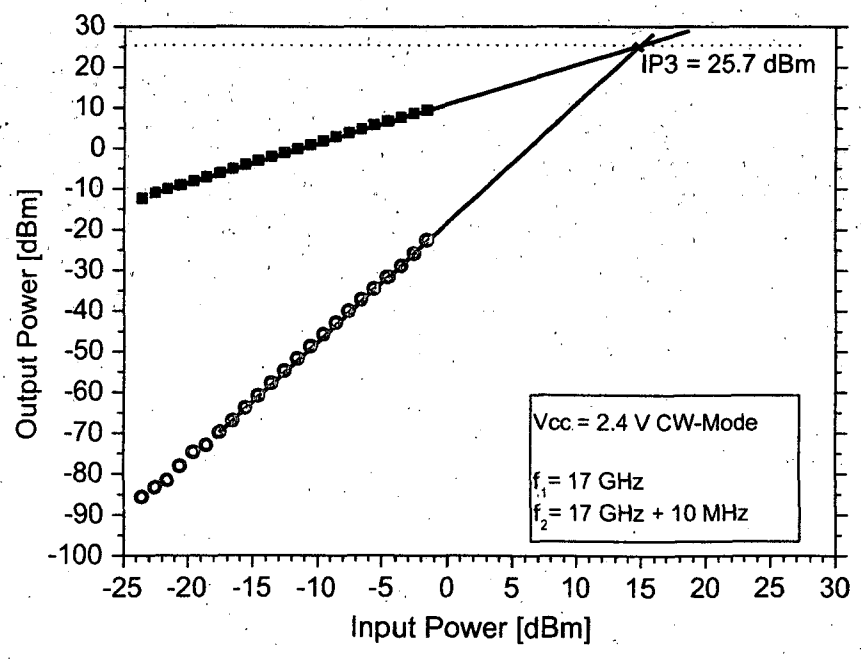


Figure 7.17: Two-Tone measurement with 10 MHz offset.

Operating frequency	7 GHz – 18 GHz					
Small-signal gain	15 dB					
OIP3 (Vcc = 2.4 V CW)	25.7 dBm					
Supply voltage	1.2	1.5	2	2.4	2.4 CW	V
Maximum output power	12	13.9	16.1	17.5	17	dBm
(17.2 GHz, Pin=10 dBm)	(15.8)	(24.5)	(41)	(56)	(50)	mW
Power-added efficiency (17.2 GHz, Pin=6 dBm)	9.5	10.3	10.6	11	10.1	%
Output stage collector current (RF on) + bias	71 + 2	88 + 2	115 + 2	135 + 2	130 + 2	mA
Output stage collector current (RF off) + bias	32 + 2	33 + 2	34 + 2	36 + 2	38 + 2	mA
Driver stage current (RF on) + bias	53 + 8	60 + 8	70 + 8	75 + 8	72 + 8	mA
Driver stage current (RF off) + bias	34 + 8	36 + 8	40 + 8	44 + 8	44 + 8	mA

Table 7.1: Performance Summary (T=300 K, 12.5 % duty cycle, 0.600 ms pulse width - CW: continuous wave.)

Chapter 8

Conclusion and Outlook

Within this thesis SiGe bipolar based power amplifiers (PA) in the range of 2 - 18 GHz have been demonstrated. All of them are push-pull type designs using on-chip planar transformers. Different techniques of output matching dependent on the operating frequency have been introduced. For the 2.4 GHz ISM band a microstrip based output BALUN was used, while for the frequencies above 5 GHz an on-chip BALUN was integrated. The 5 GHz PA further shows similar performance levels considering efficiency and linearity as III-V-technologies based technologies. The 17 GHz PA is a demonstrator for the limits in the use of on-chip transformers. As current densities for high speed SiGe technologies increase and the optimum outlines for the transformers decrease, we find the point where a real optimum can no more be found. Due to the reduced bulk wavelength for higher frequencies, other matching elements like on-chip transmission lines and stripline coupler become more and more of advantage. Similar structures are typically found in III-V based amplifiers for the 70-100 GHz range. The presented PAs show that Si BJTs and SiGe HBTs can be used for mass products, and the field of RF PAs is not limited to III-V technologies.

In summary the main results are:

- A highly integrated 2.4 GHz ISM PA with a minimum of external components [Bakalski 02,e, Bakalski 02,d, Bakalski.02,a] using a microstrip based output BALUN has been presented. It shows outstanding efficiency of over 50% at 2 V of supply voltage [Bakalski 02,b] at a saturated output power level of 400 mW.

- The first fully-integrated wireless LAN PA for the 5 GHz band in SiGe-bipolar is presented. It fulfills the needs on linearity required for Wireless LAN systems. Due to the integrated BALUN it is the first Si-based PA free of any external matching components including DC-block capacitors [Bakalski 03,b, Bakalski 03,c]. Further it shows almost perfect in- and output matching. It further shows efficiency levels comparable with solutions

requiring expensive external networks or ceramic or laminate substrates [Bakalski 03;a, Ilkov 03,b, Simbürger 01, Bakalski 02,c].

- The first reported SiGe-bipolar PA working up to 18 GHz. It also features the integration of all matching components on-chip [Bakalski 03,d]. It is an example for the technological limits as it rises up to an f_{max}/f_{op} of only about 4.2. It is further an example for the limits in the usage of on-chip transformers.

For the future, further improvements in the PA designs are always desired. Considering fully integrated PAs, a thick copper metalization will help to improve the quality factors and thus help to reduce losses in the transformers and the BALUN structure.

Looking on the high frequencies, we find future PA applications in automotive radar systems. Operated at 24 GHz and 77 GHz, it will be the next challenge in the design of RF building blocks. Especially for PAs the trade-off between breakdown voltages and high speed transistors will require very accurate breakdown models. Further, on-chip power combiners become feasible but lossy. A new challenge will be the focus on efficient power combining schemes.

Another major market are the mobile phones: Dominated today by III-V technologies, several publications [Simbürger 99, Baltus 01] did show the possibility to realise such PAs in Si-bipolar based processes. Considering products, transistors have to be improved in the field of ruggedness, hence higher breakdown voltages have to be realised. Another point is the necessity of higher integration of PAs with other building blocks such as antenna switches on laminate carriers for mobile phone PAs. A further space reduction and increasing efficiencies are future tasks on the development on Si-based mobile phone PAs such as for UMTS and GSM.

Acknowledgements

I would like to express sincere appreciation to my advisor Prof. Dr. Arpad L. Scholtz for his guidance, support and insight throughout the study. My gratitude also goes to Prof. Dr. Gottfried Magerl for critical reading of the manuscript.

I would like to express my thanks to Werner Simbürger and his team for enabling this work. The work presented was supported by INFINEON Technologies AG, Corporate Research, Department for High Frequency Circuits, Munich.

I am also grateful to my colleagues Herbert Knapp, Martin Wurzer and Hans-Dieter Wohlmuth for informative discussions and for their help during the measurements. My gratitude also goes to Mirjana Rest for supporting me with the layouts, to Ronald Thüringer, Christoph Kienmayer, Werner Perndl and Daniel Kehrer for useful comments and help. Further I want to thank Robert Sedlmaier from Infineon Secure Mobile Solutions (SMS) for the support and possibility to use the Wireless LAN test set.

Finally, I would like to take this opportunity to thank my parents, my brother Roland for their encouragement, unshakable faith and valuable support in any situation of my life.

Curriculum vitae

Personal

Name	:	Winfried Bakalski
Date of birth	:	November 29, 1973
Place of birth	:	Augsburg, Germany
Marital status	:	unmarried
Nationality	:	German

Education

june, 1993	:	Abitur. Rudolf-Diesel Gymnasium Augsburg, Germany (Mathematic-scientifc Grammar school)
october, 2001	:	Dipl.-Ing. degree in Communications Engineering with distinction, Technical University of Vienna, Karlsplatz 13, A-1040 Vienna, Austria. Thesis: "Integrated 2.45 GHz Power Amplifier".

Experience

1994	:	Industrial mechanical training at Haindl Papier, Augsburg, Germany (today: UPM Kymene) and Erhard&Leimer Apparatebau, Augsburg, Germany
1995-1998	:	Vacation work as chemical assistant at PCI Polychemie Augsburg, Germany. Field: Development of floor covering materials. Vacation work as mechanic at Erhard&Leimer Apparatebau, Augsburg, Germany Field: Production of textile industry machines. Brauhaus Riegele, Augsburg, Germany.
april 1999 - september 1999	:	Member of the technical staff at Philips Consumer Products, ICAP, Vienna, Austria. Field: Measurements setup and design of vacuum flourescent display driver circuits.
march 2001 - october 2001	:	Diploma thesis at Infineon Technologies AG, Corporate Research, CPR HF. Thesis: "Integrated 2.45 GHz Power Amplifier"
november 2001 to now	:	PHD student at Infineon Technologies AG, Corporate Research, CPR HF, Field: Design of Microwave Power Amplifiers.

Further skills:

Languages:	German, English, French
Other:	German driving licence class 3, Amateur radio licence class 1
Main project focus at Infineon, Corporate Research :	RF Power Amplifiers circuit R&D. Advanced packaging. Support to the IFX business units, support on Wireless LAN PA chip PMB8825.

Address :

Metzstr. 26
D-86316 Friedberg, Germany
Tel.: +49 (0) 821 663086, Fax.: +49 (0) 821 667734
Mob.: +49 177 6910609
Email.: bakalski@web.de

Business address:

INFINEON Technologies AG
Corporate Research, Dept. CPR HF
Otto-Hahn-Ring 6
D-81739 Munich, Germany
Tel.: +49 (0)89 234 45102, Fax.: +49 (0)89 234 47069
Email.: winfried.bakalski@infineon.com
http://www.infineon.com/

Friedberg, November 2003

Bibliography

[3GPP 03] 3GPP, "3rd Generation Partnership Project; Technical Specification Group GSM/EDGE Radio Access Network; Radio transmission and reception - 3GPP TS 45.005 V6.2.0 (2003-04)", www.3gpp.org, april 2003.

[Agilent 88] Agilent, "Broadband microstrip mixer design - the butterfly mixer", *Agilent Technologies Application Note*, vol. 976, pp. 4–6, 1988.

[Agilent 02,a] Agilent, "Characterizing Digitally Modulated Signals with CCDF Curves", Application Note from http://www.agilent.com, 2002.

[Agilent 02,b] Agilent, "Using Error Vector Magnitude Measurements to Analyze and Troubleshoot Vector-Modulated Signals", Agilent PN 89400-14 product note from http://www.agilent.com, 2002.

[Albulet 01] Mihai Albulet, *RF Power Amplifiers*, Noble Publishing, 1st edition, 2001.

[Allers 03] K.-H. Allers, Brenner, P., and Schrenk, M., "Dielectric Reliability and Material Properties of Al_2O_3 in Metal Insulator Metal capacitors (MIMCAP) for RF Bipolar technologies in comparison to SiO_2,SiN and Ta_2O_5", *in Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting*, Toulouse, France, September 2003. IEEE.

[Allison 79] Richard Allison, "Silicon Bipolar Microwave Power Transistors", *IEEE Transactions on Microwave Theory and Techniques*, vol. 27, pp. 415–422, may 1979.

[Aoki 01] I. Aoki, Kee, S. D., Rutledge, D., and Hajimiri, A., "A 2.4 GHz, 2.2 W, 2 V fully integrated CMOS circular geometry active transformer power amplifier", *in IEEE Custom integrated circuits conference*, San Diego, May 2001. IEEE.

[Ashburn 88] P. Ashburn, *Design and Realization of Bipolar Transistors*, John Wiley & Sons, Chicester, 1988.

[Ashby 96] K.B. Ashby and I. A. Koullias, "High Q Inductors for Wireless Applications in a Complementary Silicon Bipolar Process", *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 4–8, Jan 1996.

[Aufinger 01] Klaus Aufinger, *Physikalische Modellierung der Rauscheigenschaften von Silizium- und Silizium-Germanium-Höchstfrequenz-Bipolartransistoren*, PhD thesis, Leopold-Franzens-University Innsbruck, Austria, may 2001.

[Bakalski 01] Winfried Bakalski, "Integrated 2.45 GHz Power Amplifier", Master's thesis, Technical University of Vienna, october 2001.

[Bakalski 02,a] W. Bakalski, "Baluns for Microwave Applications", *VHF-Communications*, vol. 3 and 4, 2002.

[Bakalski 02,b] W. Bakalski, Simbürger, W., Thüringer, R., Rest, M., Ahrens, C., Kühn, C., and Scholtz, A.L., "A Monolithic 2.45 GHz Power Amplifier in SiGe-Bipolar with 0.4 W Output Power and 53 %PAE at 2 V", *in Proceedings of the 28th European Solid-state Circuit Conference*, pp. 223–225, Firenze,Italy, September 2002. IEEE.

[Bakalski 02,c] W. Bakalski, Simbürger,W., Kehrer,D., Wohlmuth,H.-D., Rest,M., and Scholtz,A.L., "A monolithic 2.45 GHz, 0.56 W power amplifier with 45 % PAE at 2.4 V in standard 25 GHz f_T Si-bipolar", *in Proceedings of IEEE International Symposium on Circuits and Systems*, Scottsdale, Arizona, May 2002. IEEE.

[Bakalski 02,d] W. Bakalski, Simbürger,W., Knapp,H., and Scholtz,A.L., "Baluns für Mikrowellenanwendungen", *UKW-Berichte*, vol. 1 and 2, pp. 51–57 and 77–85, 2002.

[Bakalski 02,e] W. Bakalski, Simbürger,W., Knapp,H., and Scholtz,A.L., "Lumped and Distributed Lattice-type LC-Baluns", *in Proceedings of IEEE International Microwave Symposium*, Seattle, June 2002. IEEE.

[Bakalski 03,a] W. Bakalski, Ilkov, N., Dernovsek, O., Matz, R., Simbürger, W., Weger,P., and Scholtz, A.L., "A 5-6.5 GHz LTCC Power Amplifier Module with 0.3W at 2.4V in Si-bipolar", *IEE Electronics Letters*, vol. 39, pp. 375–376, february 2003.

[Bakalski 03,b] W. Bakalski, Simbürger, W., Thüringer, R., Vasylyev, A., and Scholtz, A.L., "A fully integrated 5.3 GHz, 2.4 V, 0.3 W SiGe-Bipolar Power Amplifier with 50 Ω output", *in Proceedings*

of the 29th European Solid-state Circuit Conference, Estoril,Portugal, September 2003. IEEE.

[Bakalski 03,c] W. Bakalski, Simbürger,W., Thüringer,R., Wohlmuth,H.D., and Scholtz,A.L., "A fully integrated 4.8-6 GHz Power Amplifier with on-chip output balun in 38 GHz-f_T Si-Bipolar", *in IEEE International Microwave Symposium*, Philadelphia, June 2003. IEEE.

[Bakalski 03,d] W. Bakalski, Vasylyev, A., Simbürger, W., Thüringer, R., Wohlmuth, H.-D., Scholtz, A.L., and Weger, P., "A fully integrated 7-18GHz Power Amplifier with on-chip output balun in 75 GHz-f_T SiGe-Bipolar", *in Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting*, Toulouse, France, September 2003. IEEE.

[Baltus 01] P. Baltus and van Bezooijen, A., "Design considerations for rf power amplifiers demonstrated through a gsm/edge amplifier module", *in AACD 2001 Workshop*. AACD, april 2001.

[Banerjee 02] M. Banerjee and Desquiotz, R., "Generating 3GPP Mulit Carrier Signals for Amplifier Tests with R&S SMIQ03HD and WINIQSIM", Application Note from http://www.rohde-schwarz.com, 2002.

[Bartsch 99] Hans-Jochen Bartsch, *Taschenbuch mathematischer Formeln*, Fachbuchverlag Leipzig im Carl-Hanser Verlag, Munich,Vienna, 18th edition, 1999.

[Berkner 02] Jörg Berkner, *Kompaktmodelle für Bipolartransistoren*, Expert Verlag, first edition, 2002.

[Böck 96,a] J. Böck, Felder, A., Meister, T.F., Franosch, M., Aufinger, K., Wurzer,M., Schreiter, R., Boguth, S., and Treitinger, L., "A 50GHz Implanted Base Silicon Bipolar Technology with 35GHz Static Frequency Divider", *Technical Digest of IEEE Symposium on VLSI Technologies*, pp. 108–109, 1996.

[Böck 96,b] Josef Böck, *Emitter-Basis-Dotierstoffprofile für Höchstfrequenz-Silizium-Bipolartransistoren, Dissertation*, PhD thesis, Fakultät Physik, Universität Regensburg, Germany, 1996.

[Bonek 00] Ernst Bonek, "Wellenausbreitung 1", Script for the course Wellenausbreitung 1 at the Technical University of Vienna, october 2000.

[BT SIG] BT SIG, "Specification of the Bluetooth System,Core, Version 1.1", Bluetooth Special Interest Group, SIG, 2001.

[Chang 03] H.-Y. Chang, H. Wang, M. Yu, and Y. Shu, "A 77-GHz MMIC Power Amplifier for Automotive Radar Applications", *IEEE Microwave and wireless components letters*, vol. 13, pp. 143–145, april 2003.

[Cheung 98] D. T. S. Cheung, Long, J.R., Hadaway, R.A., and Harame, D.L., "Monolithic Transformers for Silicon RF IC Design", *in 1998 Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 105–108, Minneapolis, 27-29 Sept. 1998. IEEE.

[Cooke 71] Harry F. Cooke, "Microwave Transistors: Theory and Design", *Proc. IEEE*, vol. 59, pp. 1163–1181, august 1971.

[Cripps 99] Steve C. Cripps, *RF Power Amplifiers for Wireless Communications*, Artech House, Norwood, MA 02062, first edition, 1999.

[Cuno 03] H.-H. Cuno and Graf, U., "ADR-100A - Schrittmacher für Zukunftstechnik", *CQ DL*, vol. 3, pp. 148–151, 2003.

[Ebers 54] J.J. Ebers and J.L. Moll, "Large-Signal Behavior of Junction Transistors", *Proceedings of IRE 42*, pp. 1761–1772, Dec. 1954.

[El-Hamamsy 94] S. A. El-Hamamsy, "Design of High-Efficiency RF Class-D Power Amplifier", *IEEE Transactions on Power Electronics*, vol. 9, pp. 297–308, May 1994.

[Endo 84] N. Endo, Tanno, K., A. Ishitani, Y. Kurogi, and H. Tsuya, "Novel Device Isolation Technology with Selective Epitaxial Growth", *in IEEE Transactions on Electron Devices ED-31(9)*, pp. 1283–1288. IEEE, 1984.

[Flecker 84] Harald Flecker, "Ein Rauschgenerator mit definierter Rauschleitung für Anwendungen bis in den Mikrowellenbereich", *UKW-Berichte*, vol. 2, pp. 73–81, 1984.

[Freyer 87] Ulrich G.P. Freyer, *Anpassung und Fehlanpassung*, Franzis-Verlag, Munich, first edition, 1987.

[Gabl 97] Reinhard Gabl, "Spice Modeling of C-E-Breakdown for High-Power Bipolar Applications", Technical report, SIEMENS, ZT ME 2, now Infineon CPR HF (Corporate Research) and CL (Corporate Logic), Otto-Hahn-Ring 6, 81739 Munich, 1997.

[Gonzales 84] G. Gonzales, *Microwave Transistor Amplifiers Analysis and Design*, Prentice Hall, Englewood Cliffs, NJ 07632, 1984.

[Gottlieb 87] I.M. Gottlieb, *Power Control with solid-state devices*, TAB Books, 1987.

[Graaf 90] H.C. Graaf and F.M. Klaasen, *Compact Transistor Modelling for Circuit Design*, Springer-Verlag, Wien, first edition, 1990.

[Greenhouse 74] H. M. Greenhouse, "Design of planar rectangle microelectronic inductors", *IEEE Trans. Parts, Hybrids, Packag.*, vol. 10, pp. 101–109, June 1974.

[Grover 46] F. W. Grover, *Inductance Calculations*, Dover Publications Inc, New York, 1946.

[Gummel 70] H.K. Gummel and Poon, H.C., "An Integral Charge Control Model of Bipolar Transistors", *The Bell System Technical Journal*, may/june 1970.

[Hammerstad 75] E.O. Hammerstad, "Equations for microstrip circuit design", *Proc. of the European Microwave Conference*, vol. , pp. 261–272, 1975.

[Hastings 01] Alan Hastings, *The Art of Analog Layout*, Prentice Hall, New Jersey, first edition, 2001.

[Higashiyama 95] Katsuhiko Higashiyama, "Spice Simulation of a Variant Class H Hybrid Power Module", *in Proceedings of the International Manufacturing Technology Symposium*, pp. 477–480. IEEE, 4-6 Dec. 1995.

[Hlawatsch 99] Franz Hlawatsch, "Analog and Digital Communication Techniques", Script for the course Übertragungsverfahren at the Technical University of Vienna, october 1999.

[Howe 74] Harlan Howe, *Stripline Circuit Design*, Artech House, Norwood, MA, USA, 1st edition, 1974.

[Ilkov 03,a] N. Ilkov, Bakalski, W., Matz, R., Metzger, W., and Walter, S., "LTCC design flow in microwave applications", *in 10.Keramiktag der BAM- Foliengiessen und Multilayertechnologie für funktionskeramische Anwendungen*, Berlin, 10-11.April 2003.

[Ilkov 03,b] N. Ilkov, Bakalski, W., Matz, R., Simbürger, W., Dernovsek, O., and Weger, P., "A 5 to 6.5 GHz LTCC Power Amplifier Module", *in 36th International Symposium on Microelectronics (IMAPS) (accepted)*, Boston, MA, USA, 16-20.November 2003. IEEE.

[Johansson 97] Ted Johansson, "Inside the RF Power Transistor", *Applied Microwaves & Wireless*, pp. 34–45, 1997.

[Johnson 84] Richard C. Johnson and Jasik, Henry, *Antenna Enineering Handbook*, McGraw-Hill, New York, second edition, 1984.

[Katz 03] A. Katz and Gray, R., "Noise Power Ratio Measurement Tutorial", http://www.lintech.com/infodown.htm, 2003.

[Kehrer 00] D. Kehrer, "Design of Monolithic Integrated Transformers in Silicon-based Technologies up to 20 GHz", Master's thesis, Technical University of Vienna, Austria, December 2000.

[Kehrer 01] D. Kehrer, Simbürger,W., Wohlmuth,H.D., and Scholtz,A.L., "Modeling of Monolithic Lumped Planar Transformers up to 20 GHz", *in IEEE Custom Integrated Circuits Conference CICC 2001*, pp. 401–404, San Diego, May 2001.

[Kenington 00] Peter B. Kenington, *High-Linearity RF Amplifier Design*, Artech House, Boston, London, 1st edition, 2000.

[Klein 99] W. Klein and Klepser, B.U.H., "75GHz Bipolar Production Technology for the 21th Century", *in Proceedings of the ESSDERC 1999*, pp. 88–94. IEEE, 1999.

[Kloosterman 89] W. J. Kloosterman and de Graaf, H. C., "Avalanche multiplication in a compact bipolar transistor model for circuit simulation", *IEEE Transactions on Electron Devices*, vol. 36(7), pp. 1376–1380, 1989.

[Klose 93] H. Klose and et al., "B6HF: A 0.8 Micron 25GHz/25ps Bipolar Technology for "Mobile Radio" and "Ultra Fast Data Link" IC Products", *in IEEE Bipolar Circuits and Technology Meeting*, pp. 125–127. IEEE, 1993.

[Kraus 99] Gunthard Kraus, *Erdung in HF-und Mikrowellenschaltungen*, UKW-BERICHTE, 4/1999.

[Krischke 95] Alois Krischke, *Rothammels Antennenbuch*, Franck-Kosmos, Stuttgart, 11th edition, 1995.

[Lange 69] Julius Lange, "Interdigitated Strip-Line Quadrature Hybrid", *IEEE Transactions on Microwave Theory and Techniques*, July 1969.

[Long 00] J.R. Long, "Monolithic transformers for silicon rf ic design", *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1368–82, 2000.

[Magerl 98] Gottfried Magerl, "Hochfrequenztechnik 1", Script for the course Hochfrequenztechnik at the Technical University of Vienna, March 1998.

[March 91] Steven L. March, "Simple equations characterize bond wires", *Microwaves & RF*, pp. 105–110, November 1991.

[Marchand 44] N. Marchand, "Transmission line conversion transformers", *Electronics*, vol. 17, pp. 142–145, Dec. 1944.

[Meister 92] T.F. Meister, Stengl, R., Meul, H.W., Weyl, R., Packan, P., Felder, A., Klose, H., Schreiter, R., Popp, J., Rein, H.M., and Treitinger, L., "Sub-20ps Silicon Bipolar Technology Using Selective Epitaxial Growth", *in International Electron Devices Meeting*, pp. 401–404, San Francisco, 1992. IEEE.

[Meister 95] T.F. Meister, Schafer, H., Franosch, M., Molzer, W., Aufinger, K., Scheler, U., Walz, C., Stolz, H., Boguth, S., and Bock, J., "SiGe Base Bipolar Technology with 74 GHz f_{max} and 11 ps Gate Delay", *in International Electron Devices Meeting*, pp. 739–42, Washington, 10-13 Dec. 1995. IEEE.

[Meister 03] T.F. Meister, Schäfer, H., Aufinger, K., Stengl, R., Boguth, S., Schreiter, R., Rest, M., Knapp, H., Wurzer, M., Mitchell, A., Böttner, T., and Böck, J., "SiGe Bipolar Technology with 3.9ps Gate Delay", *in Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting*, Toulouse, France, September 2003. IEEE.

[Mongia 99] R. Mongia, Bahl, I., and Bhartia, P., *RF and Microwave Coupled-Line Circuits*, Artech House, Norwood,MA 02062, first edition, 1999.

[Nakashiba 80] H. Nakashiba, Ishida, I., Aumura, K., and Nakamura, T., "An Advanced PSA Technology for High-Speed Bipolar LSI", pp. 1390–1394, 1980.

[Nicolics 97] Johann Nicolics and Walter Smetana, "Packaging Technologien", Script for the course Packaging at the Technical University of Vienna, january 1997.

[Niknejad 00] Ali M. Niknejad, *Inductors and Transformers for Si RF ICs*, Kap, 2000.

[Ning 81] T. H. Ning, Isaac, R. D., Solomon, P. M., Tang, D. D.-L., Yu H.-N., Feth, G. C., and Wiedmann, S. K., "Self-Aligned Bipolar Transistors for High-Performance and Low-Power-Delay VLSI", pp. 1010–1013, 1981.

[Parkhurst 98] R. Parkhurst, Weber, D., Jansen, B., Wingra Fang, Hendin, N., Kolk, J., and Repeta, M., "Silicon bipolar 3 v power amplifier for gsm900/gsm1800 handsets", *in 1998 Bipolar/BiCMOS Circuits and Technology Meeting*, pp. 117–19, Minneapolis, 27-29 Sept. 1998.

[Philips 98] Philips, "TDA 8574 Class-H high output voltage level line driver", 1998, http://www.semiconductors.philips.com.

[Raab 75] F. H. Raab, "High efficiency amplification techniques", *IEEE Circuits Syst. Newslett.*, vol. 7, pp. 3–11, December 1975.

[Raab 77] F. H. Raab, "Idealized operation of the Class E tuned power amplifier", *IEEE Trans. Circ. Syst.*, vol. CAS-24, pp. 725–735, December 1977.

[Raab 78,a] F. H. Raab, "Effects of Circuit Variations on the Class E Tuned Power Amplifier", *IEEE Journal of Solid-State Circuits*, vol. SC-13, pp. 239–247, April 1978.

[Raab 78,b] F. H. Raab and N. O. Sokal, "Transistor power losses in the Class E tuned power amplifiers", *IEEE Journal of Solid-State Circuits*, vol. SC-13, pp. 912–914, December 1978.

[Raab 03] F. Raab, Asbeck, P., Cripps, S., Kennington, P.B., Popovich, Z., Pothecary, N., Sevic, J.F., and Sokal, N., "RF and Microwave Power Amplifier and Transmitter Technologies", *High Frequency Electronics*, vol. 2, pp. 22–36, may 2003.

[Rabjohn 89] G. G. Rabjohn, *Balanced Planar Transformers*, United States Patent with Patentnumber 4,816,784, 1989.

[Raicu 98] Dan Raicu, "Design of planar, single-layer microwave baluns", *in IEEE MTT-S International Microwave Symposium Digest.* IEEE, 1998, Cat.No.98CH36192.

[Raytheon 02] Raytheon, "Product Information - RTPA 5250-130 3.3 V UNII Band Power Amplifier MMIC/Switch Module for WLAN", january 2002, http://www.raytheon.com.

[Rein 80] H.-M. Rein, *Integrierte Bipolarschaltungen*, Springer-Verlag, first edition, 1980.

[Reisch 03] Michael Reisch, *High-Frequency Bipolar Transistors*, Springer, first edition, 2003.

[Rickelt 99] M. Rickelt and Rein, H.-M., "Impact-ionization induced instabilities in high-speed bipolar transistors and their influence on the maximum usable output voltage", *in Bipolar/BiCMOS Circuits and Technology Meeting*, Minneapolis, September 26-28 1999. IEEE.

[Rickelt 02] M. Rickelt and Rein, H.-M., "A novel transistor model for simulating avalanche-breakdown effects in si bipolar circuits", *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 1184–1197, 2002.

[Rodgers 03] John Rodgers and Clavin Plett, *Radio Frequency integrated circuit design*, Artech House, Norwood, MA, USA, 1st edition, 2003.

[Ruge 84] Ingolf Ruge, *Halbleiter-Technologie*, Springer-Verlag, Berlin, second edition, 1984.

[Schrenk 78] Hartmut Schrenk, *Bipolare Transistoren*, Springer, first edition, 1978.

[Schweinzer 96] H. Schweinzer and Patzelt, R., *Elektrische Messtechnik*, Springer-Verlag, Vienna, second edition, 1996.

[Shockley 50] W. Shockley, *Electrons and Holes in Semiconductors with Applications to Transistor Electronics*, D. van Nostrand Company, Toronto, 1950.

[Shumaker 02] J. Shumaker, Basset, R., and Skuratov, A., "High-Power GaAs FET Amplifiers: Push-Pull versus Balanced Configurations", *Applied Microwave & Wireless*, vol. may, pp. 26–32, 2002.

[Simbürger 99] W. Simbürger, Wohlmuth, H.D., and Weger, P., "A Monolithic 3.7W Silicon Power Amplifier with 59% PAE at 0.9GHz", *in IEEE International Solid-State Circuits Conference*, pp. 230–231, San Francisco, February 1999. IEEE.

[Simbürger 00,a] W. Simbürger, Heinz, A., Wohlmuth, H.D., Böck, J., Aufinger, K., and Rest,M., "A Monolithic 2.5V, 1W Silicon Bipolar Power Amplifier with 55% PAE at 1.9 GHz", *in IEEE MTT-S IMS Digest*, pp. 853–856, Boston, June 2000. IEEE.

[Simbürger 00,b] W. Simbürger, Wohlmuth, H.D., Heinz, A., Tiebout, M., and Liebermann, T., "Monolithic Integration of Power Amplifers in Silicon-based Technologies", *in Proceedings of the 26th European Solid-state Circuit Conference*, Stockholm, Sweden, 19.-21.September 2000. IEEE.

[Simbürger 01] W. Simbürger, Bakalski, W., and Kehrer, D. et al., "A monolithic 5.8 GHz silicon power amplifier in a 25 GHz f_T silicon bipolar technology", *in Proceedings of the european Gallium Arsenide and other compound semiconductors application symposium*, September 2001.

[Sokal 75] N. O. Sokal and A. D. Sokal, "High efficiency tuned switching power amplifier", *U.S. Patent*, pp. 1–32, November 1975.

[Sokal 77] N. O. Sokal and F. H. Raab, "Harmonic output of class E RF power amplifiers and load coupling network design", *IEEE Journal of Solid-State Circuits*, vol. SC-12, pp. 86–88, February 1977.

[Tholl 76] Herbert Tholl, *Bauelemente der Halbleiterelektronik*, B.G.Teubner Stuttgart, first edition, 1976.

[Thüringer 02] Ronald Thüringer, "Characterization of Integrated Lumped Inductors and Transformers", Master's thesis, Technical University of Vienna, April 2002.

[Vathulya 01] V.R. Vathulya, Sowlati, T., and Leenaerts, D., "Class 1 Bluetooth Power Amplifier with 24 dBm Output Power and 48 % PAE at 2.4 GHz in 0.25 μm CMOS", *in Proceedings of ESSCIRC 2001*, Villach,Austria, September 2001. IEEE.

[Vinding 67] J.R. Vinding, "Radial line stubs as elements in strip line circuits", *Nerem Record*, vol. , pp. 108–109, 1967.

[Vizmuller 95] Peter Vizmuller, *RF Design Guide - Systems, Circuits, and Equations*, Artech House, first edition, 1995.

[Wadell 91] Brian C. Wadell, *Transmission Line Design Handbook*, Artech House, Boston, London, first edition, 1991.

[Walker 03] John Walker, "RF Power Transistors", *in IEEE International Microwave Symposium Workshop Notes*, Philadelphia, PA, USA, June 2003. IEEE MTT-S, Handouts on CD-ROM.

[Weber 97] S. Weber, Donig, G., and ed. Schellenberg, J.M., "An Integrated 2 GHz 500 mW Bipolar Amplifier", *in 1997 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 139–42, Denver, 8-11 June 1997.

[Weinrichter 91] Hans Weinrichter and Hlawatsch, Franz, *Stochastische Grundlagen nachrichtentechnischer Signale*, Springer, Wien, New York, first edition, 1991.

[Wilkinson 60] Ernest J. Wilkinson, "An N-way hybrid power divider", *IRE Transactions on Microwave Theory and Techniques*, January 1960.

[Wohlmuth 00] Hans-Dieter Wohlmuth, *Monolithische Integration von HF-Oszillatoren in Silizium-Bipolartechnik*, PhD thesis, Technical University of Vienna, June 2000.

[Wolf 01] K. Wolf, Klein, W., Elbel, N., Berthold, A., Gröndahl, S., Huttner, T., Drexl, S., and Lachner, R., "SiGe-HBTs for bipolar and BICMOS-applications: from research to ramp up of production", *IEICE Transactions on Electronics*, vol. E84-C, pp. 1368–82, 2001.

[Yoshida 98] Isao Yoshida, Katsueda, M., Morikawa, M., Matsunaga, Y., Fujioka, T., Hotta, M., Nunogawa, J., Kobayashi, K., Shimuzu, S., and Nagata, M., "A 3.6V 4W 0.2cc Si Power-MOS-Amplifier Module for GSM Handset Phones", *in ISSCC98 Digest of Technical Papers*, pp. 50–51. 1998 IEEE International Solid-State Circuits Conference, February 1998.

[Yue 98] Yue, "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's ", *IEEE of Solid-State Circuits*, vol. 33, pp. 743–815, May 1998.

[Zhang 99] X. Zhang, Henderson, G., and Souchuns, C., "An Accurate Physics-Based Large-Signal Model for High Power SiGe BJT's", *in Proceedings of IEEE International Microwave Symposium*. IEEE, June 1999.