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DISSERTATION

Solid State Power Amplifier for DAB in L-Band

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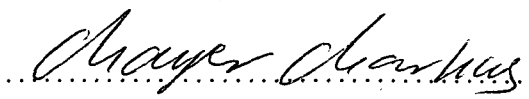

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Kurzfassung

Digital Audio Broadcasting, DAB, ist die fundamentalste Weiterentwicklung in der Rundfunktechnologie seit der Einführung von UKW Stereo Rundfunk. Es ermöglicht dem Zuhörer einen kristallklaren Empfang, leicht zu bedienende Empfangsgeräte und ein deutlich umfangreicheres Angebot and Sendern und Services.

Volle Flächendeckung eines dicht bebauten Gebietes kann durch die Schattenbildung hoher Gebäude oder ähnlicher Hindernisse nur durch eine zusätzliche Versorgung abgedeckt werden. Für diesen Zweck werden "Gap-Filler" Sendeeinheiten benötigt die das Signal des Hauptsenders empfangen und verstärkt in die nicht versorgten Gebiete abstrahlen. Die Ausgangsleistung derartiger Sendeeinheiten beträgt typischerweise einige Watt.

Das DAB System verwendet Sendesignale mit hoher Amplitudendynamik die hochlineare Verstärker erfordern. Für den autonomen Betrieb von Gap-Filler Sendeeinheiten muss eine Maximierung des Wirkungsgrades angestrebt werden um eine Energieversorgung durch Solarenergie zu ermöglichen. Des Weiteren soll die Baugröße der Sendeeinheiten minimiert werden. Dünnfilmtechnologie ist für eine mittlere Stückzahl im Vergleich zu MMIC Technologie eine hervorragende und kosteneffiziente Möglichkeit der Miniaturisierung. Das verlustarme Keramiksubstrat erlaubt den Entwurf von passiven Bauteilen mit kontinuierlichem Wertespektrum, hoher Güte und hoher Fertigungsgenauigkeit.

Im Rahmen dieser Dissertation wurde ein halbleiterbasierender DAB-Leistungsverstärker in Dünnfilmtechnologie entwickelt um die konzeptionelle Machbarkeit einer gleichzeitigen Linearitäts- und Wirkungsgradoptimierung zu zeigen.

In den letzten 20 Jahren wurden von vielen Forschern Möglichkeiten zur Wirkungsgradsteigerung bei halbleiterbasierenden Mikrowellenleistungsverstärkern untersucht. Mit der Einführung von komplexen digitalen Modulationsverfahren mit hoher Amplitudendynamik (z.B. OFDM, CDMA, ...) verstärkte sich in den letzten 5-10 Jahren das Forschungsinteresse an hochlinearen Leistungsverstärkern. Dabei wurden die Quellen der Nichtlinearitäten untersucht und leistungsfähige Linearisierungstechniken von verschiedenen Forschern entwickelt. Die Linearitätsverbesserung einer Verstärkerschaltung wurde meistens durch eine Verbesserung der Halbleitertechnologie und sorgfältiger Arbeitspunktwahl erreicht, selten aber durch eine Optimierung der Verstärkerschaltung selbst.

Klasse F ist ein wohlbekanntes Konzept für den hocheffizienten Verstärkerentwurf. Dennoch gibt es nur wenige Untersuchungen am Linearitätsverhalten der harmonischen Klasse F Ausgangsterminierung und in keiner uns bekannten Publikation wurden die optimalen Phasenwinkel der harmonischen Terminierungen für optimale Linearität angegeben. In dieser Arbeit wurde, basierend auf nichtlinearen Simulationen, das Klasse F Verstärkerkonzept in Hinblick auf die Optimierung von Linearität und Wirkungsgrad erforscht. Um die Linearität weiter zu steigern, wurde eine harmonische Terminierung am Transistorein-

gang auf ihr Potential zur Verbesserung von Linearität und Wirkungsgrad untersucht. Eine Hybridkonfiguration wurde zur Erreichung der erforderliche Ausgangsleistung gewählt. Zur einfachen Charakterisierung und zur erhöhten Flexibilität wurde der Verstärker in einem modularen Konzept entwickelt.

Da es am Institut keine Erfahrung mit Dünnfilmtechnologie gab, wurde der Fertigungsprozess des gewählten Herstellers evaluiert um die Tauglichkeit der verwendeten Bauteilmodelle zu prüfen. Für multiharmonische Verstärkerterminierung werden passive Bauteile mit hoher Güte und Computermodelle mit hoher Genauigkeit benötigt. Da es in der verwendeten Simulationsumgebung kein ausreichend genaues Modell für Dünnfilmspiralinduktivitäten vorhanden war, wurde ein neues, skalierbares Spiralinduktivitätsmodell entwickelt das eine genaue Vorhersage inklusive aller parasitären Elemente und der geometrischen Parameter in einem weiten Induktivitätsbereich erlaubt. Dieses Modell ist ein fundamentales Tool für die Entwicklung von harmonischen Abschlüssen da es einen iterativen Spulenentwurfsprozess eliminiert. Im Weiteren wurden alle verwendeten passiven Bauteilserien charakterisiert und auch von diesen wurden skalierbare Modelle entwickelt. Um eine hohe Zuverlässigkeit der Transistoren zu gewährleisten wurde die Montagetechnik des ungehäusten Transistors untersucht und optimiert.

Für den Entwurf und die Optimierung von harmonisch gesteuerten Verstärkern sind verlässliche Großsignal-Computermodelle notwendig. Da für die verwendeten Transistoren kein derartiges Modell in der verwendeten Simulationsumgebung vorhanden war, wurde ein Computermodell basierend auf Gleichspannungsmessungen und einer Vielzahl von Kleinsignal-S-Parametermessungen, die bei unterschiedlichen Arbeitspunkten durchgeführt wurden, generiert. Messungen zeigen nicht nur im klassischen Klasse A Bereich eine gute Übereinstimmung mit den Simulationsergebnissen, sondern auch in Bereichen, die für hocheffiziente Applikationen wesentlich sind.

Simulationsergebnisse zeigten dass mit einem bis zur zweiten Oberwelle multiharmonisch abgeschlossenem realem Transistor der theoretisch maximal mögliche Klasse F Wirkungsgrad von 81.65 % beinahe erreicht werden kann. Diese wird im Wesentlichen nur durch den Kniespannungsfaktor $\varkappa = \frac{V_{DD}-V_K}{V_{DD}}$ reduziert. Die Annahme, dass Linearität und Wirkungsgrad bei Klasse F Terminierung gleichzeitig maximiert werden, konnte durch nichtlineare Simulationsergebnisse bestätigt werden. Es stellte sich dabei heraus dass der Abschluss der ersten Oberwelle dabei die wesentlichste Rolle für die Optimierung von Linearität und Wirkungsgrad spielt. Linearität und Wirkungsgrad wurden durch einen geeigneten Abschluss der ersten Oberwelle am Transistoreingang zur Kompensation der Nichtlinearitäten zweiter Ordnung der Gate-Source Kapazität verbessert.

Das endgültige Verstärkermodul erfüllt die gestellten Anforderungen. Bei nominaler DAB Anspeisung liefert der Verstärker eine Ausgangsleistung von 37.3 dBm bei der geforderten Schulterdistanz von 20 dB mit einem Gesamtwirkungsgrad von 41 %. Bei reduzierter Eingangsleistung (back-off Betrieb) liefert das Modul eine Ausgangsleistung von 34.5 dBm bei der geforderten Schulterdistanz von 30 dB wobei ein Gesamtwirkungsgrad von 31 % erreicht wird. Im Vergleich zu kürzlich publizierten hocheffizienten und hochlinearen Leistungsverstärkern erreicht das Verstärkermodul durchschnittliche Wirkungsgradresultate, die hauptsächlich auf einen suboptimalen Entwurf des Ausgangskombinationsnetzwerks zurückzuführen sind. In Bezug auf Linearität aber bietet der neu entworfene Verstärker exzellente Ergebnisse.

Abstract

Digital Audio Broadcasting, DAB, is the most fundamental advance in radio technology since the introduction of FM stereo radio. It gives listeners interference-free reception of high-quality sound, easy-to-use radios, and the potential for wider listening choice through many additional stations and services.

Full coverage of an area, in particular in big towns can only be achieved by retransmitting the DAB-signals into regions which are otherwise in the shadows of big buildings or similar obstacles. For this purpose fill-in or gap-filler transmitters are needed. The output power needed for such transmitters is usually in the range of several Watts.

The DAB system has to handle high dynamic range signals that can only be attained by the design of a low intermodulation distortion (IMD) amplifier. For stand-alone operation the efficiency of gap-filler transmitters have to be maximized to allow for solar powering. Furthermore, size has to be minimized for versatile use. Thin film technology is one miniaturization route which is for a medium number of units more cost effective than MMIC technology. Low-loss alumina substrate allows the design of passives with high quality factors and high manufacturing accuracy. Furthermore, the realization of components with a continuous spectrum of values is possible.

In this doctoral thesis a solid state power amplifier (SSPA) module fulfilling DAB requirements in thin film technology was developed showing conceptional feasibility for achieving simultaneously good linearity and good DC-power conversion rate.

The improvement of power added efficiency of microwave solid state power amplifiers has been investigated by many researcher in the last 20 years. With the introduction of complex digital modulation schemes with a non constant envelope (e.g. OFDM, CDMA, ...) interest in high linearity power amplifier design increased in the last 5-10 years. The sources for nonlinearities were investigated and effective linearisation techniques have been invented by several researchers. Improving linearity of the amplifier circuit was mostly done by an improvement in device technology and careful bias selection but rarely by an optimization of the amplifier circuit itself.

Class F mode of operation is well known for high efficiency. But investigations on linearity of class F termination have been reported rarely and the optimum termination angles of the harmonic loads in terms of linearity were not reported at all. In this thesis class F operation mode was investigated in terms of linearity and efficiency optimization based on nonlinear simulations. To improve linearity further, harmonic termination at the input was investigated on its capability to improve linearity and efficiency. To reach the required output power a balanced amplifier configuration was chosen since it offers many advantages, such as minimized input VSWR and increased stability. For easy characterization and flexibility the amplifier was designed in a modular way.

As no experience with thin film technology was available at the institute the thin film process of the selected foundry was evaluated to ensure the validity of the used component models. For multiharmonic amplifier termination passive components with high quality factor are needed. Since no accurate model for spiral thin fim inductors was available in the simulation software used, a new spiral inductor model was developed being capable of predicting all parasitic elements and being scalable in a wide range of inductance values. This model is a fundamental tool in the design of harmonic terminations since it eliminates an iterative spiral inductor design process. All selected lumped components were characterized and scaleable models were made for those also. To ensure high reliability the bonding technique of the active devices was investigated and optimized.

To design and optimize a harmonic controlled amplifier, reliable large-signal transistor models are necessary. As no such models were available in the used harmonic balance simulation software, computer models were generated from transistor DC and multiple bias small-signal scattering parameter measurements. The generated models agree well with measurements even at those regions which are crucial for high efficiency applications.

Simulation results of the 3rd order multiharmonic terminated transistor showed that with a non-ideal device the theoretical maximum of class F efficiency of 81.65 % is closely achievable only reduced by the knee voltage factor $\varkappa = \frac{V_{DD}-V_K}{V_{DD}}$. The assumption that linearity and efficiency are maximized simultaneously with class F termination was proven by non-linear circuit simulations. Termination of the 2nd harmonic at the output was found to be crucial for linearity and efficiency optimization. Linearity and efficiency were further improved by a 2nd harmonic termination concept at the device input to compensate for the 2nd order nonlinearities of the gate-source capacitance.

The final amplifier module fulfils the requirements for DAB operation. It delivers at nominal DAB drive an output power of 37.3 dBm with the requested shoulder distance of 20 dB and operating at a power added efficiency of 41 %. At reduced input power level (back-off condition) the module delivers at DAB excitation an output power of 34.5 dBm with the requested shoulder distance of 30 dB and providing a power added efficiency of 31 %. Compared to recent high efficiency and high linearity power amplifiers the developed amplifier module shows average results with respect to efficiency mainly due to suboptimal output combiner design. With respect to linearity, however, the newly developed power amplifier achieves excellent results.

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List of Abbreviations

ACPR	**A**djacent **C**hannel **P**ower **R**atio
AM/AM	Output amplitude to input amplitude ratio
AM/PM	Output phase to input amplitude ratio
BJT	**B**ipolar **J**unction **T**ransistor
BW	**B**and**w**idth
CCDF	**C**omplementary **C**ummulative **D**istribution **F**unction
CDMA	**C**ode **D**ivision **M**ultiple **A**ccess
CF	**C**rest **F**actor
CL	**C**ombiner **L**oss
DAB	**D**igital **A**udio **B**roadcast
DC	**D**irect **C**urrent
DLL	**D**ynamic **L**oad **L**ine
DUT	**D**evice **u**nder **T**est
EER	**E**nvelope **E**limination and **R**estoration
EM	**E**lectro**m**agnetic
ETSI	**E**uropean **T**elecommunications **S**tandard **I**nstitute
FET	**F**ield **E**ffect **T**ransistor
FFT	**F**ast **F**requency **T**ransform
FM	**F**requency **M**odulation
GaAs	**Ga**llium **As**enide
HBT	**H**eterojunction **B**ipolar **T**ransistor
HCA	**H**armonic **C**ontrolled **A**mplifier
hHCA	**h**alfsinusoidally driven **H**armonic **C**ontrolled **A**mplifier
HRA	**H**armonic **R**eaction **A**mplifier
ICA	**I**sotropically **C**onductive **A**dhesive
ICI	**I**nter-**C**arrier **I**nterference
IMD	**I**nter**m**odulation **D**istortion
IMDD	**I**nter**m**odulation **D**istortion **D**istance
LDMOS	**L**aterally **D**iffused **M**etal **O**xide **S**emiconductor
LINC	**L**inear **A**mplification by **N**onlinear **C**omponents
MESFET	**M**etal **S**emiconductor **FET**
MIC	**M**icrowave **I**ntegrated **C**ircuit
MMIC	**M**onolithic **M**icrowave **I**ntegrated **C**ircuit
M-IMD	**M**ultitone - **I**nter**m**odulation **D**istortion
NPR	**N**oise **P**ower **R**atio
OFDM	**O**rthogonal **F**requency **D**ivision **M**ultiplexing

PAE	**P**ower **A**dded **E**fficiency
PAPR	**P**eak-to-**A**verage **P**ower **R**atio
pHEMT	**P**seudomorphic **H**igh **E**lectron **M**obility **T**ransistor
rHCA	rectangularly driven **H**armonic **C**ontrolled **A**mplifier
RF	**R**adio **F**requency
SD	**S**houlder **D**istance
SFN	**S**ingle **F**requency **N**etwork
Si	**Si**licon
SMD	**S**urface **M**ount **D**evice
SSPA	**S**olid **S**tate **P**ower **A**mplifier
TRL	**T**hru-**R**eflect-**L**ine Calibration
VSWR	**V**oltage **S**tanding **W**ave **R**atio

List of Symbols

A	Amplitude
C	Capacitance
D	FET drain contact
f	Frequency
f_0	Fundamental frequency
$2f_0,\ 3f_0$	2^{nd} and 3^{rd} harmonic frequency
G	Power gain, FET gate contact
G_E	Efficiency gain
G_{MAX}	Maximum available gain
g	Conductance
g_m	Transconductance
I_{DC}	DC current
I_{DS}	Drain-source current
I_{DSS}	Saturated drain-source current
I_{GS}	Gate-source current
I_m	Maximum drain-source current
H_{LG}	Load-gate transfer function
H_{LD}	Load-drain transfer function
k	Rollet stability factor
L	Inductance
P_{DC}	DC power
P_{DISS}	Dissipated power
P_{IN}	Input power
P_{IP3}	3^{rd} order intercept point
P_{OUT}	Output power
P_{1dB}	1 dB compression point
Q	Charge
R	Resistance
$R_{L,opt}$	Optimum load resistance
S	FET source contact
$S_{11}...S_{22}$	S-Parameter
t	Time
T	Temperature
V_{BI}	Built-in voltage
V_{BR}	Breakdown voltage

V_{DC}	DC voltage
V_{DD}	Drain bias voltage
V_{DS}	Drain-source voltage
$V_{DS,\max}$	Maximum drain-source voltage
V_{GG}	Gate bias voltage
V_{GS}	Gate-source voltage
V_{IN}	Input voltage
V_K	Knee voltage
V_{OUT}	Output voltage
V_P	Pinch-off voltage
Z	Impedance
α	Current conduction angle
Γ	Reflection coefficient
η_D	Drain efficiency
$\varkappa$	Knee voltage factor
φ	Phase
Θ	Normalized frequency
λ	Wavelength
ω	Angular frequency

Chapter 1

Motivation

Digital Audio Broadcasting, DAB, is the most fundamental advance in radio technology since the introduction of FM stereo radio. It gives listeners interference-free reception of high-quality sound, easy-to-use radios, and the potential for wider listening choice through many additional stations and services.

DAB is a time and frequency interleaving continuous-wave system which uses Orthogonal Frequency Division Multiplexing (OFDM) modulation scheme. OFDM allows for very high efficient spectrum use by a special feature called the Single Frequency Network (SFN). A broadcast network can be extended virtually without any limit by operating all transmitters on the same radio frequency due to the strongly reduced impact of multipath propagation. It has to be noted that the transmit power of the single transmitter must not cover a range greater than the maximum transmitter separation distance. Full coverage of an area, in particular in big towns can only be achieved by retransmitting the DAB-signals into regions which are otherwise in the shadows of big buildings or similar obstacles. For this purpose fill-in or gap-filler transmitters are needed in high quantity. Due to the SFN gap-filler transmitters can be implemented easily into the network operating at the same frequency as the main transmitter. Figure 1.1 shows a typical application for such a gap-filler transmitter. The output power needed for such transmitters is usually in the range of several Watts.

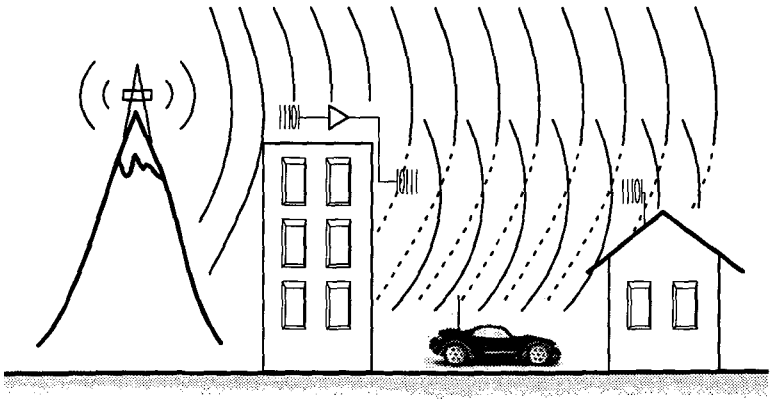


Figure 1.1: Providing full radio coverage using a fill-in transmitter.

The DAB system has to handle high dynamic range signals that can only be attained by the design of a low intermodulation distortion (IMD) amplifier. For stand-alone operation the efficiency of gap-filler transmitters have to be maximized to allow for solar powering. Furthermore, size has to be minimized for versatile use. In conventional microwave integrated circuits passive components are surface mounted devices, consuming a large area and yielding a high mounting cost. Therefore, miniaturization and integration of the passive components have become a major task. Using thin film technology is one possible miniaturization route. Low-loss alumina substrate allows the design of passives with high quality factors and high manufacturing accuracy. Furthermore, the realization of components with a continuous spectrum of values is possible.

The main goal of this work is to develop a solid state power amplifier (SSPA) module in thin film technology showing conceptional feasibility for achieving simultaneously good linearity and good DC-power conversion rate. The required performance is summarized in Tab. 1.1.

Signal Characteristics:	
- Type of signal:	continuous wave, multi-carrier
- Frequency range:	1.452 – 1.492 GHz (40 MHz)
- RF-output Power:	see output performance
- VSWR (input/output):	$\leq$ 1.2 / minimized (50 Ω load, no isolators)
Gain Performance:	
- Power gain:	$\geq$ 15 dB (20 dB as a goal)
- Amplitude ripple:	$\leq$ 0.5 dB
- Phase ripple:	$\leq$ 10 deg
- Group delay variation:	$\leq$ 0.2 ns
Spurious Response:	
- Harmonics ($2f_0$, $3f_0$):	-20 dBc / -30 dBc
- Non Harmonics:	-70 dBc
- Other	-60 dBc
Output Performance:	
DAB signal (nominal drive)	
- Output power:	$\geq$ 37 dBm
- Linearity (shoulder distance):	20 dB
- Efficiency:	to be maximized (50 % as a goal)
DAB signal (back-off condition)	
- Output power:	$\geq$ 33 dBm
- Linearity (shoulder distance):	30 dB
- Efficiency:	to be maximized (35 % as a goal)
DC Supply Voltage (drain/gate):	depending on semiconductors
Operational Stability:	unconditionally stable under different load conditions with isolator at output (input/output)

Table 1.1: Electrical requirements.

Chapter 2

Digital Audio Broadcast

The Digital Audio Broadcasting (DAB, [1]) system, which is standardized by ETSI [2], is a reliable multiservice digital broadcasting system for reception by mobile, portable and fixed receivers with a simple non-directional antenna. It can be operated at any frequency from 30 MHz to 3 GHz for mobile reception (higher for fixed reception) and may be used on terrestrial, satellite, hybrid (satellite with complementary terrestrial) and cable broadcast networks. In addition to supporting audio programs with a wide range of sound coding rates and hence qualities, it also has a flexible, general purpose digital multiplex which carries a number of services, including audio-program associated data and independent data services.

The DAB System is a rugged, yet highly spectrum- and power-efficient sound and data broadcasting system. It uses advanced digital audio compression techniques (MPEG 1 Audio Layer II and MPEG 2 Audio Layer II) to achieve a spectrum efficiency equivalent to or higher than that of conventional FM radio. A closely-controlled coding redundancy is applied to the signal in order to provide strong error protection and high power efficiency. The transmitted information is spread in both frequency and time so that the effects of channel distortions and fades are eliminated in the receiver, even under conditions of severe multipath propagation (Fig. 2.1).

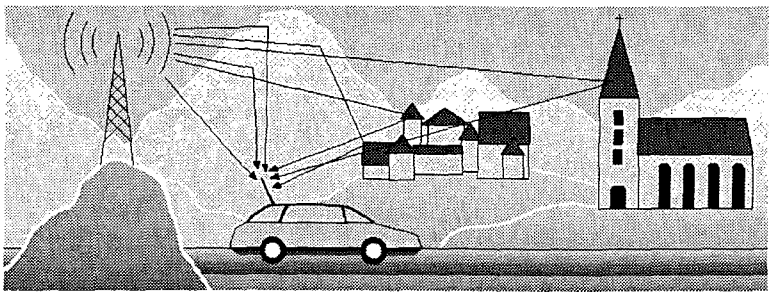


Figure 2.1: Multipath propagation.

The efficiency of spectrum use is increased by a special feature called the Single Frequency Network (SFN). A broadcast network can be extended virtually without any limit by operating all transmitters on the same radio frequency.

The DAB transmission signal carries a multiplex of several digital services simultaneously. Its overall bandwidth is 1.536 MHz, providing a useful bit-rate capacity of approximately 1.5 Mbit/s in a complete "ensemble". Each service is independently error protected with a coding overhead ranging from about 25% to 300% (25% to 200% for sound), the amount of which depends on the requirements of the broadcaster (transmission coverage, reception quality). The ensemble contains audio programs, data related to the audio program and optionally other data services. Usually, the receiver will decode several of these services in parallel. A specific part of the multiplex contains information on how the multiplex is actually configured, so that the receiver can decode the signal correctly. It may also carry information about the services themselves and the links between different services. In particular, the following principal features have been specified:

Flexible audio bit-rate, from 8 kbit/s to 384 kbit/s, which allows the multiplex to be configured in such a way that it provides typically 5 to 6 high-quality stereo audio programs or up to 20 restricted-quality mono programs.

Data service, each service can be a separately defined stream or can be divided further by means of a packet structure.

Programme Associated Data (PAD), embedded in the audio-bitstream, for data transmitted together with the audio program (e.g. lyrics, phone-in telephone-numbers). The amount of PAD is adjustable (min. 667 bit/s), at the expense of capacity for the coded audio signal within the chosen audio bit-rate.

Conditional Access (CA), applicable to each individual service or packet in the case of packet-mode data. Specific subscriber management does not form part of the DAB System Specification, however, the DAB ensemble transports the CA information and provides the actual signal scrambling mechanisms.

Service Information (SI), used for operation and control of receivers and to provide information for program selection to the user. SI also establishes links between different services in the multiplex as well as links to services in other DAB ensembles and even to FM/AM broadcasts.

2.1 Basic DAB System Description

Generation of a DAB Signal

Figure 2.2 shows the block diagram of a conceptual DAB signal generator. Each service is coded individually at source level, error protected and time interleaved in the channel coder. Then the services are multiplexed in the Main Service Channel (MSC), according to a predetermined, but adjustable, multiplex configuration. The multiplexer output is combined with Multiplex Control and Service Information, which travel in the Fast Information Channel (FIC), to form the transmission frames in the Transmission Multiplexer.

Finally, Orthogonal Frequency Division Multiplexing (OFDM) is applied to shape the DAB signal which consists of a large number of carriers. The signal is then transposed to the appropriate radio frequency band, amplified and transmitted.

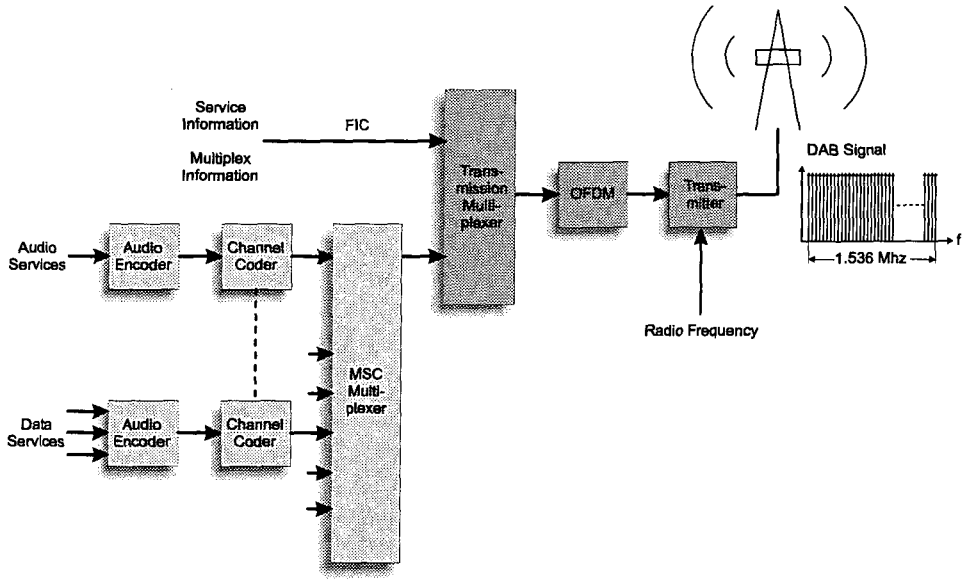


Figure 2.2: Concept of DAB signal generation.

Reception of a DAB Signal

Figure 2.3 shows a conceptual DAB receiver. The DAB ensemble is selected in the analog tuner, the digitized output of which is fed the OFDM demodulator and channel decoder to eliminate transmission errors. The information contained in the FIC is passed to the user interface for service selection and is used to set up the receiver appropriately. The MSC data is further processed in an audio decoder to produce the left and right audio signals or in a data decoder (Packet Demux).

2.2 Details of the DAB System

Audio Services

Compared to conventional PCM sound coding, in DAB the bit-rate is reduced sixfold to twelvefold by means of a digital audio compression technique. It is a low bit-rate sub-band coding system enhanced by a psycho-acoustic model: due to the specific behavior of the inner ear, the human auditory systems perceives only a small part of the complex audio spectrum. Only those parts of the spectrum located above the masking threshold of a given sound contribute to its perception, whereas any acoustic action occuring at the same time but with less intensity and thus situated under the masking threshold will not be heard because it is masked by the sound event.

To extract the perceptible part of the audio signal the spectrum is split into 32 equally-spaced sub-bands. In each sub-band, the signal is quantized in such a way that the quantizing noise matches the masking threshold. This coding system for high-quality audio signals known as MUSICAM is standardized by ISO/IEC 11172-3 (MPEG 1 Audio Layer II) and ISO/IEC 13818-3 (MPEG 2 Audio Layer II).

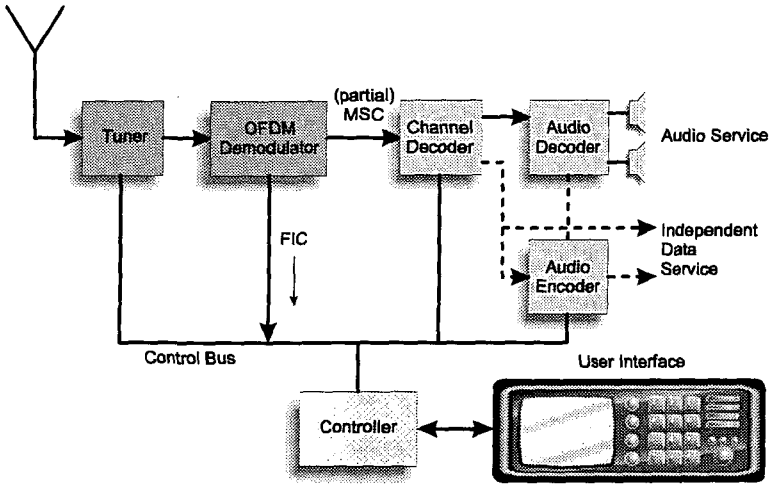


Figure 2.3: Concept of DAB reception.

The DAB Specification permits full use of the flexibility of Layer II except for the fact that only the standard studio sampling frequency of 48 kHz and the half sampling frequency of 24 kHz are used. Layer II is capable of processing mono, stereo and dual-channel such as bilingual programmes. Different encoded bit-rate options are available (8, 16, 24, 32, 40, 48, 56, 64, 80, 96, 112, 128, 144, 160 or 192 kbit/s per monophonic channel). In stereophonic or dual-channel mode, the encoder produces twice the bit-rate of a mono-channel.

The range of possible options can be utilized flexibly by broadcasters depending on the quality required and the number of sound programs to be broadcast. A stereophonic signal may be conveyed in the stereo mode, or – particularly at lower bit-rates – in the joint stereo mode. This mode uses the redundancy and interleaving of the two channels of a stereophonic program to maximize the overall perceived audio quality.

Data Services

Programme Associated Data Each audio program contains Programme Associated Data (PAD) with a variable capacity (minimum 667 kbit/s, up to 65 kbit/s) which is used to convey information together with the sound program.

The PAD Channel is incorporated at the end of the DAB/ISO audio frame. Typical examples of PAD applications are dynamic range control information, a dynamic label to display program titles or lyrics, speech/music indication and text with graphic features.

Independent Data Services In addition to PAD, general data may be transmitted as a seperate service. This may be either in the form of a continous stream segmented into 24 ms logical frames with a data rate of $n \times 8$ kbit/s ($n \times 32$ kbit/s for some code rates) or in packet mode, where individual packet data services may have much lower capacities and are bundled in a packet sub-multiplex. A third way to carry Independent Data Services is as a part of the FIC (Fast Information Channel). Typical examples of Independent Data

Services are a Traffic Message Channel, correction data for Differential GPS, paging and an electronic newspaper.

Conditional Access

Every service can be fitted with Conditional Access if desired. The Conditional Access (CA) system includes three main functions: scrambling/descrambling, entitlement checking and entitlement management. The scrambling/descrambling function makes the service incomprehensible to unauthorized users. Entitlement checking consists of broadcasting the conditions required to access a service, together with encrypted secret codes to enable descrambling for authorized receivers. The entitlement management function distributes entitlements to receivers.

Service Information

The following elements of Service Information (SI) can be made available to the listener for program selection and for operation and control receivers:

- basic program-service labels (i.e. the name of a program service)
- program-type labels (e.g. news, sports, classic music)
- dynamic text labels (e.g. the program title, lyrics, names of artists)
- program language
- time and date, for display or recorder control
- switching to traffic reports, news flashes or announcments on other services
- cross-reference to the same service being transmitted in another DAB ensemble or via AM or FM and to other services
- transmitter identification information (e.g. for geographical selection of information)

Essential items of SI that are used for program selection are carried in the FIC. Information that is not required immediately when switching on a receiver, such as a list of all the day´s programs, may be carried separately as a general data service (Auxiliary Information Channel).

Channel Coding and Time Interleaving

The data representing each of the program services is subjected to energy dispersal scrambling, convolutional coding and time interleaving. For energy dispersal a pseudo-random bit sequence is added to the data in order to randomize the shape of the DAB signal and thus efficiently use power amplifiers. The convolutional encoding process involves adding redundancy to the data in order to help the receiver detect and better eliminate transmission errors. In the case of an audio signal, some parts of the audio frame are less sensitive to transmission errors than others and accordingly, the amount of redundancy added is reduced for these. This method is known as Unequal Error Protection (UEP).

Main Service Multiplex

The encoded and interleaved data is fed to the Main Service Multiplexer (MUX) where every 24 ms the data is gathered in sequences. The combined bit-stream output from the multiplexer is known as the Main Service Channel (MSC) and has a gross capacity of 2.3 Mbit/s. Depending on the the convolutional code rate, which can differ from one application to another, the net bit-rate ranges from approximately 0.6 to 1.8 Mbit/s, accommodated in a DAB signal with a 1.536 MHz bandwidth. The DAB system allows the Main Service Multiplex to be reconfigured from time to time. The precise information about the contents of the Main Service Multiplex is carried by the Fast Information Channel to communicate to the receiver how to access the services. This information is known as the Multiplex Configuration Information (MCI). This data is highly protected and repeated frequently to ensure its ruggedness. When the multiplex configuration is about to change, the new information, together with the timing of the change, is transported via the MCI and with details in advance what changes are going to take place.

Transmission Frame

In order to facilitate receiver synchronization, the transmitted signal is designed according to a frame structure with a fixed sequence of symbols. Each transmission frame (see Fig. 2.4) begins with a null symbol for coarse synchronization (when no RF signal is transmitted), followed by a phase reference symbol for differential demodulation. The next symbols are reserved for the FIC and the remaining symbols provide the MSC. The total frame duration is 96 ms, 48 ms or 24 ms, depending on the transmission mode (see Table 2.1). Each service within the MSC is allocated a fixed time slot in the frame.

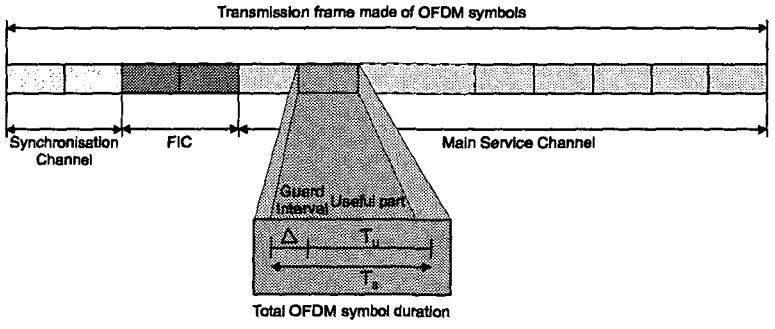


Figure 2.4: Total OFDM symbol duration.

Modulation with OFDM and Transmission Modes

The DAB system uses a multicarrier scheme known as Orthogonal Frequency Division Multiplexing (OFDM, [3], [4]). This scheme meets the exacting requirements of high-bit-rate digital broadcasting to mobile, portable and fixed receivers, especially in multipath environments. Before the transmission the information is divided into a large number of bit-streams with low bit-rates each. These are then used to modulate individual orthogonal carriers in such a way that the corresponding symbol duration becomes larger than

System Parameter	Transmission Mode			
	I	II	III	IV
Frame duration	96 ms	24 ms	24 ms	48 ms
Null symbol duration	1297 μs	324 μs	168 μs	648 μs
Guard intervall duration	246 μs	62 μs	31 μs	123 μs
Nominal maximum transmitter separation for SFN	96 km	24 km	12 km	48 km
Nominal frequency range (for mobile reception)	$\leqslant$ 375 MHz	$\leqslant$ 1.5 GHz	$\leqslant$ 3 GHz	$\leqslant$ 1.5 GHz
Speed/coverage trade-off	No	No	No	Yes
Useful symbol duration	1 ms	250 μs	125 μs	500 μs
Total symbol duration	1246 μs	312 μs	156 μs	623 μs
Number of carriers	1536	384	192	768
Carrier spacing	1 kHz	4 kHz	8 kHz	2 kHz

Table 2.1: DAB transmission parameters for each transmission mode.

the delay spread of the transmission channels. The modulation scheme used for DAB is $\frac{\pi}{4}$-shifted D-QPSK (Fig. 2.5b). The $\frac{\pi}{4}$ rotation of the signal constellation between two consecutive symbols prevents the envelope from reaching zero which reduces the peak to average signal ratio. This can be easily seen if Fig. 2.5a is compared to Fig. 2.5b.

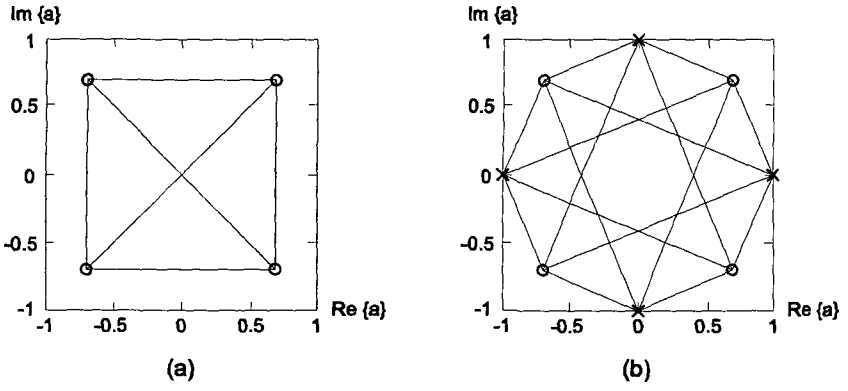


Figure 2.5: (a) Signal constellation of QPSK; (b) Signal constellation of a $\frac{\pi}{4}$-shifted D-QPSK modulation scheme.

To ensure that no Inter-Carrier Interference (ICI)[1] occurs the carriers have to be orthogonal. When one thinks of a symbol with duration T the Fast Fourier Transformed (FFT) amplitude spectrum of this pulse is equal to $\mathrm{sinc}(\pi f T)$ (Fig. 2.6a), which has zeros for all frequencies f that are an integer multiple of $\frac{1}{T}$. This effect is shown in Fig. 2.6b, which shows the overlapping sinc spectra of individual subcarriers. At the maximum of each subcarrier spectrum, all other subcarrier spectra are zero.

[1] In the time-domain one would talk about Inter-Symbol Interference (ISI).

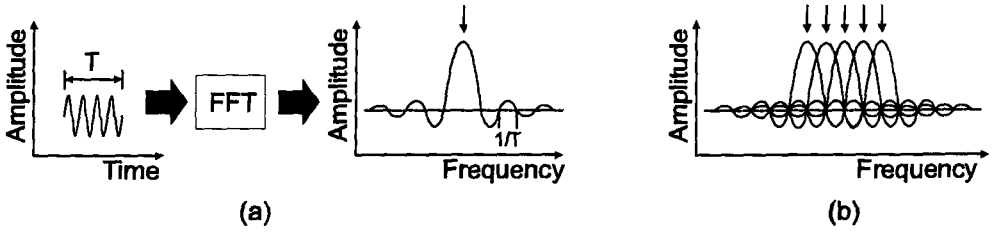


Figure 2.6: (a) FFT of a modulated sub-carrier; (b) multiplexed frequency domain serial signal.

Due to multipath propagation the individual subcarriers will have different propagation delays. To prevent ICI in this case, a temporal guard interval by cyclic extension of the signal between successive symbols is introduced, see Fig. 2.7.

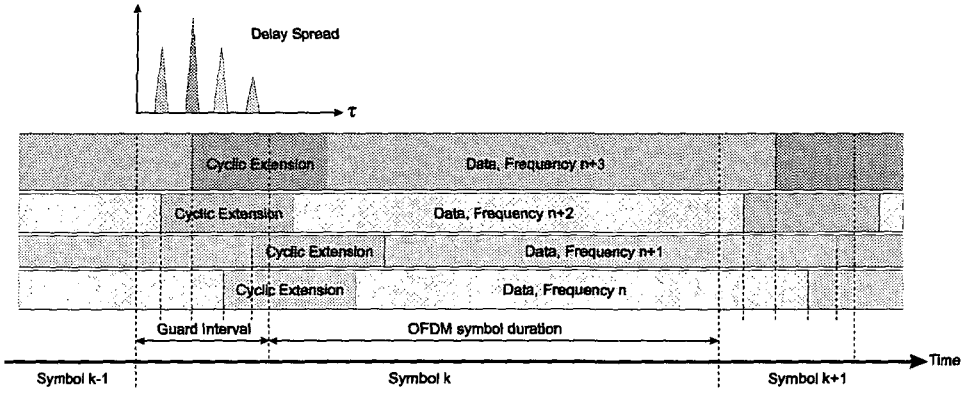


Figure 2.7: Orthogonal Frequency Division Multiplexing (OFDM).

The system provides four transmission-mode options which allow for a wide range of transmission frequencies between 30 MHz and 3 GHz and network configurations. For the nominal frequency ranges, the transmission modes have been designed to suffer neither from Doppler spread nor from delay spread, both inherent in mobile reception with multipath echoes.

Table 2.1 gives the temporal guard interval durations, the nominal maximum transmitter separations and frequency ranges for the different modes. The noise degradation at the highest frequency is equal to approximately 1 dB at 100 km/h under the most critical multipath conditions, which do not occur frequently in practice. The table shows that the higher the frequencies, the shorter the guard interval available and hence the smaller the maximum non-destructive echo delay. Mode I is most suitable for a terrestrial Single-Frequency Network in the VHF range (87 MHz – 108MHz, 174 MHz – 240 MHz), because it allows the greatest transmitter separations. Mode II will preferably be used for medium-scale SFN in L-band (1.452 GHz – 1.492 GHz) and for local radio applications that require one terrestrial transmitter. Larger transmitter spacing can be accommodated by inserting artificial delays at the transmitters and by using directional transmission an-

tennas. Mode III is most appropriate for cable, satellite and complementary terrestrial transmission, since it can be operated at all frequencies up to 3 GHz for mobile reception and has greatest phase-noise tolerance. Mode IV is also used in L-band and allows a greater transmitter spacing in SFNs. However, it is less resistant to degradation at higher vehicle speeds.

Spectrum and Peak-to-Average Power Ratio

The spectrum of the resulting signal is approximately rectangular, Gaussian noise-like, and occupies a bandwidth of 1.536 MHz. Figure 2.8 shows an example of the transmitter output spectrum after it has been amplified and filtered.

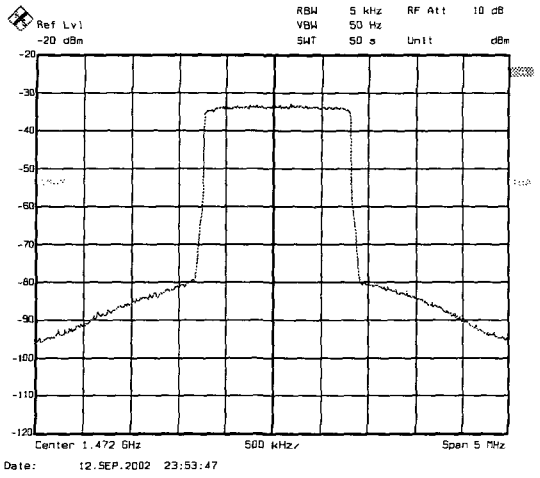


Figure 2.8: Transmitter signal output spectrum (L-band).

With multipath propagation, some of the carriers are amplified by constructive signals, while others suffer destructive interference (frequency selective fading). Therefore, the OFDM system provides frequency interleaving by a re-arrangement of the digital bit-stream among the carriers, so that successive source samples are not affected by selective fade. In stationary receivers, this diversity in the frequency domain is the prime means to guarantee unimpaired reception; the time diversity due to time-interleaving provides further assistance to a mobile receiver. Consequently, multipath propagation is a form of diversity of which DAB takes advantage, in stark contrast to conventional FM or narrow-band digital systems, where it completely destroys a service.

As outlined above, an OFDM signal consists of a number of independently modulated subcarriers, which can give a large Peak-to-Average Power Ratio (PAPR) when added up coherently. When N signals are added with the same phase, they produce a peak power that is N times the average power. Due to the stochastical nature of the phase relation between the OFDM subcarriers, the resulting time domain envelope signal is comparable to band filtered noise with the same bandwidth as the DAB signal. The peak power is defined as the power of a sine wave with an amplitude equal to the maximum envelope value. Hence, an unmodulated carrier has a PAPR of 0 dB.

$$PAPR = 10 \cdot \log\left(\frac{P_{Peak}}{P_{Avg}}\right) \tag{2.1}$$

An alternative measure of the envelope variation of a signal is the Crest factor (CF), which is defined as the maximum signal value divided by the rms signal value.

$$CF = 20 \cdot \log\left(\frac{\hat{V}}{\sqrt{\overline{V^2}}}\right) \tag{2.2}$$

For an unmodulated carrier, the Crest factor is 3 dB. This 3 dB difference between PAPR and Crest factor also holds for other signals, provided that the center frequency is large in comparison with the signal bandwidth.

Figure 2.9 shows the complementary cumulative distribution function for the peak power of a DAB mode II signal. The CCDF describes the probability that the PAPR is greater than some threshold level. The graph shows that PAPRs of some 10 dB are possible, showing the unpleasant nature of a multicarrier signal. In practice, the peak-to-mean ratio can be limited to about 8 dB by digital processing, although this is not required by the standard [2].

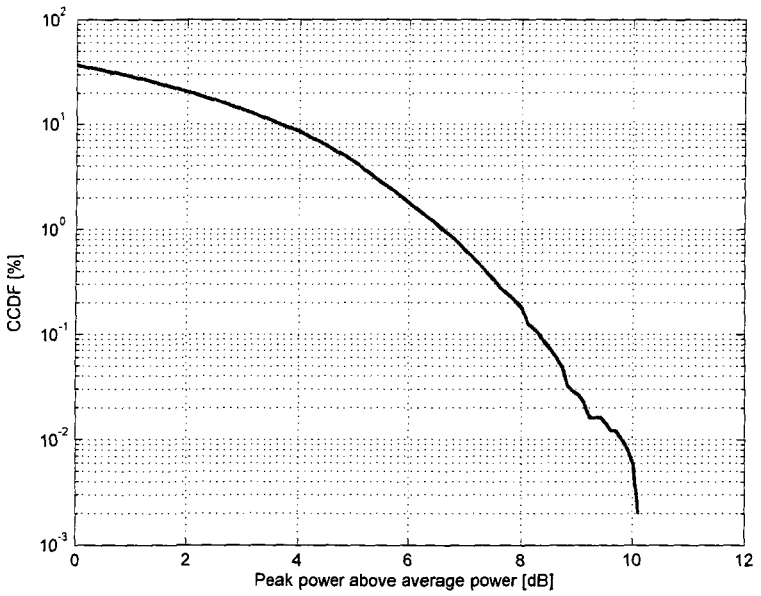


Figure 2.9: Complementary cumulative distribution function (CCDF) of a DAB mode II $\frac{\pi}{4}$-shifted D-QPSK modulated signal.

This extremely dynamic signal characteristic makes it evident that the amplifier will have to be highly linear to amplify the signal in such a way that it fulfils the requirements.

Chapter 3

Amplifier Theory

This chapter gives an overview of state-of-the-art efficient power amplifier concepts, linearization techniques and combiner techniques. The characteristics of the concepts in terms of efficiency and linearity are discussed and a design concept for a linear and efficient DAB amplifier module is presented. Further, semiconductor technologies are discussed briefly with a focus on important aspects of the active device properties with respect to power amplifier design.

3.1 Efficiency

Efficiency is a crucial parameter for RF power amplifiers. It is important when the available power is limited, such as in battery-powered portable or mobile equipment. It is also important for high-power equipment where cooling becomes a major issue.

Efficiency is output power versus input power. However, this definition is too broad, because "output power" and "input power" may have different meanings. Input power may include both the DC-input power and the RF input power, or only the DC-input power. The most common definitions for RF power amplifier efficiency are presented below.

3.1.1 Drain or Collector Efficiency

Drain or collector efficiency is defined as

$$\eta_D = \frac{P_{OUT}}{P_{DC}} \tag{3.1}$$

where P_{OUT} is the RF output power at the fundamental frequency and $P_{DC} = V_{DC} \cdot I_{DC}$ is the input power supplied by the DC supply to the drain (or collector) contact of the amplifier.

3.1.2 Power Added Efficiency

Although it is a very convenient measure of a circuit's performance, drain efficiency does not account for the drive power required, which may be quite substantial in a power amplifier. Power gains of less than 10 dB are common at high RF frequencies. In general,

RF power amplifiers designed for high drain efficiency tend to achive a low power gain, which is a disadvantage for the overall power budget.

Power added efficiency, PAE, is a definition that includes the effect of the drive power and is defined as

$$PAE = \frac{P_{OUT} - P_{IN}}{P_{DC}} = \eta_D \cdot \left(1 - \frac{1}{G}\right) \tag{3.2}$$

where

$$G = \frac{P_{OUT}}{P_{IN}} \tag{3.3}$$

is the power gain at the fundamental frequency.

3.2 Amplitude Distortion

Modulation schemes producing signals with high crest factors are common for the airlink of all modern mobile communication systems. For such signals highly linear power amplifiers are needed and amplifier's distortion plays an important role in the design. Therefore, the necessary basics on distortion in RF power amplifiers for a successful design are briefly described below.

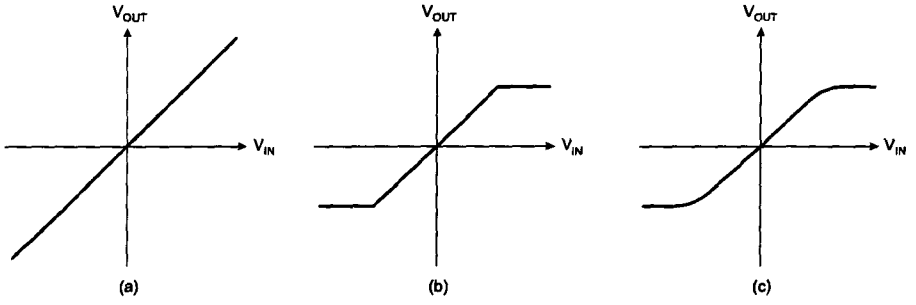


Figure 3.1: Linear and nonlinear amplification.

A perfect amplifier would have a linear transfer characteristic (Fig. 3.1a), where the output voltage would be a scalar multiple of the input voltage. The output shape from such an amplifier will be identical to that of the input and no additional frequency components will be introduced either within or outside of the amplifier bandwidth. Such an amplifier cannot be realized for all amplitudes. So it is desireable to get linear amplification to a certain threshold (Fig. 3.1b). Output signals above this threshold are hard-limited. Such an amplifier can be used up to its clipping level (saturation) without any loss of linearity. However , a real amplifier will not change from linear operation to saturation immediately. There will be a smooth transition (Fig. 3.1c) over a certain range of input/output signal levels. This transition will cause nonlinear distortions.

A good description of nonlinearity is given by power series. To describe the behavior of Fig. 3.1c a 1st and 3rd order-term do a good approximation. If $v_{in}(t)$ is the input signal, $v_{out}(t)$ the output signal , the gain is fixed to 1 and d controls 3rd order gain one can write:

$$v_{out}(t) = v_{in}(t) - d \cdot v_{in}^3(t). \tag{3.4}$$

This equation cannot model a constant saturation. But this is not necessary since an amplifier will not be operated in this region (Fig. 3.2). It should be noted that the amplification is not perfectly linear for small input levels. It just gets more and more linear with decreasing magnitudes.

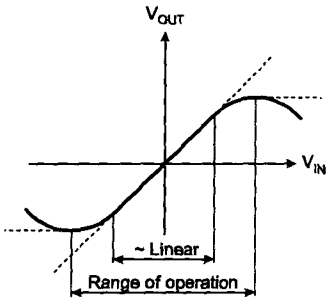


Figure 3.2: Transfer characteristic 3rd order approximation.

It must be stated here that (3.4) can only approximate the behavior of a real amplifier. To come closer to the real behavior higher order terms are necessary and for unsymmetric behavior even order terms have to be taken into consideration. For the sake of simplicity the following explanations are based on a model described by (3.4). A discussion of higher orders is given at the end of this section.

3.2.1 Single-Tone Effects of 3rd Order Nonlinearities

The simplest case for studying nonlinear effects is to apply a sinewave (a so called 'single-tone ') at the amplifier's input. If the input signal is given by

$$v_{in}(t) = a \ \cos(\omega t) \tag{3.5}$$

the resulting output signal after a 3rd order nonlinearity (Equ. 3.4) becomes

$$v_{out}(t) = \left(a - \frac{3a^3 d}{4}\right) \cos(\omega t) - \frac{a^3 d}{4} \cos(3\omega t). \tag{3.6}$$

Additional to the fundamental frequency ω the amplifier generates 3rd order harmonic frequencies at 3ω. Equation (3.6) also shows that the amplitude of the third harmonic is proportional to the third power of the amplitude at the fundamental and depends linearly on the amplifier's nonlinearity parameter d. It can also be seen that the voltage gain at the fundamental a is decreased by the third power of d. All distortions are generated outside of the signal band. They can be removed by filtering.

3.2.2 Two-Tone Effects of 3rd Order Nonlinearities

Because a single-tone signal doesn't carry any information it is much better to study the amplifier's behavior under presence of two carriers separated by a relatively small frequency

difference. This corresponds to an amplitude modulation (AM) and is a simple model for a narrowband modulated signal. The input signal is given by

$$v_{in}(t) = a\ [\cos(\omega_1 t) + \cos(\omega_2 t)]\,. \tag{3.7}$$

At the output of a nonlinear amplifier described by (3.4) one gets

$$\begin{aligned} v_{out}(t) &= \left(a - \frac{9a^3 d}{4}\right)\ (\cos(\omega_1 t) + \cos(\omega_2 t)) \\ &+ \left(-\frac{a^3 d}{4}\right)\ (\cos(3\omega_1 t) + \cos(3\omega_2 t)) \\ &+ \left(-\frac{3a^3 d}{4}\right)\ (\cos((2\omega_1 - \omega_2)\, t) + \cos((2\omega_2 - \omega_1)\, t)) \\ &+ \left(-\frac{3a^3 d}{4}\right)\ (\cos((\omega_1 + 2\omega_2)\, t) + \cos((2\omega_1 + \omega_2)\, t)) \end{aligned} \tag{3.8}$$

which is illustrated in Fig. 3.3. Additional to the harmonic terms at $3\omega_1$ and $3\omega_2$, which can easily be filtered, unwanted signals close to the carriers ω_1 and ω_2 are generated. These are the so called intermodulation products which occur at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$.

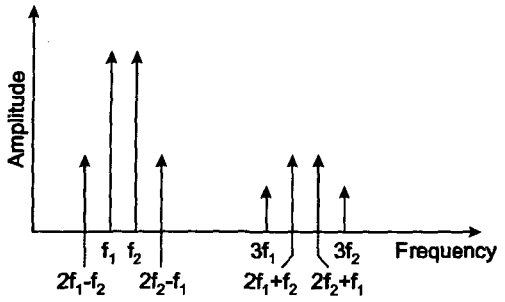


Figure 3.3: Two-tone response of a 3rd order nonlinear amplifier.

3.2.3 Higher Order Nonlinearities

As already mentioned above, the 3rd order terms are not sufficient to model the behavior of an amplifier exactly. Hence, higher order terms (5th, 7th, ...) as well as even order terms (2nd, 4th, ...) are required. The output signals of such an amplifier are shown in Fig. 3.4. Notice that frequency parts above the third harmonic zone are not shown but can be extended in mind.

Figure 3.4 also introduces a measure for the suppression of intermodulation products termed intermodulation distortion (IMD). The IMD defines the ratio of the desired carrier's power to those of the adjacent intermodulation products. It is also shown that the even order terms lead to DC and baseband components of the output signal. Such frequency components cause amplitude modulation of the output signal.

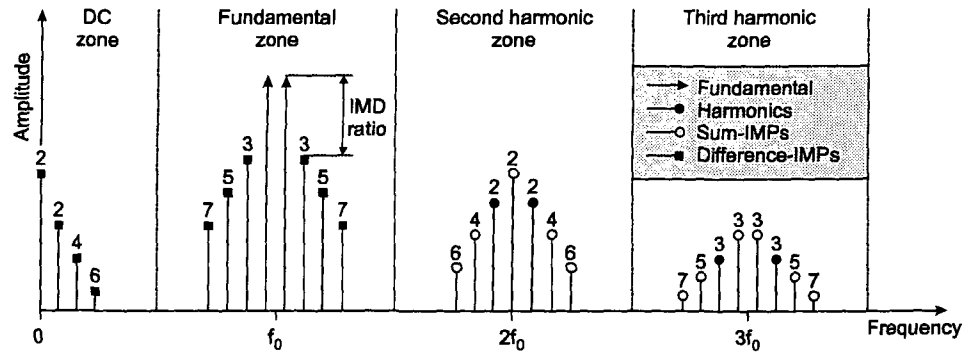


Figure 3.4: Two-tone response of 7^{th} order nonlinear amplifier [5].

Without listing the mathematical derivation in detail the following can be stated: If p is the order of the nonlinearity (in the example given $p = 7$) then the following output frequencies can occur for a two-tone signal:

$$m\omega_1 \pm n\omega_2 \quad \forall \quad m + n \leq p \tag{3.9}$$

To characterize the overall signal distortion of an amplifier the ratio between the two-tone signal power level of the carriers and the power level of all intermodulation products up to p^{th} order at the amplifier output is calculated and is called intermodulation distortion distance (IMDD) (3.10).

$$IMDD = 10 \cdot \log \left(\frac{\sum_m P_{Carrier,m}}{\sum_n P_{IMDn}} \right), \qquad m = 1..2; n = 3, 5, 7, ..., p \tag{3.10}$$

Figure 3.5 presents a power sweep of a nonlinear amplifier at two-tone excitation. The 1 dB compression point refers to the output power level at which the amplifier's transfer charactersitic deviates from that of an ideal, linear, characteristic by 1 dB. A further measure of nonlinearity is the intercept point. The 3rd order intercept point (IP_3) is defined as the point where the third order intermodulation product $P_{2f_1-f_2}$ intercepts with the fundamental output power P_{f_1}, when the amplifier is assumed to be linear.

3.2.4 Large-Signal IMD Sweet Spots

When operating an amplifier at a quiescent bias point close to pinch-off, generally the intermodulation products are observed to reduce in level. Figure 3.6 shows a typical performance of a Class B amplifier. This reduction in intermodulation distortion is called "sweet spot". Especially for efficient and highly linear amplifier the sweet spot is of great interest since it offers high linearity at much better efficiency when compared to the usually used reduction of input power level, called input back-off method.

Sweet spots occur by intermodulation cancellation of different odd order products which are out of phase for a distinct input level. Consider an amplifier modeled by a 5^{th} order polynomial

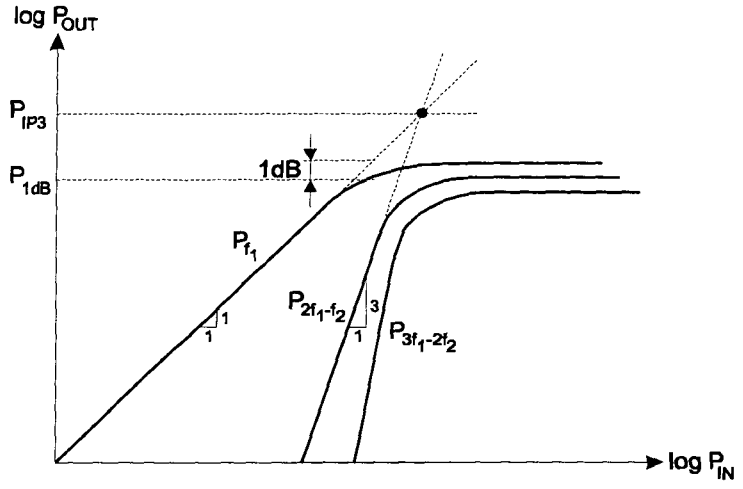


Figure 3.5: 1dB compression point P_{1dB} and 3rd order intercept point P_{IP3}.

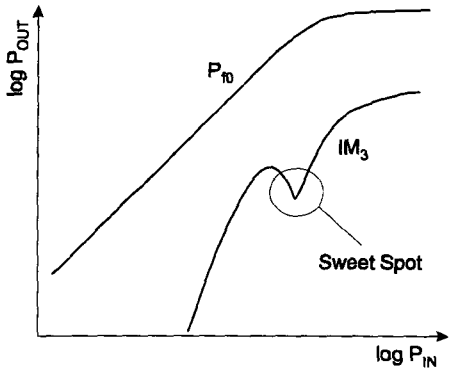


Figure 3.6: Typical Class B two-tone performance showing a sweet spot in IM_3.

$$V_{OUT} = a_1 V_{IN} + a_2 V_{IN}^2 + a_3 V_{IN}^3 + a_4 V_{IN}^4 + a_5 V_{IN}^5 \tag{3.11}$$

and a two tone input voltage

$$V_{IN} = V\cos(\omega_1 t) + V\cos(\omega_2 t). \tag{3.12}$$

The resulting 3rd order in-band intermodulation products have the magnitude

$$V_{OUT}(2\omega_{1,2} - \omega_{2,1}) = \frac{3}{4}a_3 V^3 + \frac{25}{8}a_5 V^5. \tag{3.13}$$

For a Class AB near Class B bias point the coefficient a_5 generally has negative value forcing IM3 products to decrease at a certain voltage level.

A more general approach for IMD prediction was presented in [6]. Small-signal analyses are based on Volterra series while large-signal is handled by Describing Function techniques [7]. The authors showed for a specific device operated in Class AB and Class B that it is possible to optimize IMD behavior by tuning load impedances of the baseband matching network and the 2nd harmonic matching network.

3.2.5 Complex Distortion Measures

In modern telecommunications circuits more complex signals than a two-tone signal are in use. With a complex modulation signal, like OFDM, no distinct intermodulation products occur, but a continuous power spectrum will be generated in the transmission channel and the adjacent channels. The generation of signal power in the adjacent channels is also called spectral regrowth. For such signals the two-tone IP_3 standard is no longer a good figure of merit. Therefore, more robust distortion measures, such as adjacent channel power ratio (ACPR), noise power ratio (NPR), and multitone intermodulation ratio (M-IMD), are in use.

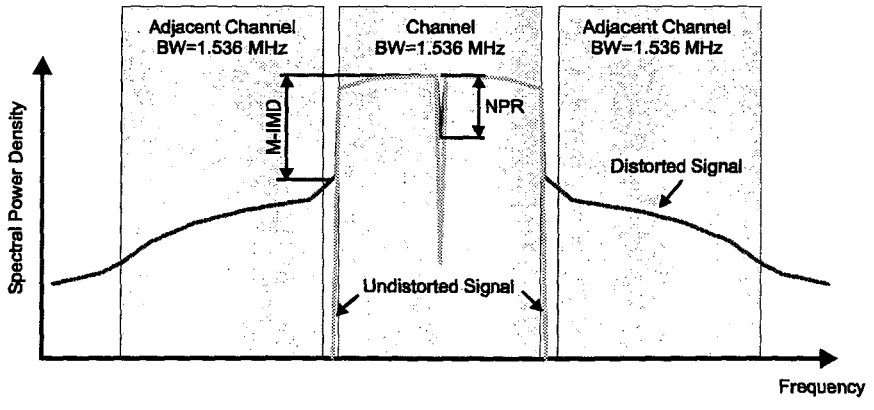


Figure 3.7: Spectral power density of an undistorted DAB signal and a DAB signal distorted by amplifier nonlinearities; definition of ACPR, NPR, and M-IMD.

ACPR is defined as the ratio between the total adjacent-channel integrated power and the power of the useful signal band.

NPR is the ratio between the in-band distortion and useful signal spectral densities when an in-band noise spectrum slice is removed.

M-IMD is the ratio between a useful tone power and the highest distortion tone power outside, but close to, the useful band. Figure 3.7 shows graphical representations of these three parameters.

A relationship between these multitone distortion measures and the more easily measured or simulated two-tone intermodulation distortion (IMD) would enable the full characterization/simulation of the device under multitone excitation using the well-known two-tone intermodulation test.

Based on simple 3rd order modeling of an amplifier characteristic an approximation of this relationship was derived in [8] and [9]. This process has many potential areas of inaccuracy, but it does serve to provide a roughly estimation of the desired response. The process is based on Volterra-Wiener theories, which state that any 3rd order system may be completely characterized by a three-tone test. Increasing the number of tones, therefore, will not yield any further information about the system and any additional effects seen in practice, when performing multitone testing, are due to the presence of higher order products.

By examination of the statistics of a multitone signal with uncorrelated phases and greater than about 10 carriers, the central limit theorem indicates that the resulting waveform tends toward a narrow-band noise excitation and the response of the system, therefore, approximates a noise power ratio test. Examination of a multicarrier signal utilizing an analytical approach can therefore be used to derive approximate measures of the complex signal discussed above.

Based on the definitions below, the following equations may be derived:

IMD_{2-tone}	Two-tone intermodulation distortion [dBc]
n	Number of tones
r	Adjacent channel number ($r = 1$ for the closest)
b	Number of tones on one side of the 'gap', where one or more tones are removed for NPR testing. For removal of a single tone at the center of the band, b =div$(\frac{n-1}{2})$.

ACPR

$$-ACPR_{dBc} = IMD_{2-tone,dBc} - 6\ dB + 10\log\left(\frac{n^3}{4A+B}\right) \tag{3.14}$$

$$A = \frac{2n^3 - 3n^2 - 2n}{24} + \frac{\mathrm{mod}\left(\frac{n}{2}\right)}{8}$$

$$B = \frac{n^2 - \mathrm{mod}\left(\frac{n}{2}\right)}{4}$$

NPR

$$NPR_{dBc} = IMD_{2-tone,dBc} - 6\ dB + 10\log\left(\frac{n^2}{4C+D}\right) \tag{3.15}$$

$$C = \left(\frac{n-b-2}{2}\right)^2 - \frac{\mathrm{mod}\left(\frac{n+b}{2}\right)}{4} + \left(\frac{b-1}{2}\right)^2 - \frac{\mathrm{mod}\left(\frac{b+1}{2}\right)}{4} + b(n-b-2)$$

$$D = \left(\frac{n-b-2}{2}\right) - \frac{\mathrm{mod}\left(\frac{n+b}{2}\right)}{2} + \left(\frac{b-1}{2}\right) + \frac{\mathrm{mod}\left(\frac{b+1}{2}\right)}{2}$$

M-IMD

$$M\text{-}IMD_{dBc} = IMD_{2-tone,dBc} - 6\ dB + 10\log\left(\frac{n^2}{4E+F}\right) \tag{3.16}$$

$$E = \left(\frac{n-r}{2}\right)^2 - \frac{\mathrm{mod}\left(\frac{n+r}{2}\right)}{4}$$

$$F = \left(\frac{n-r}{2}\right) + \frac{\mathrm{mod}\left(\frac{n+r}{2}\right)}{2}$$

Figure 3.8 plots these characteristics normalized to two-tone intermodulation ratio. These allows the relative level of each measure to be judged and indicates that ACPR is the closest to a two-tone equivalent, with NPR beign the furthest from the two-tone case.

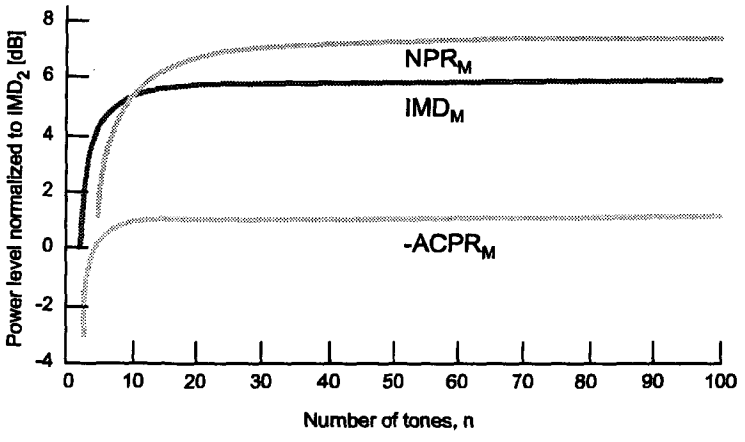


Figure 3.8: Normalized relationship between the various nonlinearity measures for multi-tone signals.

3.3 Phase Distortion

The discussion so far in this section has concentrated on amplitude nonlinearity. This is often termed AM-AM conversion. Another effect is, however, also present and that is conversion from amplitude modulation on the input signal to phase modulation on the output signal. This is known as AM-PM conversion. In general, AM-PM effects can be traced to the signal-level dependency of several key transistor model elements; in particular for FETs the input capacitance and both the depletion and the junction resistance of the gate-source diode. All these effects in themselves are interactive, highly complex and generally defy any attempt at simplified physical modeling, such as can be successfully employed for compression and clipping effects.

Consider a sinusoidally-modulated input carrier, $P_{IN}(t)$, with a modulating signal defined by

$$M(t) = A_M \cos(\omega_M t). \tag{3.17}$$

For an ideal amplifier, the output phase is given by

$$\Phi\left(P_{IN}\left(t\right)\right) = K_\Phi \tag{3.18}$$

where K_Φ is constant. In other words, the output phase remains constant, irrespective of the amplitude of the input signal.

In the case of a real amplifier, however, AM/PM conversion will result, hence (3.18) becomes

$$\begin{aligned} \Phi\left(P_{IN}\left(t\right)\right) &= K_\Phi \cos\left[\omega_C t + A_M \cos\left(\omega_M t\right)\right] \\ & \quad K_\Phi \sum_{n=-\infty}^{\infty} J_n(A_M) \cos\left[\left(\omega_C + n\omega_M\right) t\right] \end{aligned} \tag{3.19}$$

where J_n is a Bessel function of order n and ω_C is the angular frequency of the carrier signal. The resulting spectrum is that of a phase-modulated carrier with a sinusoidal modulated signal, hence forming IMD products similar to those resulting from an amplitude nonlinearity.

A real amplifier will, of course, suffer from both forms of nonlinearity to some degree and the output spectrum will consist of a superposition of both effects. This superposition can cause asymmetry of the IMD products, since the upper and lower IMD products resulting from AM/AM conversion are in phase, whereas a component of those resulting from AM/PM conversion can be 180° out of phase.

The phase difference and IMD product inequality can arise from various effects described below.

Supply Modulation Effects

A very common cause of asymmetrical IM effects in RF power amplifiers is inadequate supply rail decoupling. A deep Class AB power amplifier draws current from the supply in synchronism with the AM of the input signal; the "DC" supply is now a high-level

broadband signal, stretching up into the megahertz region for multicarrier signals. This large current variation should be isolated from the power supply circuitry by means of the decoupling network. This network should be mounted as close to the required point and should consist of a range of values and technologies to ensure that all envelope frequencies of interest are adequately decoupled.

Imperfections in the decoupling network will result in a supply voltage variation in synchronism with the envelope current drawn from the supply. This in turn will result in an unwanted envelope modulation of the output signal. The reactive nature of the decoupling network will apply the envelope modulated signal with a different phase angle to the wanted modulation. This in turn will result in asymmetry in the resulting IMD products [10].

Bias Modulation Effects

The device biasing circuitry can also suffer from a similar problem to that outlined above, although not generally due to cycling currents being drawn from the supply. The function of the bias network is to supply an appropriate and constant voltage or current to the gate or base of the device. For RF signals it should appear as high impedance and to modulation signals very low impedance. Signals at the modulation frequency are generated by nonlinearities in the base or gate of the active device and these are often reflected, rather than absorbed by the matching network. The reflected signals will combine with the wanted input signals and cause modification of the IMD products in most cases including asymmetry.

Interstage Reflections

As mentioned above, the input to an active device generates distortion. This distortion can be passed by the input matching network (modified arbitrarily in amplitude and phase) to the output of the preceeding stage. This in turn will modify, again arbitrarily in amplitude and phase, the distortion and will reflect it back to the originating input. This additional input signal has effect on the resulting output distortion.

Solutions to these problems include changes in the matching network to reduce or eliminate these signals (e.g. arranging the network to have a low impedance at the harmonics and/or the envelope frequencies) or including interstage isolation (e.g. an isolator).

Thermal Effects

Supply current variation, as mentioned above, will also influence the temperature of the active device. Due to the thermal low pass characteristics of an active device the "DC" bias point will change with the envelope frequency. This will modulate the device and, therefore, generate distortion at the transistor's output.

Thermal effects are caused by electro-thermal couplings, which affect low modulation frequencies up to 1 MHz. The dissipated power of a FET device can be expressed as

$$P_{DISS} = V_{DS} \cdot I_{DS} \tag{3.20}$$

where V_{DS} is the drain-source voltage and I_{DS} the drain-source current. Since two 1st order fundamental signals are multiplied together, the spectrum of the dissipated power always includes 2nd order signal components, i.e. DC, envelope, sum and 2nd harmonics. The temperature variations caused by the dissipated power are determined by the thermal impedance, which describes the heat flow from the device. Due to the finite mass of the component, thermal impedance in the active device is not purely resistive, but instead it forms a distributed low-pass filter with a wide range of time constants. This means that the temperature changes caused by the dissipated power do not occur instantaneously, but due to the mass of the semiconductor and package, frequency-dependent phase shifts always exist.

The thermal effects will cause distortion at the transistor's output and asymmetry in IMD products. Furthermore, due to the fact that temperature changes do not occur instantaneoulsy the transistor's behavior is dependent of its thermal history – it has a thermal memory.

Memory Effects

Memory effects are defined in [11] as modulation frequency dependence of the distortion components, and it is clear that electrical and thermal memory effects of this kind do exist. The electrical ones are produced by non-constant node impedances inside the frequency bands, with non-constant envelope impedance, which is usually caused by bias impedance, causing most of these effects. Thermal memory effects are produced by the chip temperature, which is modulated by the signal applied. Since the chip temperature varies at the envelope frequency and some of the electrical parameters of the transistor are affected by temperature, IMD components are generated. As the temperature rise caused by dissipated power is highly dependent on the modulation frequency, IMD components become dependent on it, too, and memory effects occur.

Figure 3.9 shows the measured AM/AM and AM/PM response of a GaAs power amplifier for different modulation schemes. Without memory effects the reponse to the different modulation schemes is expected to be equal. Figure 3.9 clearly shows that for the amplifier's AM/PM conversion this is not true. The AM/PM response is strongly influenced by the amplifier's memory effects.

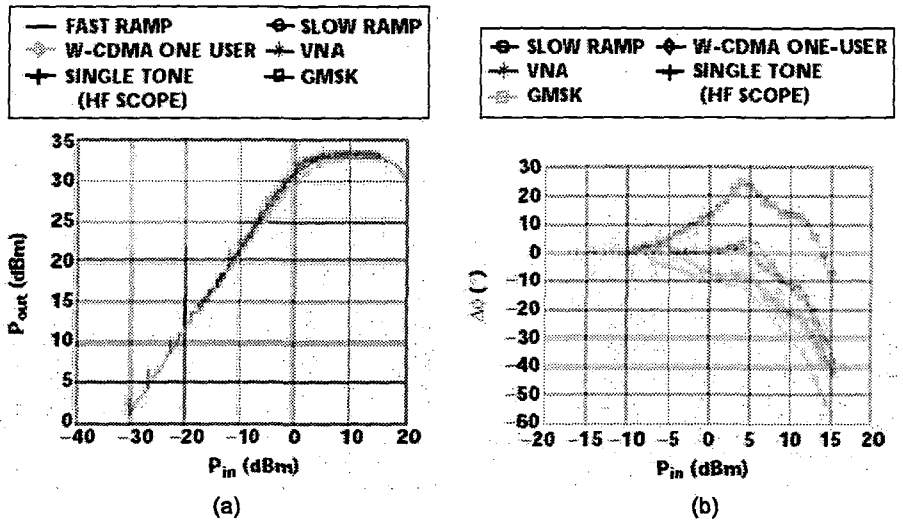


Figure 3.9: Distortion of a GaAs power amplifier [12]. – (a) AM/AM response; (b) AM/PM response.

3.4 Efficient Amplifier Concepts

Power amplifiers are classified according to their mode of operation.

For better understanding of the most important device parameters and idealized FET input and output characteristics are explained here.

Figure 3.10 illustrates the drain to source current I_{DS} versus gate to source voltage V_{GS} input characteristic and drain to source current versus drain to source voltage V_{DS} output charactersitic for an n-channel junction FET. The characterization of a FET starts with the identification of the most important physical parameters:

- The pinch-off voltage V_P, identifies the gate to source voltage where the channel is completely depleted and, therefore, no drain to source current can flow.
- The maximum drain to source current I_m, is normally not equal to the current at zero gate to source voltage I_{DSS} (saturated drain to source current) and is determined by the built-in voltage V_{BI}. Above this voltage boundary the gate barrier disappears and a forward current is induced into the device, and this increases the channel resistance.
- In this rather crude FET model, the slope of the input characteristic is linear between VP and VBI (this is a permissible approximation of many GaAs power FETs). This means that the transconductance g_m, which is defined as the derivative of drain to source current I_{DS} on gate to source voltage V_{GS}, is constant in this region.
- The output characteristics of a FET can be divided into three regions: ohmic, saturation, and breakdown region. In the ohmic region, the drain to source current is a (linear) function of drain to source voltage for a constant gate to source voltage. In the saturation region the device operates as a voltage controlled current source. Ideally, I_{DS} shows little dependence on V_{DS} which is, therefore, not considered here. The lower limit of the saturation region is given by the knee voltage V_K, the upper one by that drain to source voltage where gate to drain breakdown occurs(V_{DSmax}).
- In the breakdown region I_{DS} rises abruptly due to avalanche ionization and tunnelling breakdown. The corresponding drain to source voltage V_{DSmax} is a function of V_{GS}, and can either increase or decrease with increasing V_{GS}. Here, we assume that $V_{DS\,\mathrm{max}}$ is independent of V_{GS}.
- The drain to source V_{DD} is defined to be exactly between V_K and $V_{DS\,\mathrm{max}}$ and corresponds with the drain to source to bias voltage V_{DS0} for optimum power operation for all classical amplification modes.

3.4.1 Class A, AB, B, C

The classical approach of a power amplifier is illustrated in Fig. 3.11 in a simplified form (no matching circuits). The tank circuit at the output ensures that the output voltage is sinusoidally shaped (this is important for non-class A amplifier concepts). The classes A to C are distinguished by the conduction angle α. The conduction angle indicates the

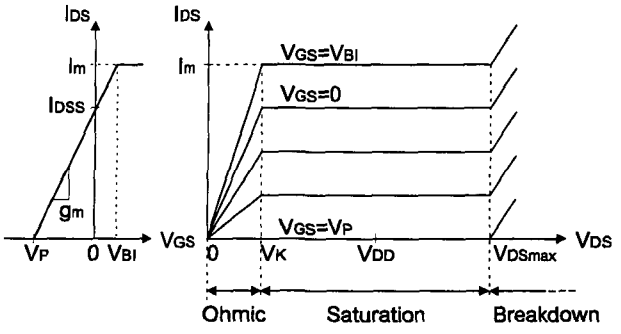


Figure 3.10: Input and output characteristics of an idealized FET.

proportion of the RF cycle for which conduction occurs (this is where the drain to source current I_{DS} is non-zero). Due to the symmetry of the cosine function about zero there has been some confusion about the definition of the conduction angle. It is often seen that the conduction angle is defined as $\frac{\alpha}{2}$. Table 3.1 defines the classical amplifier modes of operation, in terms of quiescent bias point and conduction angle.

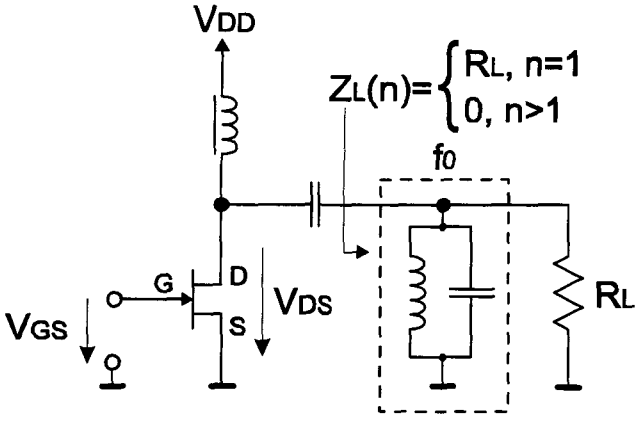


Figure 3.11: Circuit diagram of a tuned loaded FET.

Figure 3.12 displays the device control characteristics including the load line for optimum output power, the input voltage waveform and the drain to source current and voltage waveforms of a FET operated in classes A to C. The optimum load impedance can be calculated as the maximum voltage swing at the fundamental frequency to the maximum current swing at the fundamental frequency. As an example, for a class A operation the current swing, which is purely sinusoidal, is limited by zero and the maximum current I_m and the voltage swing is limited by the knee voltage V_K and the breakdown voltage V_{DSmax}. Therefore, the optimum load impedance for class A mode is

$$R_{L,opt} = \frac{\Delta V}{\Delta I} = \frac{2(V_{DD} - V_K)}{I_m}. \tag{3.21}$$

If one looks at the current waveform in Fig. 3.12, it is intuitive that the mean (DC)

Mode	Bias Point	Quiescent Current	Conduction Angle
A	$\frac{V_P+V_{BI}}{2}$	$\frac{I_m}{2}$	2π
AB	$V_P - \frac{V_P+V_{BI}}{2}$	$0 - \frac{I_m}{2}$	$\pi - 2\pi$
B	V_P	0	π
C	$< V_P$	0	$0 - \pi$

Table 3.1: Classical modes of operation.

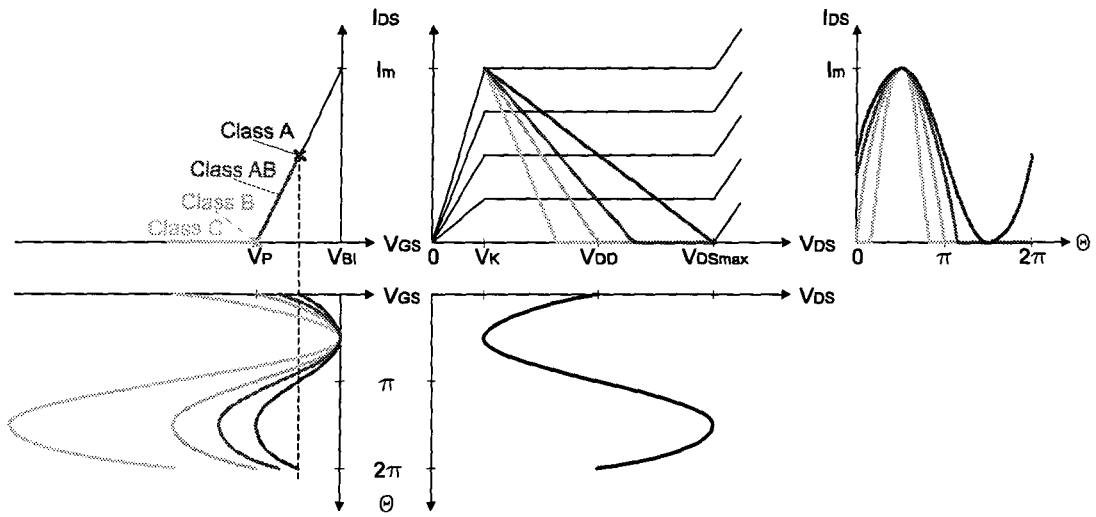


Figure 3.12: Idealized input and output FET characteristics and the optimum load impedances for Class A, AB, B, and C operation.

component will decrease as the conduction angle is reduced. It is less obvious what happens to the fundamental and harmonic components. The answer can be found by Fourier analysis of the waveforms.

The waveform can be written as

$$I_{DS}(\Theta) = \begin{cases} I_{DS,0} + (I_m - I_{DS,0})\cos(\Theta) & -\frac{\alpha}{2} < \Theta < \frac{\alpha}{2} \\ 0 & -\pi < \omega t < -\frac{\alpha}{2}; \frac{\alpha}{2} < \omega t < \pi \end{cases} . \tag{3.22}$$

The mean current, or DC component, is then given by

$$I_{DS,0} = \frac{1}{2\pi}\int_{-\frac{\alpha}{2}}^{\frac{\alpha}{2}} \frac{I_m}{1-\cos\frac{\alpha}{2}}\left(\cos\Theta - \cos\frac{\alpha}{2}\right) d\Theta = \frac{I_m}{2\pi}\frac{2\sin\frac{\alpha}{2} - \alpha\cos\frac{\alpha}{2}}{1-\cos\frac{\alpha}{2}} \tag{3.23}$$

and the magnitude of the n$^{\text{th}}$ harmonic is

$$I_{DS,n} = \frac{1}{\pi}\int_{-\frac{\alpha}{2}}^{\frac{\alpha}{2}} \frac{I_m}{1-\cos\frac{\alpha}{2}}\left(\cos\Theta - \cos\frac{\alpha}{2}\right)\cos(n\Theta)\, d\Theta \tag{3.24}$$

where no quadrature components occur due to the selection of an even function for the RF current waveform.

The results from the evaluation of these integrals up to $n = 5$ are shown in Fig. 3.13. Examining this figure it becomes quite clear that the DC component decreases monotonically as the conduction angle is reduced. The only significant harmonic, other than the fundamental, throughout the class AB range and up to midway class B condition is the second. The odd harmonics can be seen to pass through zero at the class B point, but in AB mode, the third harmonic is not negligible, which means that intermodulation distortion will occur. In general, at normalized drain current levels lower than about 0.1, weakly nonlinear components of the transconductance characteristic may substantially change the overall picture. Figure 3.14a shows the output versus input power characteristics of a FET amplifier in class A to class B mode with a constant transconductance g_m. Only class A and class B show linear characteristic up to the onset of voltage clipping. Figure 3.14b shows the input-output charactersitics for the same operation modes simulated with a more realistic transconductance. The square-law tail of the transconductance causes the class B gain to fall off at lower drive levels. That can be compensated by running in a deep class AB mode, in which excellent linearity can be obtained.

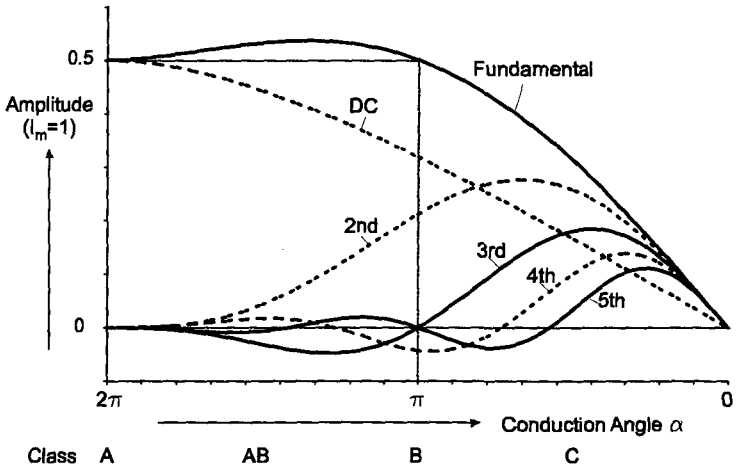


Figure 3.13: Fourier analysis of reduced conduction angle mode.

Figure 3.15 shows the RF ouput power at the fundamental frequency, the power gain and drain efficiency versus conduction angle α for an amplifier circuit as shown in Fig. 3.11. Ideal conditions have been assumed: a perfect harmonic short, maximum linear current swing up to I_m, and a maximum voltage swing of $2V_{DD}$, with no knee region. If the knee region is taken into account all three curves are decreased by the factor $\varkappa = \frac{V_{DD}-V_K}{V_{DD}}$.

The main features of class A to class C operation can be determined from the curves shown in Fig. 3.15. Between class A and class B operation, the fundamental RF output power is approximately constant, showing an increase of a few tenths of a decibel in the mid-AB range over the class A power output. Although the class B condition produces the same power as class A the efficiency is increased to a maximum of 78.5 % due to the reduced quiescent current. The higher efficiency is payed for by a gain reduction of 6 dB (only half the input voltage swing is used). This may be a significant problem if a device

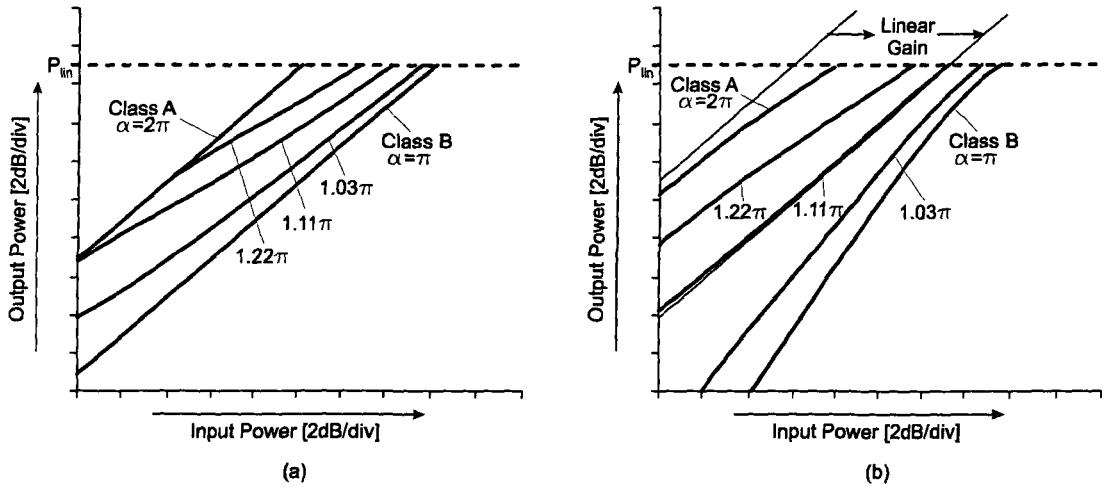


Figure 3.14: Input-output power characteristics for class A to class B [10]. – (a) ideal (constant) transconductance g_m; (b) non-ideal transconductance g_m.

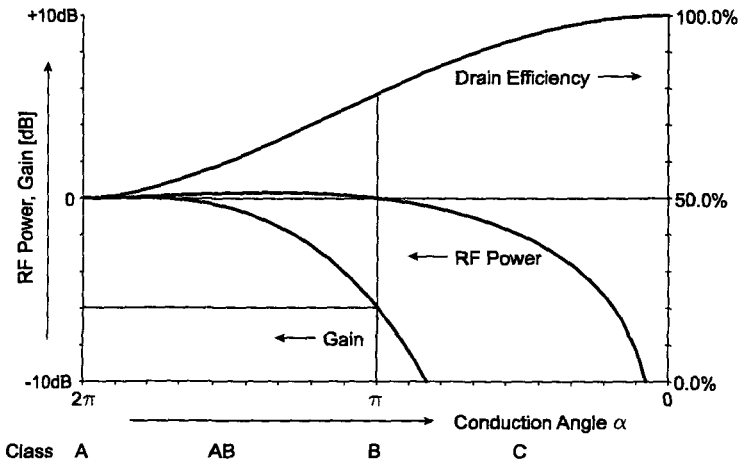


Figure 3.15: RF power, gain, and drain efficiency as a function of conduction angle; optimum load and harmonic short (tank circuit) assumed. Power and gain are normalized to class A operation.

with low gain is used. The class C condition shows rapidly increasing drain efficiency with decreasing conduction angle. However, that efficiency is accompanied by a substantial reduction in RF power.

Since transistor breakdown is determined by the drain to gate voltage the maximum drain to source voltage $V_{DS,\max}$ is reduced for non-class A operation by the overshoot voltage ΔV_{OS}, which is the voltage difference from pinch-off voltage V_P to the negative input voltage peak, to

$$V_{DS,\max} = V_{BR} + V_P - \Delta V_{OS}, \tag{3.25}$$

where V_{BR} is the breakdown voltage (note that V_P is negative valued). Therefore, the maximum DC drain to source voltage $V_{DD,\max}$ is lowered as compared to class A and, consequently, the maximum RF output power is decreased too.

Results found in literature of class AB, B, and C mode operated power amplifier in L-band are listed in Tab. 3.2.

Reference (Year)	Mode of Operation	f [GHz]	PAE [%]	η_D $\{\eta_C\}$ [%]	P_{OUT} [dBm]	G [dB]	Device (Style)
BOUTHILLETTE 1996 [13]	AB	1.6	65	67	40.9	16.1	PHEMT
ONO 1994 [14]	AB	1.5	62	75	30.8	7.8	PHEMT Chip
WANG 1993 [15]	AB	1.8	45	{52}	30	9	HBT
TATENO 1994 [16]	B	0.9	70	{72}	30	15.7	HBT Packaged
OTA 1992 [17]	B	0.95	75	79	32.5	12.5	FET Chip
IWAI 2000 [18]	B	1.95	42	42	27	30.5	HBT MMIC
MALLET 1996 [19]	C	1.8	90	{91}	23	18	HBT

Table 3.2: Results reported at classes AB, B, and C in L-band.

3.4.2 Harmonic Controlled Amplifiers – HCA

To maximize drain/collector efficiency power dissipation in the active device has to be minimized. The optimal dynamic load line for minimized power dissipation is displayed in Figure 3.16. Theoretically, an efficiency of 100 % is possible at negligible knee voltage V_K. A significant knee voltage will reduce efficiency by the factor $\kappa = \frac{V_{DD}-V_K}{V_{DD}}$. To achieve the shown dynamic load line drain-source voltage V_{DS} have to be zero when drain-source current I_{DS} is high and vice versa. This is realized for class E operation mode by using the

transistor as a switch and can be also be realized by harmonic manipulation of the drain-source voltage and current, respectively. Such amplifiers are called harmonic controlled amplifiers.

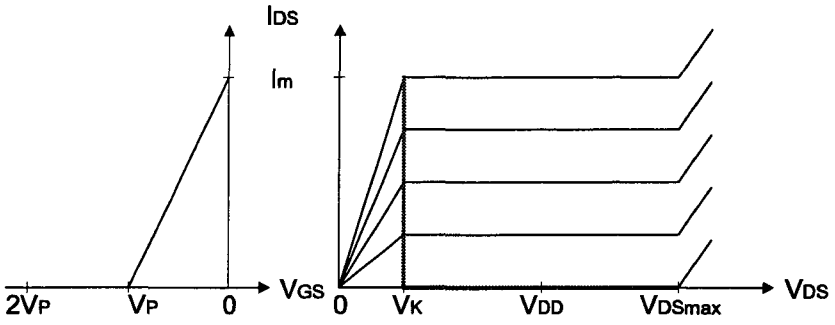


Figure 3.16: Dynamic load line for maximum efficiency.

Class E

In class E amplifiers the transistor operates as an on/off switch and the load network shapes the voltage and current waveforms to prevent simultaneous high voltage and high current in the transistor; that minimizes power dissipation, especially during the switching transitions. The schematic of a class E amplifier is depicted in Fig. 3.17. It consists of a resonant circuit (C_S, L_S) which is tuned to the fundamental frequency and a parallel capacitor C_P consisting of the parasitic capacitance of the active device output and an additional one for optimum tuning.

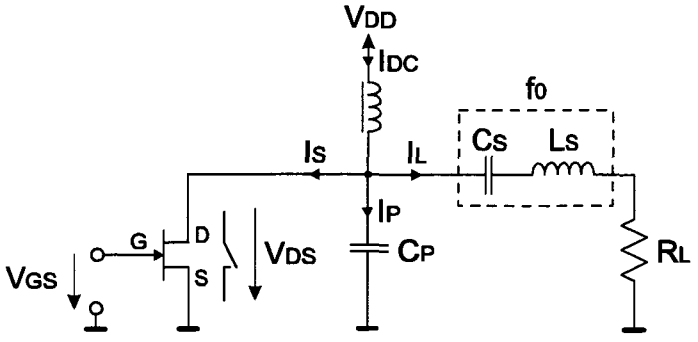


Figure 3.17: Circuit diagram of a class E amplifier.

Since the series resonant circuit in Fig. 3.17 is tuned to the fundamental frequency the load current I_L has to be sinusoidally shaped. Applying Kirchhoff's Current law one gets

$$I_{DC} - I_L = I_S + I_P. \tag{3.26}$$

Since the left side of (3.26) is a current sinewave with amplitude I_L and DC offset I_{DC}, this must hold for the right side as well. Furthermore, if the amplifier is in a steady

state, the capacitor current I_P cannot have a DC component, which leads to the current waveforms shown in Fig. 3.18. The voltage across the switch, V_{DS}, is easily obtained by integration of the drain to source current I_S during the time the switch is open. As can be seen in Fig. 3.18 there are no overlaps of drain to source voltage and current, no harmonics can reach the load resistor and, consequently, the drain efficiency is 100 % (when the knee voltage of the device is neglected).

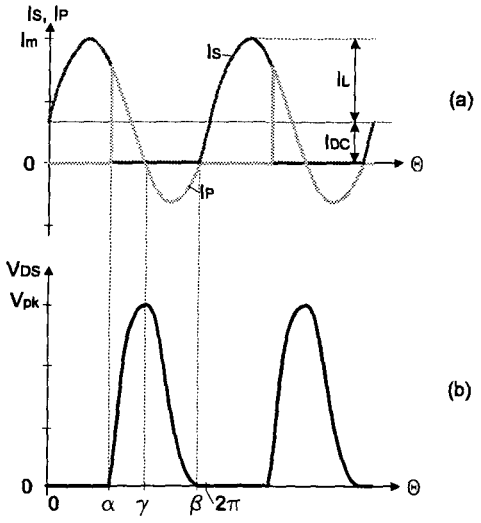


Figure 3.18: Class E RF waveforms. – (a) switch current I_S and shunt capacitor current I_P; (b) switch/shunt capacitor voltage V_{DS}.

In [20] it has been demonstrated that the peak drain to source voltage V_{PK} reaches $3.6V_{DD}$ and this normally precludes the use of class E amplifiers with GaAs FETs at higher output power, as they have a low gate to drain breakdown voltage. Another limiting factor is the inherent drain to source capacitance of the active device, because it determines the maximum operating frequency and it further can change significantly with drain to source and gate to source voltage.

Class E is a not a promising mode of operation to minimize distortion. As the device output current contains odd-order harmonics, which are responsible for intermodulation distortion, the distortion characteristics of such an amplifier will not be sufficient for linear operation.

The performance of class E amplifiers operating in L-band which was reported in literature is listed in Tab. 3.3.

Reference (Year)	f [GHz]	PAE [%]	η_D $\{\eta_C\}$ [%]	P_{OUT} [dBm]	G [dB]	Device (Style)
SOWLATI 1996 [21]	1.8	57	–	23	16	2xFET MMIC
MADER 1995 [22]	1.0	73	75	29.7	14.7	FET
GREBENNIKOV 2003 [23]	1.8	52	{53}	30	20	HBT MMIC

Table 3.3: Results reported at class E operation in L-band.

Class F

The best known harmonic controlled amplifier is the class F amplifier [24]. Class F amplifiers use multiple-resonator output filters to control the harmonic content of their drain-source voltage and drain current waveforms. To achieve maximum efficiency the drain-source voltage is shaped rectangularly while the drain-source current is shaped half sinusoidally (Fig. 3.19). For inverted class F operation the roles of voltage and current are reversed.

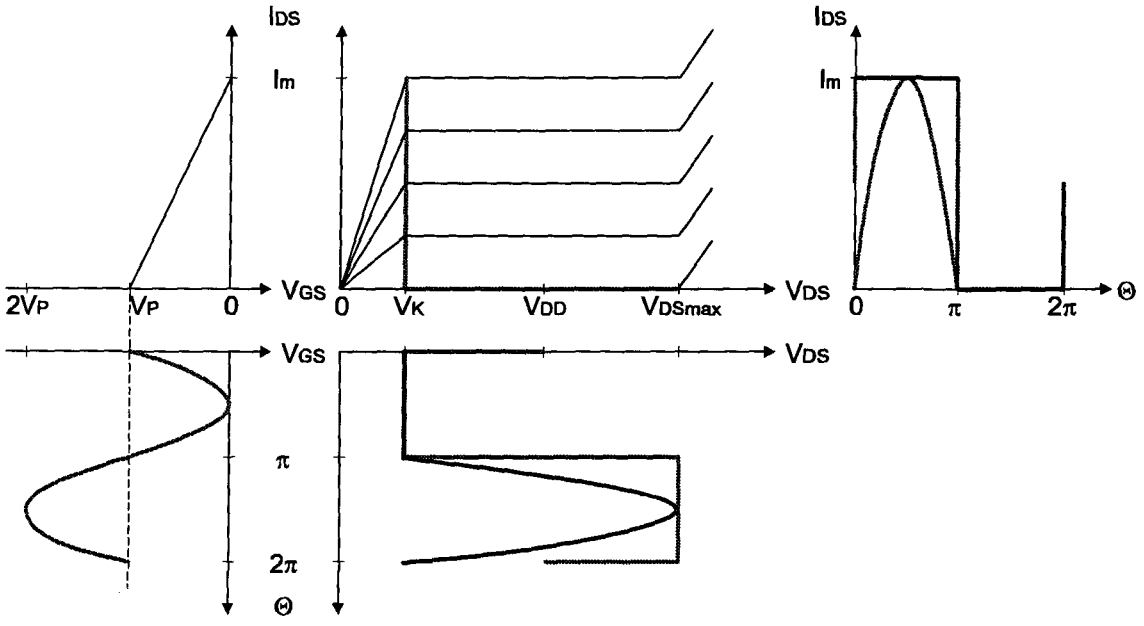


Figure 3.19: Optimum dynamic load line and voltage and current waveforms for class F operation. - Red: Class F (odd class F); Blue: inverted class F (even class F).

Fourier analysis of the rectangular drain-source voltage and of the half sinusoidal drain-source current lead to

$$\begin{aligned} V_{DS}(t) &= V_{DD} - \\ &\quad -\frac{4}{\pi}\cdot(V_{DD}-V_K)\cdot\sin(\omega_0 t) - \\ &\quad -\frac{4}{\pi}\cdot(V_{DD}-V_K)\cdot\left(-\frac{\sin(3\omega_0 t)}{3^2}+\frac{\sin(5\omega_0 t)}{5^2}-\ldots\right), \end{aligned} \tag{3.27}$$

$$\begin{aligned} I_{DS}(t) &= \frac{I_m}{\pi} + \\ &\quad +\frac{I_m}{2}\sin(\omega_0 t) - \\ &\quad -\frac{2I_m}{\pi}\cdot\left(\frac{\cos(2\omega_0 t)}{1\cdot 3}+\frac{\cos(4\omega_0 t)}{3\cdot 5}+\frac{\cos(6\omega_0 t)}{5\cdot 7}+\ldots\right). \end{aligned} \tag{3.28}$$

Equations (3.27) and (3.28) show that only odd harmonics are present in V_{DS} and even harmonics are present in I_{DS}, respectively. Thus, class F output termination can be achieved by the circuit depicted in Fig. 3.20. To all even harmonics a short cicuit is presented zeroing the drain-source voltage and allowing the drain-source current which is generated by the device to flow. To shape the drain-source voltage rectangularly and to zero the drain-source current an open circuit is presented to all odd harmonics. From (3.27) and (3.28) the optimum load impedance for the fundamental can be derived to

$$R_{L,opt,CLASS\ F} = \frac{V_{DS,f_0}}{I_{DS,f_0}} = \frac{4}{\pi} \cdot \frac{2(V_{DD} - V_K)}{I_m} = \frac{4}{\pi} \cdot R_{L,opt,CLASS\ A}. \tag{3.29}$$

and the maximum output power can be computed to

$$P_{\max,CLASS\ F} = \mathrm{Re}\,(V_{DS,f_0}.I_{DS,f_0}) = \frac{4}{\pi} \cdot \frac{(V_{DD} - V_K) \cdot I_m}{4} = \frac{4}{\pi} \cdot P_{\max,CLASS\ A} \tag{3.30}$$

which is an increase of output power of 1.05 dB compared to class A operation. Since a class F amplifier is biased in class B condition a gain reduction of 6 dB compared to class A will occur. This reduction is reduced by the output power increase to 5 dB compared to class A operation.

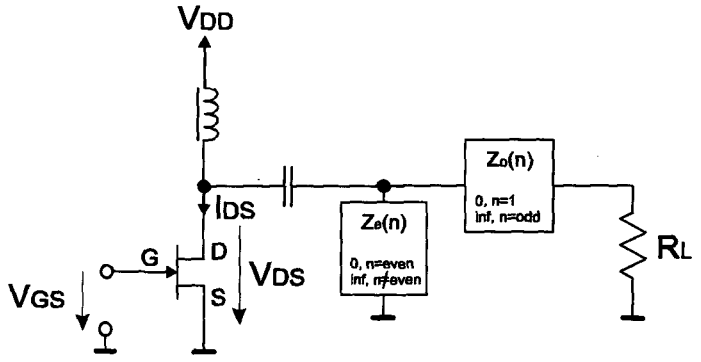


Figure 3.20: Ideal circuit for class F operation.

For practical realization of a class F amplifier the number of controlled harmonics must be limited to get a feasible design since the drain-source capacitance, lead inductance, lead length, and dispersion make implementation of reasonably ideal tuned circuits difficult. Furthermore, many active microwave devices do not have enough gain at higher harmonics. Therefore, usally termination is implemented up to the third harmonic, neglecting or short circuiting all higher harmonic signals.

Maximum flat waveforms represent the limiting case of perfect (low resistance) saturation of the RF-power device during conduction of peak drain-source current. The waveform factors for maximally flat waveforms are derived in [24] by setting various derivatives of the waveforms to zero. The resulting power and efficiency, while typical, are not the maximum possible. Investigations on the maximum efficiency and output power level were made in [25]. For a more detailed understanding the dependency of efficiency and output power on the 2^{nd} harmonic current ratio and the 3^{rd} harmonic voltage ratio of the drain-source

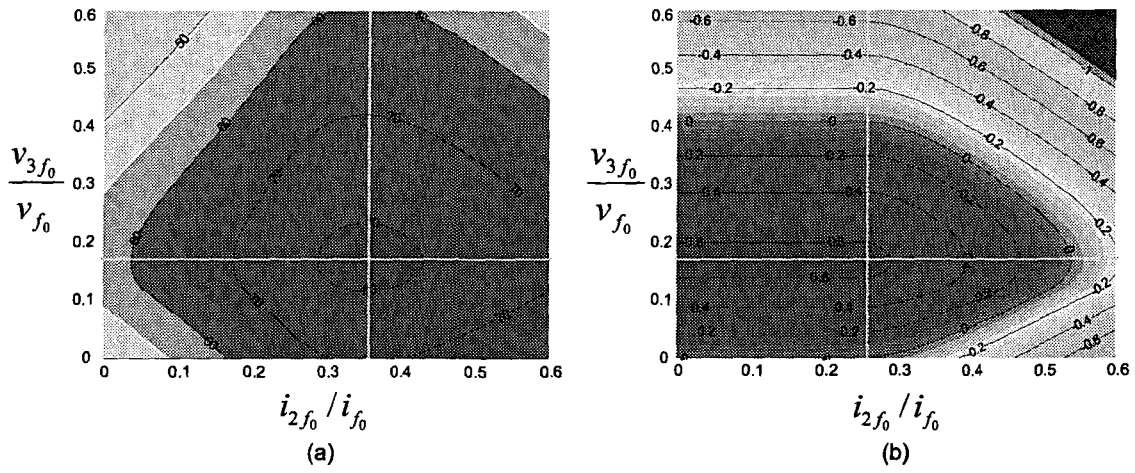


Figure 3.21: Dependency of efficiency and output power on normalized 3rd harmonic voltage and normalized 2nd harmonic current. – (a) Drain efficiency; (b) potential output power increase in dB compared to class A operation.

waveforms were computed and the result is shown in Fig. 3.21. The dashed lines indicate the optimum ratios for maximum efficiency and maximum output power. While the 3rd order voltage ratio can be optimized $\left(\frac{v_{3f_0}}{v_{f_0}} = \frac{1}{6}\right)$, different optima for the 2nd order current ratio are derived. The resulting ratio for optimum efficiency is $\frac{i_{2f_0}}{i_{f_0}} = 0.3535$ while the optimum for maximum output power is in the range of $\frac{i_{2f_0}}{i_{f_0}} = 0...0.25$ where $\frac{i_{2f_0}}{i_{f_0}} = 0.25$ equals the ratio for optimally flat drain-source current. The achieved ideal results of efficiency and output power are summarized in Tab. 3.4 for different harmonic ratios. The resulting waveforms and dynamic load lines for both optima are displayed in Fig. 3.22. In contrast to the maximally flat current waveform for maximum power the maximum efficiency current waveform exhibit slight ripples.

$\frac{i_{2f_0}}{i_{f_0}}$	$\frac{v_{3f_0}}{v_{f_0}}$	η_D [%]	$\frac{P_{OUT,class\ F}}{P_{OUT,class\ A}}$ [dB]
0.25 (flat)	0.111 (flat)	74.91	0.506
0.3535	0.111 (flat)	79.54	0.381
0.25 (flat)	0.166	76.98	**0.625**
0.3535	0.166	**81.65**	0.495

Table 3.4: Results obtained from different harmonic ratios.

Deeper investigations on linearity were not found in literature but class F is a promising mode of operation to minimize distortion even in saturation (see Fig. 3.19). As the device output current does not contain odd-order harmonics, which are responsible for intermodulation distortion, the distortion characteristics of such a harmonic controlled amplifier is similar to that of class A/AB (see Fig. 3.13 and 3.14). Further investigations on the linearity of class F amplifiers and harmonic termination will be presented in Chapter 5.2.

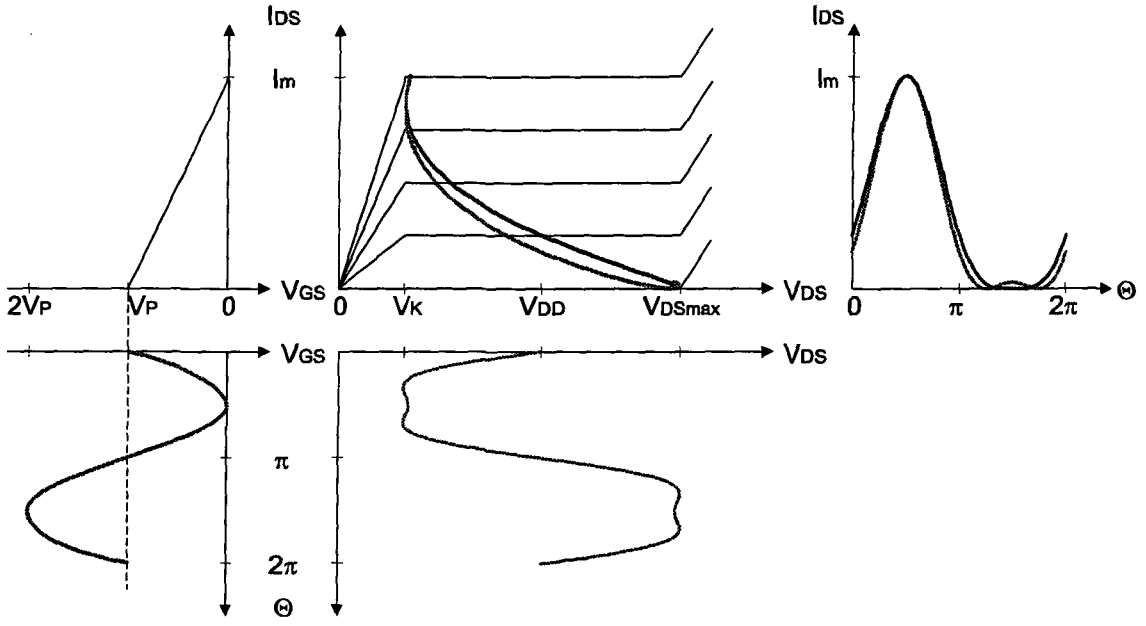


Figure 3.22: Dynamic load line and drain source voltage and current waveforms for maximum efficiency and maximum output power, respectively. – Red: maximum efficiency, Blue: maximum output power.

The performance of class F amplifiers operating in L-band which was reported in literature is listed in Tab. 3.5.

Reference (Year)	f [GHz]	PAE [%]	η_D $\{\eta_C\}$ [%]	P_{OUT} [dBm]	G [dB]	Device (Style)
DUVANAUD 1993 [26]	1.75	71	77	24.5	11	FET (Chip)
MALLET 1996 [27]	1.8	68	{71}	26.8	13.3	HBT
WEI 2000 [28]	0.94	83.1	86.8	13.7	24.4	pHEMT
BARATAUD 1999 [29]	1.8	84	87	21.1	14.6	MESFET
PEDRO 1998 [30]	1.8	50	55	19.5	10.5	MESFET MMIC

Table 3.5: Results reported at class F operation in L-band.

hHCA and rHCA

To enhance class F gain reduction, class F operation was further developed in [31] into the half sinusoidally driven harmonic controlled amplifier (hHCA) and the rectangularly driven harmonic controlled amplifier (rHCA). The according signal waveforms are displayed in Fig. 3.23. These harmonic controlled amplifiers use a class F and inverse class F output termination network, respectively, to shape the drain waveforms but applies a half sinusoidal signal or a rectangular signal at the transistor's input. The amplifier is biased in a class AB condition for hHCA and in a class A condition for rHCA at the gate, respectively, to achieve full input voltage swing (Fig. 3.23). Since the input voltage swing is only half compared to class F a gain improvement of 6 dB is achieved for hHCA/rHCA operation leading to a gain improvement of 1 dB compared to class A operation. Furthermore, the drain gate voltage which is responsible for breakdown, is reduced by a value equal to the pinch-off voltage thus improving reliability or allowing for higher drain-source voltage swing.

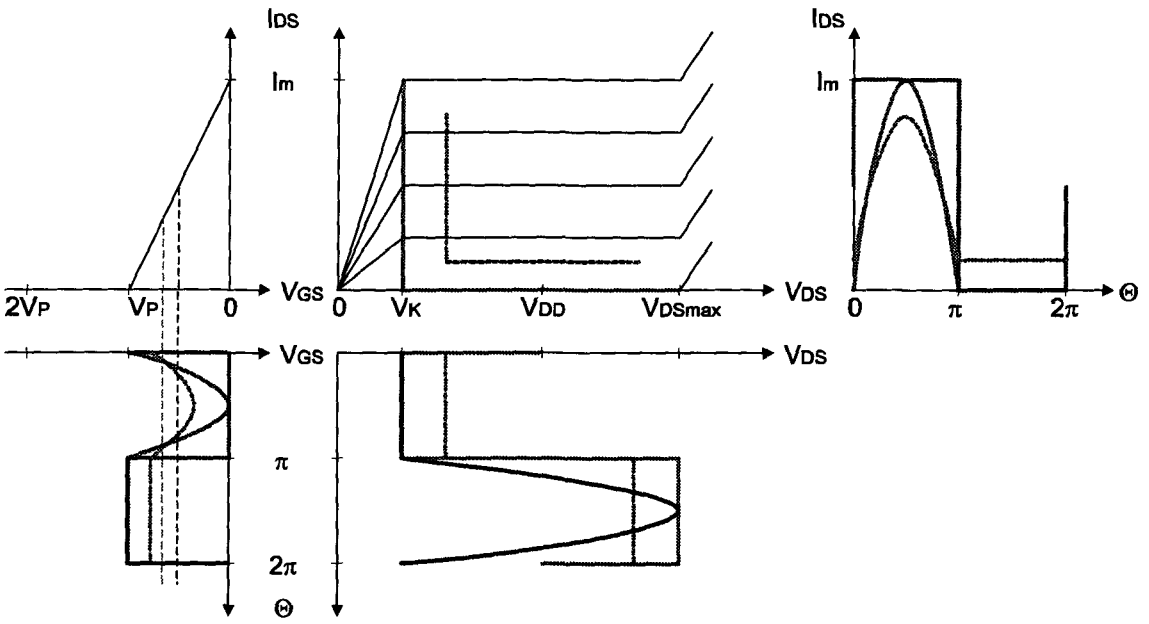


Figure 3.23: Optimum dynamic load line and voltage and current waveforms for half sinusoidally and rectangularly driven harmonic controlled amplifier, respectively. The red dotted lines indicate hHCA operation at reduced input power level. – Red: hHCA operation; Blue: rHCA operation.

For optimum efficiency over a wide range of input power the lowest input voltage should be close to pinch-off voltage. This is true for class F and class B operation. For hHCA and rHCA operation this is not true as it is shown in Fig. 3.23. The dotted lines depict operation at reduced input level which show clearly that efficiency will decrease. For high efficiencies at reduced input drive a gate bias voltage control has to be implemented.

However, for devices with low power gain this concept is very promising because gain is 6 dB higher than for class F operation thus power added efficiency is improved at the

same drain/collector efficiency for optimum input power level.

The performance of class F amplifiers operating in L-band which was reported in literature is listed in Tab. 3.6.

Reference (Year)	f [GHz]	PAE [%]	η_D $\{\eta_C\}$ [%]	P_{OUT} [dBm]	G [dB]	Device (Style)
INGRUBER 1998 [32]	1.65	74	77	27.9	22.4	MESFET
INGRUBER 1998 [33]	1.62	70	71	28.1	21.4	MESFET

Table 3.6: Results reported at class hHCA/rHCA operation in L-band.

Class G

For amplifier stages operating at low-voltage conditions, where the bias voltages are governed by the minimization of the number of battery cells the class F approach is not the best solution since the drain-source voltage is symmetric around the bias point, due to the absence of even harmonics, thus not exploiting the full output voltage and current swing. In this case a major improvement of power performances can be obtained utilizing a 2^{nd} harmonic manipulation of the output voltage, namely class G design strategy [34]. In class G operation termination control is limited to the 2^{nd} harmonic while higher harmonics are short circuited (e.g. by the drain-source capacitance of the active device itself). The optimum drain-source waveforms are shown in Fig. 3.24. One can note the reduced drain bias voltage V_{DD}.

In this approach it is assumed that the active device acts as a voltage controlled current source, while the output voltage depends on the harmonic loads; the latter are assumed to be purely resistive. To achieve the requested voltage waveform (proper flattening of the voltage waveform reaching the knee voltage) the 2^{nd} harmonic voltage component has to be out of phase with respect to the fundamental voltage. Therefore, an open circuit has to be presented to the output for 2^{nd} harmonic termination. Since this is detrimental to the half sinusoidal shaping of the drain-source current, the 2^{nd} harmonic for the current is generated by proper harmonic termination of the 2^{nd} harmonic at the input of the device. The 2^{nd} harmonic at the input is generated by the non-linear behavior of the gate source capacitance C_{gs}.

The performance of class G amplifiers operating in L-band which was reported in literature is listed in Tab. 3.7.

Class G operation is a well suited high efficient design approach when the amplifier has to be operated at low voltage or when the device's output capacitance is very high so that the harmonic content of the output signal is too low for harmonic manipulation (e.g. operation at higher frequencies).

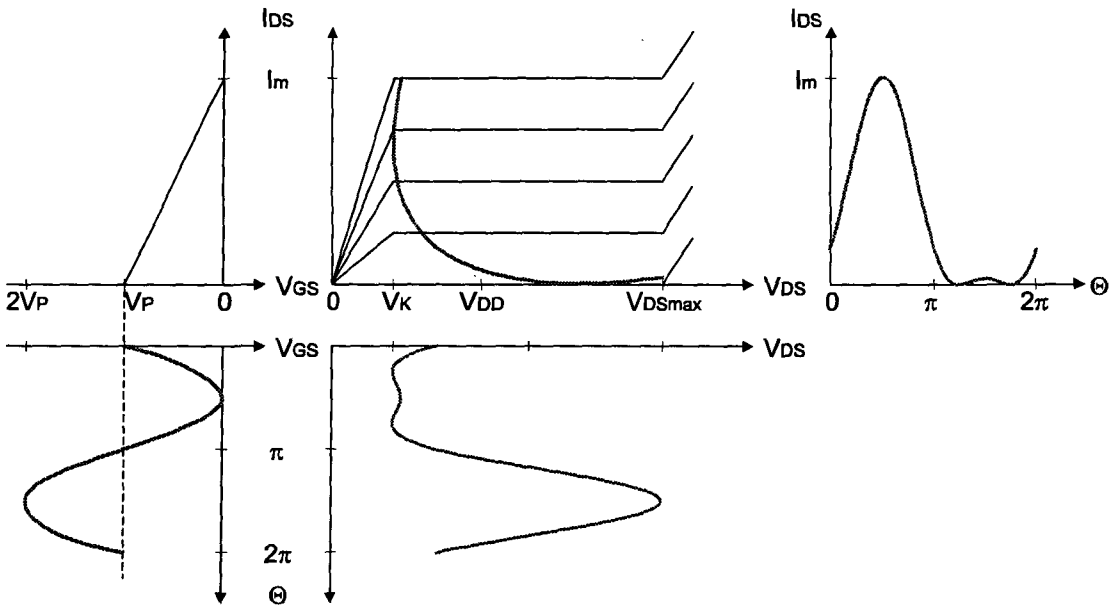


Figure 3.24: Optimum dynamic load line and voltage and current waveforms for class G operation.

Reference (Year)	f [GHz]	PAE [%]	η_D $\{\eta_C\}$ [%]	P_{OUT} [dBm]	G [dB]	Device (Style)
COLANTONIO 1998 [35]	2	64	66	25.1	15.6	FET

Table 3.7: Results reported at class G operation in L-band.

Harmonic Reaction Amplifier – HRA

The fundamental conceptional structure for the HRA is shown in Fig. 3.25. Although the fundamental structure is similar to the balanced amplifier (see also Chapter 3.6.2), a critical difference is that a 2nd harmonic resonance transmission path is added to the FETs in the HRA. Moreover, in the 2nd harmonic path there are two band rejection filters to block fundamental signal components, and a harmonic rejection filter acting as a high impedance termination for harmonic components is inserted into each FET output signal path.

Under class B or class AB biased, there are large 2nd harmonics generated at the output of each FET. This harmonic content flows only into the 2nd harmonic path. Since the 2nd harmonic path is assumed to be well matched with the FET's outputs at the concerned frequencies, each FET mutually injects a 2nd harmonic component into the other FET without reflection through the 2nd harmonic path (the FETs behave here as a kind of push-pull amplifier (see also Chapter 3.6.3) with respect to 2nd harmonics). Here, the 2nd harmonic path lengths have to be adjusted such that a voltage null appears at both FET-

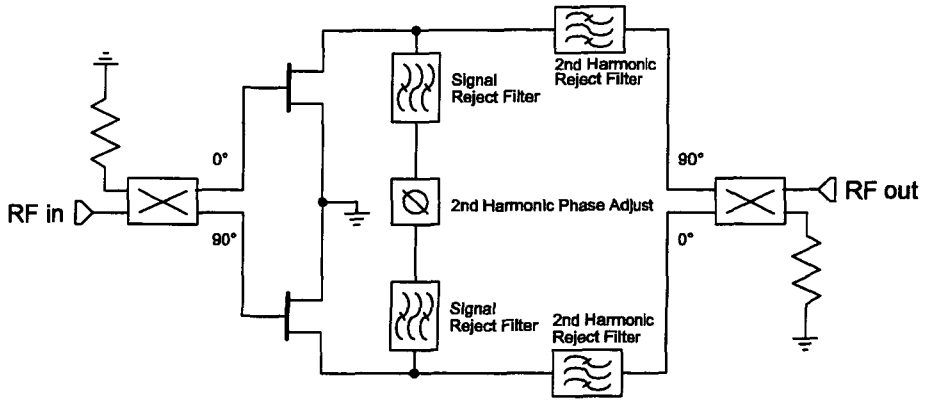


Figure 3.25: Fundamental conceptional structure of the harmonic reaction amplifier.

chip output points. This condition coincides with the 2nd harmonic output terminating condition in the class F amplifier. Therefore, the required switching mode of operation can be efficiently realized with the HRA. Since each FET's 2nd harmonic current works as a reaction force to increase efficiency, this device is called a Harmonic Reaction Amplifier.

The performance of harmonic reaction amplifiers operating in L-band which was reported in literature is listed in Tab. 3.8.

Reference (Year)	f [GHz]	PAE [%]	η_D $\{\eta_C\}$ [%]	P_{OUT} [dBm]	G [dB]	Device (Style)
NISHIKI 1987 [36]	1.7	75	83	34	9	2xFET
NOJIMA 1988 [37]	2.0	70	75	37	13.5	2xFET

Table 3.8: Results reported for harmonic reaction amplifiers in L-band.

3.4.3 Doherty Amplifier

The Doherty amplifier (see Fig. 3.26) is a traditional efficiency boosting concept [38] utilizing two amplifiers. When the main amplifier begins to saturate it is supported by the auxiliary amplifier.

For a better understanding the power gain is shown in Fig 3.27. When the main amplifier (A1) comes to saturation the auxiliary amplifier (A2) starts to deliver the difference to achieve the same power gain. Therefore, the main amplifier should be biased for example in class A whereas the auxiliary amplifier should operate in class B or class C mode. The benefit of this method is the increase in power added efficiency in the following way: At lower power levels just before A2 delivers a signal, A1 is close to saturation and has high efficiency. At maximum power level both A1 and A2 are close to saturation which results in high efficiency again. Hence, efficiency has two maxima. One at maximum power and

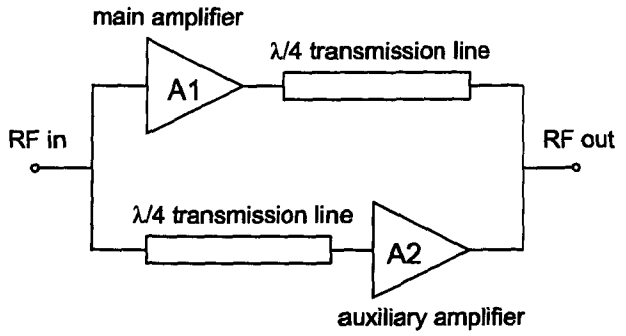


Figure 3.26: Basic structure of a Doherty amplifier.

one some decibels below which depends on where A2 starts with amplification. This means that power added efficiency can be kept nearly constant over a 3-6 dB range. This concept can be extended to more than one auxiliary amplifier extending the range of constant PAE.

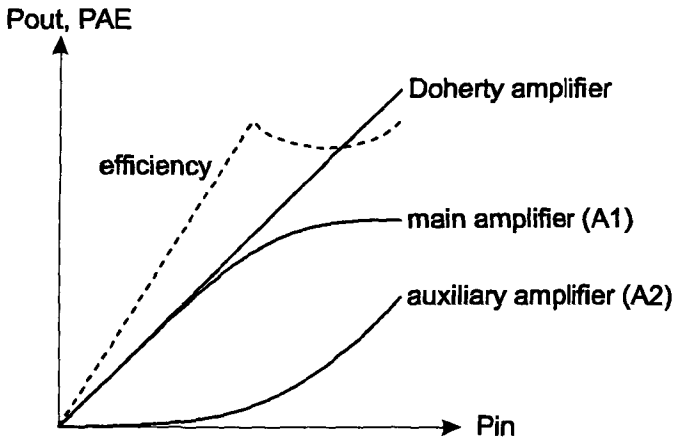


Figure 3.27: Doherty amplifier – transfer function and power added efficiency.

The main problem of this configuration is that the auxiliary amplifier must compensate for the main amplifier's saturation. As depicted in Fig. 3.27 the auxiliary amplifier must deliver exactly the difference between a perfect linear and the main amplifier (A1). This can only be done as a rough approximation. Hence, linearity becomes very bad which limits the use of Doherty amplifiers [5].

3.5 Linearity Aspects

The trade-offs between intermodulation distortion and power added efficiency of solid state microwave power amplifiers have been investigated by many researchers. The classical approach to operate an amplifier for multi-carrier signals is to drive it with a sufficient input power back-off. Of course, this reduces power added efficiency and cannot be considered as an optimum. Promising modes of operation to minimize distortion even in saturation are class F, class G, and hHCA (see Fig. 3.13). As the device output current does not contain odd-order harmonics, which are responsible for intermodulation distortion, the distortion characteristics of such a harmonic controlled amplifier is similar to that of class A/AB (see Fig. 3.14).

Many linearization techniques have been developed reducing intermodulation distortion significantly. Since the scope of this work was to enhance linearity by power amplifier circuit design improvement only, linearization by a system approach, such as feedforward technique, LINC, EER and predistortion (analog or digital), was therefore not considered. The disadvantage of systems like feedforward technique or LINC are that a lot of additional system components are needed which will reduce power added efficiency significantly. Such systems are more interesting for power amplifiers with higher output power levels (several 10 W). Also, for systems like adaptive digital predistortion, which is a very promising technique for linearization, access to the digital baseband signal must be available which is not the case for gap-filler transmitters.

3.5.1 Feedback Techniques

Besides of driving an amplifier at back-off condition the simplest and most obvious method of reducing amplifier distortion is by some form of feedback. Since its invention feedback has been applied almost universally to error correction of all forms.

At audio frequencies, device gain is usually inexpensive to accomplish, and stability is relatively easy to achieve due to the comparatively small bandwidths required. The inherent disadvantages of feedback, in terms of the much larger phase shifts and electrical lengths that amplifying devices display at gigahertz frequencies and the sacrifice of gain for linearity, are not a problem. When considering RF amplification, the problems of using feedback become more pronounced and the overall design must be considered much more carefully. Also, the linearity required in an RF system is often much greater than that required in an audio system.

In a simple feedback system (Fig. 3.28) where distortion is added as $d(t)$ the final output signal is

$$y(t) = \frac{K}{K+A}\left(Ax(t) + d(t)\right). \tag{3.31}$$

The distortion produced by the main amplifier and the gain A of the main amplifier is reduced by a factor $\frac{K}{K+A}$ by the inclusion of the feedback loop. Thus, only for amplifiers with high gain A and a small ratio $\frac{K}{A}$ a recognizable improvement in distortion will be achieved.

Equation 3.31 shows clearly that for RF devices where gain is limited the feedback concept will reduce gain and, therefore, power added efficiency significantly though almost

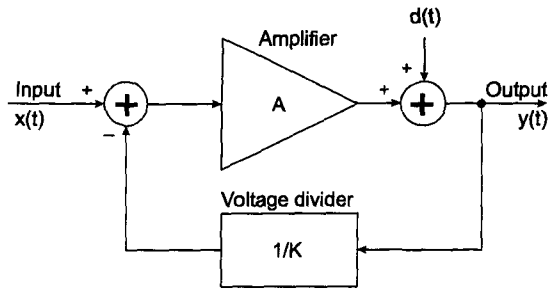


Figure 3.28: Feedback applied around an amplifier with distortion.

no distortion improvement is achieved. Furthermore, RF feedback methods suffer from a basic problem. Electrical delays around the feedback loop restrict the bandwidth of signals that can be linearized, and can still ultimately lead to instability.

Such limitations have restricted the usefulness of these well established techniques in modern multicarrier systems.

3.5.2 Injection/Termination Techniques

The sources of nonlinearities can be divided into the nonlinearity of the transconductance g_m and nonlinearties of the device input. If the device is not driven into gate-source junction forward conduction, the nonlinear behavior is mainly due to the gate-source capacitance (C_{gs}). Investigation of its influence on the drain-source voltage has been done by several researchers ([39], [40], [41]).

Investigations show that an improvement of intermodulation distortion can be achieved by injection of 2nd harmonic signal and/or baseband signal. Different methods of injection have been reported in the literature: direct 2nd harmonic injection into the gate [41], direct baseband and 2nd harmonic injection [39], 2nd harmonic feedback [42], and baseband feedforward [43]. Not only injection but also proper termination of the 2nd harmonic signal can improve linearity significantly [44].

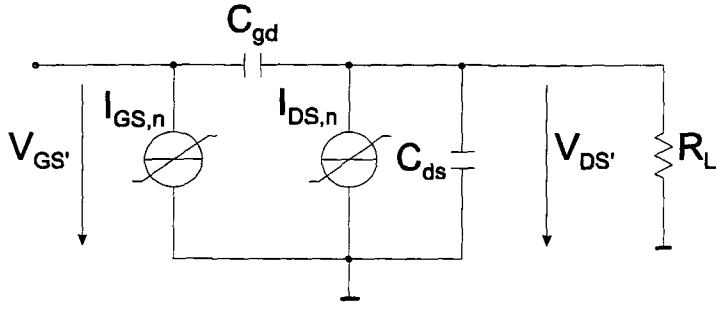


Figure 3.29: Equivalent circuit for nonlinear analysis.

For derivation a simple equivalent circuit (Fig. 3.29) can be assumed. The nonlinear current sources at the FET drain and gate are $i_{DS,n}$ and $i_{GS,n}$, respectively, where

$$i_{DS,n} = g_{m,1}v_{GS}(t) + g_{m,2}v_{GS}^2(t) + g_{m,3}v_{GS}^3(t) \quad (3.32)$$

$$i_{GS,n} = \frac{d}{dt}\left[C_{gs,1}v_{GS}(t) + C_{gs,2}v_{GS}^2(t) + C_{gs,3}v_{GS}^3(t)\right]. \quad (3.33)$$

Using Volterra series and the method of nonlinear current [45], the third order intermodulation distortion signal at the output load is

$$v_{DS}(\omega_1, \omega_1, -\omega_2) = i_{DS,3}(\omega_1, \omega_1, -\omega_2) \times H_{LD} + i_{GS,3}(\omega_1, \omega_1, -\omega_2) \times H_{LG} \quad (3.34)$$

where H_{LD} and H_{LG} are the transfer functions from the $i_{DS,n}$ and $i_{GS,n}$ to the load, respectively. $i_{DS,3}(\omega_1, \omega_1, -\omega_2)$ and $i_{GS,3}(\omega_1, \omega_1, -\omega_2)$ are presented in [39].

Assuming that

$$\begin{aligned} \omega_0 &\approx \omega_1 \approx \omega_2 \\ v_{GS,1}(\omega_1) &\approx v_{GS,1}(\omega_2) = v_{GS,1}(-\omega_2) = |v_{GS,1}(\omega_2)| \\ v_{GS,2}(\omega_1, -\omega_2) &= v_{GS,2}(\Delta\omega) = |v_{GS,2}(\Delta\omega)| \\ v_{GS,2}(\omega_1, \omega_1) &= v_{GS,2}(2\omega_1) = |v_{GS,2}(2\omega_1)|\, e^{j\Theta}. \end{aligned}$$

where $v_{GS,2}(\Delta\omega)$ and $v_{GS,2}(2\omega_1)$ are the magnitudes of injected signals. As a result one gets

$$v_{DS}(\omega_1, \omega_1, -\omega_2) = \alpha v_{GS,1}^3(\omega_1) + 2\beta v_{GS,2}(\Delta\omega) + \beta v_{GS,2}(2\omega_1) \quad (3.35)$$

where

$$\alpha = g_{m,3}H_{LD} + j\omega_0 C_{gs,3}H_{LG} \quad (3.36)$$

$$\beta = \frac{2}{3}g_{m,2}v_{GS,1}(\omega_1)H_{LD} + j\omega_0\frac{2}{3}C_{gs,2}v_{GS,1}(\omega_1)H_{LG}. \quad (3.37)$$

It is clear from the expression above that by adjusting the magnitudes of $v_{GS,2}(\Delta\omega)$ and $v_{GS,2}(2\omega_1)$ properly by injection or termination, the distorted signal $v_{DS}(\omega_1, \omega_1, -\omega_2)$ may be reduced to zero and hence an improvement in intermodulation distortion performance occurs.

3.6 Power Combining Techniques

Power combination is an important topic in power amplifier design. Since the optimal load impedances get very small for high power devices and, therefore, are hard to realize a practical way is to combine several power amplifier modules to get the desired output power. For a high efficiency power amplifier a careful design of the power combination circuit is essential to minimize the power loss and thus a decrease in efficiency. Equation (3.38) gives the decrease of drain efficiency when combiner loss is present. $P_{OUT,0}$ is the power

at the output of an ideal combiner and P_{OUT} is the power at the output of a combiner with combiner loss CL. As loss and gain in microwave engineering is commonly given in logarithmic units $G_E = 10^{-\frac{CL}{10}}$ gives the combining gain, or efficiency gain, in linear units. Figure 3.30 displays the efficiency gain versus combiner loss. As an example, at a combiner loss of 0.5 dB efficiency is reduced by 11 %. This relationship is also true for power added efficiency as long as the combiner loss at the input equals the combiner loss at the output of the amplifier.

$$\eta_D = \frac{P_{OUT}}{P_{DC}} = \frac{P_{OUT,0}}{P_{DC}} \cdot \frac{P_{OUT}}{P_{OUT,0}} = \eta_{D,0} \cdot G_E \tag{3.38}$$

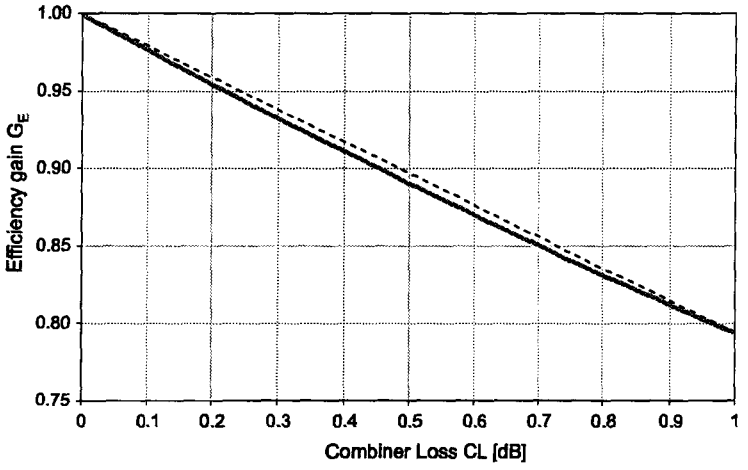


Figure 3.30: Reduction of efficiency gain G_E influenced by combiner loss CL.

Commonly used methods for power combination are the use of a Wilkinson power combiner, a balanced amplifier configuration, and a push-pull amplifier configuration. Since passive combining networks are reciprocal, the same network can be used either as a power combiner or a power divider.

3.6.1 Wilkinson Power Combiner

The Wilkinson splitter is the simplest and most widely used two-way in-phase power combiner/divider network and it is shown in Fig. 3.31. It is easily designed and fabricated and the narrow bandwidth can be increased by having two or even more quarterwave matching sections. Furthermore, due to the inherent symmetry of the structure, zero amplitude and phase difference exist between the two outputs. The function of the isolation resistor is to terminate any odd-mode signals, which also becomes apparent as a midband null in transmission between opposite combining ports. The midband isolation is able to suppress odd-mode instability between the combined amplifiers.

In practical applications ports 2 and 3 will be terminated in imperfect loads. In-phase power combiner/divider networks suffer from one major problem under these circumstances. The resulting input VSWR seen at port 1 will, in general, be worse than the

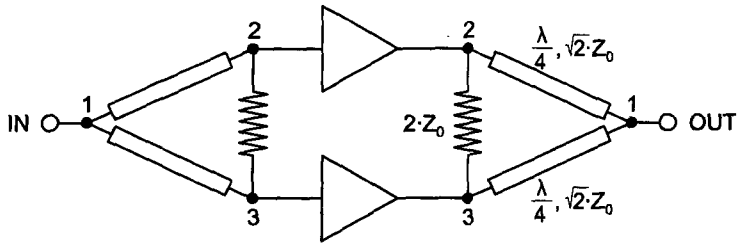


Figure 3.31: In-phase power combiner using single-section Wilkinson power combiners.

VSWR of the load. Thus the amplifiers to be combined must have an excellent input and output VSWR if the resulting power-combined amplifier is to have a good VSWR.

3.6.2 Balanced Configuration

In Fig. 3.32 a balanced amplifier configuration is shown. Two identical amplifiers are fed from an input power splitter, which produces two signals in phase quadrature, the outputs being recombined using a similar device connected in reverse. The principal advantage of this configuration is that any mismatch reflections from the amplifiers pass back through the couplers and appear antiphase and , therefore, cancel at the RF input (or output) port. Reflected energy is diverted to the terminated coupler ports. Provided the two amplifiers are identical in their characteristics and the couplers have ideally flat amplitude and phase responses, the match seen at the input and output will be essentially perfect, regardless of the reflective nature of the individual amplifier stages.

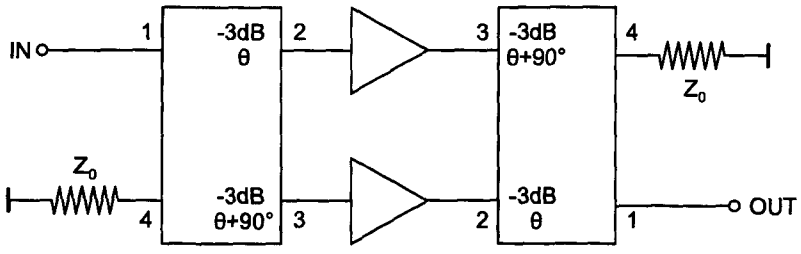


Figure 3.32: Configuration of balanced amplifier.

This feature has great significance to power amplifier interstage matching. If amplifier stages are all balanced, interstage matching becomes a redundant issue. Essentially, all balanced modules have a 50 Ω impedance and have performance designed and measured with 50 Ω terminations. A power module with known power characteristics can be confidently expected to produce the same performance when used as a driver for a higher power output stage if both modules are realized in balanced form.This is far from being the case when a driver transistor output is matched directly into the power amplifier device in a single-ended configuration.

For the realization of a balanced configuration a quadrature 3 dB coupler is needed. This can be a pair of broadside coupled quarterwave transmission lines which can be only

realized in stripline technology. Such tight coupling can also be realized in microstrip technology by the interdigitated Lange coupler (Fig. 3.33a), where the two coupled lines are broken into a number of strips to multiply the number of edges available for coupling purposes. Such a structure has very narrow linewidths and is not suited for power combining at the amplifier output. For this purpose a branchline coupler (Fig. 3.33b) is very suitable. Branchline couplers are easy to manufacture but they have the disadvantage to be narrowband and to consume considerable space on the MIC.

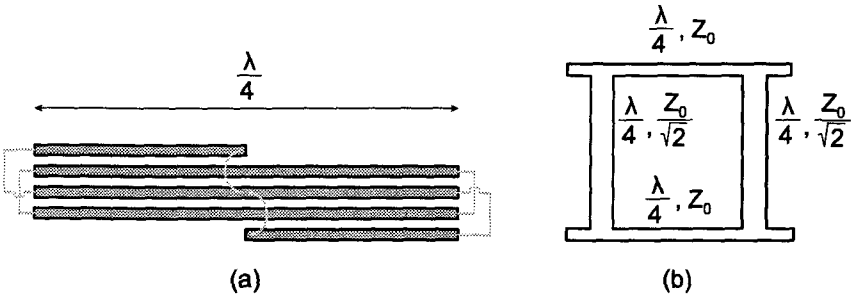


Figure 3.33: Quadrature 3 dB couplers. – (a) Lange coupler; (b) branchline coupler.

In the presence of nonideal coupling an automatic compensation mechanism occurs if both amplifiers are completely linear. When the amplifiers are driven into gain compression, the unequal coupling response will cause one amplifier to compress more than the other, but it can be shown [10] that the output voltage has a rather insensitive dependency on the coupling factors. Figure 3.34a shows the power transfer characteristic plotted for a few representative values of coupling factor and a typical compression characteristic. It can be seen that the power transfer characteristic is remarkably unchanged from the ideal 3 dB coupling characteristic for coupling factors down to 1.5 dB. A coupling factor of 2 dB appears to soften the characteristic by only 0.2 dB.

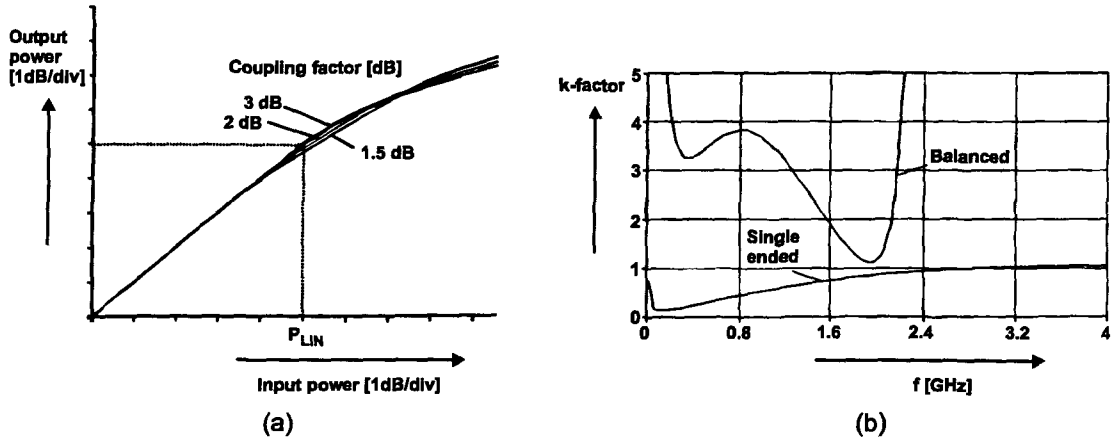


Figure 3.34: Balanced power amplifier. – (a) compression characteristics [10]; (b) single-ended vs. balanced k-factor comparison [10] (typical class A amplifier).

Balanced configuration provides a greater stability compared to single-ended designs [10]. Figure 3.34b shows that the k-factor for a single-ended class A amplifier is falling well below unity at lower frequencies. This would be a serious stability issue. But a balanced configuration of such an class A amplifier has an impressive stability over a very wide bandwidth.

All these advantages make the quadrature coupler to be an excellent power combiner.

3.6.3 Push-Pull Configuration

An RF push-pull amplifier consists of a pair of class AB, B, D, or F stages where the stages are driven differentially. Figure 3.35 shows the schematic of a push-pull amplifier. This amplifier retains the even harmonic short circuit on each device to constrain the individual drain-source voltages to a sine or rectangularly shaped wave required by class B or class F operation. This kind of amplifier has the same efficiency as each individual single-ended component but has two important advantages over single-ended operation: reduced common lead effects and impedance doubling.

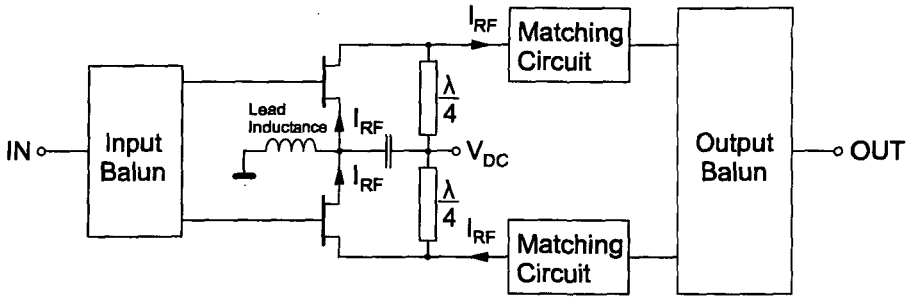


Figure 3.35: RF push-pull amplifier.

One of the key benefits of push-pull operation of this kind is that the fundamental frequency components of the two device currents will be equal and opposite. If there is a common lead connecting the sources to ground, cancellation will occur and no feedback voltage will be developed across the lead inductance. This, of course assumes that the two devices and the differential excitation are exactly in balance. Such common lead effects cause substantial gain reduction at each doubling of transistor periphery in single-ended designs.

The second benefit is probably its impedance doubling. If differential RF excitation is available, then the composite impedance presented by the push-pull pair at both the input and the output is a factor of 2 higher than that which would be presented by one single-ended device. That is in strong contrast to the impedance of a parallel pair, where the impedances would be halved in comparison to a single device. So there appears to be a 4:1 impedance benefit for a push-pull combining sheme in an equal-power comparison to simple parallel connection. When the device impedances are down in the 1 Ω range, this is a highly significant benefit. At high output power levels and low maximum bias voltages, as it is true for silicon devices, the load impedances are quite low and here push-pull MMICs have been successfully realized [46], [47].

3.7 Active Device Aspects

A growing number of semiconductor technologies are being applied to RF power transistor applications. Table 3.9 lists key parameters for competing RF power device technologies.

Technology	Power Density	Supply Voltage	Linearity	Frequency	PAE
Si BJT	Medium	26 V	Poor	< 2 GHz	Low
SiGe BJT	Medium	< 20 V	Good	> 2 GHz	High
Si LDMOS FET	Low	26 V	Very Good	< 3 GHz	Medium
GaAs MESFET	Medium	12 V	Good	> 2 GHz	Medium
GaAs pHEMT	Medium	8 V to 12 V	Very Good	> 20 GHz	High
GaAs HBT	High	8 V to 26 V	Good	> 20 GHz	High
SiC MESFET	Very High	48 V	Good	> 4 GHz	Medium
GaN HEMT	Very High	48 V	Promising	> 12 GHz	High

Table 3.9: Overview of competing solid-state RF power transistor technologies [48].

Silicon based technologies offer low cost devices for low frequency application. In the last time SiGe devices gain attractivity for efficient power amplifiers [49], [50].

GaAs based devices offer high frequency operation with good linearity at high efficiency. The best GaAs technology in terms of efficiency and linearity is GaAs pHEMT. Wide bandgap technologies (SiC and GaN) offer very high power densities and look very promising for future applications. At the time being these devices are still under development and have to reach maturity.

Parasitic Inductances

In an amplifier active devices have to be connected by transmission lines or bond wires which have inductive behavior and, therefore, will influence the amplifier's behavior. Figure 3.36 illustrates a schematic of an amplifier showing these inductances at each transistor port.

Drain inductance L_D and gate inductance L_G will cause a phase shift, becoming significant for high frequencies and at the harmonics. This phase shift can be corrected by an adapted input and output matching network. The source inductance L_S causes a current feedback and reduces amplifier gain substantially. This effect cannot be compensated by circuit design methods. The only way to reduce the influence of source inductance is to keep the source inductance as small as possible.

Figure 3.37 shows the dependency of a class A amplifier on the source inductance at $f_0 = 1.472\ GHz$. The amplifier gain is reduced by 10 dB with a source inductance value of 80 pH only. This inductance is equal to a bond wire length of about 150 μm which is in fact a short bond wire. The inductance can be further decreased by using multiple bond wires. However, if the amplifier is designed in microstrip technology there is a further source inductance arising from via interconnects to ground on the substrate which depend on the substrate height (typically several 100 μm). An improved method is to realize

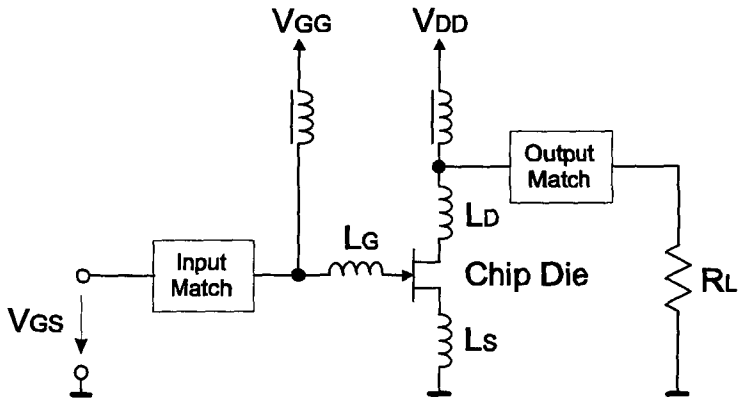


Figure 3.36: Amplifier schematic illustrating parasitic extrinsic inductances L_G, L_D, and L_S.

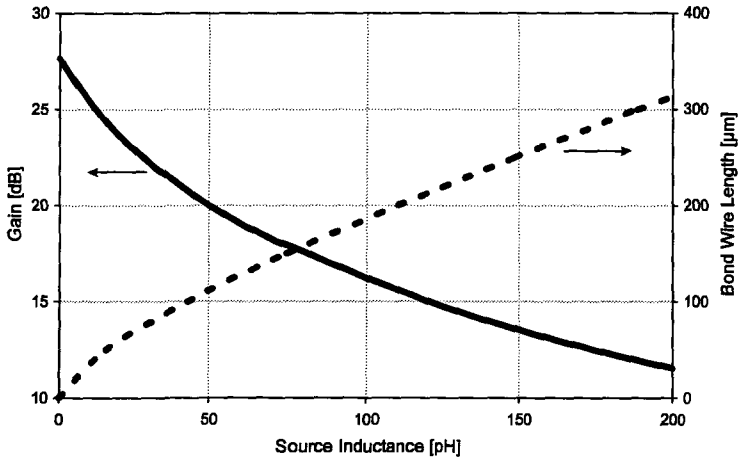


Figure 3.37: Influence of source inductance on amplifier gain and associated bond wire length. The shown data are simulation results of the class A test amplifier described in 4.4.6. $f_0 = 1.472\ GHz$.

via interconnections directly on chip and applying a metallization on the backside. This technique reduces the source inductance significantly, especially when the die is thinned for better thermal capability. For high-level GaAs power devices this technique is widely in use. In [51] it is shown that source inductance can be further reduced by providing separate paths on-chip for the drain and gate return currents by multiple via holes.

Power Handling Capability

The low thermal conductivity of GaAs (44 W/m·K compared to 150 W/m·K of Si at 300 K, see also Fig. 4.4) requires careful thermal design to improve lifetime and reliability of the device by minimizing the influence of thermomechanically induced stress and thermal load.

The maximum dissipated power in a device depends on the achievable power density and the maximum device operating temperature. For reliable operation, the peak operating temperature should be kept below 120 °C [52]. Power density depends on several device parameters. These are [53]:

- **Wafer thinning:** Wafer thinning will reduce thermal resistance of the transistor although not in a linear extent than one might think of. Results in [53] show that thinning a GaAs die from 630 μm to 100 μm reduces the chip peak temperature by 10 °C only.Although just a small reduction in device temperature is achieved by thinning the chip, in GaAs devices this can lead to a considerable increase in life time.

- **Gate pitch:** For a fixed peak temperature, devices with a gate pitch of 30 μm and 50 μm reach a considerably higher power density than devices with a 16 μm pitch. This translates to a higher possible drain bias voltage and, therefore, to a higher output power, given a sufficiently high breakdown voltage. The influence of increasing gate pitch can also be observed by the resulting maximum device drain current. Due to the mutual gate heating the device with a large number of fingers has the lowest drain current. By increasing the gate pitch the mutual thermal influence of the gate becomes less, disappearing finally (gate pitch > 50 μm in [53]).

- **Heat spreader:** A heat spreader which is directly applied on the backside of the device (several micrometers thick electroplated metal) can reduce the peak temperature by some degrees while the average temperature is increased.

- **Thermal conductivity of die bonding material:** The thermal performance of a given GaAs device is mainly influenced by the thermal resistance of the bonding layer between chip and chip carrier (heatsink). Temperature reduction of multiples of 10 °C can occur. Thus the influence of bonding parameters on the thermal behavior of a GaAs chip device was further investigated in Chapter 4.1.2.

State-of-the-art GaAs FET power devices achieve typically a power density of 1 W/mm (dissipated power per millimeter gate width).

3.8 Conclusion

In this chapter the fundamental theory of power amplifier design, the classical amplifier operation modes (A, B, C) and several operation modes for improved efficiency (E, F, hHCA, rHCA, G, HRA, Doherty) were discussed. Additionally, concepts for improving linearity, power combining techniques (Wilkinson, balanced configuration, push-pull) and relevant aspects of the active device (parasitic inductances, layout issues) were presented. Furthermore, achievements on high efficiency amplifier design reported in the collected literature were reviewed.

It was shown that with the classical operation modes the highest gain is delivered by a class A amplifier, but its drain efficiency is limited to 50 %. The theoretical maximum of efficiency of a class B is 78.5 %, but its gain is 6 dB lower than for class A. This lowers the power added efficiency significantly for low gain active devices. Additionally, high negative input voltage peaks of twice the value of class A occur which may limit the device reliability. With class C amplifiers a theoretical drain efficiency of 100 % can be achieved, but at the same time the output power is zero.

With harmonic controlled amplifiers (HCA) the optimum efficiency of 100 % drain efficiency can be achieved at non-zero output power and gain. Drain-source voltage and drain-source current waveforms are controlled in such a way that losses inside the device are minimized. Special harmonic loads are needed to control the harmonics generated by the transistor. To generate these harmonics the devices are mainly driven at class B or at class AB close to class B in all these harmonic controlled amplifier modes. Therefore, the same drawbacks as in class B arise here, too.

Within a class E and class G amplifier high drain-source voltage peaks occur and this normally precludes the use of such amplifiers in the microwave frequency range due to the limited brakdown behavior of microwave transistors. However, for amplifier stages operating at low-voltage conditions, where the bias voltages are dictated by the minimization of the number of battery cells these amplifier concepts are advantageous.

In a class F or hHCA amplifier all even harmonics are short circuited and all odd harmonics are open circuited to achieve rectangular drain-source voltage and half sinusoidal drain-source current. In practice only the 2^{nd} and 3^{rd} harmonics are controlled, as at microwave frequencies transistors do not have enough gain at higher harmonics and to simplify device output matching. This limitation of harmonics reduce the maximum achievable drain efficiency to 81.65 %. hHCA concept has over class F the advantage that reliability and gain is improved due to the reduction of negative input voltage peaks. The improvement in gain is very interesting for operation at higher microwave frequencies where the gain of transistors is usually low. The 2^{nd} harmonic content in the half sinusoidal input voltage, however, requires bias control for reduced input power level.

A HRA consists of two identical amplifiers operating in a balanced configuration, connected via a 2^{nd} harmonic terminating path between the drains of both transistors. The electrical length is adjusted in such a way that the 2^{nd} harmonic component of the drain-source voltage of each device is cancelled. In terms of 2^{nd} harmonic component the balanced configuration is acting as a push-pull amplifier where one drain is acting as the termination for the other alternately. This maximizes the amplifier efficiency.

In Doherty configuration two amplifers are operating at different input power levels. When the main amplifier comes to saturation an auxiliary amplifier starts to deliver the

difference to compensate for the saturated main amplifier to establish perfectly linear gain. This compensation can only be done as a rough approximation. Hence, linearity of Doherty amplifiers is limited.

In Chapter 3.5 linearity issues were discussed. It was found that the absence of odd-order harmonics in the drain-source current promotes the device distortion characteristic without degrading its efficiency. Class F, class G and hHCA amplifiers seem to be optimum in the light of high efficiency at low intermodulation distortion. The well established feedback method was shown to have severe limitations for the use in microwave amplifiers. It was presented that injecting or terminating the 2^{nd} harmonic low frequency (baseband) and/or high frequency ($2f_0$) signal can improve linearity significantly since this technique compensates for the 2^{nd} order nonlinearity of the gate-source capacitance and is further able to reduce the nonlinearity of the transconductance.

Power combining techniques are needed to combine two or more amplifier modules to increase output power. Combining is necessary when the required output power cannot be delivered by a single device or when the source/load resistance is too low for proper impedance matching. For a high efficiency power amplifier a careful design of the power combination circuit is essential to minimize the power loss and thus to avoid a substantial decrease in efficiency.

A Wilkinson combiner combines two in-phase signals with the same magnitude. The most severe drawback of this combination technique is that the input VSWR of the single stages have to be close to 1 because the overall input VSWR is higher than the single stage VSWR. This problem is solved by a balanced configuration which combines two signals with the same magnitude but with a 90° phase relation. The single amplifier modules are, therefore, decoupled and VSWR is always good as long as the single module VSWR behavior is equal. Furthermore, balanced designs are more stable than the corresponding single ended stages. In the presence of nonideal coupling an automatic compensation mechanism occurs if both amplifiers are completely linear.

Push-pull technique is a further combination technique where two out of phase signals with the same magnitude are combined. The main advantages of this technique are that the influence of source inductances can be minimized and that the load impedance for each single stage is doubled compared to the other combination techniques. This is a major advantage for very low load impedances (e.g. $< 1\ \Omega$).

Out of a huge number of available semiconductor technologies and devices GaAs pHEMTs seem to be the best choice for efficient and linear power amplifiers for medium output power levels. GaAs pHEMTs are characterized by high efficiency, high linearity, and high transit frequency. For higher output power levels GaAs HBTs are the prefered choice since the power density in a HBT device is higher than it is in a pHEMT. Power density can be improved by proper transistor layout and wafer thinning. Furthermore, the device performance for power amplification can be significantly improved by low source inductance values by via interconnections directly on-chip and backside metallization. The source inductance is further improved by wafer thinning. Using transistors as chip dies without case reduces inductance values to a minimum and reduces further the size of the transistor and consequently of the amplifier module.

3.8.1 DAB Amplifier Realization Concept

Out of the presented efficient amplifier concepts class F operation mode seems to be the best concept for high efficiency while still promising good linearity. As the device output current does not contain odd-order harmonics, which are responsible for intermodulation distortion, the distortion characteristics of such a harmonic controlled amplifier is similar to that of class A/AB (see Fig. 3.13 and 3.14). Therefore, the class F concept was chosen as the basic concept for the DAB power amplifier module. Further investigations on class F linearity based on non-linear simulations are presented in Chapter 5.2.

For further linearisation proper 2^{nd} harmonic input termination promises to be an excellent and simple means to improve linearity and efficiency simultaneously. The impact on efficiency and linearity was further investigated in Chapter 5.2 by non-linear simulations.

The active device was chosen to be a GaAs pHEMT chip device with backplane processing on a thinned wafer with source via interconnections due to its generally excellent performance in terms of efficiency, linearity, and source inductance. Since drain bias voltages of GaAs devices are generally below 10 V the optimum load impedance will be quite low. Therefore, a balanced configuration was chosen to combine two amplifier modules where the load impedance for each stage is twice the value for the complete amplifier which simplifies the design of the matching circuit or makes it even feasible. Furthermore, the amplifier design can benefit of all further advantages of balanced configuration, like improved stability, minimized VSWR and Q-hybrid compensation mechanism.

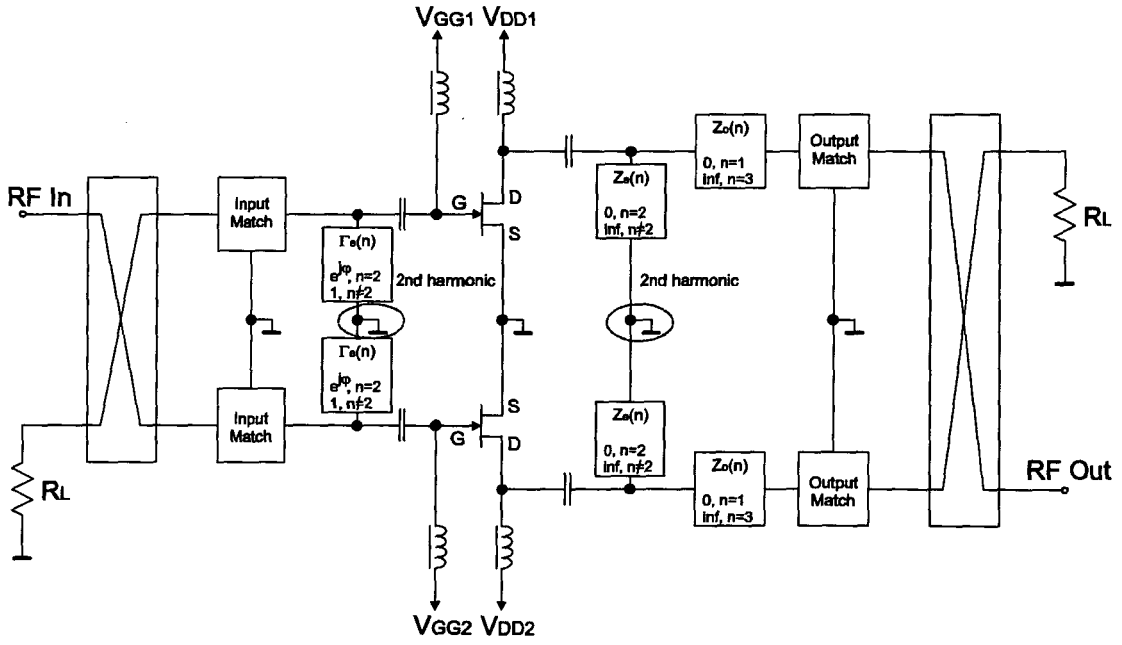


Figure 3.38: Balanced concept for complete DAB amplifier.

The concept for the complete DAB amplifier is presented in Fig. 3.38. This configuration offers also the possibility to investigate the impact of harmonic reaction amplification (HRA) on the linearity of the amplifier at both, 2^{nd} harmonic at the output and, newly,

at the input of the device. HRA operation can be easy achieved by disconnecting the ground connection (encircled by the dotted line) of the 2^{nd} harmonic paths at the in- and output. As long as the amplifier modules are absolutely equal no change in performance will occur. For not absolutely equal amplifier modules it is assumed that a compensation mechanism will result in improved efficiency and linearity. Measurement results are presented in Chapter 5.6.

For the realization of the presented concept in thin film technology the following investigations had to be done:

- **Thin film process evaluation:** As long as no experience with thin film technology was available at the institute the thin film process of the foundry had to be evaluated to ensure the validity of the used component models.
- **Packaging:** Investigations on the bonding technique of the active devices had to be performed to ensure high reliability.
- **Passive device characterization and modeling:** For accurate amplifier prediction by simulation influences from substrate, mounting technique and component parasitics have to be taken into account and thus all passive components had to be characterized and modeled. For thin film spiral inductors a new scalable model had to be developed to accurately predict the bahavior of the spiral inductor and its parasitics.
- **Active device characterization and modeling:** To get accurate amplifier simulation results for large signal excitation a suitable large signal device model had to be selected, the device had to be characterized and the model had to be finally fitted to the measurement results.
- **Linearity investigations on class F termination:** To consolidate the above mentioned statement that class F output termination improves not only efficiency but also linearity further investigations had to be done on the influence of harmonic termination on linearity.
- **Investigation on 2^{nd} harmonic input termination:** The influence of proper 2^{nd} harmonic termination on efficiency and linearity had to be further investigated to optimize the amplifiers output performance.
- **Investigation on harmonic reaction operation mode:** Harmonic reaction mode at the ouput and, newly, at the input had to be investigated because it is assumed that linearity can be improved by harmonic reaction operation.

Chapter 4

Characterization and Modeling

This chapter gives a brief description on the selection, characterization, and modeling of the used passive and active devices. The components were carefully selected to fullfil the criteria for high performance circuit design. For accurate amplifier prediction by simulation influences from substrate and mounting technique have to be taken into account and thus all components were characterized and modeled. Further, to integrate and minimize the amplifier module thin film components were developed, characterized and modeled. As no experience with thin film technology [54] in general and with the selected foundry in particular was available at the institute the thin film process of the foundry had to be evaluated to ensure the validity of the used component models. Further details on the process evaluation and the characterization and modeling of thin film components can be found in [55]. All the computer models were developed for the simulation software Microwave Office^{TM} from Applied Wave Research.

4.1 Technology

4.1.1 Evaluation of Thin Film Process

Thin Film Technology

Thin film circuits are composed of films formed by molecular deposition techniques such as evaporation, sputtering, electroplating, or chemical vapor deposition. The patterns are formed by photolithography and etching. The selection of specific materials to realize a particular thin film component is determined by the desired electrical and mechanical properties as well as the available deposition techniques and the compatibility with other materials on the same substrate. Since the thin film technology is grown by a process involving individual atoms or molecules, the deposition conditions are critical because they determine the properties of the resulting film. In this thesis the used substrate material is alumina, the conductor material is gold and the material used to realize printed resistors is CrNi. The deposition techniques are sputtering and electroplating.

Deposition Techniques

Sputtering is the most widely used deposition technique in thin film processing. It is a plasma process in which argon ions are created and accelerated toward a target of the material to be deposited (Fig. 4.1). Upon impact, target atoms are ejected or sputtered from the target surface. These sputtered atoms then coat the substrate.

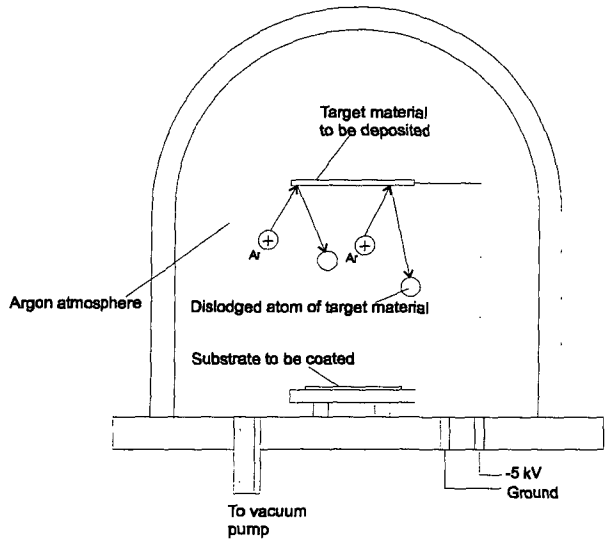


Figure 4.1: DC sputtering chamber.

Electroplating is often used to increase conductor thickness. Electroplating is the electrodeposition of an adherent metallic coating upon an electrode by electrolysis. The part to be plated must be electrically conductive, which is often accomplished by depositing a seed layer by sputtering.

The resulting gold layers are: 0.1-0.5 μm with vacuum deposition and 1-5 μm with electroplating.

Substrates

Commonly used substrate materials for thin film deposition include alumina, glass, beryllia, aluminium nitride, and silicon. Ceramic materials are often used for thin film applications since ceramics possess high thermal conductivity and good chemical stability and are also resistant to thermal and mechanical shocks. The properties of the substrates used to grow defect-free films for thin film circuits include good surface smoothness, proper thermal expansion coefficient, good mechanical strength, high thermal conductivity, chemical stability, inertness to chemicals, high electrical resistance, and reasonable uniformity of material composition. Substrate flatness directly influences the minimum achievable linewidth and spacing. In general, films are tolerant of surface roughness less than an order of magnitude of the film thickness. High mechanical strength and thermal shock resistance are required in order to enable the substrate to withstand the rigors of processing and normal usage. Ceramic materials are superior to fulfill this function effectively.

High thermal conductivity is required in order to remove heat, allowing circuits with high component densities. Ceramic materials posess better chemical stability than glasses, especially at higher temperatures. These materials are not attacked by etchants used in processing thin film circuits.

In the present thesis the used substrate is polished alumina from Coors Ceramics Company. The properties of this substrate are summed up in Tab. 4.1.

Alumina Content	Density	Surface Finish	Dielectric Strength	Dielectric Constant data sheet / measured	$\tan\delta$ data sheet
99.6 %	3.87 g/cm^3	< 1 μinch	23 kV/mm	9.9 / 9.7	0.0001

Table 4.1: Material properties of Superstrate 996.

Conductor Materials

Conductor films are typically formed of several metals in order to achieve the desired properties of a thin film metallization. These properties include high conductivity, good adhesion to both the substrate and the other deposited films, resistance to etchants, capability of being etched to line widths on the order of a few micrometers using conventional photolithographic technology, ease of bonding, and compatibility with other materials and processes. Metals with good conductivity usually exhibit poor adhesion to substrate material. One can enhance the adhesion property of these high conductivity metals by providing intermediate layer(s) of titanium, chromium, nichrome, or titanium-tungsten. Typical conductor materials are copper, gold and aluminum.

The transistor used in this thesis (for further details see 4.4) has a gold metallization and it will be connected to the transmission lines at the substrate by wire bonding. Therefore, gold was chosen as the thin film conductor material and as the bond wire material to have a single metal system. With a single metal systems no problems due to e.g. diffusion can occur.

Gold can be either evaporated or sputtered and is used as a top layer to protect lower evaporated (or sputtered) layers. It can also be used to achieve the required metallization and/or to form capacitor electrodes. An adhesive underlayer of titanium, chromium, or titanium-tungsten is often used since gold does not adhere well to most substrate materials. Gold is more difficult to solder to, since it usually alloys with soft solders, causing mechanically poor connections. This can be prevented to a certain extent by providing a thick conductor layer by electroplating. Still soldering has to be done carefully.

Resistor Materials

The selection of thin film resistor materials depends on basic considerations such as temperature coefficient of resistance (TCR), voltage coefficient of resistance (VCR), electrical noise figure, resistance stability, achievable sheet resistivity R_s, allowable power density, compatibility with other materials, and film deposition method used. The bulk resistance of a thin film resistor is a basic material property. The sheet resistance (R_s, in $\Omega/\square$) refers to the volume or bulk resistivity normalized with respect to the thickness of the

film. Typical thin film sheet resistances range from 10 to 2000 Ω/□ with an initial tolerance on the order of ±10 %. Laser trimming can be performed to bring these resistance values to tighter tolerances (0.01 %) if desired. The temperature coefficient of resistance (TCR) provides useful information in characterizing the properties of the deposited thin films. TCR (in ppm/K) is defined as $\frac{1}{R}\frac{dR}{dT} \cdot 10^6$, where dR and dT refer to a change in the resistance value R due to a change in the ambient temperature T. This parameter is especially important in some applications which require circuit operation in unstable ambient temperature, thus affecting considerably the circuit performance. In general, thin films have very low TCR values compared to bulk materials. Typical TCR values are well within ±100 ppm/K. Very low values of TCR, approaching zero, can also be achieved in some cases.

Resistor stability is closely related to substrate inertness, substrate surface smoothness, and substrate thermal conductivity. Therefore, thin film resistor design and performance are greatly affected by the choice of substrate material. Thin film resistors are known to exhibit good stability over time under different environmental conditions.

NiCr resistors offer the lowest temperature coefficient of resistance. In general, the ratio of nickel to chromium can vary from 40:60 to 80:20. The sheet resistance achieved with these ratios is in a range from 20-150 Ω/□.The TCR obtained depends on the nickel-chromium ratio as well as specific deposition conditions. Nickel-chromium films are commonly obtained by sputtering but can also be deposited by vacuum evaporation.

Foundry Process

In the present thesis the thin film process was provided by the "Radeberger Hybridelektronik GmbH" (RHE) at Radeberg, Germany. The complete guidelines for this process is provided by RHE [56]. A summary of the technical parameters of the chosen process is listed in Tab. 4.2.

Test Structures

In order to check both, the reliability of the RHE process and the accuracy of the simulation software, a substrate with several test structures was designed. This substrate contains basic elements like resistors, capacitors, spiral inductors, couplers, and via holes. Mainly structures with minimum line width (25 μm) and minimum line spacing (25 μm) were designed in order to check the capability of the manufacturer to realize these structures. Some components were realized multiple to check reproducibility.

The resistors were designed with different ratios of resistor width to length. In order to keep capacitance to ground small each value of resistance was also realized with minimum area. The spiral inductors were realized with different shapes (circular and square), different numbers of turns, furthermore, line width and spacing between the turns were varied. In the case of the interdigital capacitors the number of fingers, the spacing between the fingers, the length and the width of the fingers were varied.

Figure 4.2 shows some layout samples of the realized test structures.

Substrate:	Superstrate 996 (polished)
Thickness:	381 μm
Layers:	
Resistor Layer:	CrNi
Barrier Layer:	TiW
Conductor Layer:	Au (sputtered gold 0.1 μm, galvanically reinforced to 5 μm)
Minimum spacing between two conductors:	25 μm
Minimum line width:	25 μm
Width tolerance:	± 2 μm
Thin film resistors:	
Sheet resistance:	80 $\Omega/\square$
Minimum resistor structure size (L>W):	L_{Min}=100 μm, W_{Min}=50 μm
Minimum resistor structure size (L<W):	L_{Min}=80 μm, W_{Min}=150 μm
Conductor–resistor overlap:	> 100 μm
Via holes:	
Minimum diameter:	0.5 times substrate thickness
Minimum distance between two vias:	> substrate thickness
Metallization around via hole:	200 μm

Table 4.2: Technical process parameters of the thin film process.

Evaluation Results

The measurement results of the manufactured test structures were compared to the simulation results of available component models and EM simulation results, respectively. Details on the used calibration procedure can be found in 4.2. Some typical measurement results and suitable models for passive thin film components are presented in 4.3.2.

The evaluation process led to the following results:

- The manufacturer has no problems in realizing the small structures within the given tolerances. The reproducibility is very good.
- The manufacturer has problems in realizing the sheet resistance of the CrNi resistor layer within the given tolerance. The expected sheet resistance of 80 $\Omega/\square$ turned out to be 60 $\Omega/\square$, which is a deviation of 25 %. For more exact resistor values laser trimming has to be performed.
- EM simulation results are in very good agreement with the measurement results.
- Some available computer models can be used for circuit design. For more detail see 4.3.2.

4.1.2 Packaging

Packaging is a critical issue for the optimal operation of a microwave power amplifier. Various parameters are dependent on the packaging method. The most important are:

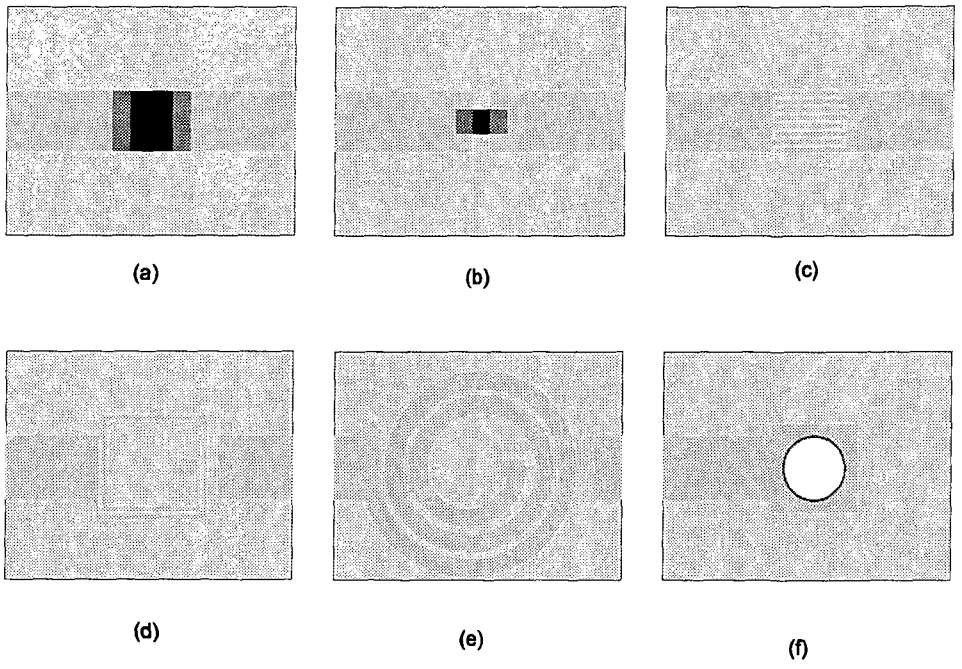


Figure 4.2: Test structures – (a) 50 Ω resistor; (b) 50 Ω resistor with minimum area; (c) interdigital capacitor with minimum line width and minimum spacing; (d) square spiral inductor with minimum line width and minimum spacing; (e) circular spiral inductor with 100 μm line width and 25 μm spacing; (f) via hole.

- *Low RF parasitics.* Parasitic capacitances should be kept small to reduce feedback and to reduce capacitive load at the transistor's input and output. Short bond wires are beneficial to reduce inductive and resistive losses. The source inductance should be small to reduce current feedback.
- *Low DC resistance.* To ensure high efficiency the DC resistance should be low.
- *Heat removal capability.* The heat generated by the dissipated power in the active device has to be removed sufficiently to prevent the device from overheating.

Figure 4.3 presents the packaging technique used in this thesis. The alumina substrates are bonded on a substrate carrier (see also next two sub-sections) by an isotropically electrically conductive adhesive (ICA). The open chip die is bonded directly on the substrate carrier by ICA to ensure a good thermal and electrical contact. The used active devices were designed by the manufacturer in microstrip technology with via connections to the backplane for the source contact. This reduces the source inductance and resistance significantly. Furthermore, it increases thermal conductivity of the die since thermal conductivity of GaAs is not very high [57]. To ensure top performance the thermal and electrical conductivity of the ICA have be very high. As it is shown in Fig. 4.3 the chip surface is mounted level with the alumina substrate to minimize bond wire lengths, which reduces inductive and resistive losses.

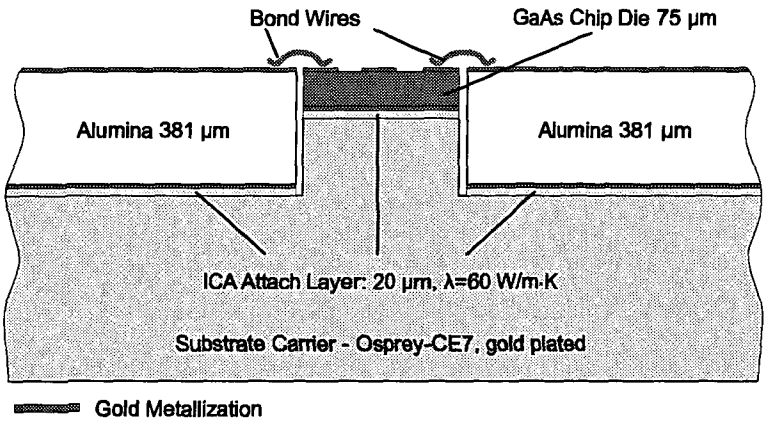


Figure 4.3: Packaging cross section.

Die Attachement Using Isotropically Conductive Adhesive

The low thermal conductivity of GaAs (44 W/m·K compared to 150 W/m·K of Si at 300 K, Fig. 4.4) requires a careful thermal design. Investigation of the thermal performance is needed to improve lifetime and reliability of the device by minimizing the influence of thermomechanically induced stress and thermal load. However, the thermal performance of a given GaAs device is mainly influenced by the thermal resistance of the bonding layer between chip and chip carrier. Thus the influence of bonding parameters on the thermal behavior of a GaAs chip device was investigated.

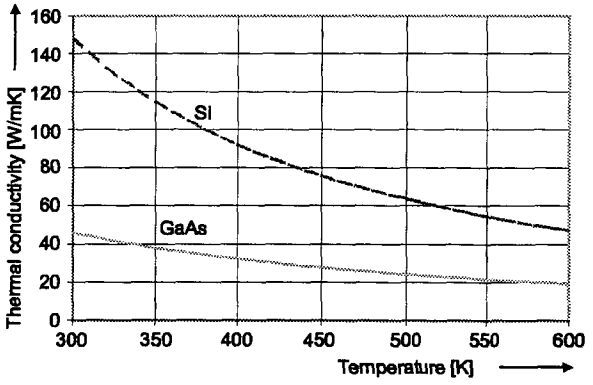


Figure 4.4: Temperature dependent thermal conductivity of silicon (Si) and gallium arsenide (GaAs) [57].

For this purpose the thermal simulation tool TRESCOM II developed at the Institute of Industrial Electronics and Material Science at the Vienna University of Technology was used. The tool is based on an efficient model creation procedure and allows to generate, change and maintain models in short time. Thermal parameters of common materials are implemented in a material database. The developed solver based on an alternating direction implicit (ADI) algorithm is efficiently processing high node numbers (up to sev-

eral 10^6) for computing nonlinear steady-state and unsteady-state heat transfer problems including the consideration of temperature dependent material parameters and boundary conditions [58], [59].

Figure 4.5 shows a microscopic view of the structure of the investigated GaAs power transistor (Excelics EPA480CV, further details on the transistor will be given in 4.4). The lateral chip dimension is 680 μm x 620 μm, the chip thickness is 75 μm ($\pm$13 μm), and the depth of the conducting channel was assumed to be approximately 0.3 μm. The metallization consists of several vapor deposited layers of gold with an assumed total thickness of 0.3 μm over the gates and 2.6 μm elsewhere.

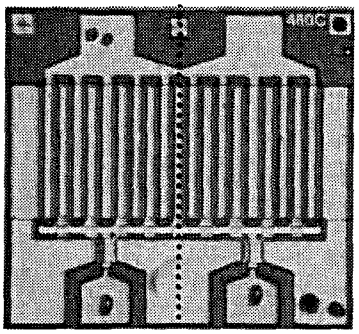


Figure 4.5: Microscopic view of the top side of the investigated GaAs power FET (dotted line marks thermal symmetry plane).

The die was bonded on a chip carrier, as shown in Fig. 4.3, with overall dimensions of 7.62×7.01×0.51 mm. In the experimental set-up chip and chip carrier were placed on a temperature controlled heat sink using a thermocouple for temperature measurement and peltier elements for cooling. In this way a known and constant temperature is achieved as boundary condition at the bottom of the carrier while natural convection and heat radiation are the boundary conditions at other surfaces.

The concept of the model creation procedure of the thermal simulation tool is based on dividing the object into layers according to its vertical structure and each layer is subdivided into volume elements (cells). For modeling the complete assembly consisting of the GaAs power FET, the die attach layer, and the chip carrier 15 layers were used. The layer thickness increases as the distance to the active channel increases. It is assumed that heat is generated under the gate within the 0.3 μm thick channel and each channel generates an equal quantity of heat. The temperature dependent thermal conductivity of GaAs was considered using a simple power law. This approximation is in good agreement with experimental data [57]. Due to the existing thermal symmetry only one half of the assembly has to be modeled (see dotted line in Fig. 4.5).

In this thesis, the chip is attached to the chip carrier using high thermal conductivity Ag/Epoxy adhesive paste (DIEMAT DM6030Hk), which has a silver content of more than 90 % (cured). According to the datasheet, the thermal conductivity of this adhesive is 60 W/m·K[1]. Due to the fact, that the thermal performance of the GaAs device is influenced by tolerances of this value the adhesive's thermal conductivity was measured [60]. As a

[1] Commonly used ICAs have a thermal conductivity of approx. 8 W/m·K.

result of this measurement a mean value of the thermal conductivity λ of 57 W/m·K was obtained.

For investigating the thermal behavior of the power transistor, transient and steady-state simulations were carried out [61], [62], and [60]. The goal was to establish the influence of chip bonding parameters on the temperature distribution within the active layer. For reliable operation, the continuous channel temperature must be kept below 150 °C, exceeding a channel temperature above 175 °C may result in permanent damage of the investigated transistor. All simulations were carried out for 25 °C ambient and heat sink temperature.

For illustrating the thermal behavior of the power transistor, temperature vs. time functions at significant points as well as a line scan of the temperature at the surface of the component are given (locations see Fig. 4.6).

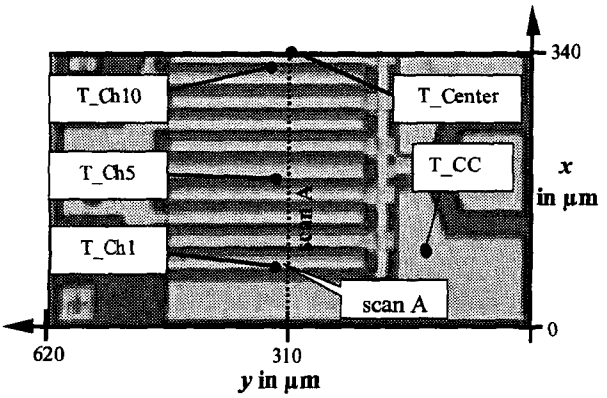


Figure 4.6: Significant points and line scans used for illustrating the thermal behavior of the transistor.

For proving the validity of the simulation some results were compared with those established experimentally at a distinct measurement point. Direct measurement of chip temperatures is difficult to achieve [63]. Frequently an integrated diode serves as temperature sensor [53]. However, the investigated chip was not provided with such a sensor. As a new approach a thin wire thermocouple using wedge bonding of gold and aluminum wires (25 μm diameter, respectively) was realized. The wires were bonded with the gold metallization of the chip (location T_CC in Fig. 4.6) and the temperature dependent thermal voltage between gold and aluminum wire was measured. Since the thermoelectric voltage (Seebeck coefficient) is strongly influenced on the composition of the involved materials and the Al wire is alloyed with 1 % silicon for an improved bondability, the Seebeck coefficient had to be established in a separated calibration measurement and a value of approximately 4.6 μV/K was found.

The influence of the thermal conductivity of the die attach layer on the gate temperature in the vicinity of the symmetry plane is depicted in Fig. 4.7a. These results were established at a power loss of 6 W and 75 μm chip thickness. In order to study the impact of the ICA's thermal conductivity on the gate temperature a variation from 20 W/m·K to 60 W/m·K, as it is a common range for high thermal conductivity adhesives, was considered. This variation causes a certainly remarkable temperature difference of up

to approximately 20 K in the gate regions. This means that the device can be operated at a lower temperature which improves the reliability, or, the device can be operated with a higher power loss at the same temperature. In the particular case the power loss can be increased by 11.5 %.

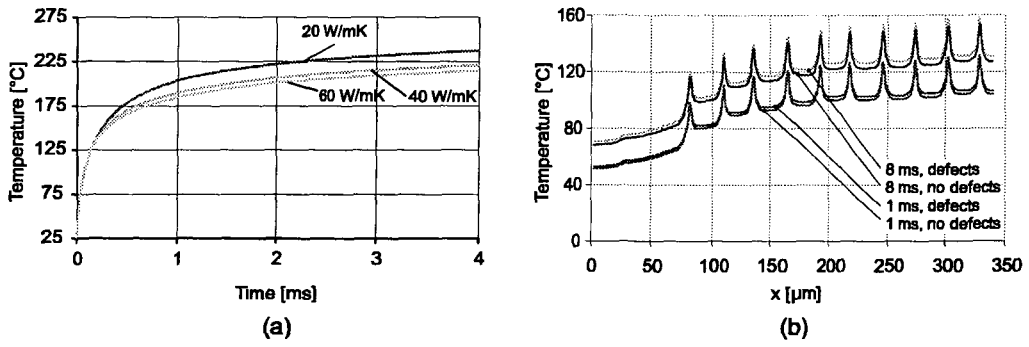


Figure 4.7: Simulation results. – (a) Temperature vs. time functions at T_Ch10 (Fig. 4.6) for varying thermal conductivity of the adhesive; (b) Temperatures along line scan A (Fig. 4.6) at different time stages for models with and without 10 % defect bonding area.

Figure 4.7b depicts the influence of bonding defects on the temperature distribution within the active layer. A defect bonding area (bubbles) of 10 % was assumed. The figure shows the temperature along a line scan (scan A in Fig. 4.6) established at 1 ms and 8 ms after power on. Simulations were carried out for 4 W power loss and 30 W/m·K was assumed for the thermal conductivity of the chip attach layer (layer thickness: 20 μm, chip thickness: 75 μm).

As can be seen in Fig. 4.7b, heat generation within the GaAs power transistor is concentrated in a few small discrete locations. This in combination with the low thermal conductivity results in large thermal gradients.

The reliability of a power device can be significantly enhanced by the use of an adhesive with high thermal conductivity.

Substrate Carrier

As presented above, transistor packaging makes it necessary to have a substrate carrier for the amplifier module. For bonding the substrates onto the carrier and for soldering the components in a reflow oven it is important that the material has a similar coefficient of thermal expansion as alumina, because temperatures of up to 220 °C will occur. To act as a heatsink for the active devices the material has to have high thermal conductivity. Since the substrate carrier is used as the transistor's source contact the electrical conductivity has to be high as well. Furthermore, machining and gold plating should be easy. Figures 4.8a and Fig. 4.8b show the coefficient of thermal expansion and the thermal conductivity for various metal alloys and alumina, respectively.

As can be seen in Fig. 4.8a, Kovar and Osprey–CE7 are the materials that fit best to the coefficient of thermal expansion of alumina. When comparing these two materials with respect to there thermal conductivity it becomes evident that Osprey CE–7 has a far

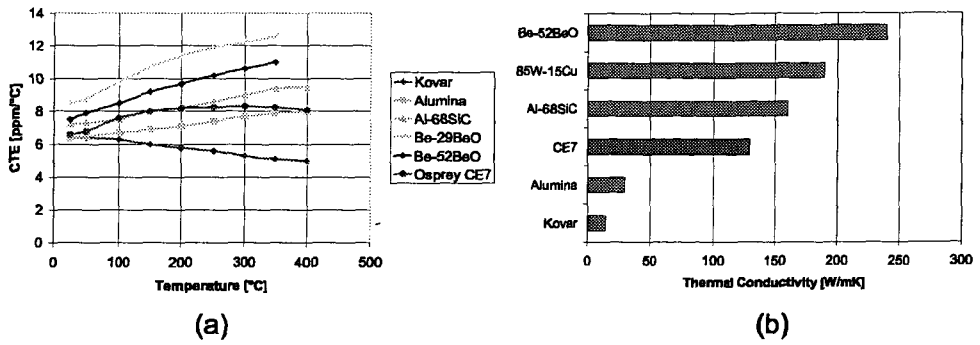


Figure 4.8: Metal alloys – (a) coefficient of thermal expansion; (b) thermal conductivity.

better thermal conductivity than Kovar. Osprey–CE7 is a Si-30wt% Al alloy and features an electrical resistivity of $<10^{-6}$ Ωm, has good machining capabilities, is lightweight (2.4-2.5 g/cm^3, lighter than pure aluminum) and ready for goldplating.

The substrates are finally bonded to the machined and gold plated substrate carriers by a conductive adhesive (ICA) as it is also used for active device bonding. Figure 4.9 shows the way from the machined substrate carrier to the bonded substrates, which are then ready for further assembly.

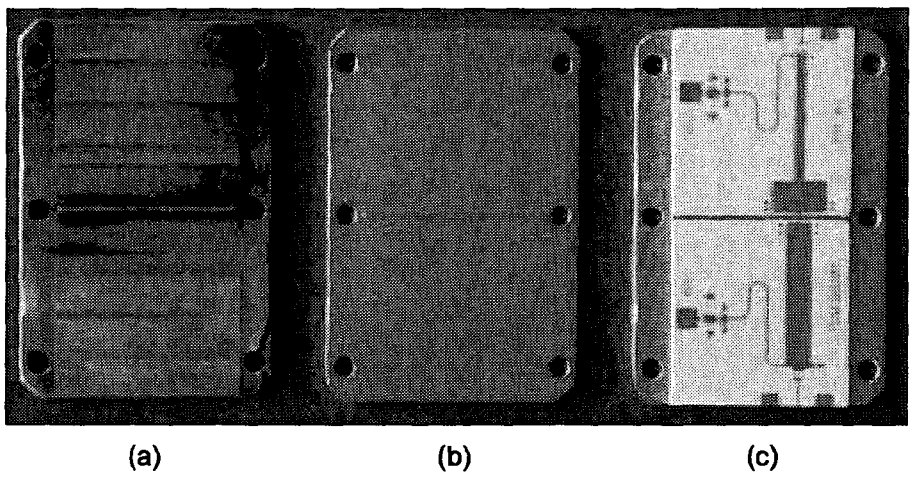


Figure 4.9: Substrate assembly procedure – (a) machined metal; (b) gold plated metal; (c) bonded substrates.

4.2 TRL Calibration Technique

Accurate measurement results can only be obtained if if the inherent systematic errors of the measurement system are removed by calibration. Figure 4.10 depicts a measurement setup with a test fixture to with a device under test (DUT) mounted on a substrate is

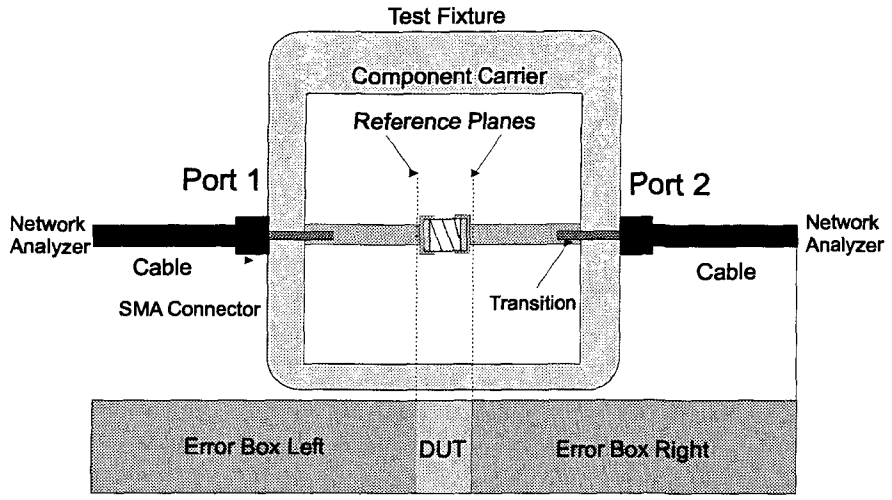


Figure 4.10: Measurement setup with test fixture and network analyzer.

connected. By means of calibration the influence of the network analyzer itself, network analyzer cables, connectors and test fixture transistions is corrected up to the reference planes. The correction data is stored in error boxes, one for each port. With those error boxes the S-parameters of the DUT can be de-embedded. To characterize DUTs in microstrip environment Thru-Reflect-Line (TRL) calibration method is prefered [64]. The quality of the TRL calibration depends on the knowledge of the characteristic impedance of the LINE element whereas the precise characteristics of the REFLECT standard need not be known. For useful calibration the phase offset of a LINE element refered to the THRU-element has to be in a range of 20 ° and 160 °. This limits the possible ratio of the upper calibration frequency to the lower frequency to 8. To be able to calibrate a wider frequency range additional LINE elements have to be used. For low frequencies the physical length of the LINE element may be too large for practical implementation. In this case it can be substituted by a matched termination, and is then called Thru-Reflect-Match (TRM) calibration.

For characterization within this thesis two different test fixtures were used. For the characterization of the passive and active components a test fixture from Intercontinental Microwaves (ICM) was used (Fig. 4.11a). This fixture works like a vice. Contact pins are used to make reproducible connections between the fixed SMA connectors of the network analyzer and the DUT. A midsection acts as a carrier for the different test structures. ICM also provides a TRL calibration kit for alumina substrates (Fig. 4.11b) with the elements listed in Tab. 4.3.

For the characterization of assembled modules (amplifiers, couplers, bias-Ts) a test fixture from ConneXion Rosenberger was used (Fig. 4.12). This test fixture has the advantage that no midsection is needed and the module size can be chosen freely. Furthermore, up to 10 transitions can be placed on each side which allows for multiport probing (e.g. couplers).

For this test fixture a TRL calibration kit had to be developed. The desired frequency range is 0.6 GHz to 10 GHz. For this range two LINE standards are needed. The effective

	Physical Length [mm]	Relative el. Delay [ps]	Frequency Range [GHz]
Thru	5.08	0	0 – 26.5
Reflect (Short)	0.00	- 20	0 – 26.5
Match	2.54	1	0 – 1.98
Line 1	7.65	20	1.98 – 5.99
Line 2	6.1	7.5	5.99 – 26.5

Table 4.3: Intercontinental Microwaves calibration kit elements.

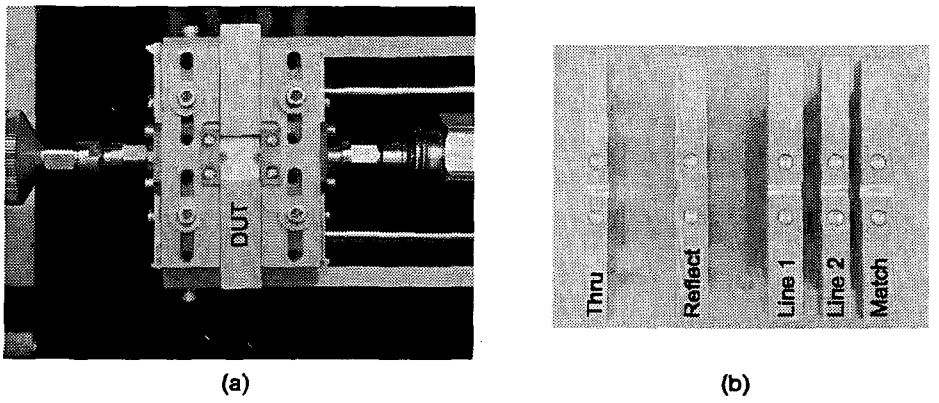


Figure 4.11: ICM test fixture - (a) test fixture with DUT in midsection; (b) TRL calibration kit.

dielectric constant for alumina at 0.6 GHz is $\varepsilon_{r,eff} = 6.5$ for 50 Ω lines. The longer line should have a phase offset of more than 20 ° at 0.6 GHz. Thus the minimum length of the longer LINE element calculates to

$$l_{1,\min} \geq \frac{20°}{360°} \frac{c}{0.6GHz\sqrt{6.5}} = 10.89mm, \tag{4.1}$$

where $\frac{c}{0.6GHz\sqrt{6.5}}$ is the wavelength at 0.6 GHz. The length of the shorter LINE element should not exceed 160 ° at 10 GHz. The effective dielectric constant for Alumina at 10 GHz is $\varepsilon_{r,eff} = 6.8$ for 50 Ω lines. Thus the maximum length of the shorter LINE element is

$$l_{2,\max} \leq \frac{160°}{360°} \frac{c}{10GHz\sqrt{6.8}} = 5.13mm. \tag{4.2}$$

The lengths finally chosen are l_1=11.5 mm and l_2=5.1 mm. Table 4.4 summarizes the elements of the calibration kit.

The calibration kit is shown in Fig. 4.13. Additionally to the calibration elements a short and a resonator were realized. The short enables measurements of the DC cable resistances. The resonator is used for calibrating the circuit simulator's relative dielectric constant value. Since the physical parameters are well known (and this is assumed to be the case for thin film) the measurement results of the resonator can be compared to the

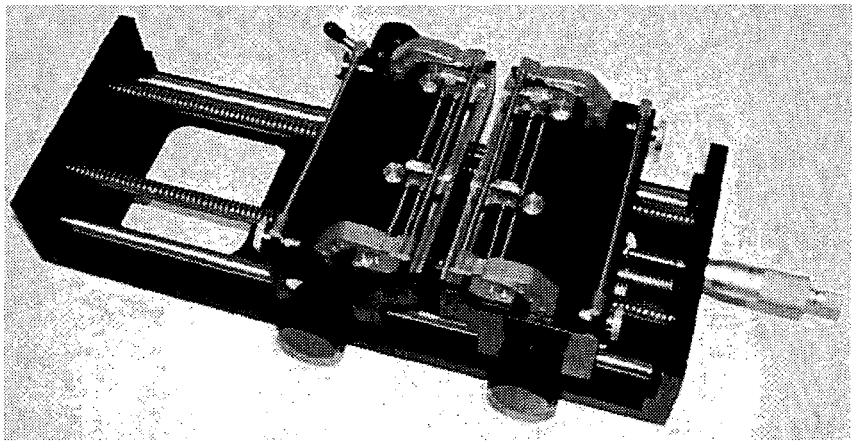


Figure 4.12: ConneXion Rosenberger test fixture.

	Physical Length [mm]	Relative el. Delay [ps]	Frequency Range [GHz]
Thru	5.08	0	0 – 10
Reflect (Open)	2.54	0	0 – 10
Line 1	16.58	98	0.6 – 3.2
Line 2	10.15	45	3.2 – 10

Table 4.4: ConneXion Rosenberger calibration kit elements.

simulation results of the circuit simulator. To calibrate the circuit simulator the relative dielectric constant is changed in a way that simulation results fit the measurement results. If the simulator is known to give accurate results the obtained value is also equal to the real value for the relative dielectric constant ε_r.

4.3 Passive Devices

To ensure optimum performance of the thin film amplifier only components with high quality factor (Q) and low insertion loss may be used. The behavior of these components

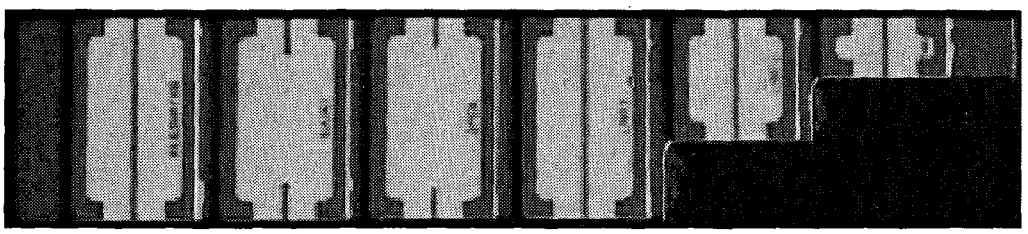


Figure 4.13: Calibration kit for the ConneXion Rosenberger test fixture.

must be described very well by computer models to get reliable simulation results. Thus various comercially available lumped element capacitors and inductors as well as thin film components were selected and characterized to ensure the validity of the passive models. As no computer models for the lumped components were available scaleable models for these elements were developed. For thin film components some computer models had to be adapted or newly developed.

4.3.1 Lumped Components

The criteria for the selection of the lumped components were:

- Low insertion loss (low ESR)
- Very high self resonant frequency
- Low temperature coefficient (capacitors: NPO)
- High current capability (bias inductors)
- Tight tolerance
- Small size

The lumped components finally chosen for characterization are listed in Tab. 4.5.

Capacitors:	Size	Value Range	Min. Tolerance
ATC 500 BMC Series	0603	0.1 – 10 pF	±0.05 pF – ±2 %
ATC 600S Series	0603	0.1 – 100 pF	±0.05 pF – ±1 %
Tecdia Single Layer Size B	0101	0.1 – 1.8 pF	±0.05 pF – ±20 %
Tecdia Single Layer Size H	0202	0.5 – 6.8 pF	±0.1 pF – ±5 %
Inductors:	**Size**	**Value Range**	**Min. Tolerance**
Coilcraft 0402CS Series	0402	1 – 40 nH	±5 %
Coilcraft 0603CS Series	0603	1.6 – 270 nH	±2 %
Coilcraft 0603HC Series	0603	1.6 – 24 nH	±2 %

Table 4.5: Lumped components selected for amplifier development.

A set of each component series representing the whole value range and an empty foot print (please, see Fig. 4.14) of that component size were characterized by S-parameter measurements. Small thin film substrates (10.16×8.6 mm) were manufactured with the recommended footprint connected with 50 Ω transmission lines. The components were mounted on these plates and characterized with the test fixture shown in Fig. 4.11a using TRL calibration technique. Since the carrier substrate had the same dimensions for all components (the same midsection was used) the line extensions from the calibration reference plane to the desired reference plane were de-embedded with the circuit simulator.

The development of models for the passive lumped devices was performed in three steps:

1. Development of foot print model.
2. Development of individual device models.
3. Development of scaleable models based on individual models

Foot Print Models

To be able to extract the component parameters the influence of the foot print metal and the substrate have to be known. Therefore, the empty foot print was measured for every different component size. The scattering parameters were modeled by an equivalent circuit (Fig. 4.14) which describes the microstrip structure by individual microstrip models. Dissipation of radiation was taken into account by two shunt resistors R_1 and R_2, respectively. But for a low-loss substrate, like alumina, these resistors can also be neglected.

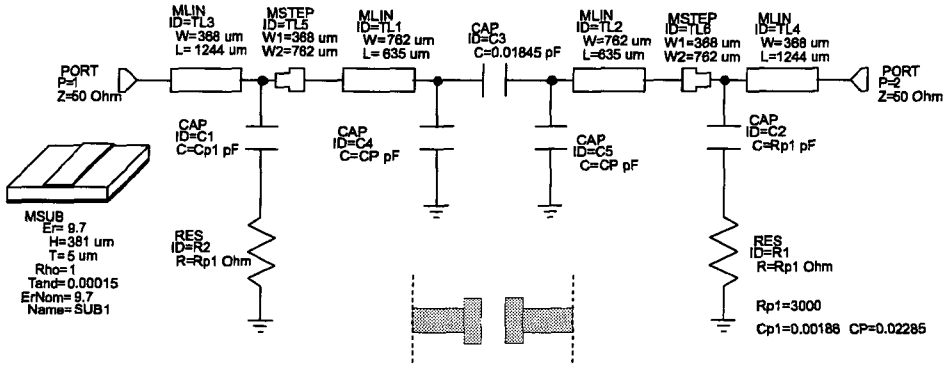


Figure 4.14: Equivalent circuit diagram for device foot print.

Individual Models

For all measured devices individual models were developed. The capacitors showed only one resonance in the frequency range up to 10 GHz, so a simple RLC series resonant circuit would sufficiently model these devices. However, better results were achieved by introducing a small parasitic RLC series resonant circuit in parallel. Inductors with small values could also be modeled with one parallel resonant circuit. For inductors with larger values additional resonant circuits had to be added to get accurate device models. An additional transmission line was used to model time delays caused by the device dimensions. Figure 4.15 and Fig. 4.17 show the equivalent model of a 1.3 pF ATC500 capacitor and of a 24 nH Coilcraft 0603CS inductor. In Fig. 4.16 and Fig. 4.18 the measurement and model results are displayed and show good agreement.

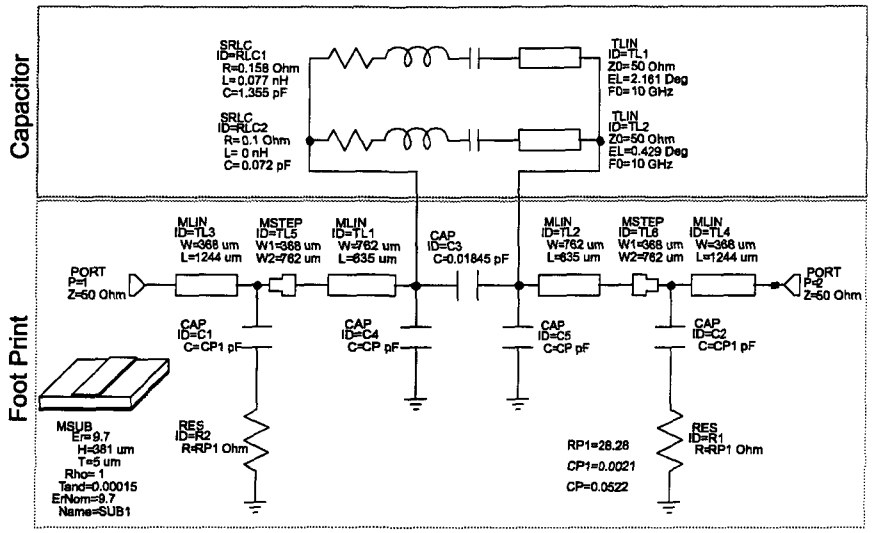


Figure 4.15: Equivalent circuit diagram for an ATC500 BMC capacitor, 1.3 pF.

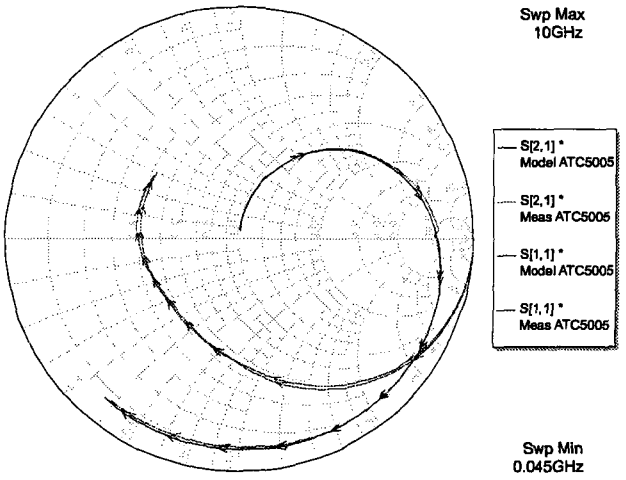


Figure 4.16: Modeled vs. measured S-parameters of an ATC500 BMC capacitor, 1.3 pF.

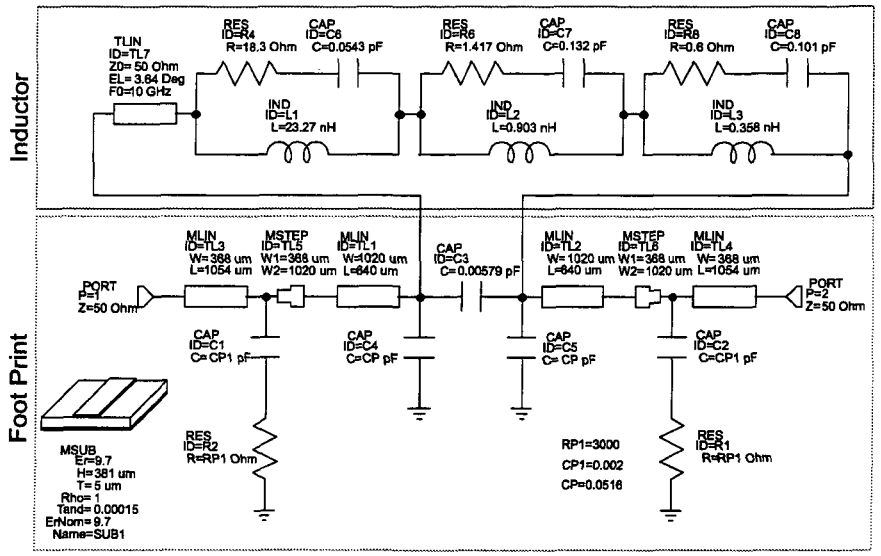


Figure 4.17: Equivalent circuit diagram for a Coilcraft 0603CS inductor, 24 nH.

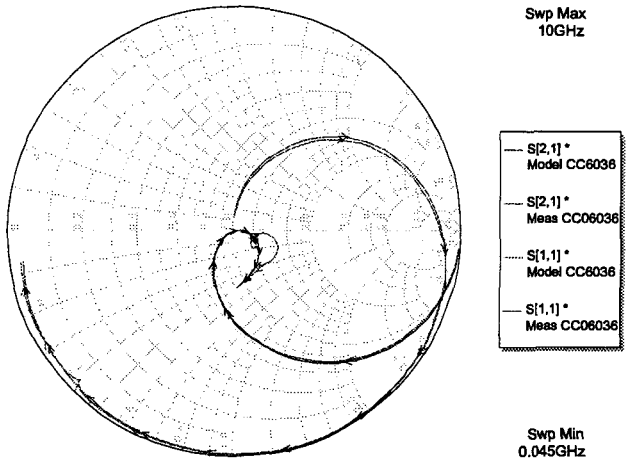


Figure 4.18: Modeled vs. measured S-parameters of a Coilcraft 0603CS inductor, 24 nH.

Scaleable Models

To simplify the usage of the models in a simulation environment scaleable models based on the individual models were generated. Therefore, analytical expressions were developed to describe the dependence of the equivalent circuit elements on the capacitance or inductance values. Figure 4.19 shows an example of a scaleable model for the ATC500 series capacitor.

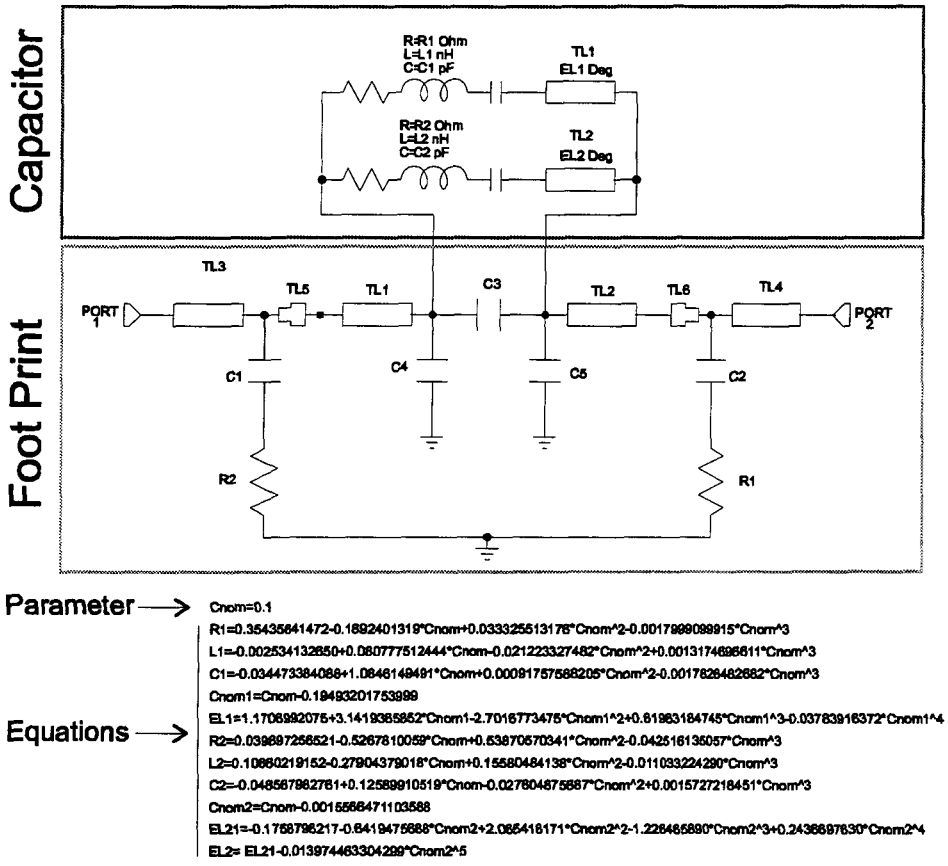


Figure 4.19: Scalable model for the ATC500 BMC capacitor series.

4.3.2 Thin Film Components

As outlined above several test structures were realized to evaluate the thin film process and to verify the computer models. The test structures and 50 Ω transmission lines for connection were realized on a small thin film substrate (10.16×8.6 mm). The components were characterized with the test fixture shown in Fig. 4.11a using TRL calibration technique. Since the carrier substrate had the same dimensions for all components (the same midsection was used) the line extensions from the calibration reference plane to the desired reference plane were de-embedded with the circuit simulator. The following sub-sections present and compare measurement and model results of various thin film components. For further details see [55].

Interdigital Capacitors

Interdigital capacitors, as shown in Fig. 4.2c, can be easily and accurately modeled using 2-dimensional, method of moments based models of coupled lines which are already implemented in a simulation software. These coupled lines are used to simulate the finger-structure of the interdigital capacitors, as it is illustrated in Fig. 4.20a.

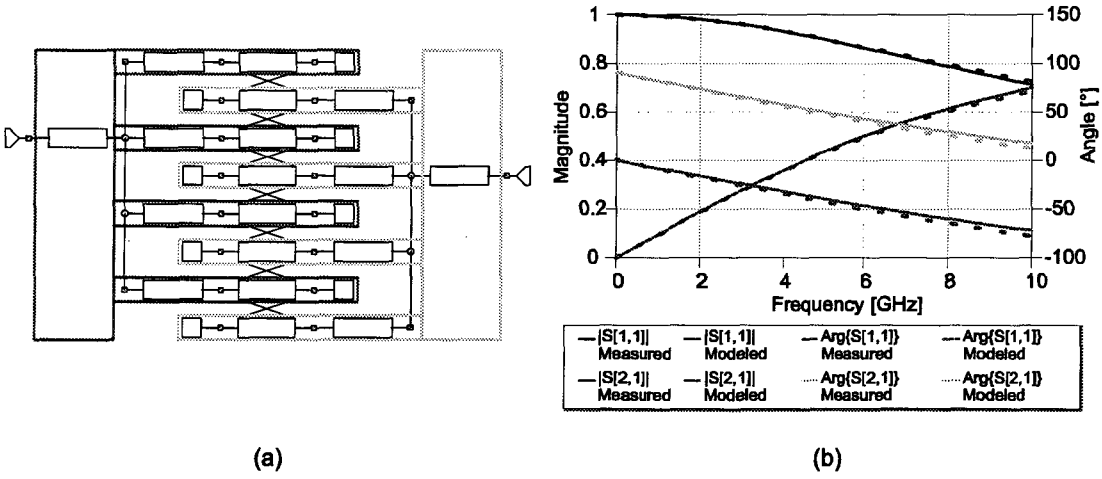


Figure 4.20: Interdigital capacitor. – (a) simulation structure; (b) comparison of measured and modeled scattering parameters.

Figure 4.20b shows modeled scattering parameters and measurement results. As can be seen in Fig. 4.20b the agreement between simulated results and scattering parameters obtained with the structure shown in Fig. 4.20a is very good.

Due to the process limited line spacing of 25 μm only very small capacitance values (< 0.1 pF) can be realized. Since the minimum line width is also limited to 25 μm the parasitic capacitors built up by the lines and the ground plane of the substrate have comparable (or higher) capacitance values than the desired one. This limits the usability significantly and makes interdigital capacitors only interesting for ground terminated capacitors.

Thin Film Resistors

As mentioned in 4.1.1 the manufacturer has problems in realizing exact values for the sheet resistance. Thus it is difficult to verify the accuracy of the circuit simulator's thin film resistor model. Figure 4.21 shows a comparison between measured and modeled scattering parameters. For the model the sheet resistance was supposed to be 60 Ω/□. From Fig. 4.21 it follows, that the match between model and measurement is very good if the thin film resistors are produced with the supposed sheet resistance.

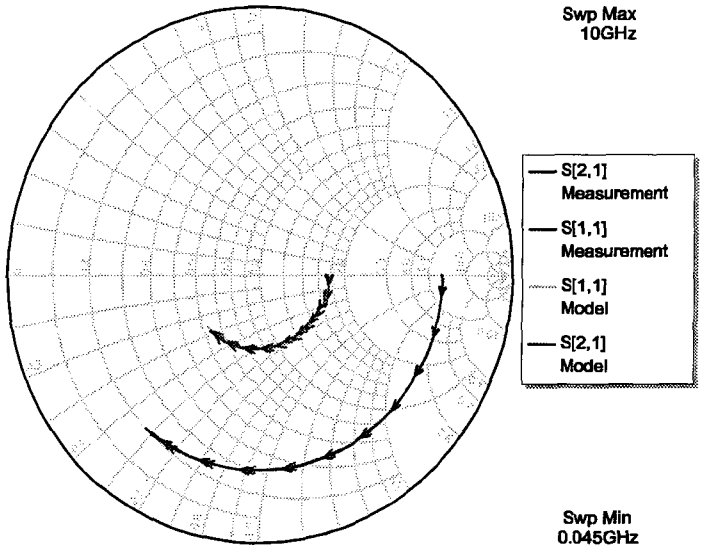


Figure 4.21: Comparison of modeled and measured 50 Ω resistor (design value based on 80 Ω/□).

Via Interconnections

Vias can be modeled using microstrip line and step elements and an already existing via model. The additional line and step models are needed to model the metal around the via. The complete model is shown in Fig. 4.22.

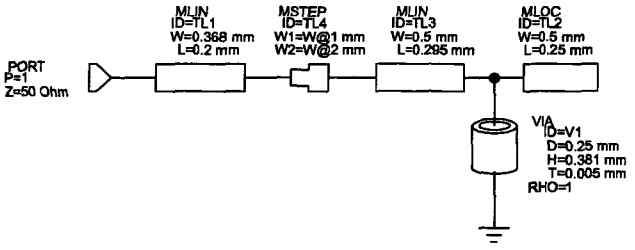


Figure 4.22: Via model.

In this model the parameters for the linewidth and the length are slightly tuned com-

pared to the manufactured physical dimensions in order to get best agreement between model and measurement. The model and measurement results are presented in Fig. 4.23.

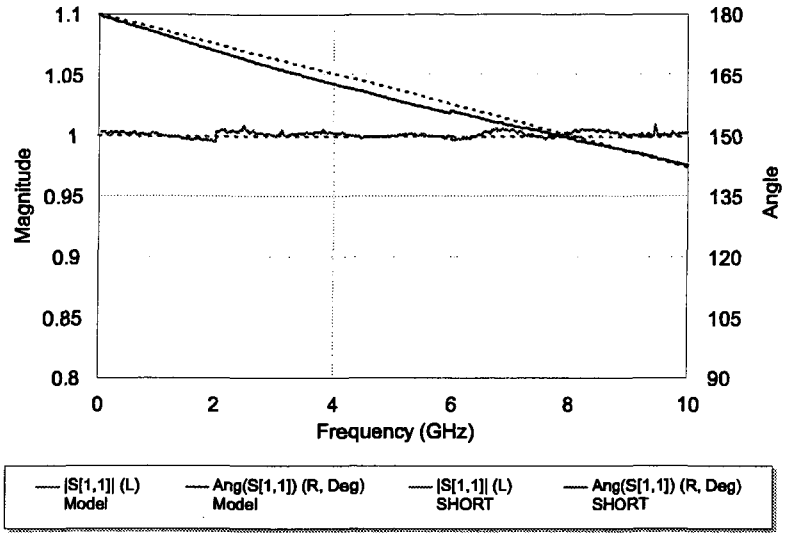


Figure 4.23: Comparison of modeled and measured via interconnect. Solid lines: measurement results; Dotted lines: simulation results.

Spiral Inductors

The measurements on planar spiral inductors during the evaluation phase showed very promising results. Inductance values in the range of <1 nH to >10 nH were achieved with quality factors of up to 50. Investigations on the available circuit simulator spiral inductor model showed that this model is not accurate enough to fit the measurement results sufficiently, but results obtained by EM simulations match quite well to the measurements. However, during the computer aided design of the amplifier the input and output networks are tuned in order to achieve optimal results. For this tuning process it eases the design by far if a scaleable spiral inductor model is available. Therefore, a scaleable, highly accurate thin film spiral inductor model was developed [65], [55].

When using inductors, one is only interested in its behavior up to the first resonant frequency. Therefore, a single section lumped element model shown in Fig. 4.24a will characterize the component with sufficient accuracy [66].

In this model, R_{ser} accounts for the resitive losses, L_{mod} includes the desired inductive effect, and the C's model the capacitive coupling effects (C_{gnd1} and C_{gnd2} are related to the capacitive coupling between the inductor and the surrounding ground plane, C_{par} models the coupling between the turns of the inductor itself). Since a low-loss substrate is used, the substrate conductance switched in parallel with the capacitances to ground may be omitted. In addition a wire element is introduced to model the effects of the bondwire, which is used to connect the center of the spiral inductor with the transmission line (Fig. 4.24b).

After measurements on spiral inductors with different numbers of turns, different shapes and different values for the line width, of the spacing of the lines and of the diameter of

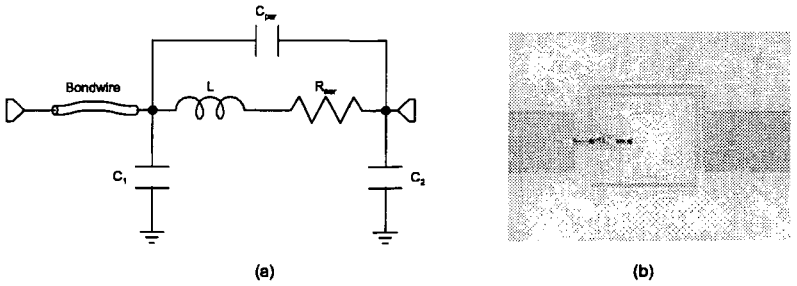


Figure 4.24: Spiral inductor. – (a) model; (b) layout.

the spiral, it was decided to use square spirals with a spacing of 25 μm and a line width of 50 μm for further investigations and for the development of the scaleable model.

After verfying the reliability of the EM simulator by comparing simulated and measured scattering parameters of different thin film structures, it was decided to develop the spiral inductor model based on simulation results and to calibrate this model by a set of measurements. For the design of scaleable models it is necessary to find dependencies between the model parameters (L_{mod}, R_{ser}, C_{par}, C_{gnd1}, C_{gnd2}) and the design parameters of the spiral inductor (number of turns, spacing, line width, outer diameter). The final model should be able to return the values of all parasitic elements for a given value of inductance L_{mod}.

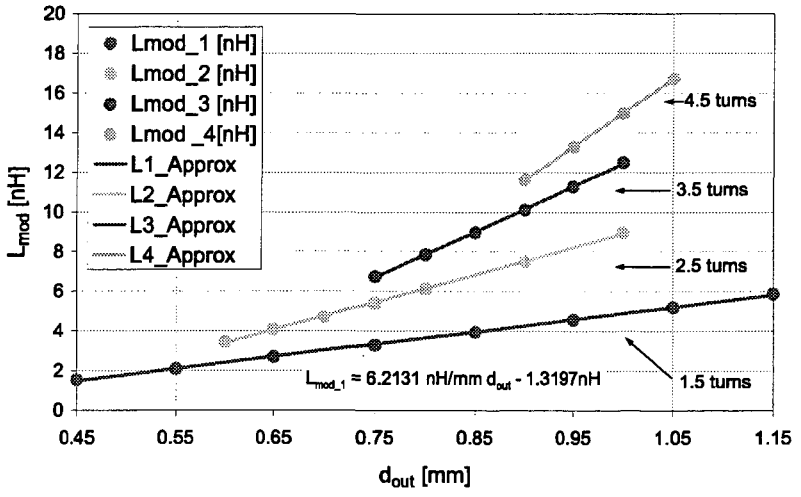


Figure 4.25: Inductance L_{mod} vs. the outer diameter d_{out} for various number of turns.

Figure 4.25 shows the inductance values of square spiral with different numbers of turns, 25 μm spacing and 50 μm line width. As it follows from Fig. 4.25 the inductance dependency on the outer diameter d_{out} is almost linear. The change of the inductance is approximately 60 pH per 10 μm change of the outer diameter for an inductor with 1.5 turns. This moderate rate of change and the linear behavior made it very interesting to use the outer diameter for the fine tuning of the inductance value. The chosen approach

for the realization of the scaleable model was to leave the number of turns constant for a given range of inductivity, and to tune the inductance value by the outer diameter d_{out}. The number of turns n was changed in steps of integer numbers starting from 1.5. One advantage of this method is, that the length of the bondwire, which is also a parameter in the model, is constant for a given number of turns, and therefore can be easily modeled.

For the scalability of the final model it is necessary to find the dependency on d_{out} for all components of the first order model shown in Fig. 4.24a. It was found that the parasitic parameters also depend approximately linear on the outer diameter d_{out}. A set of equations was determined for a constant number of turns from 1.5 to 4.5 in steps of whole turns. Figures 4.26a and 4.26b show the dependency of the model parameters C_{gnd2}, and R_{ser} on the outer diameter d_{out}.

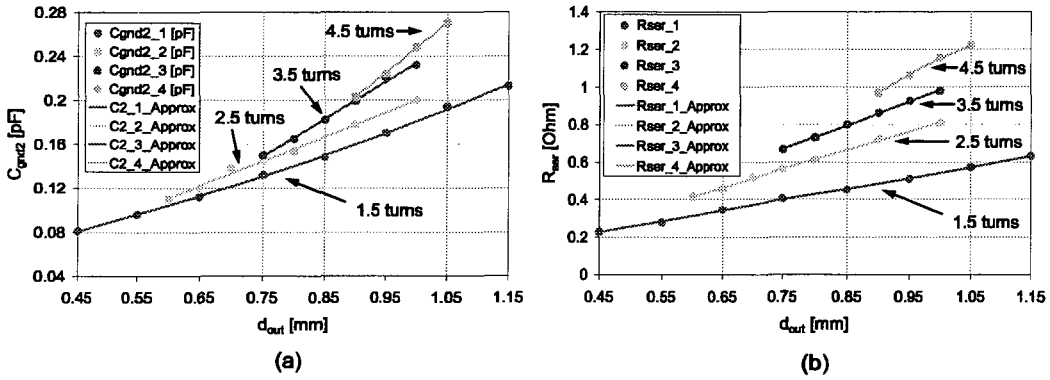


Figure 4.26: Parasitics vs. outer diameter d_{out}. – (a) C_{gnd2} vs. d_{out}; (b) R_{ser} vs. d_{out}.

To consider phenomena like skin effect and eddy currents the model equation for the series resistor R_{ser} has to be frequency dependent,

$$R_{ser} = R_{DC} + R_{AC}\sqrt{f} + R_d \cdot f, \tag{4.3}$$

where R_{DC} stands for the DC resistance of the conductor, and R_{AC} and R_d represent model resistances due to skin effect, eddy current excitation, and dielectric losses in the substrate [67]. The model equations for R_{AC} and R_d were found by matching the modeled quality factors to the simulation results. Figures 4.27a and 4.27b display a comparison of simulated and modeled spiral inductors. They show a good match between simulated and modeled scattering parameters and quality factors up to the first resonant frequency.

In order to increase the accuracy of the spiral inductor model, the simulation based model was calibrated by a set of measurements. A number of spiral inductors with varying outer diameter and different numbers of turns were manufactured and measured, using TRL calibration technique. The measured scattering parameters were compared with the simulated S-parameter data and the model equations were slightly adapted in order to match the spiral inductor model to the measured results. The resulting equations for spiral inductors with 1.5 turns are given in (4.4) – (4.10).

$$L_{mod} = 6.47\frac{nH}{mm} \cdot d_{out} - 1.8nH \tag{4.4}$$

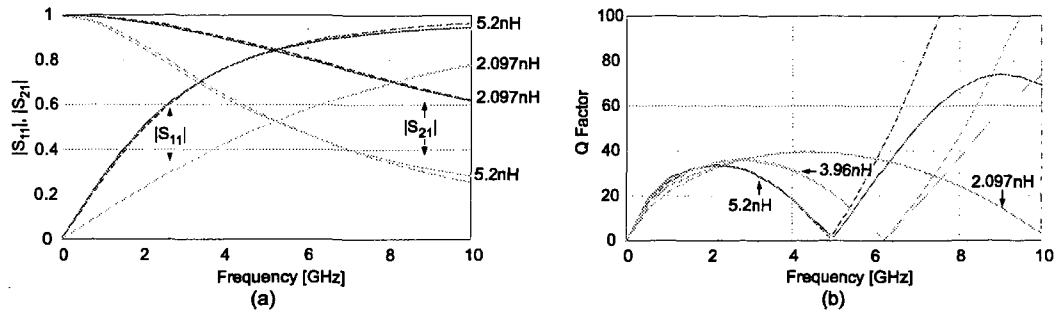


Figure 4.27: Comparison of EM simulation and modeling results. – (a) Scattering parameters; (b) quality factor.

$$C_{gnd1} = -0.040\frac{pF}{mm^2} \cdot d_{out}^2 + 0.2300\frac{pF}{mm} \cdot d_{out} - 0.005pF \tag{4.5}$$

$$C_{gnd2} = -0.042\frac{pF}{mm^2} \cdot d_{out}^2 + 0.2100\frac{pF}{mm} \cdot d_{out} - 0.005pF \tag{4.6}$$

$$C_{par} = -0.010\frac{pF}{mm^2} \cdot d_{out}^2 + 0.0023\frac{pF}{mm} \cdot d_{out} + 0.021pF \tag{4.7}$$

$$R_{DC} = 0.5700\frac{\Omega}{mm} \cdot d_{out} - 0.0320\Omega \tag{4.8}$$

$$R_{AC} = 0.3487\frac{\Omega\sqrt{s}}{mm} \cdot d_{out} + 0.0637\Omega\sqrt{s} \tag{4.9}$$

$$R_d = 0.2564\frac{\Omega s}{mm} \cdot d_{out} - 0.0479\Omega s \tag{4.10}$$

Figure 4.28 shows a comparison of measured, simulated, and modeled scattering parameters for a spiral inductor with 1.5 turns and 950 μm outer diameter. As can be seen in Fig. 4.28 there are slight deviations between simulation and measurement, but the match between modeled and measured scattering parameters is very good. Therefore, the final spiral inductor model allows an accurate prediction of the components inductance value, quality factor, and frequency behavior, based on the geometrical parameters. This is very important in the circuit design phase in order to have a "first time right" realization of the inductor.

In highly efficient amplifiers it is often necessary to have tuning capabilites in the finally mounted circuit in order to optimize the amplifier's performance. One possibility to do so is to change the bond wire position or the bond wire length. Figure 4.29a shows an example: Instead of bonding onto the bonding pad, the bondwire is connected to the trace of the inductor. Thereby the value of the inductance can be reduced by reducing the effective length of the spiral inductor. Figure 4.29b presents how the resonant frequency of a series resonant circuit can be tuned with this method. The resonant circuit consists of an ideal 1 pF capacitor in series with a spiral inductor with 525 μm outer diameter.

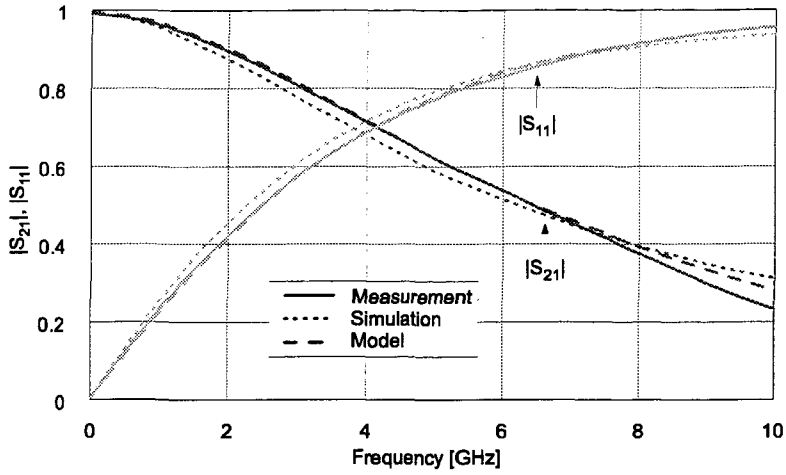


Figure 4.28: Comparison of measured, simulated, and modeled scattering parameters.

This is equivalent to a nominal inductance of 1.6 nH. As can be seen in Fig. 4.29b, the resonant frequency of the resonant circuit can be tuned from <4 GHz to >6 GHz. This is equivalent to inductance tuning from 1.6 nH to 0.65 nH.

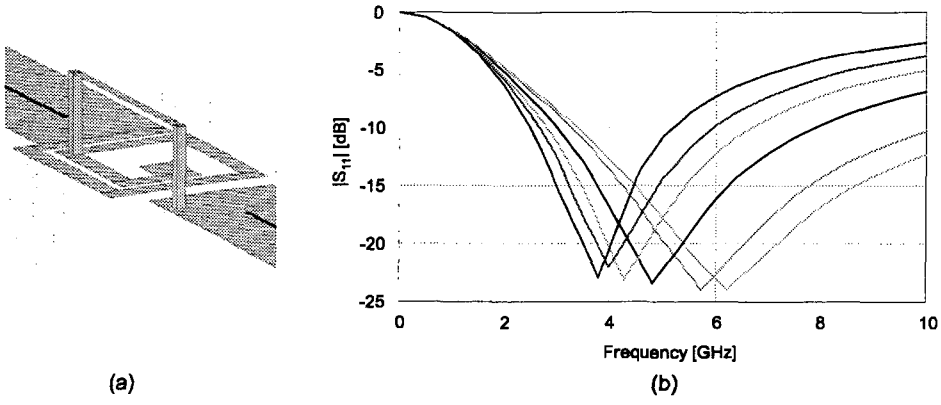


Figure 4.29: Tuning the inductor value. – (a) procedure; (b) $|S_{11}|$ of a series resonant circuit with tuned inductor.

4.4 Active Devices

Many criteria have to be fulfilled by the transistor since it is the active device which significantly influences the overall behavior of the final amplifier. Criteria for a high efficiency device are [31] :

- High transit frequency f_T to provide sufficient gain at the 3^{rd} harmonic is necessary for rectangular pulse shaping at the drain.
- High gain G will increase the power added efficiency
- High breakdown voltage V_{BR} enables a higher drain supply voltage which increases output power.
- Low drain resistance $R_{D,on}$ will decrease the knee voltage and, therefore, increase output power.
- Low pinch-off voltage $|V_P|$ will increase output power.
- Hard pinch-off ΔV_P is needed for optimum switching characteristic.
- High r_{DS} will minimize the losses inside the device.
- Low parasitic gate inductance L_G will increase output power and decrease gate stress due to decrease of negative voltage peaks at the gate (resonance effects) ($\rightarrow$ unpackaged die).
- Low parasitic drain inductance L_D will ease pulse shaping at the drain due to lower resonance effects ($\rightarrow$ unpackaged die).
- Low parasitic source inductance L_S will decrease gain loss due to voltage drop at L_S ($\rightarrow$ via connections, unpackaged die).
- Thinned die will decrease thermal stress and allows higher power dissipation.

To find the best suited, commercially available GaAs pHEMT device a sound survey was made. Finally, unpackaged power transistors from Excelics company were found to fulfill the requirements best. Based on a base cell with a gate width of 0.5×2400 μm scaled transistors are available up to five cells in parallel which gives a transistor with a gate width of 0.5×12000 μm. Since a single cell transistor was not available with source via connections, transistors with two cells and transistors with five cells were purchased. The smaller transistor is important for characterization and modeling since a transistor with 12000 μm gate width has very low input resistance and, therefore, hard to measure accurately. Figures 4.30a and 4.30b show the layout of the EPA480CV and EPA1200AV, respectively, while in Tab. 4.6 the data found in the datasheet are given.

For accurate large signal model development a precise and extensive characterization of DC and small signal RF behavior is needed. To gain knowledge on the self heating effect of the devices, DC-IV curves were also characterized at various temperatures. Former RF measurements at various temperatures showed that the influence of temperature on the scattering parameters is not significant [68].

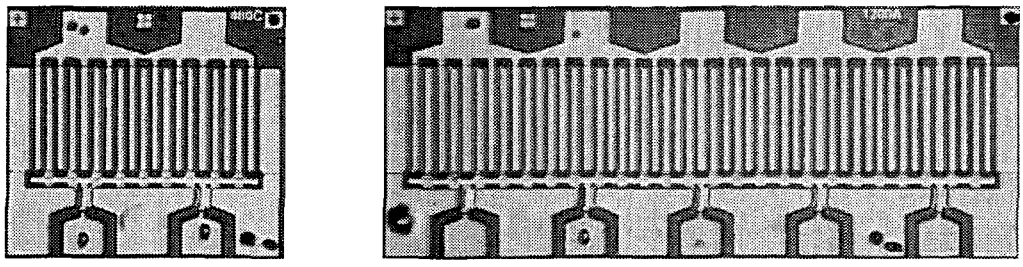


Figure 4.30: Transistor layout. – (a) EPA480CV; (b) EPA1200AV.

4.4.1 Characterization Setup

For characterization the transistors were mounted on metal chip carriers as it is shown in Fig. 4.3. The gate and drain contact were connected to the 50 Ω transmission lines on the alumina substrate by wire bonding. The layout of the substrates and the bonded devices are depicted in Fig. 4.31. For the EPA1200AV the line width was adjusted to the transistor to connect all bond wires. To get the measurement results at the desired reference planes (Fig. 4.31) the line extensions (and step) to the calibrated reference plane were de-embedded. The desired reference plane was chosen 250 μm off the substrate edge to have the effects caused by bond wires included in the measurement results. Care has to be taken that the transistors will be mounted in the amplifier circuit in the same way as for measurement.

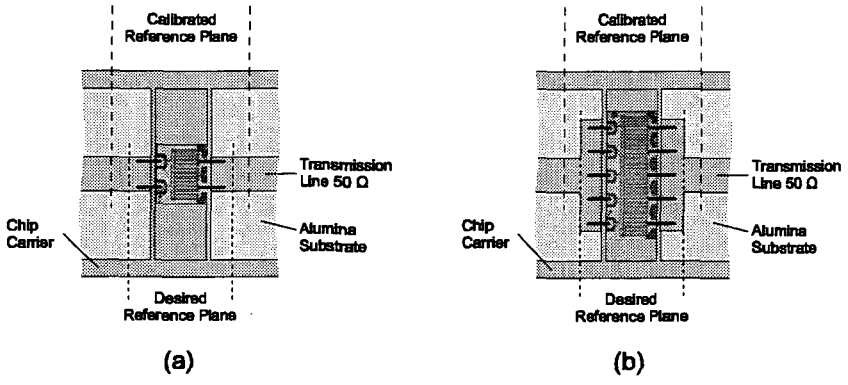


Figure 4.31: PHEMTs mounted on chip carrier. – (a) EPA480CV; (b) EPA1200AV.

These chip carriers were then placed in a midsection which was mounted into the ICM test fixture (Fig. 4.11a). To characterize the devices at different temperatures the ICM test fixture was extended with a temperature sensor to measure the temperature close at the device and a "snap-on" peltier heater/cooler was added to control the temperature [69]. The whole arrangement was placed in a temperature chamber to set the approximate ambient temperature. To prevent moisture condensation at the open chip device, a sophisticated control algorithm ensures that the device temperature is constantly kept 5 °C

Physical Dimensions:		EPA480CV	EPA1200AV	
Gate Width		0.5×4800	0.5×12000	μm
Chip Thickness		75 ±13	50 ±10	μm
Chip Size (Length × Width)		680×620	1470×620	μm
Electrical Characteristics:				
P_{1dB}	Typical Output Power	36.0	39.5	dBm
G_{1dB}	Gain at 1dB Compression	19.0	20.0	dB
PAE	Power Added Efficiency	55	50	%
I_{DSS}	Saturated Drain Current	1440	3600	mA
V_P	Pinch-off Voltage	-1.0	-1.0	V
R_{th}	Thermal Resistance	12	3.5	K/W
Cont. Maximum Ratings at 25 °C:				
V_{DS}	Drain-Source Voltage	8.0	8.0	V
V_{GS}	Gate-Source Voltage	-3.0	-3.0	V
I_{DS}	Drain Current	1200	4000	mA
I_{GSf}	Forward Gate Current	40	100	mA
T_{CH}	Channel Temperature	150	150	°C
P_T	Total Power Dissipation	9.5	32	W

Table 4.6: Transistor Datasheet.

above the ambient temperature.

4.4.2 DC Characterization

The DC measurements on both active devices had the purpose to gain measurement results as a basis for the development of large signal models. Special care has to be taken at the bias network of the measurement setup. This bias network is most important for the suppression of unwanted oscillations. The source of these oscillations is either the DC-source or the DUT. Oscillations of the regulated DC-source are rare and can be avoided by using a tantalum capacitance in parallel with the DUT. A one ohm resistor in series with the capacitor reduces the turn on current and provides a known fixed port impedance for low frequencies. Oscillations of the DUT can have thermal or electrical reasons. Thermal instabilities lead to relatively low oscillation frequencies and can be avoided with the same tantalum capacitor as used for stabilizing the DC-source. The tendency to instability is dependent on the bias. The potentially unstable region of the output characteristic (I_D vs. V_{DS}) of a MESFET or HEMT shows a negative slope. To find instable bias conditions, the measurement system [70] tracks the RF output power with a spectrum analyzer during an automatic bias sweep. If there is an oscillation, the size and position of the instable bias region is automatically determined. By adding small SMD capacitors in parallel to the DUT this instable bias region can be minimized. This is important for the RF measurements.

Test Setup

Different measurement setups were used each optimized for its own task. To test for oscillations the DC and RF setups were almost the same.

In the high frequency setup (Fig. 4.32) the HP 11612 OPT001 bias-T at the drain makes scattering parameter measurements from 0.4 to 26.5 GHz possible, but limits the maximum current to 2 A. The high current bias-T was used to ensure a defined output impedance for the DUT below 400 MHz. Those measurement results are needed for the extraction of the parameters of the extrinsic parasitics of the large signal model since resonances caused by the extrinsic parasitics will occur at higher frequencies.

As shown in Tab. 4.6, the EPA1200AV transistor can achieve current values up to 4 A. Therefore, for the upper current range a high current setup (Fig. 4.33) was built by replacing the drain bias-T with a high current bias-T. This bias-T [71] enables measurements up to 8 A, but limits the frequency range to 10 GHz.

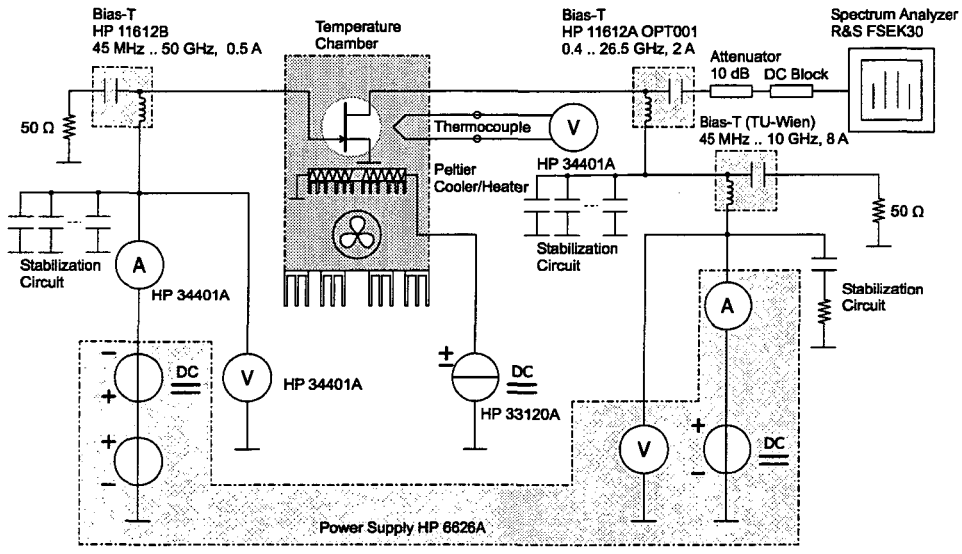


Figure 4.32: High frequency DC test setup with temperature control.

Measurement Results

The temperature of the active transistor channel depends on the ambient temperature. Since the transistor will be destroyed when the maximum channel temperature is exceeded, the maximum dissipated power has to be corrected according to the ambient temperature. Therefore, the bias range is increased for lower ambient temperatures and vice versa.

Figures 4.34 and 4.35 show the measured I/V curves of the EPA480CV and EPA1200AV, respectively. It was not possible to avoid oscillations during transistor characterization. The regions where oscillation occured is shown as an amber area in the high current region. The EPA1200AV showed further instabilites in the range of $I_D = 0.3$ to 1.5 A and $V_{DS} = 0.8$ to 2 V. The saturation currents I_{DSS} were measured to be 1.87 A and 4.38 A for the EPA480CV and the EPA1200AV, respectively. These saturation currents occur at

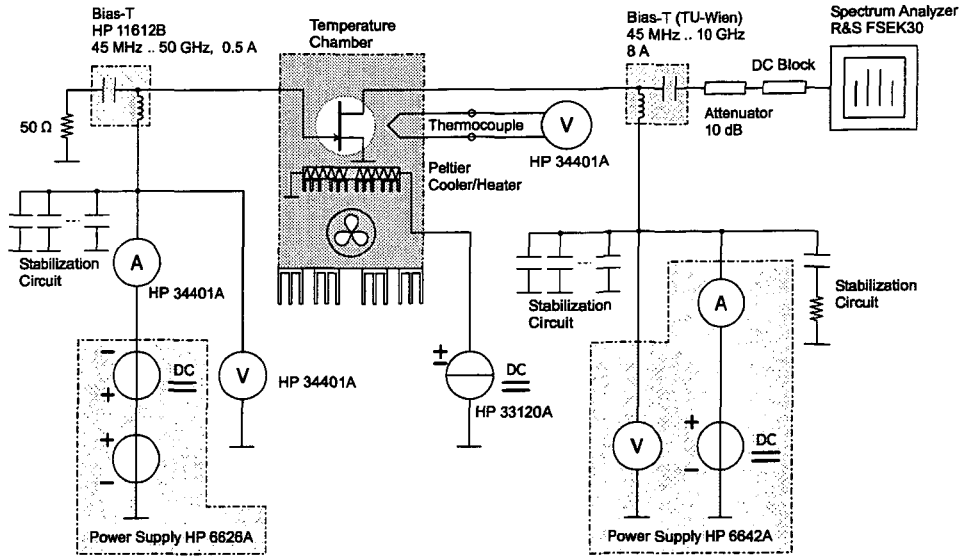


Figure 4.33: High current DC test setup with temperature control.

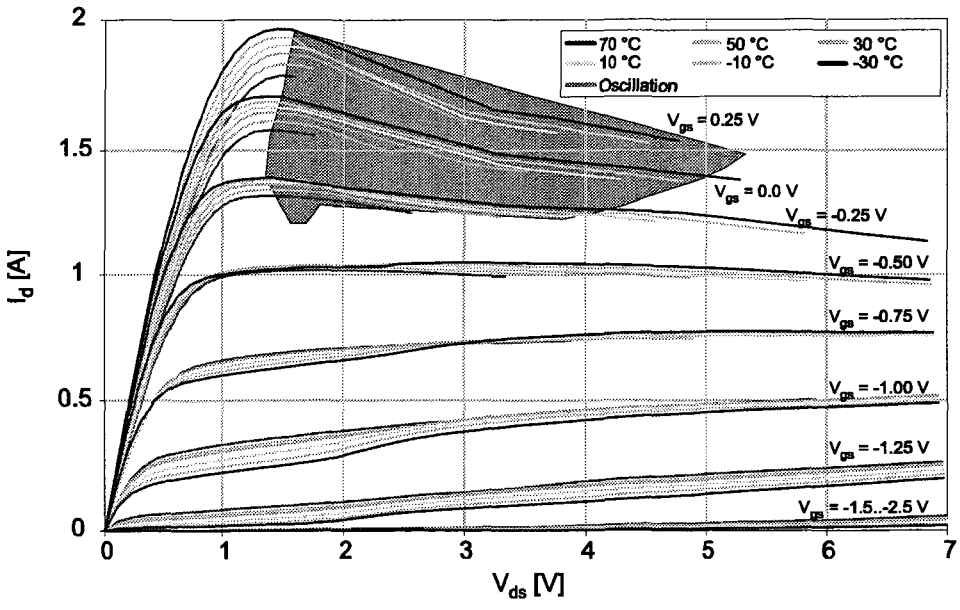


Figure 4.34: DC I/V characteristic of a EPA480CV device measured at different ambient temperatures.

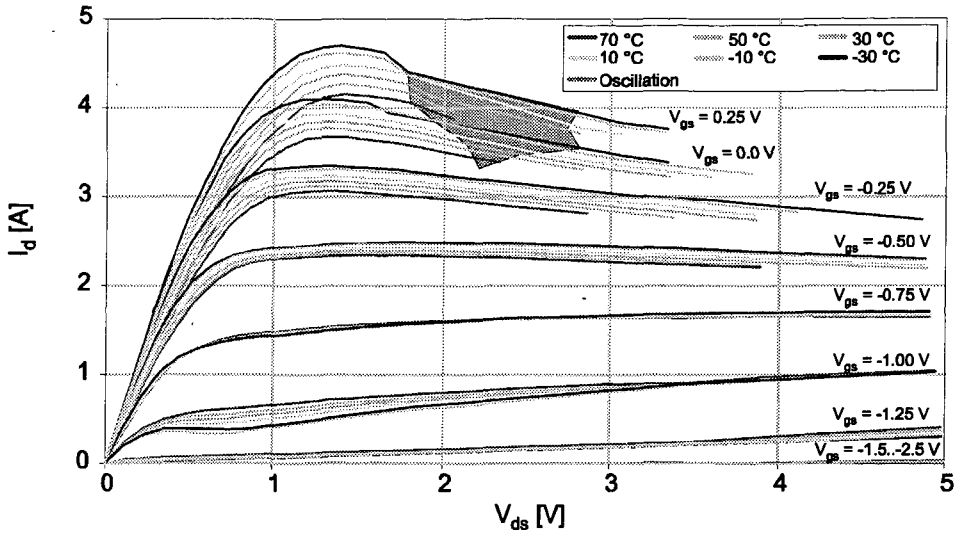


Figure 4.35: DC I/V characteristic of a EPA1200AV device measured at different ambient temperatures.

V_{DS} = 1.5 V and V_{GS} = 0.25 V at an ambient temperature of 30 °C. The values of I_{DSS} vary ±5 % with temperature where the drain current at such high current values has a negative temperature coefficient, as expected in theory. At lower current values this effect is compensated and finally dominated by carrier injection due to thermionic field emission at the gate contact. The pinch-off voltage V_P of the devices was measured to some -1.5 V.

4.4.3 Small Signal RF Characterization

For characterization of the small signal scattering parameters of the transistors under different bias conditions a network analyzer was used. To develop an accurate large signal model S-parameter measurements with bias points in the regions of the output I/V plane, where the dynamic load line will occur, are most interesting. Therefore, various bias conditions were chosen in the typical class A region, in the ohmic and knee region (high current and low voltage), and in the pinch-off region (low current and high voltage). Further, for the extraction of parasitic parameters measurements of the "unbiased" device (i.e. V_{DS}=0, V_{GS}=0) and of a pinched-off device (i.e. V_{DS}=0, V_{GS} <V_P) were made.

Test Setup

Figures 4.36 and 4.37 present the test setups for scattering parameter measurements. As can be seen, the setups are equal to the DC test setup, save the extension for thermal characterization. In the high frequency test setup (Fig. 4.36) it was possible to connect the spectrum analyzer to the high current bias-T RF output to detect any oscillation.

The bias test setup was exactly the same as for the DC measurements. This ensures that the instable bias regions are unchanged. The measurement software knows these bias regions from the previous DC measurement, and, therefore, avoids it during the RF measurement for two reasons. First, measurement results from an oscillating device are useless.

Second, and more important, the network analyzer can be damaged by the oscillation of a power transistor.

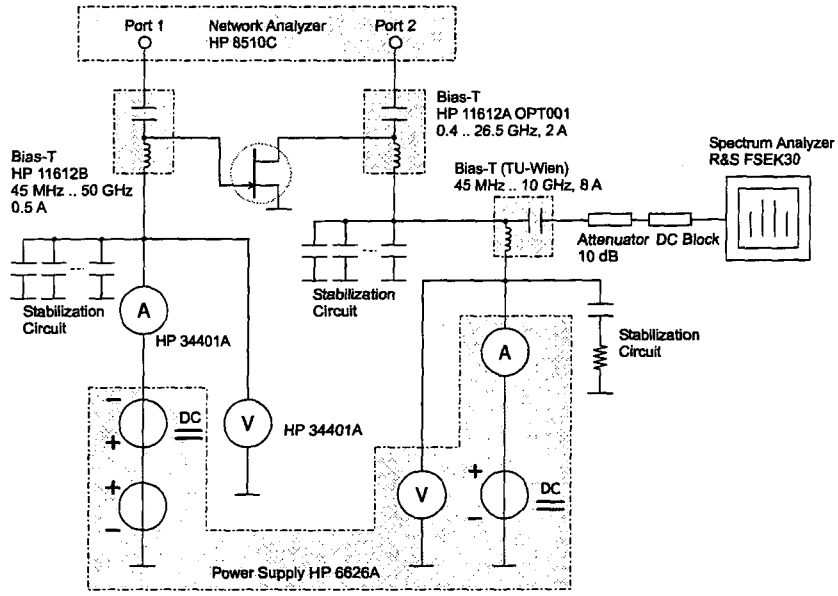


Figure 4.36: High frequency RF test setup.

Measurement Results

Figures 4.38, 4.39, and 4.40 show measurement results for three different bias points in the I/V regions mentioned above. As can be seen, the impedance values, especially at the input of the devices are very low. Measurement accuracy decreases dramatically when the ratio of measured impedance to system impedance (50 Ω) exceeds 1:10. Therefore, especially for the EPA1200AV, parasitic extraction is limited in accuracy, see 4.4.5.

The measurement results of the maximum available gain G_{MAX} (Fig. 4.40) shows that an amplifier gain of more than 20 dB is possible with these devices.

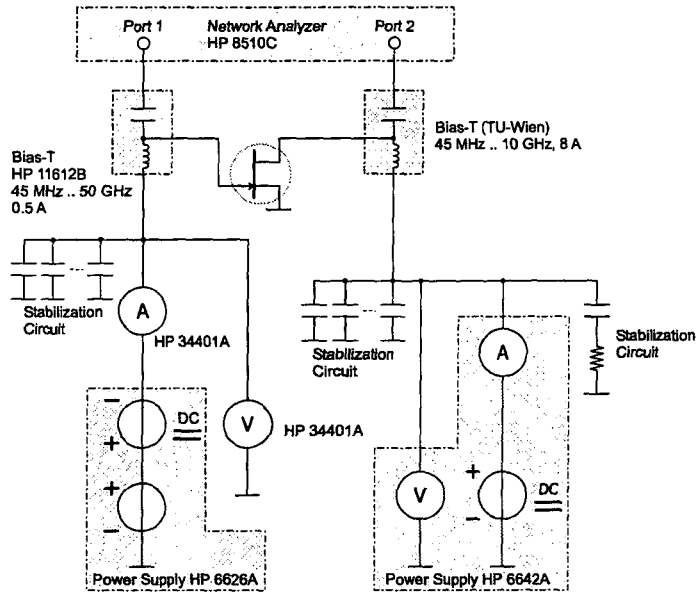


Figure 4.37: High current RF test setup.

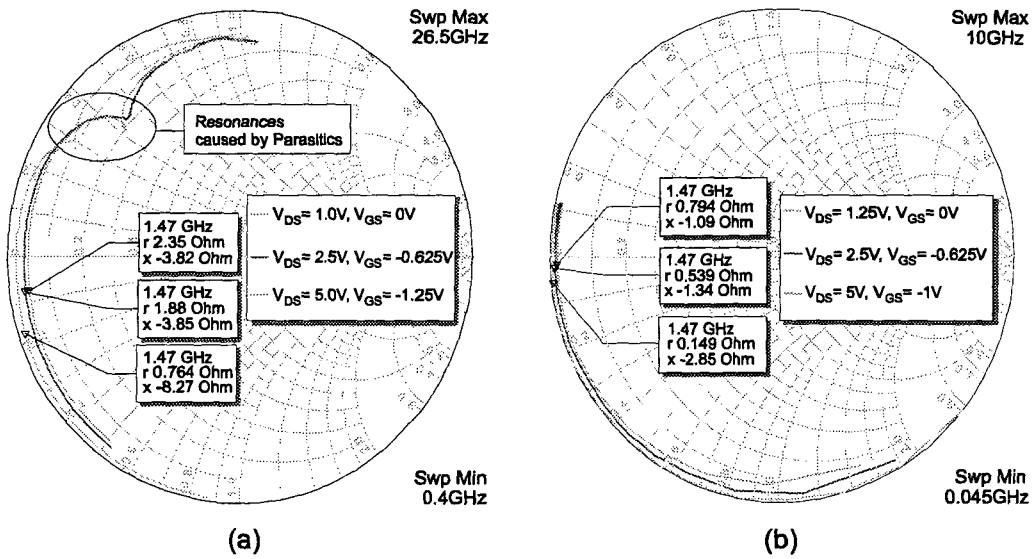


Figure 4.38: S_{11} measurement result. – (a) EPA480CV; (b) EPA1200AV.

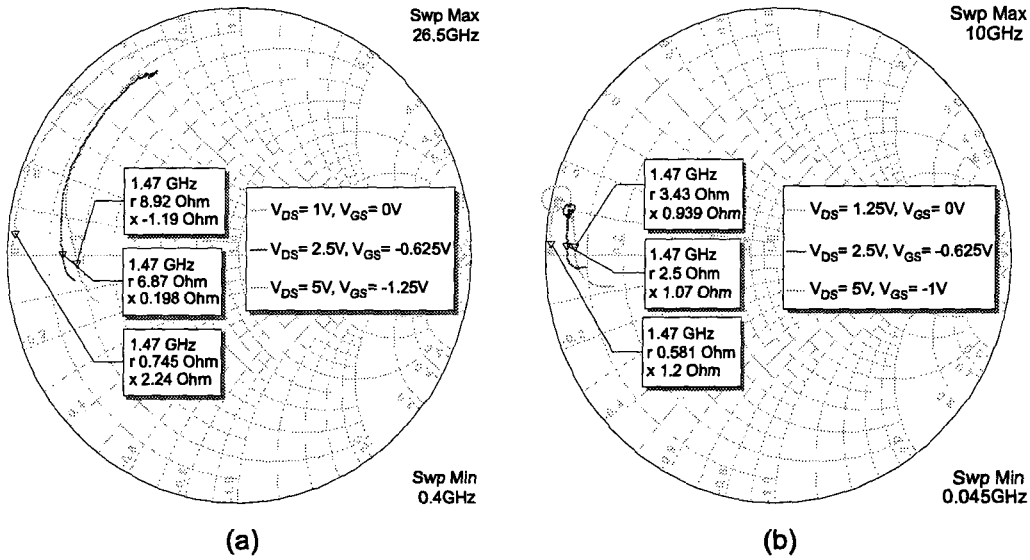


Figure 4.39: S_{22} measurement result. – (a) EPA480CV; (b) EPA1200AV.

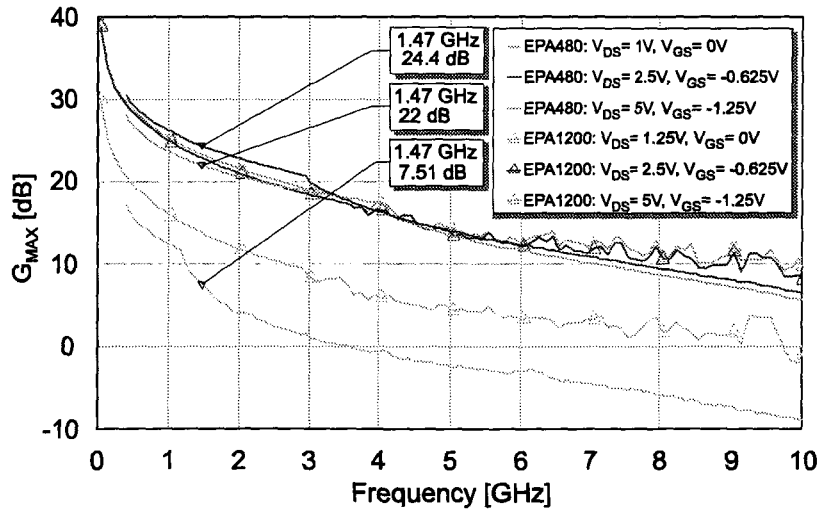


Figure 4.40: Maximum available gain G_{MAX} of the EPA480CV and EPA1200AV at different bias points.

4.4.4 Two-Tone Characterization

Two tone large signal measurements of both active devices have been performed. These measurements are necessary to evaluate large signal transistor models. The test setup is shown in Fig. 4.41.

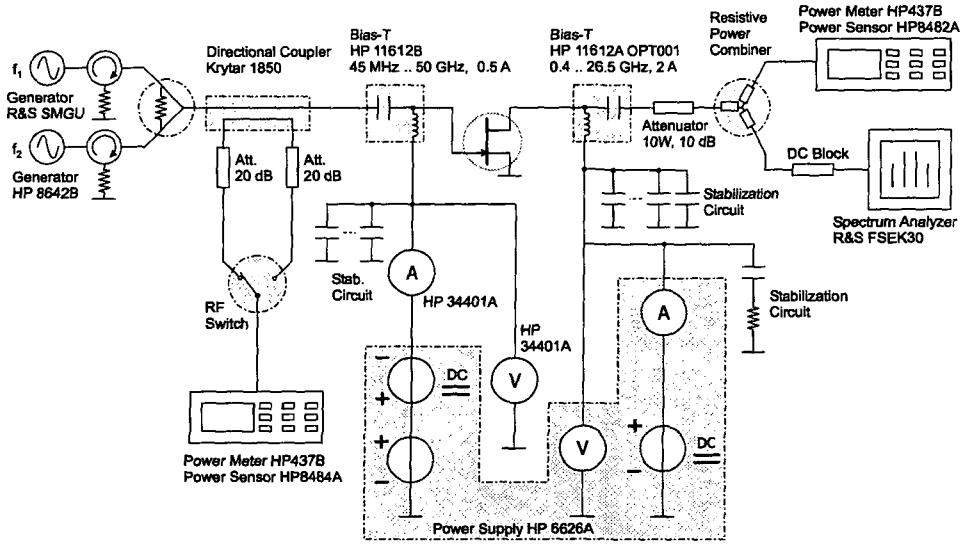


Figure 4.41: Two-tone measurement setup.

4.4.5 Modeling

The design of a power amplifier puts high demands on the large signal active device models. To get an excellent prediction of harmonic generation and intermodulation distortion the higher derivatives of the model equations have to be well behaved. Only a few computer models of this type are available. The Parker-Skellern model [72], [73] is very advanced, but a support from the Australian researchers seemed to be difficult. The Angelov model (also called the Chalmers model) [74] is simpler compared to others but the prediction of the pinch-off behavior is not so accurate as for the COBRA model [75], [76]. The COBRA model seems to to be a good compromise between accuracy and simplicity and was finally chosen. To get an even better agreement between measured and modeled performance the computer model was modified.

As mentioned above, the impedance values of the EPA1200AV are very low and measurement accuracy is restricted by the system impedance. Therefore, a transistor model for the EPA480CV was developed and scaled up by 2.5 times. These results were fine tuned to the EPA1200AV measurement results.

The COBRA Model

This model was developed by Vicentiu I. **Co**jocaru and Thomas J. **Brazil** [75] at the University College Dublin, Ireland. The model is an enhancement of the standard MESFET small signal model. A linear extrinsic model consisting of C_{pi}, C_{po}, L_g, L_s, L_d, R_g, R_d, and R_s encircles the nonlinear instrinsic model. An additional current source and a bias dependent resistor are used to correct for low frequency dispersion effects. The derivatives of the circuit equations are well behaved especially for the pinch off region [76]. The bias dependent intrinsic resistors R_{gd} and R_{gs} account for the non quasi static behavior of the gate charge at high frequencies. From the measurements it was found that no such effect occurs in the frequency region of interest. Therefore, these resistors were neglected. The connection between trapping effects and dynamic thermal effects cannot be modeled in detail with the COBRA model. These parasitic effects in power transistors are very difficult to determine. Although the details would be of great interest, it was decided to work with the simplified model.

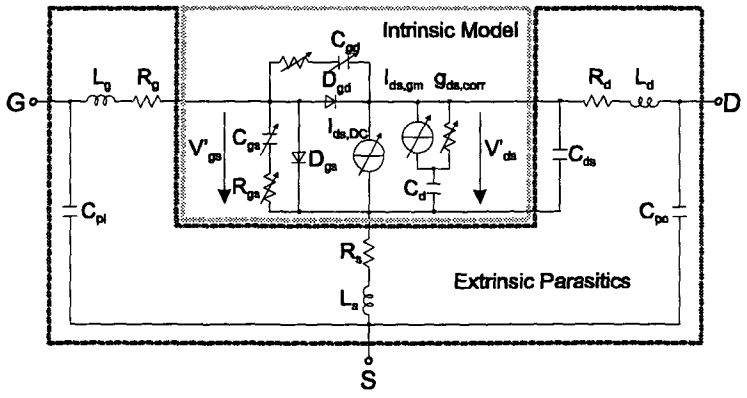


Figure 4.42: Schematic of the COBRA model.

The Extrinsic Model Because of their small values (<2 Ω) the determination of the extrinsic resistors R_g, R_d, and R_s is especially difficult for power transistors. Some methods use a small forward current through the gate diode to determine these resistances. These methods are risky. The transistor can be permanently damaged or altered by diffusion processes.

Therefore, a different method was used that was originally introduced by R. Tayrani et. al. [77] and modified by T. Brazil and V. Cojocaru where no "dangerous" operating states arise. It uses scattering parameter results from measurements at $V_{DS} = 0$ V (cold FET). For this bias the symmetry of the active channel is mainly determined by the symmetry of the depletion region under the gate and the capacitances C_{gs} and C_{gd} that model the gate charge are equal in a good approximation [75]. This is also true for an asymmetric transistor layout as it is often used in modern active devices. The model can be simplified for this special case, and all extrinsic components of the model can be calculated analytically. Because of measurement inaccuracies the results are usually frequency dependent for power transistors. By use of optimization algorithms the results can be improved.

Small Signal Models as a Basis of the COBRA Model The COBRA model is developed from small-signal models (Fig. 4.43) that have been extracted from scattering parameter measurements at bias voltages over the whole V_{DS} and V_{GS} range. After the extrinsic model is known, the intrinsic model can be calculated by the method of Berroth and Posch [78] from the deembedded [79] scattering parameter results.

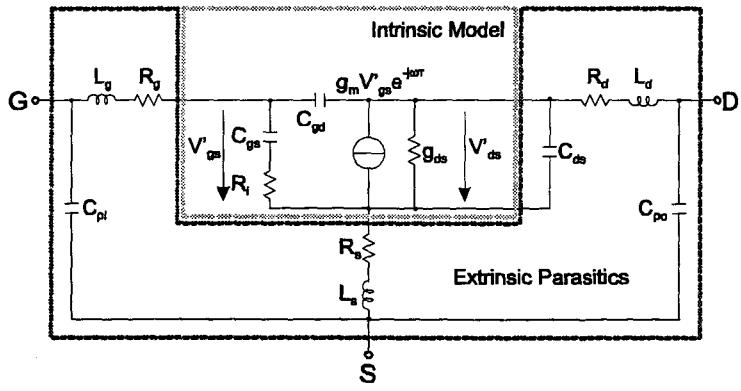


Figure 4.43: Schematic of the small-signal model.

The Drain Current Model The drain current of a MESFET or HEMT consists of a capacitive part flowing through the depletion region to the gate and the source and a resistive part flowing through the active channel to the source. This channel current can be modeled by a current source that is controlled by the gate voltage. It shows a strong frequency dependence (dispersion) at low frequencies (1 kHz .. 100 kHz). This is caused by the temperature dependence of the carrier mobility in GaAs (self heating) and by time constants connected to charging surface defects called traps. The shape

of the depletion region below the gate contact is modulated by these trapped charges. This parasitic effect changes the current through the transistor. Additionally, carrier trapping is temperature dependent. Nevertheless, at microwave frequencies the current is frequency independent. Therefore, it is not necessary for a small signal model to account for low frequency dispersion. The nonlinear behavior of a transistor under large signal excitation demodulates the RF signal and frequency components in the base band and DC (self biasing) are created. A correct simulation of the supply current of a microwave power amplifier is only possible when the low frequency dispersion of the drain current is exactly known. Test systems to characterize the low frequency behavior of a MESFET or HEMT are very sophisticated. They have to distinguish between dynamic thermal effects and trapping effects. Both have an influence on the drain current and both have similar time constants. One is influenced by changing the voltages at the transistor nodes (trapped charges), the other is influenced by altering the dissipated power or the ambient temperature (carrier mobility). Unfortunately, dissipated power and node voltages are closely connected. Pulsed or special large signal measurements can be a solution to this problem, but they are difficult to perform.

A usual compromise in modeling the low frequency behavior of a microwave MESFET or HEMT is to fix the DC and the RF characteristics, and to provide a smooth transition from low frequency to high frequency behavior. This does not account for the influence of temperature and trapped charges on the transistor's I/V characteristics. In a real device the bias point of an amplifier influences the whole I/V characteristic and, for large signals the simplified assumptions lead to some differences between simulation and measurement. On the other hand, small signal scattering parameters and the according DC results can be exactly reproduced by such a model for each bias point. This fact is the reason why this type of large signal model can be extracted from DC and small signal measurements only.

After the extrinsic elements are known, the first step of the extraction procedure is to fit an appropriate mathematical function to the measured DC characteristics. The fitting is done by changing the model function parameters to obtain a minimum of the root mean square error between the measured and the simulated DC-I/V characteristic. The COBRA model uses equation (4.11) to calculate the DC current $I_{ds,DC}$ from the intrinsic drain voltage V'_{ds} and from the intrinsic gate voltage V'_{gs}. The model parameters α, β, γ, μ, ξ, and ζ have to be greater or equal zero to ensure conservation of energy and to prevent a division by zero or other unphysical results. The parameters δ, λ and V_{T01} can have any value.

$$I_{ds,DC} = \beta \cdot V_{eff}^{\sqrt[\lambda]{1+\mu \cdot V'^2_{ds}+\xi \cdot V_{eff}}} \cdot \tanh\left(\alpha \cdot V'_{ds}\left(1+\zeta \cdot V_{eff}\right)\right) \tag{4.11}$$

$$V_{gst} = V'_{gs} - (1+\beta)^2 \cdot V_{TO1} + \gamma \cdot V'_{ds} \tag{4.12}$$

$$V_{eff} = \frac{1}{2} \cdot \left(V_{gst} + \sqrt{V_{gst}^2 + \delta^2}\right) \tag{4.13}$$

To get a smooth transition from this DC-I/V characteristic to the I/V behavior at microwave frequencies the voltage controlled current source I_{ds,g_m} and the voltage controlled conductance $g_{ds,corr}$ are connected with the large capacitance C_d in parallel to the voltage

controlled source $I_{ds,DC}$ (Fig. 4.42). At DC I_{ds,g_m} and $g_{ds,corr}$ have no influence on the drain current. For frequencies above some 100 kHz C_d can be neglected and the drain current is determined by all three circuit elements.

The I/V characteristics at microwave frequencies can be calculated from the small signal transconductance g_m and the drain conductance g_{ds} that were extracted from measured scattering parameters at different bias voltages. The integration of g_m over V'_{gs} leads to an I/V characteristic that is described by $I_{ds,g_m} + I_{ds,DC}$. I_{ds,g_m} is modeled similarly to equation (4.11) and can be found by a fitting algorithm like $I_{ds,DC}$. This new I/V characteristic represents correct g_m values for all bias points at DC and microwave frequencies, but the g_{ds} values are only correct for DC. The g_{ds} resulting from the $I_{ds,g_m} + I_{ds,DC}$ model becomes at microwave frequencies

$$g_{ds} = \frac{\partial I_{ds,DC}\left(V'_{gs}, V'_{ds}\right)}{\partial V'_{ds}} + \frac{\partial I_{ds,g_m}\left(V'_{gs}, V'_{ds}\right)}{\partial V'_{ds}} = g_{ds,DC} + g_{ds,g_m}. \tag{4.14}$$

It has to be corrected by the voltage controlled conductance $g_{ds,corr}$ to fit to the small signal measurement results. $g_{ds,corr}$ is described in the COBRA model by an equation that is similar to the first derivative of equation (4.11). The mean square error between the g_{ds} that is extracted from measurements and $g_{ds,DC} + g_{ds,g_m}$ that is calculated by the model has to be minimized to find the parameters of this equation.

The Gate Capacitance Model The ordinary way to describe a voltage controlled capacitor in a harmonic balance circuit simulator is to use a charge equation. The problem with this approach is that small signal models that are extracted from scattering parameter measurements provide bias dependent capacitance values. Trying to use a charge equation Q_{gs} that depends on two controlling voltages V'_{gs} and V'_{ds} to model the capacitance values of C_{gs} leads to the transcapacitance ($C_{T,gs}$) problem (Eq. 4.15).

$$I_{C_{gs}} = \frac{dQ_{gs}\left(V'_{gs}(t), V'_{ds}(t)\right)}{dt} = \frac{\partial Q_{gs}}{\partial V'_{gs}}\frac{dV'_{gs}}{dt} + \frac{\partial Q_{gs}}{\partial V'_{ds}}\frac{dV'_{ds}}{dt} = C_{gs}\frac{dV'_{gs}}{dt} + C_{T,gs}\frac{dV'_{ds}}{dt} \tag{4.15}$$

The current through the modeled capacitor $I_{C_{gs}}$ results not only in $C_{gs}\frac{dV'_{gs}}{dt}$ as it does in the small signal model, it also has an additional part $C_{T,gs}\frac{dV'_{ds}}{dt}$. Therefore, a direct conversion of small signal capacitance values to a charge based large signal model is not possible. The parameter optimization for the charge equations has to be done by fitting the scattering parameters of the whole gate charge model to the scattering parameters of the extracted gate capacitors.

A workaround to the transcapacitance problem is to model the controlled capacitor with two controlled sources and an inductor like in Fig. 4.44.

The left controlled source in Fig. 4.44 supplies the capacitive current

$$I_C = C\left(V'_{gs}(t), V'_{ds}(t)\right)\frac{dV_C(t)}{dt}. \tag{4.16}$$

The term $C\left(V'_{gs}(t), V'_{ds}(t)\right)$ is an analytical equation. The parameters of this equation have to be fitted for all measured bias voltages to the small signal values of this capacitor.

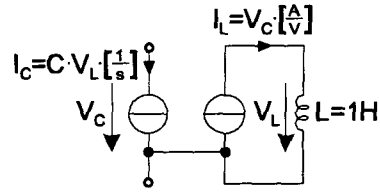


Figure 4.44: Implementation of a controlled capacitor avoiding the charge equation.

The derivative $\frac{dV_C(t)}{dt}$ is obtained from the auxiliary circuit when the second source supplies a current that has the same value as the voltage across the capacitor. The voltage across the inductor is then given by

$$\frac{dV_C(t)}{dt}\left[\frac{1}{s}\right] = V_L = L\frac{dI_L}{dt} = 1\,[H]\,\frac{dV_C \cdot \left[\frac{A}{V}\right]}{dt}. \tag{4.17}$$

Because the current is given by equation (4.16) no transcapacitance occurs and the given capacitance is correctly modeled.

The COBRA model uses this kind of capacitor implementation. Therefore, the model parameters C_{pgs}, C_{pgd}, C_{g1}, C_{g2}, C_{g3}, C_{g4}, pgs, pgd, VT0, V_{bi}, m, δ_c, and α_c can be directly extracted from the small signal results. The following equations are used to model the gate source capacitance C_{gs} and the gate drain capacitance C_{gd}.

$$\begin{aligned} C_{gs} &= C_{pgs} + C_{g1}\cdot\left(1-\frac{V'_{gs}}{V_{bi}}\right)^{-m} + C_{g2}\cdot\left(1+\tanh\left(\alpha_c\cdot\left(V'_{gs}-VT0\right)\right)\right)+\cdots \\ &\quad + C_{g3}\cdot V'_{ds}\cdot\left(1+\tanh\left(pgs\cdot\left(V'_{gs}-VT0\right)\right)\right) \end{aligned} \tag{4.18}$$

$$V_{gd1} = V'_{gs} - pgd\cdot V'_{ds} \tag{4.19}$$

$$\begin{aligned} C_{gd} &= C_{pgd} + C_{g1}\cdot\left(1-\frac{V_{gd1}}{V_{bi}}\right)^{-m} + C_{g2}\cdot\left(1+\tanh\left(\alpha_c\cdot\left(V_{gd1}-VT0\right)\right)\right)+\cdots \\ &\quad + C_{g4}\cdot V'_{ds}\cdot\frac{V'_{gs}-VT0}{\sqrt{V'^2_{ds}+\delta_c^2}} \end{aligned} \tag{4.20}$$

The parameter FC is used to avoid a division by zero in the term $C_{g1}\cdot\left(1-\frac{V_x}{V_{bi}}\right)^{-m}$.

For $V_{gs} > FC\cdot V_{bi}$ this term is replaced by $C_{g1}\cdot\frac{1-FC+m\cdot\left(\frac{V_x}{V_{bi}}-FC\right)}{(1-FC)^{m+1}}$.

COBRA Model of an EPA480CV Device

Table 4.7 lists the parameters for a COBRA model to fit the measurement results. Figures 4.45 and 4.46 display the performance of the drain current model compared to the measurement results. As can be seen, a very good agreement was achieved. Figures 4.47

and 4.48 show the strongly nonlinear behavior of the gate capacitances C_{gd} and C_{gs}, respectively. These capacitances have to be modeled accurately to achieve sound prediction of the nonlinear amplifier behavior.

Extrinsic Model Parameters								
R_g	R_s	R_d	L_g	L_s	L_d	C_{pi}	C_{po}	C_{ds}
0.84Ω	0.03Ω	0.06Ω	0.27nH	0.02nH	0.21nH	0.39pF	0.90pF	0.15pF
Drain Current Model – DC Current Source $I_{ds,DC}$								
α	β	γ	δ	λ	μ	V_{T01}	ξ	ζ
$4.69\frac{1}{V}$	1.502	0.0375	0.05V	1.397	$0.0\frac{1}{V^2}$	-0.38V	$0.04\frac{1}{V}$	$-0.89\frac{1}{V}$
Drain Current Model – RF Current Source I_{ds,g_m}								
α_1	β_1	γ_1	δ_1	λ_1	μ_1	V_{T01_1}	ξ_1	ζ_1
$4.25\frac{1}{V}$	0.088	0.0	0.1V	6.242	$0.0\frac{1}{V^2}$	-1.19V	$5.99\frac{1}{V}$	$0.0\frac{1}{V}$
Drain Current Model – $g_{ds,corr}$								
α_2	β_2	γ_2	δ_2	λ_2	μ_2	V_{T01_2}	ξ_2	ζ_2
$3.53\frac{1}{V}$	-0.028	0.0	0.1V	14.25	$0.0\frac{1}{V^2}$	-1.72V	$1.91\frac{1}{V}$	$0.0\frac{1}{V}$
Capacitance Model Parameters								
C_{g1}	C_{g2}	C_{g3}	C_{g4}	δ_c	V_{bi}	VT0	m	FC
1.52pF	1.78pF	6.06pF	$0.95\frac{pF}{V}$	14.59V	0.224V	-1.22V	0.344	0.112
C_{pgs}	C_{pgd}	pgs	pgd	α_c				
0.0pF	0.0pF	4.68	1.143	3.86				

Table 4.7: COBRA model parameters for EPA480CV.

COBRA Model of an EPA1200AV Device

To calculate the values of the equivalent circuit elements of the EPA1200AV device a smart interpolation algorithm was implemented into the parameter extraction software to suppress noise and small calibration errors in the measurement results (Fig. 4.49). For transistors with large gate widths (like the EPA1200AV) these inaccuracies would be a severe problem in parameter extraction.

Table 4.8 lists the parameters for a COBRA model to fit the measurement results. Figure 4.50 presents the performance of the drain current model compared to the measured data. It was not possible to model the current as accurately as for the EPA480CV due to a strong temperature dependence of the drain current in the knee region.

Figures 4.51 and 4.52 show the strongly nonlinear behavior of the gate capacitances C_{gd} and C_{gs}, respectively. Capacitance variations of several picofarad occur which will strongly influence the amplifier's matching and linearity.

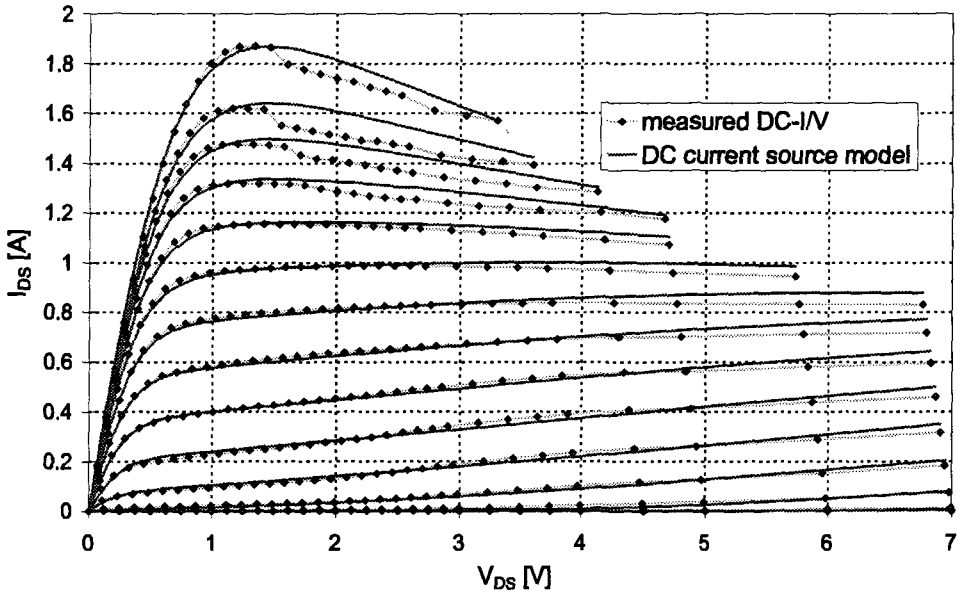


Figure 4.45: COBRA $I_{ds,DC}$ model and corresponding measurement results of an EPA480CV device.

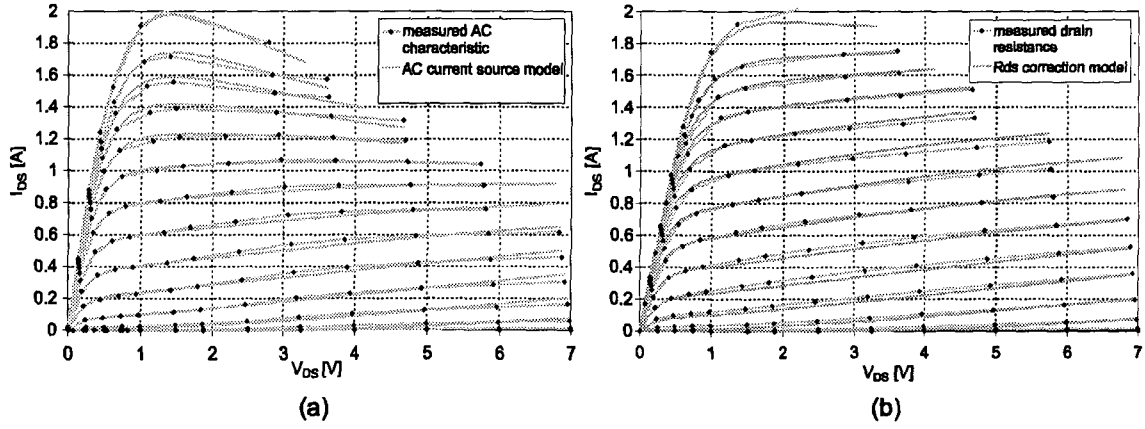


Figure 4.46: (a) AC current source model (I_{ds,g_m}) of an EPA480CV device; (b) g_{ds} correction model ($I_{ds,corr}$) of an EPA480CV device.

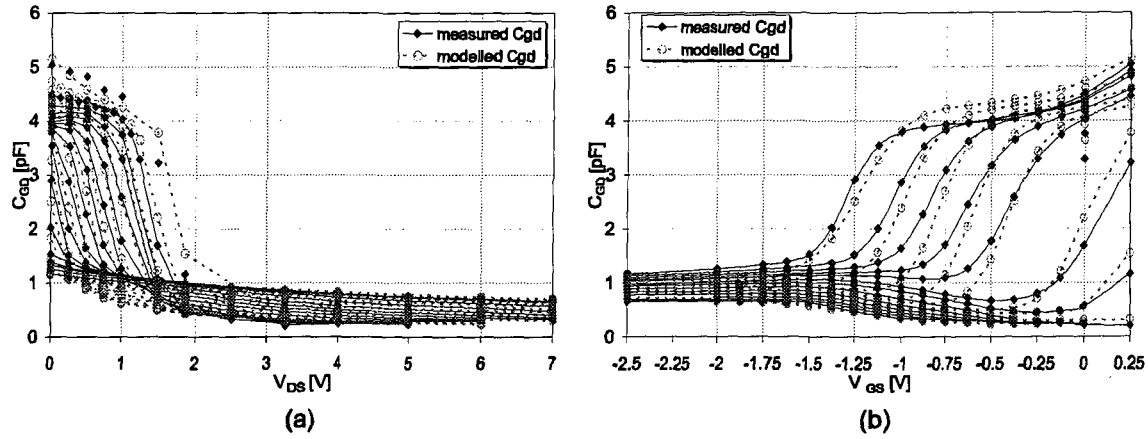


Figure 4.47: Gate-drain capacitance of an EPA480CV device. – (a) C_{gd} vs. V_{ds}; (b) C_{gd} vs. V_{gs}.

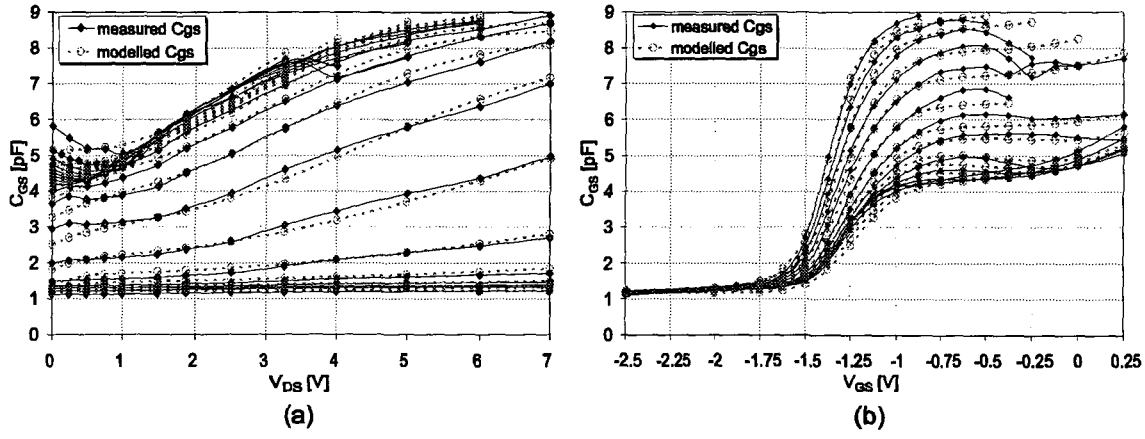


Figure 4.48: Gate-source capacitance of an EPA480CV device. – (a) C_{gs} vs. V_{ds}; (b) C_{gs} vs. V_{gs}.

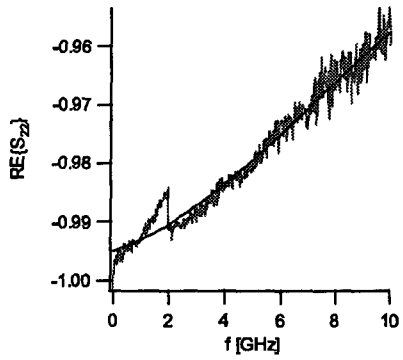


Figure 4.49: Smart interpolation (blue line) of noisy and inaccurate measurement results (ohmic region of the output characteristic).

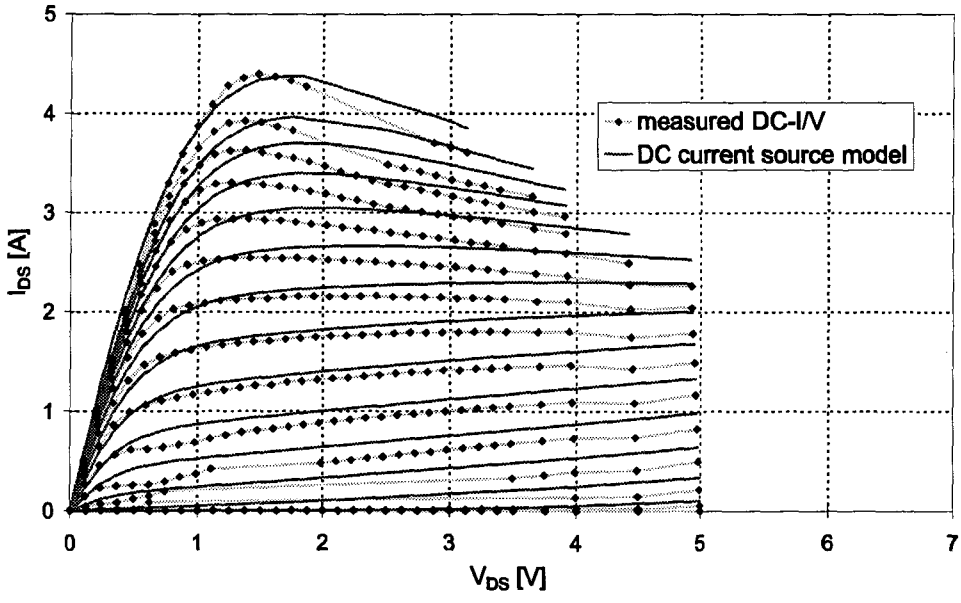


Figure 4.50: COBRA $I_{ds,DC}$ model and corresponding measurement results of a EPA1200AV device.

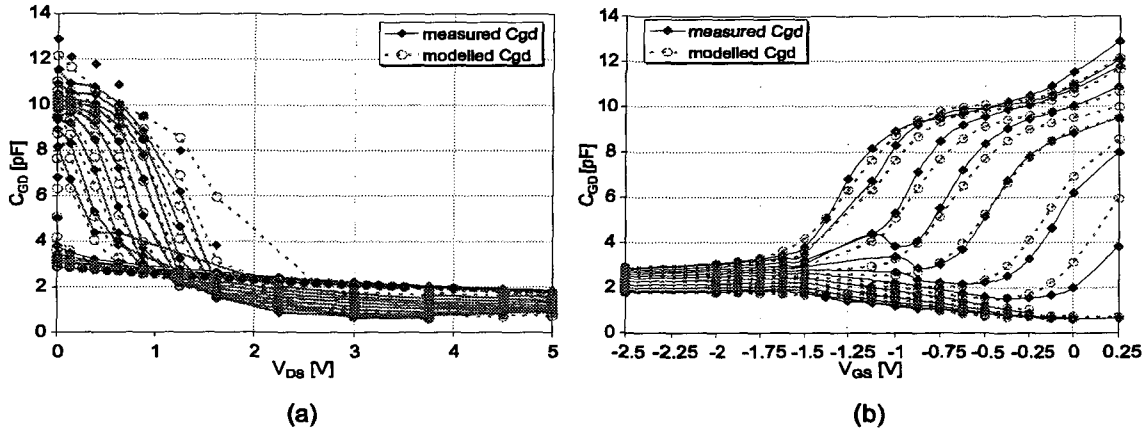


Figure 4.51: Gate-drain capacitance of an EPA1200AV device. – (a) C_{gd} vs. V_{ds}; (b) C_{gd} vs. V_{gs}.

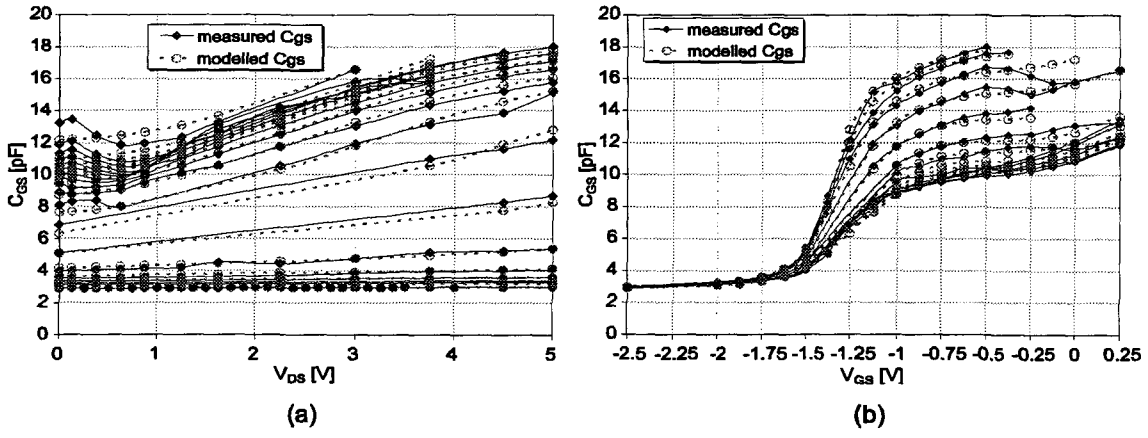


Figure 4.52: Gate-source capacitance of an EPA1200AV device. – (a) C_{gs} vs. V_{ds}; (b) C_{gs} vs. V_{gs}.

Extrinsic Model Parameters								
R_g	R_s	R_d	L_g	L_s	L_d	C_{pi}	C_{po}	C_{ds}
0.098Ω	0.0Ω	0.0Ω	0.13nH	0.02nH	0.14nH	0.84pF	0.78pF	1.8pF
Drain Current Model – DC Current Source $I_{ds,DC}$								
α	β	γ	δ	λ	μ	V_{T01}	ξ	ζ
$3.6\frac{1}{V}$	2.902	0.0294	0.05V	1.301	$0.0\frac{1}{V^2}$	-0.14V	$0.0\frac{1}{V}$	$-0.85\frac{1}{V}$
Drain Current Model – RF Current Source I_{ds,g_m}								
α_1	β_1	γ_1	δ_1	λ_1	μ_1	V_{T01_1}	ξ_1	ζ_1
$4.25\frac{1}{V}$	0.0	0.0	0.1V	6.242	$0.0\frac{1}{V^2}$	-1.19V	$5.99\frac{1}{V}$	$0.0\frac{1}{V}$
Drain Current Model – $g_{ds,corr}$								
α_2	β_2	γ_2	δ_2	λ_2	μ_2	V_{T01_2}	ξ_2	ζ_2
$3.53\frac{1}{V}$	0.0	0.0	0.1V	14.25	$0.0\frac{1}{V^2}$	-1.72V	$1.91\frac{1}{V}$	$0.0\frac{1}{V}$
Capacitance Model Parameters								
C_{g1}	C_{g2}	C_{g3}	C_{g4}	δ_c	V_{bi}	VT0	m	FC
4.41pF	3.78pF	13.3pF	$1.66\frac{pF}{V}$	14.69V	0.542V	-1.21V	0.592	0.046
C_{pgs}	C_{pgd}	pgs	pgd	α_c				
0.0pF	0.0pF	5.26	0.93	2.94				

Table 4.8: COBRA model parameters for EPA1200AV.

4.4.6 Model Verification

Small-Signal Evaluation of the COBRA model for an EPA480CV

All scattering parameters (Fig. 4.53, 4.54, and 4.55) are correctly modeled for a wide bias range with the COBRA model. Especially the ohmic region (blue traces), class A or AB (red traces) and the pinch-off region (green traces) show no remarkable difference between the modeled and the measured scattering parameters. Due to the correct modeling of g_{ds} and C_{gd}, S_{22} is correct for all bias voltages.

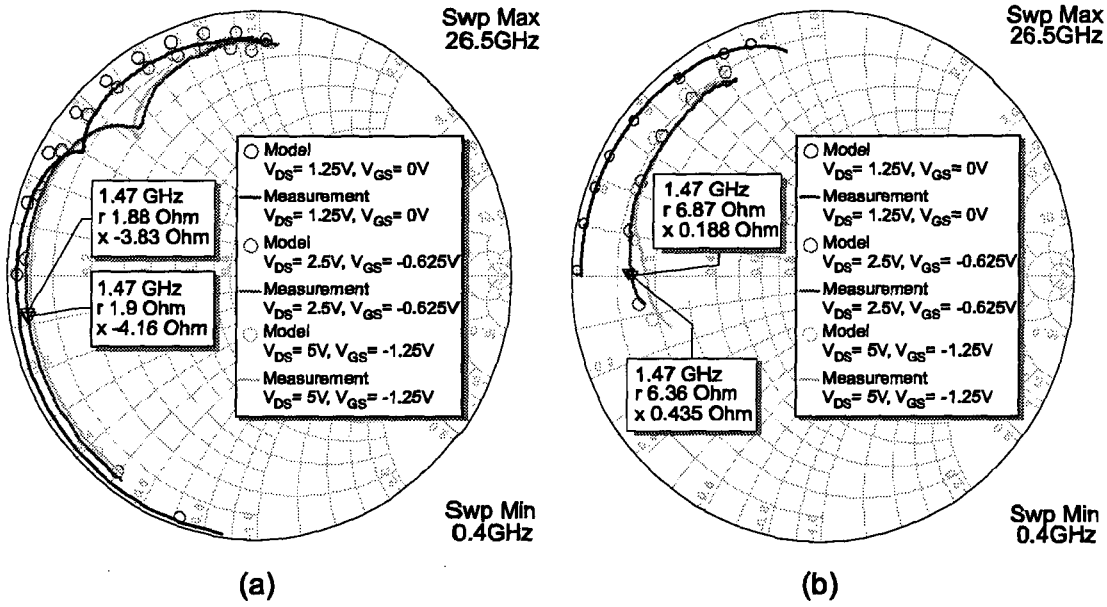


Figure 4.53: Scattering parameters of an EPA480CV device and small-signal simulation results of the COBRA model for different bias points. – (a) S_{11}; (b) S_{22}.

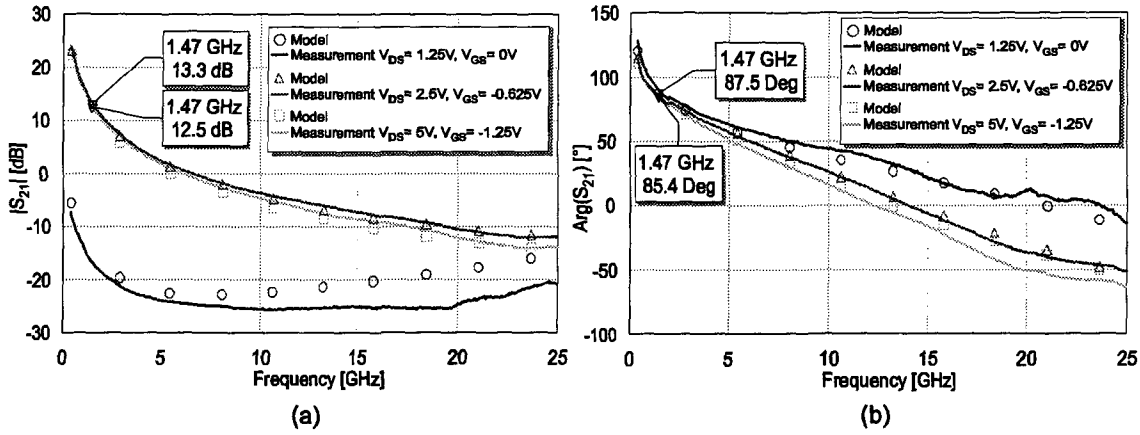


Figure 4.54: Scattering parameters of an EPA480CV device and small-signal simulation results of the COBRA model for different bias points. – (a) $|S_{21}|$; (b) Arg$\{S_{21}\}$.

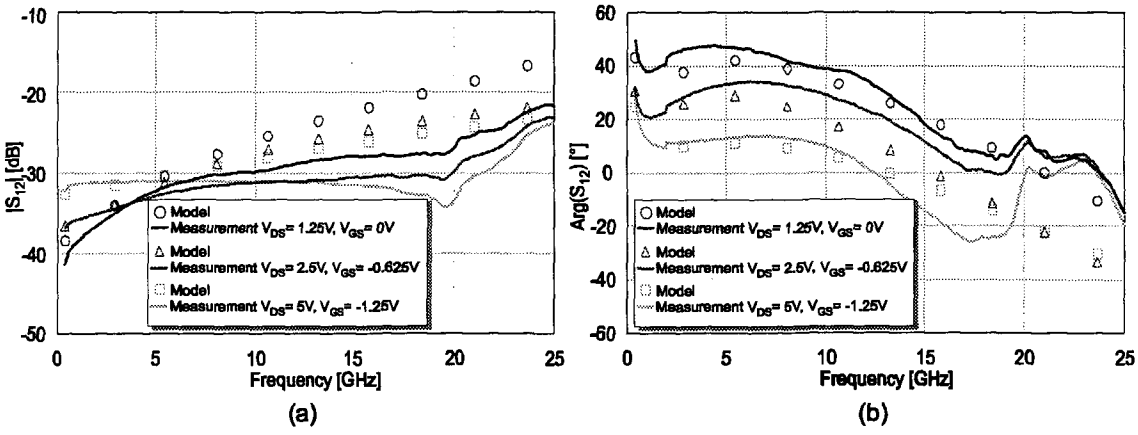


Figure 4.55: Scattering parameters of an EPA480CV device and small-signal simulation results of the COBRA model for different bias points. – (a) $|S_{12}|$; (b) Arg$\{S_{12}\}$.

Small-Signal Evaluation of the COBRA model for an EPA1200AV

Figures 4.56, 4.57, and 4.58 show a comparison of the measured to the simulated results for an EPA1200AV device. The traces show the results obtained for bias points in the ohmic region, class A or AB and the pinch-off region. The graphs show that the performance of the COBRA model of the EPA1200AV is quite similar to the performance of the COBRA model of the EPA480CV.

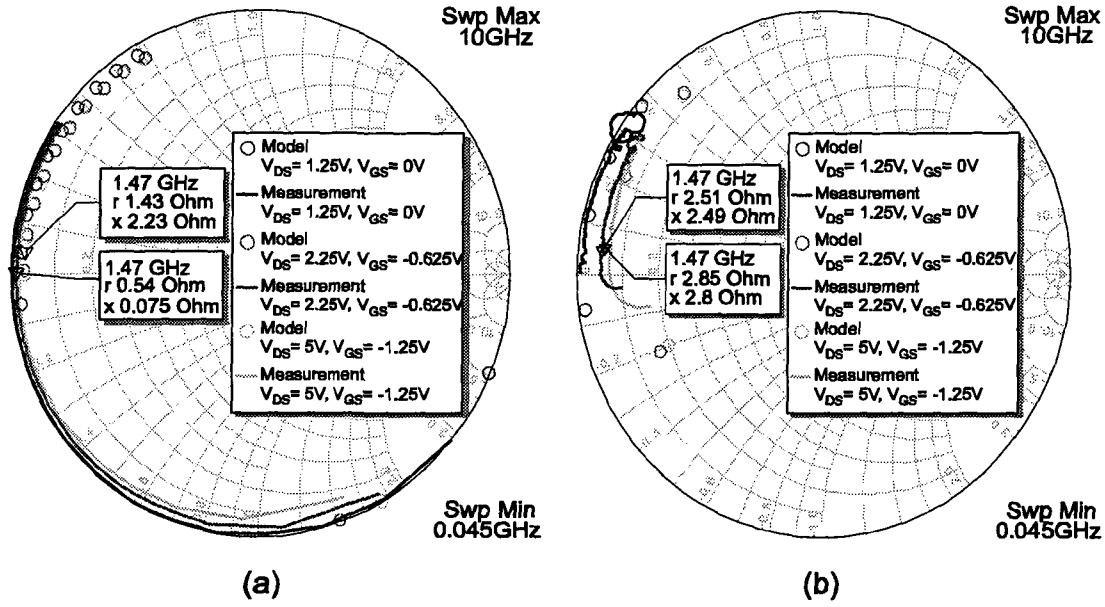


Figure 4.56: Scattering parameters of an EPA1200AV device and small-signal simulation results of the COBRA model for different bias points. – (a) S_{11}; (b) S_{22}.

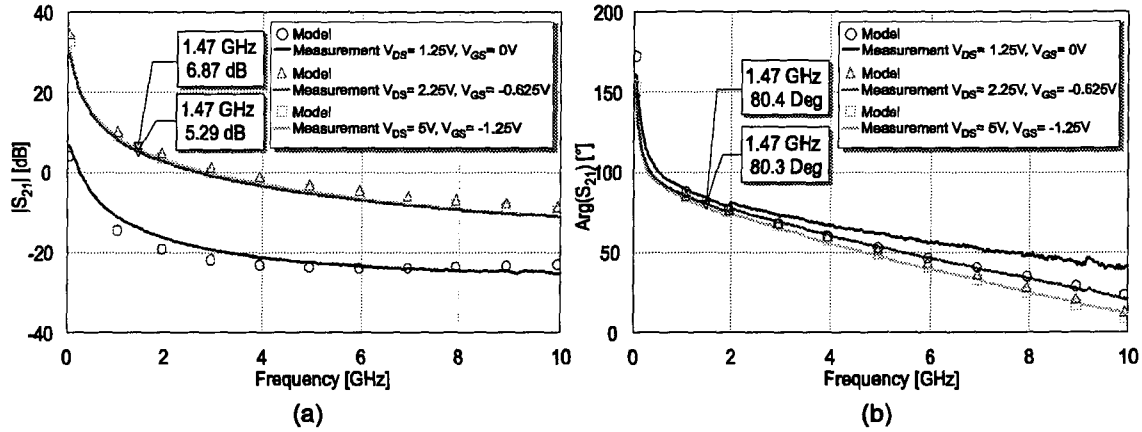


Figure 4.57: Scattering parameters of an EPA1200AV device and small-signal simulation results of the COBRA model for different bias points. – (a) $|S_{21}|$; (b) $\text{Arg}\{S_{21}\}$.

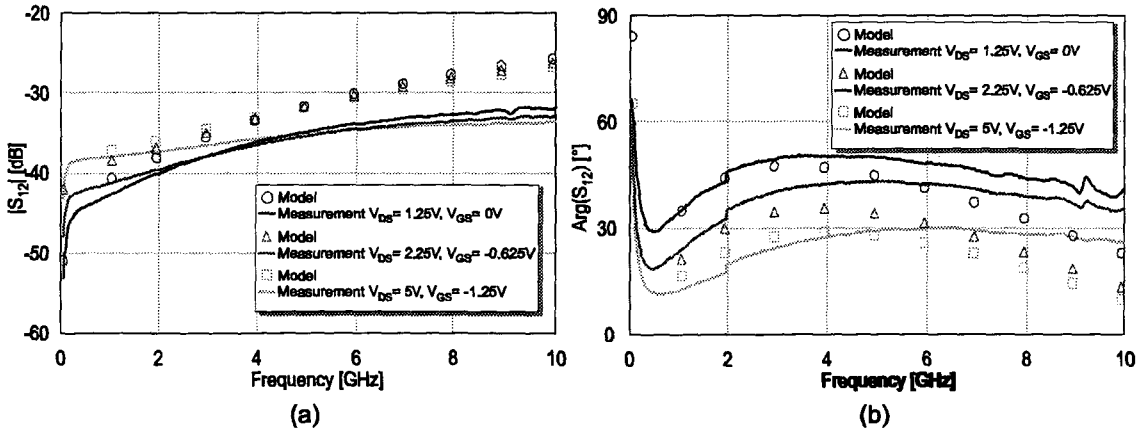


Figure 4.58: Scattering parameters of an EPA1200AV device and small-signal simulation results of the COBRA model for different bias points. – (a) $|S_{12}|$; (b) $\text{Arg}\{S_{12}\}$.

Test Amplifier Design

For large signal evaluation of the COBRA model for the EPA480CV a class A amplifier with distributed matching was chosen. Class A amplifiers can be designed with a minimum of components. This reduces the amount of contributors to the overall uncertainty. A distributed microstrip element matching at the input and output was chosen because the behavior of those elements is very well predicted by the simulator and there is almost no manufacturing tolerance as compared with lumped elements.

Since the larger device, EPA1200AV, is based on the EPA480CV transistor and the model performance is comparable it was assumed that the large-signal performance will be comparable as well, and, therefore, no test amplifier was built for the EPA1200AV.

The optimal source and load impedances for class A operation of the EPA480CV device are listed in Tab. 4.9. Due to the extrinsic components connected to the transistor the load impedance at the fundamental and at the harmonic frequencies seen by the intrinsic transistor is about 7 Ω.

Frequency	Source Impedance [Ω]	Load Impedance [Ω]
$f_0 = 1.472$ GHz	$2.41 + j7.19$	$6.86 - j1.46$
$2 \cdot f_0 = 2.944$ GHz	$0.75 - j8.54$	$6.80 - j2.93$
$3 \cdot f_0 = 4.416$ GHz	$0.75 - j8.54$	$6.21 - j4.65$

Table 4.9: Optimal source and load impedances for class A operation of EPA480CV.

Figure 4.59 shows the two simulated typical class A dynamic load lines (DLL) of the test amplifier at the intrinsic transistor kernel with distributed element matching. The purple line represents the DLL at the 1 dB compression point. At both ends of this DLL voltage clipping occurs which compresses the output power. The green line illustrates the load line 10 dB backed-off the compression point. Table 4.10 lists simulated data for single-tone excitation at the 1 dB compression point and at 3 dB and 10 dB in back-off.

Frequency	P_{IN}	P_{OUT}	Gain	PAE	V_{DD}	I_{DD}	V_{GG}
1.472 GHz	2 dBm	25.4 dBm	23.4 dB	8.2 %	6 V	705 mA	-0.8 V
1.472 GHz	9 dBm	33.0 dBm	24.0 dB	43.4 %	6 V	768 mA	-0.8 V
1.472 GHz	12 dBm	33.8 dBm	21.8 dB	48.5 %	6 V	823 mA	-0.8 V

Table 4.10: Simulated single-tone parameters of the class A test amplifier.

Figure 4.60 plots the stability circles for the input and output of the transistor and the matching impedances for the bias point chosen. As can be seen the matching impedances are outside the circles. Therefore, the amplifier is predicted to be stable. However, since the input stability circle for the fundamental frequency and the according source impedance are close to each other oscillation may occur.

Figure 4.61 shows the schematic of the amplifier. As explained above the matching at the input and output of the active device was performed with distributed line elements. Due to the small source impedance values at the input an additional lumped capacitor

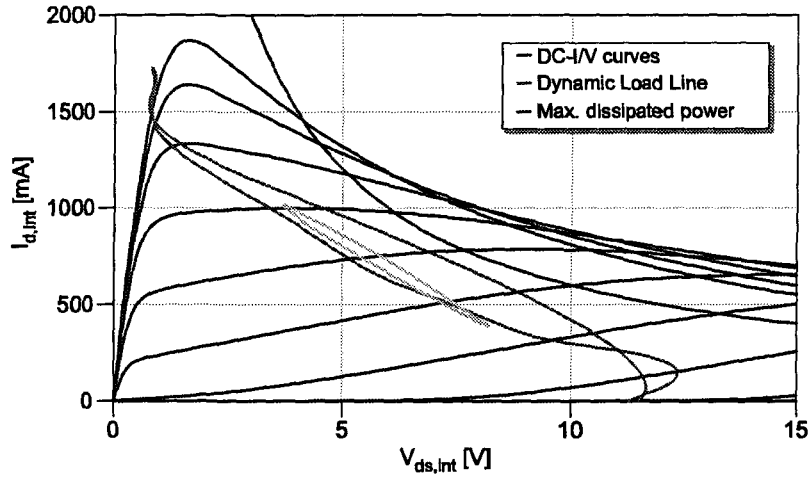


Figure 4.59: Simulated dynamic load lines of the class A test amplifier at f_0 = 1.472 GHz, V_{GG} = -0.8 V, V_{DD} = 6 V. (purple line) $P_{OUT,1dB}$ = 33.8 dBm, I_{DD} = 805 mA; (green line) P_{OUT} = 25.4 dBm, I_{DD} = 705 mA;

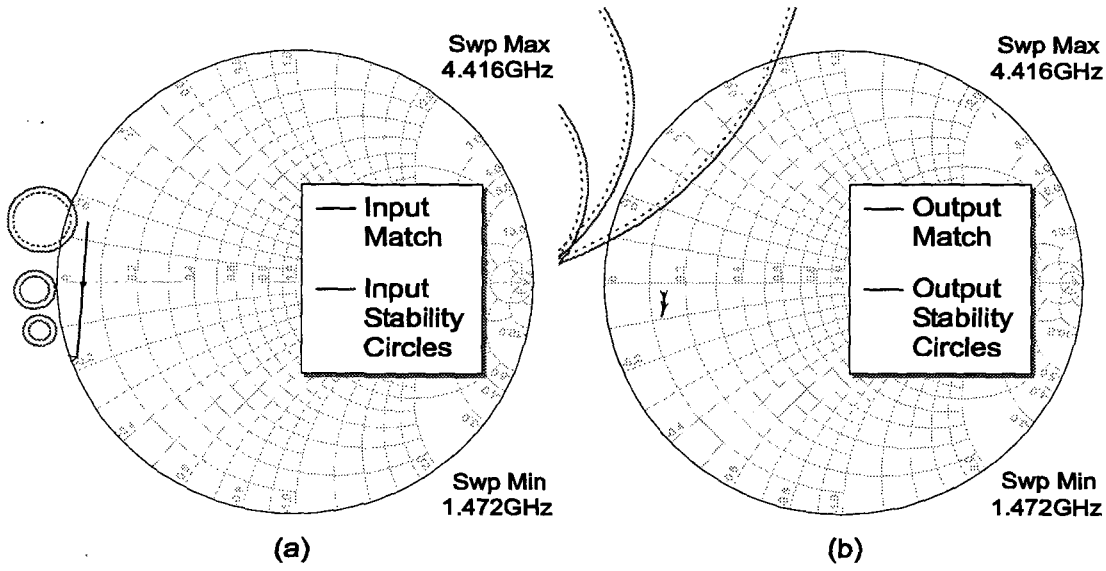


Figure 4.60: Stability circles for class A operation and ideal matching impedances. – (a) input stability; (b) output stability.

of 2.2 pF to ground was used for final input matching. Figure 4.62 depicts the layout in original size and a photograph of the assembled test amplifier.

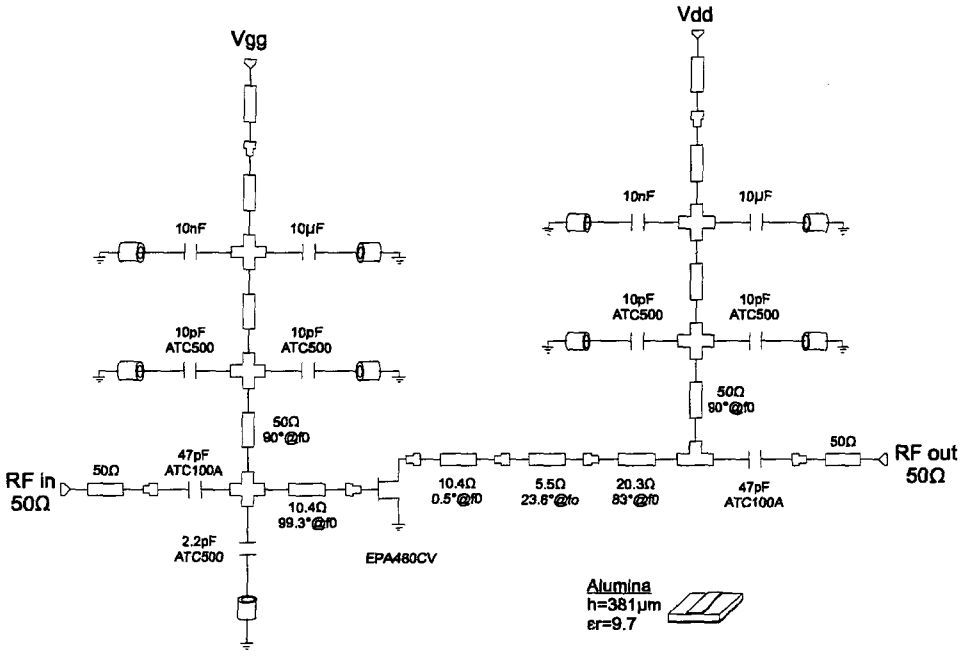
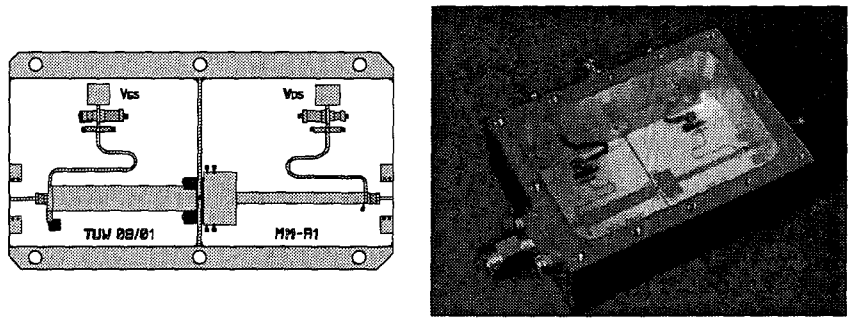


Figure 4.61: Schematic of the test amplifier.



(a) (b)

Figure 4.62: Test amplifier layout. – (a) original layout 24.5 x 52 mm; (b) photograph of final amplifier.

Figure 4.63 compares the measurement results with the simulation results for single-tone excitation versus input power. For small-signal excitation a good agreement of the measured to the simulated results can be seen. For a larger input signal gain and as a consequence output power and efficiency are predicted larger than measured. This effect is mainly influenced by self-biasing. Self-biasing is known as an effect where the bias point is varied due to large-signal excitation. Figure 4.64 displays the drain and gate DC

current versus input power. As can be seen the measured drain current doesn't increase with increasing input power, in fact it starts to decrease. This effect cannot be caused by self-heating since the current's temperature dependency at the chosen bias point is almost zero (Fig. 4.34). This self-biasing effect cannot be modeled by the COBRA model and, therefore, has to be taken additionally into account when simulating an amplifier.

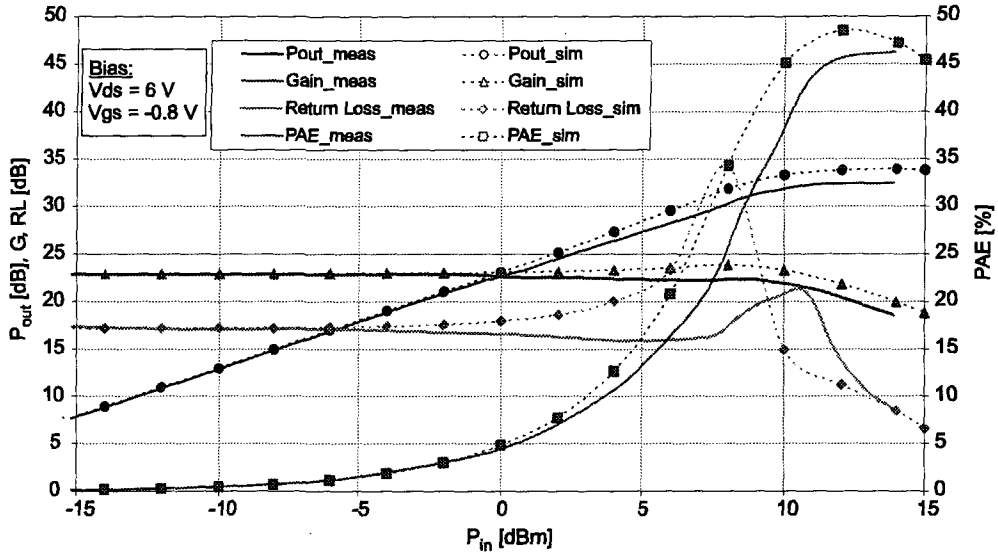


Figure 4.63: Single-tone power sweep of class A test amplifier at f_0 = 1.472 GHz, V_{GG} = -0.8 V, V_{DD} = 6 V.

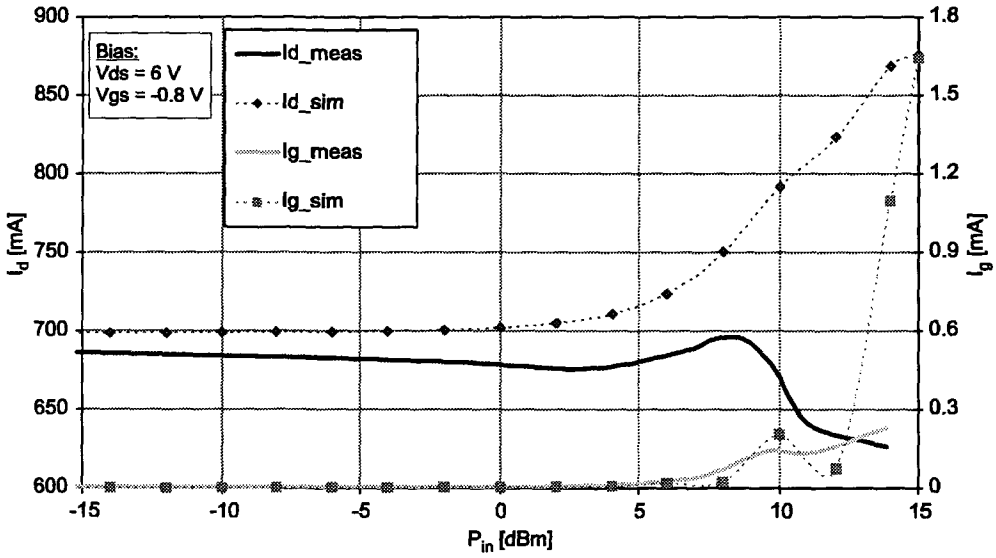


Figure 4.64: Single-tone current power sweep of class A test amplifier at f_0 = 1.472 GHz, V_{GG} = -0.8 V, V_{DD} = 6 V.

Figures 4.65 and 4.66 represent the comparison of measured and simulated results for a two-tone excitation. Also for two-tone excitation the device suffers of self-biasing. Nevertheless, prediction of intermodulation is reasonably good.

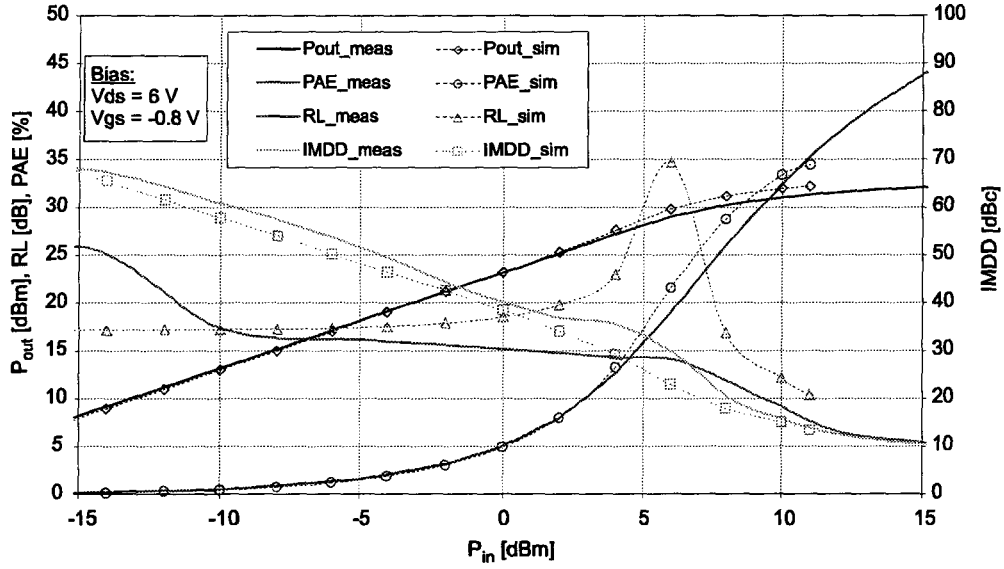


Figure 4.65: Two-tone power sweep of class A test amplifier at f_0 = 1.472 GHz, Δf = 1 MHz, V_{GG} = -0.8 V, V_{DD} = 6 V.

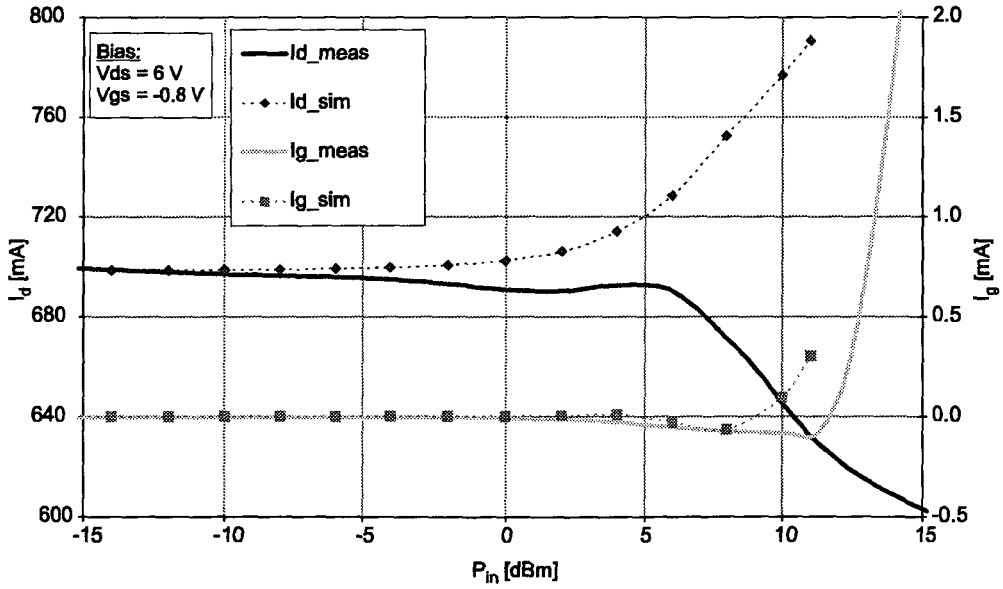


Figure 4.66: Two-tone current power sweep of class A test amplifier at f_0 = 1.472 GHz, Δf = 1 MHz, V_{GG} = -0.8 V, V_{DD} = 6 V.

4.5 Conclusion

In this chapter the selection, characterization, and modeling of active and passive devices were discussed.

Since there was no experience with thin film technology at the Institute the thin film process of the selected foundry was evaluated and verified. The geometrical accuracy of the conductors was found to be within the specifications but for integrated resistors the manufactured sheet resistance value is significantly out of specification. Thin film resistors manufactured with this process may only be used if an accurate value is not necessary. Otherwise the resistors have to be laser trimmed. Investigations on interdigital capacitors showed that due to limited line dimensions the parasitic capacitances to ground are in the same range as the desired capacity which limits the usability. Thin film spiral inductors can be manufactured in a wide range with high Q-factors. Therefore, a scaleable model of thin film spiral inductors was developed that eases accurate amplifier circuit design clearly.

Since substrate properties and mounting technique influence the behavior of the lumped components significantly all selected components were characterized and modeled. For design convenience scaleable models were developed, too.

To get an excellent prediction of harmonic generation and intermodulation distortion the COBRA model [75] was fitted to DC and small-signal RF characterization results of the selected active devices. The simulation results were compared with the measurements and fit very well to the DC and small-signal characterization results. For a practical large-signal test a class A amplifier was designed and measurements were compared with the predicted results. At higher input power level a self-biasing effect occured which is not predicted by the model. Thus, the predicted gain and output power is too high as compared with measurements. DC measurements at various temperatures were performed to check for self-heating. It was found that self-heating cannot be the reason for the self-biasing in the chosen bias point. The self-biasing effect cannot be modeled with the chosen computer model. This has to be taken into account when designing an amplifier. Linearity prediction was verified with a two-tone measurement of the test amplifier and was found to be very good. Unfortunately, the harmonic balance simulation engine hardly converges for two-tone simulations which makes it hard to perform extensive linearity investigations.

Chapter 5

Power Amplifier Realization

This chapter comprises all steps necessary for sucessful amplifier realization and presents the final measurement of the assembled and tuned amplifier.

5.1 Basic Considerations

As described in Chapter 3.8.1 a balanced amplifier design utilizing two class F amplifiers with additional 2^{nd} harmonic input termination was finally chosen. The main advantages of this architecture are:

- Balanced design:
  - Minimized return loss
  - Improved stability
  - Automatic coupler compensation mechanism
  - Suitable to meet the requirements in terms of output power
- Class F amplifier:
  - High efficiency
  - Good linearity at optimized bias point
- 2^{nd} harmonic input termination:
  - Linearity improvement
  - Efficiency improvement

To facilitate easy measurements of all modules the common 50 Ω impedance level was chosen at all module RF ports.

After selection of the active device the key parameters power added efficiency and intermodulation distortion depend in principle on the selection of bias and of the reflection coefficient at the fundamental and harmonics at the input and output.

Proper termination is restricted in this design to the fundamental and 2nd harmonic at the input of the active device and to the fundamental, 2nd, and 3rd harmonic at the output of the transistor, respectively. The proper termination of higher harmonics is undesireable as negligible benefits are outweighed by enhanced complexity.

To minimize intermodulation distortion by the use of the so called "sweet spots" the optimum output-matching network should present a very low impedance to the baseband and 2nd harmonic, respectively [6].

5.1.1 Linearity Aspects

Shoulder distance was chosen by the industry partner as a measure of linearity for the thin film amplifier module. Shoulder distance (SD) (Fig. 3.7) is defined as the ratio of the maximum power level within the DAB band and the power level at 970 kHz distance from the center frequency, measured with a resolution bandwidth (RBW) of 4 kHz [2]. This parameter is very similar to the multitone intermodulation ratio (M-IMD) that was defined in 3.2.5. The only difference is that the frequency offset for shoulder distance measurement is higher as for M-IMD measurement. Therefore, shoulder distance is generally larger than the according M-IMD.

Two-tone intermodulation distortion can be extracted in an easy way from CAD tools while designing an amplifier. Therefore, the dependency of shoulder distance on IMDD is of great interest. As shoulder distance is somewhat larger than M-IMD, M-IMD will be a good lower limit for shoulder distance. With equations (3.14) and (3.16) the offset for ACPR and M-IMD for a DAB mode II signal with $n = 384$ carriers can be calculated to

$$\begin{aligned} -ACPR &= IMDD_{2-tone} - 1.22\ dB \\ M\text{-}IMD &= IMDD_{2-tone} - 5.98\ dB. \end{aligned} \tag{5.1}$$

To prove this calculations measurements of IMDD and shoulder distance for multiple bias points at different input power levels were performed. As a result it was found that there is a roughly linear correlation of IMDD and shoulder distance (Fig. 5.1) and a good linear correlation of ACPR and shoulder distance. ACPR and shoulder distance can be approximated by

$$\begin{aligned} -ACPR &= IMDD_{2-tone} - 1.0\ dB \\ SD &= IMDD_{2-tone} - 5.5\ dB. \end{aligned} \tag{5.2}$$

The results obtained match very well with the calculated results. Therefore, two-tone IMDD simulation results were used for amplifier's linearity prediction since multi-carrier signal exciation was not supported by state-of-the-art simulation software when the amplifier was designed. Unfortunately, the implemented computer model of the active device suffers from very bad convergence. So it was hard to run two-tone simulations for high input power levels.

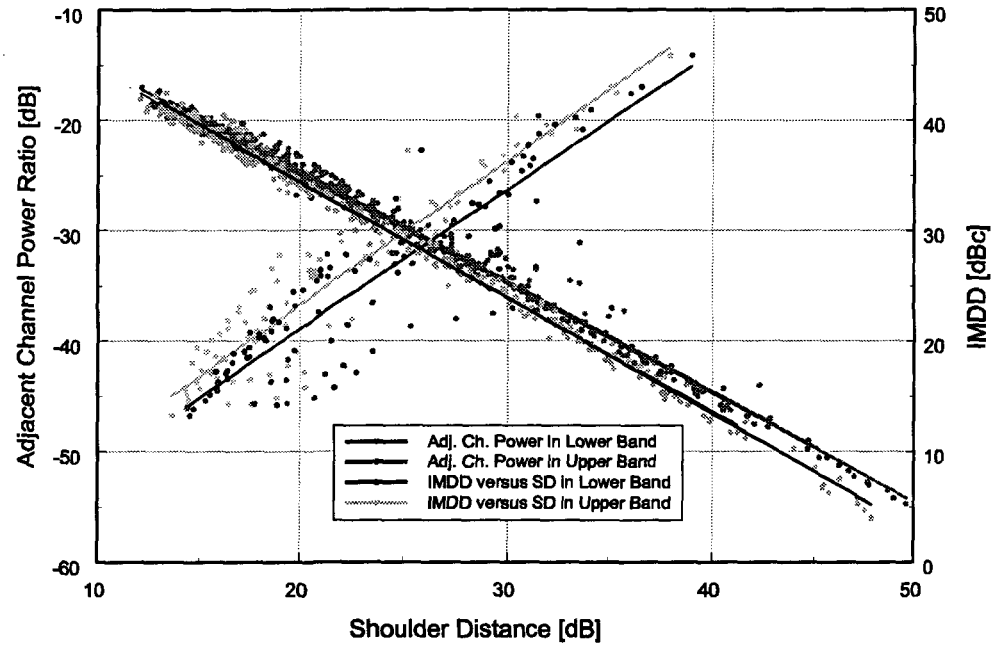


Figure 5.1: Measured relation of IMDD, shoulder distance and ACPR of an hHCA amplifier [80] for different bias and input power level conditions.

5.2 Single Stage Class-F Amplifier

5.2.1 Simulation Setup

As mentioned above the key parameters power added efficiency and intermodulation distortion depend in principle on the selection of bias and on the selection of the reflection coefficients at the fundamental and harmonics at input and output. Since the reflection coefficients depend on the selected bias an iterative design process is inevitable. To determine the optimum reflection coefficients ideal matching networks at the input and output were connected for simulation (Fig. 5.2). To separate the fundamental and harmonics, ideal filters models were developed. These filters are bandpass filters with adjustable start frequency, stop frequency, and stopband attentuation, respectively.

For tuning the fundamentals, phase shifters and transformers were utilized. Active loops (Fig. 5.3) were used to tune the harmonics and baseband, respectively. With such active loops the magnitude and angle of the desired termination load can be adjusted separately and independently. Proper termination is performed in this setup up to the 3^{rd} harmonic at the input and output. For the actual design the 3^{rd} harmonic termination at the input was not implemented since its effect is negligible.

Due to the iterative procedure the process of optimum reflection coefficients determination is a very time consuming task, but former design tasks showed that this approach is very practical. After a primary bias selection to enable pulse forming (class AB, near B) the output reflection coefficient at the fundamental is determined at a moderate power level just below the expected compression point. A good starting value for class F operation is

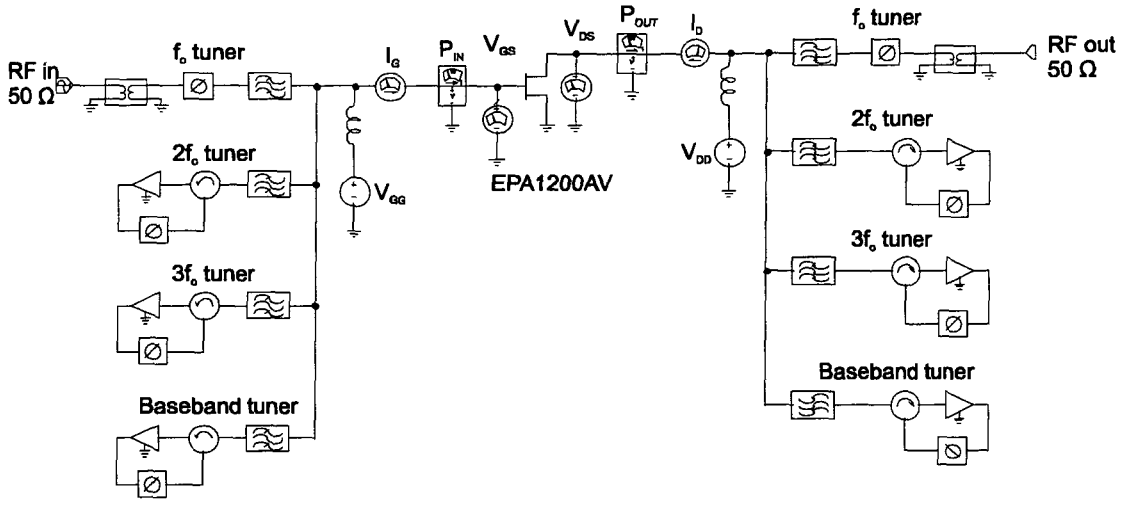


Figure 5.2: Simulation setup. Determination of reflection coefficients.

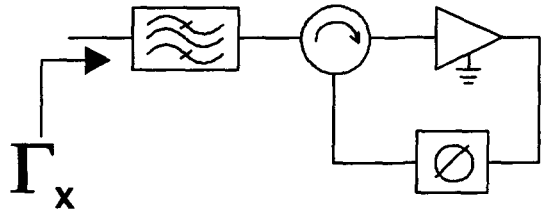


Figure 5.3: Ideal active tuner for independent adjustment of magnitude and phase.

the theoretical optimum

$$R_{L,opt} = \frac{4}{\pi} \cdot \frac{2\,(V_{DD} - V_K)}{I_{DSS}} = \frac{4}{\pi} \cdot \frac{2(6V - 1V)}{4A} = 3.18\ \Omega.$$

Next, the input reflection coefficient at the fundamental is adjusted to minimize input power mismatch. After iterative determination of the fundamental reflection coefficients the output class F network is introduced and optimized. The fundamental and harmonics at the output have to be retuned to maximize primarily gain and power added efficiency. Note that all these mentioned impedances have to appear at the intrinsic ports of the active device. Taking the extrinsic parasitics into consideration the impedances will be transformed to significantly different values. Once these coefficients are determined the 2^{nd} harmonic at the input is tuned to minimize intermodulation products. Then, after minor adjustments of the other reflection coefficients, a few iteration runs gave the final bias settings and reflection coefficients. With these settings, an input power sweep is performed to check for sufficient performance well beyond compression. After final adjustements, the required equivalent small signal reflection coefficients of the input and output matching circuit are determined and ready for realization. Figure 5.11 shows the resulting design parameters for a single power amplifier module. Note that the given values are the values

that have to be realized at the device's extrinsic ports.

5.2.2 Class-F Termination

Class F termination is well known to give high efficiency amplifiers. In this work not only efficiency but also achieving minimum 3rd order intermodulation distortion was of interest. To establish reliable amplifier operation it is of further interest that the maximum voltage peaks of the drain voltage are kept low to reduce the device stress to a minimum. Therefore, investigations on the dependency of power amplifier key parameters on the class F harmonic termination were performed. Figure 5.4 displays the simulation results showing the dependency of these key parameters on the intrinsic 2nd harmonic output termination angle ($\Gamma_{L,2f_0} = 1$) for single-tone and two-tone excitation while the 3rd harmonic signal is terminated with an open circuit.

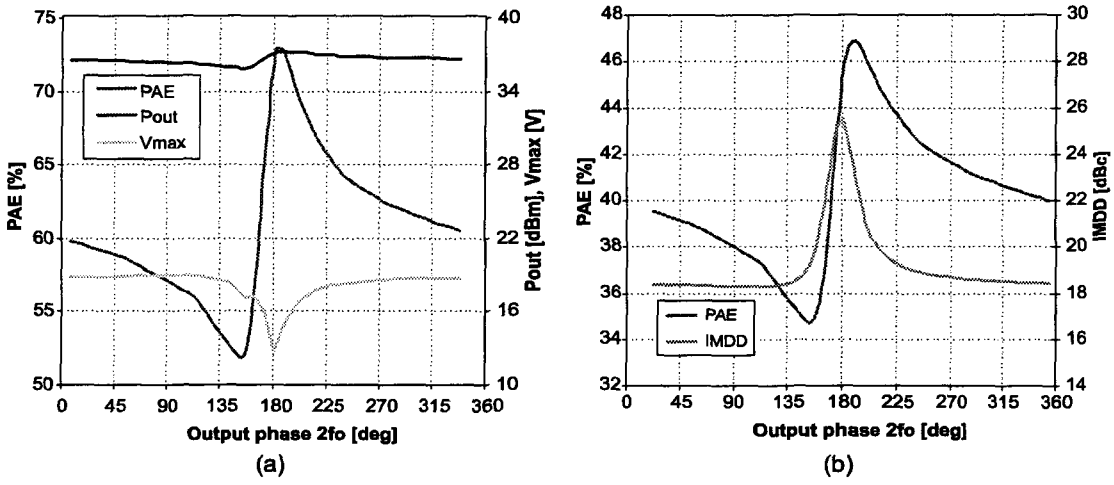


Figure 5.4: Dependency of power amplifier key parameters on intrinsic 2nd harmonic output termination angle. – (a) Single-tone excitation, $P_{IN} = 17dBm$; (b) two-tone excitation, $P_{IN} = 12dBm$, $\Delta f = 1MHz$.

Analysis of these figures leads to the conclusion that optimum efficiency and maximum output power is not achieved by the selection of an angle of 180° (short circuit) for termination. The optimum angle for maximum power added efficiency and maximum output power was found to be 190°. With respect to linearity it can be clearly seen that termination with a short circuit (φ_{2f_0} =180°) will result in a maximum intermodulation distortion distance $IMDD$. Furthermore, best reliability can be achieved also with a short circuit termination since this termination results in a symmetrical rectangular drain source voltage waveform. Since the amplifier shall be used for a multi-carrier signal with high crest factor it was decided to terminate the 2nd harmonic signal with a short circuit (φ_{2f_0} =180°) to optimize $IMDD$. The reduction of power added efficiency is here only 2 % while gaining 1.5 dB in $IMDD$ as compared to termination for optimum efficiency.

As it is impressively shown in Fig. 5.4, proper termination of the 2nd harmonic signal has a strong influence on the key parameters of a microwave power amplifier. Beside

the fundamental match it is the major parameter to optimize an amplifier circuit. For this amplifier the power added efficiency can be varied in a range from 52 % to 73 % at compression while the intermodulation distortion distance can be varied in a range from 18.5 dB to 25.5 dB in back-off condition. Also a reduction from 19 V to 13 V of the maximum drain source voltage peaks can be achieved resulting in a more reliable amplifier. However, since optimum values are only achieved in a narrow angle range the termination circuit has to be designed carefully to benefit from proper termination.

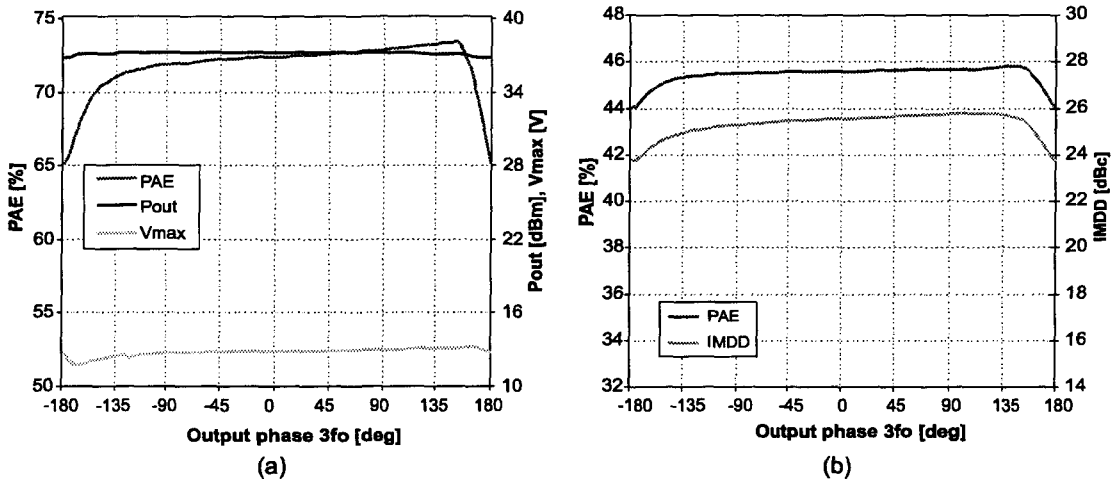


Figure 5.5: Dependency of power amplifier key parameters on intrinsic 3rd harmonic output termination angle. – (a) Single-tone excitation, $P_{IN} = 17dBm$; (b) two-tone excitation, $P_{IN} = 12dBm$, $\Delta f = 1MHz$.

Figure 5.5 shows the dependency of the key parameters on the intrinsic 3rd harmonic output termination angle ($\Gamma_{L,3f_0} = 1$) for single-tone and two-tone excitation while the 2nd harmonic signal is terminated with a short circuit. Maximum output power is achieved at an angle of 0°, the theoretical optimum. However, optimum values for both, efficiency and intermodulation distortion are achieved in an angle range of 90 to 135°. For this amplifier the power added efficiency can be varied in a range of 65 to 73.5 % at compression while the intermodulation distortion distance can be varied in a range of 24 to 25.5 dB in back-off condition. Maximum drain source voltage peaks can be reduced by 1 V but at an undesireable 3rd harmonic termination angle. Finally an angle of 100° was chosen to be the optimum.

5.2.3 2nd Harmonic Input Termination

Due to the strong second order nonlinear behavior of the gate-source capacitance C_{gs} (see Fig. 5.6) harmonic frequencies are generated at the transistor's input. To understand the IM generating mechanisms at the devices input a simplified model (see Fig. 5.6) can be considered in which the output current behavior can be described by a power series

$$I_{DS} = g_m \cdot V_{GS} + g_{m,2} \cdot V_{GS}^2 + g_{m,3} \cdot V_{GS}^3. \tag{5.3}$$

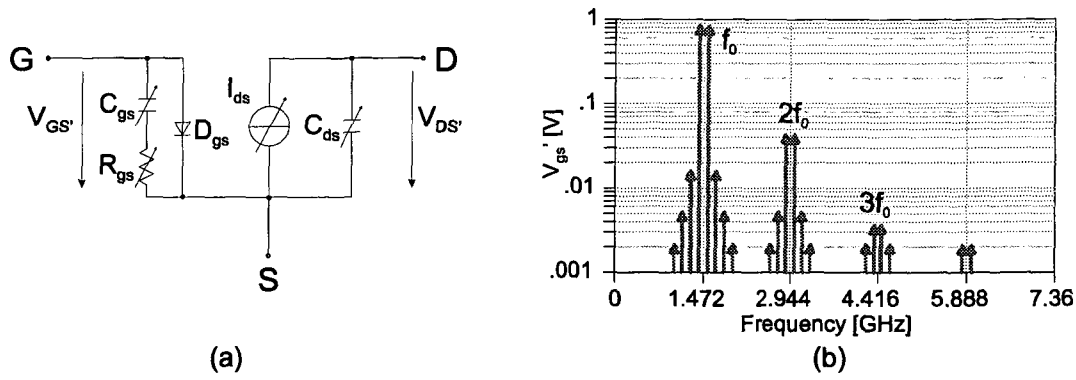


Figure 5.6: Influence of gate source capacitance C_{gs} non-linearity. – (a) Simplified device model; (b) gate source voltage V'_{GS} harmonic content.

The gate source capacitance can be described in a simplified form by

$$C_{gs} = C_{gs,0} \cdot \left(1 + \frac{V_{GS}}{V_{bi}}\right)^{-0.5} \tag{5.4}$$

where V_{bi} is the built in junction potential and $C_{gs,0}$ is the zero voltage gate source junction capacitance.

To take into account the 2nd order nonlinear behavior of C_{gs} a two tone gate source voltage can be represented by

$$V_{GS} = A_1 \cdot [\cos(\omega_1 t) + \cos(\omega_2 t)] + A_2 \cdot [\cos(2\omega_1 t) + \cos(2\omega_2 t)] \tag{5.5}$$

where A_1 is the amplitude of the external two-tone input signal and A_2 is the amplitude of the internally generated second harmonic component.

Substituting (5.5) into (5.3) the resulting intermodulation output signal is ([81], [82])

$$I_{DS,IM} = \left\{ \begin{array}{c} g_{m,2} \cdot A_1 A_2 + \\ g_{m,3} \cdot \left[\frac{3}{4} A_1^3 + \frac{3}{2} A_1 A_2^2\right] \end{array} \right\} \cdot \cos\left[(2\omega_2 - \omega_1) \cdot t\right] \tag{5.6}$$

while the fundamental output signal is

$$I_{DS,0} = \left\{ \begin{array}{c} g_m \cdot A_1 + g_{m,2} \cdot A_1 A_2 + \\ g_{m,3} \cdot \left[\frac{9}{4} A_1^3 + 3 A_1 A_2^2\right] \end{array} \right\} \cdot \cos(\omega_1 t) \,. \tag{5.7}$$

Since $g_{m,2}$ and $g_{m,3}$ usually are opposite in sign, the effect of the 2nd harmonic component at the input port ($g_{m,2} \cdot A_1 A_2$) is to reduce the overall intermodulation value. This observation has been also demonstrated in [42].

The influence of the angle of an intrinsic total reflection at the 2nd harmonic frequency on single-tone and two-tone simulation results, respectively, is shown in Fig. 5.7. With respect to power added efficiency and intermodulation distortion a similar behavior as for a sweep of termination angle at the 2nd harmonic at the drain can be recognized. Again it can be said that maximum efficiency will not occur at an angle of 180° but will optimize intermodulation distortion. Ouput power, however, is reduced exactly at an angle of 180°

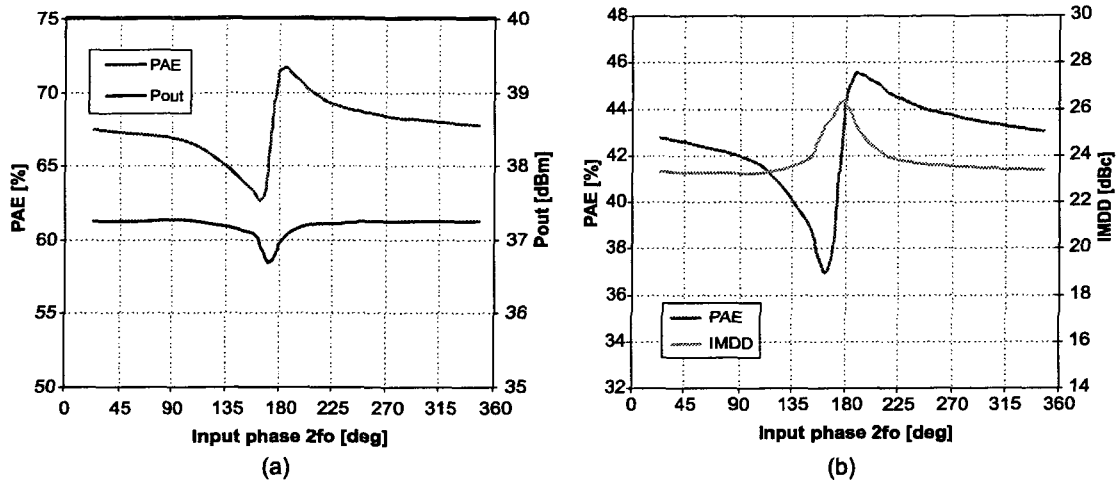


Figure 5.7: Dependency of power amplifier key parameters on intrinsic 2nd harmonic input termination angle. – (a) Single-tone excitation, $P_{IN} = 17dBm$; (b) two-tone excitation, $P_{IN} = 12dBm$, $\Delta f = 1MHz$.

by 0.5 dB. To still benefit of an improved efficiency and intermodulation distortion distance at almost no output power reduction $\varphi_{2f_0,in} = 190°$ was chosen.

5.2.4 Bias Selection

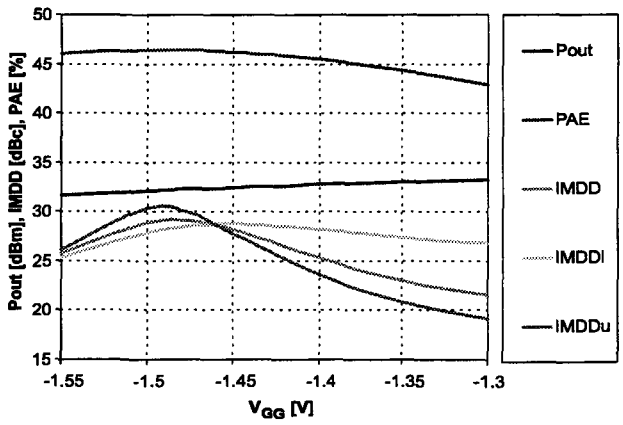


Figure 5.8: Dependency of amplifier key parameters on gate bias voltage V_{GG}, $P_{IN} = 12\ dBm$.

For proper bias selection a gate source bias voltage V_{GG} sweep simulation was performed to find the optimum bias voltage. Figure 5.8 displays the results for output power level, power added efficiency, and the overall intermodulation distortion distance. Furthermore, the upper and lower intermodulation distortion distance is presented to identify asymmetry. As can be seen the intermodulation performance is symmetric at a gate source bias voltage

of $V_{GG} = -1.46\ V$. This bias voltage is also close to the maximum of power added efficiency which has its maximum around $V_{GG} = -1.5\ V$. Output power level will decrease with more negative values but this is evident since the gate operation point is moving from class AB to class B and eventually to class C. The gate bias voltage finally chosen for the amplifier is $V_{GG} = -1.46\ V$ for symmetrical intermodulation performance.

5.2.5 Simulation Results

With the above determined values for fundamental and harmonic terminations and with the selected bias point a set of simulations was performed. The drain source voltage and current waveforms at compression are shown in Fig. 5.9a while the resulting dynamic load line is displayed in Fig. 5.9b. One can note the half sinusoidally shaped intrinsic current waveform and the rectangularly shaped intrinsic voltage waveforms as it is typical for class F amplifiers. Additionally the extrinsic waveforms are displayed to show the strong deformation of shape, especially for the drain source voltage, due to the transistor's parasitics.

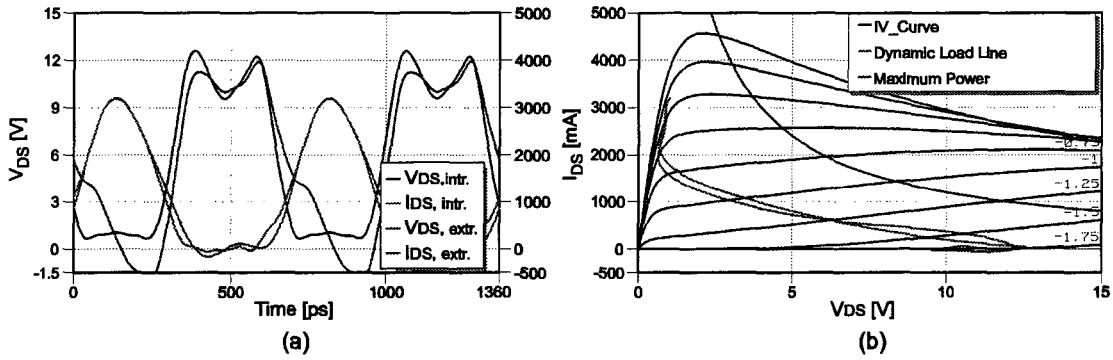


Figure 5.9: Drain voltage and current waveforms and dynamic load line of single stage amplifier ($P_{IN} = 17\ dBm$). - (a) V_{DS} and I_{DS} waveforms at the instrinsic and extrinsic device ports; (b) resulting dynamic load line.

Figure 5.10 demonstrates the simulated amplifier's behavior with respect to swept input power at single-tone and two-tone excitation. At single-tone excitation it is displayed that a power added efficiency beyond 70 % with an output compression of 37 dBm is possible. Due to the high gain the drain efficiency is 1.01·PAE. The resulting drain efficiency is very close to the theoretical maximum drain efficiency for 2nd and 3rd harmonic control of 81.65 % only reduced by the knee voltage factor $\varkappa = \frac{V_{DD}-V_K}{V_{DD}}$. For two-tone one can see that output compression and thus also maximum efficiency are reduced. The compression is decreased by some 3 dB as one can expect for a 100 % AM modulated output signal (two-tone). Further the expected shoulder distance SD is shown in Fig. 5.10b. At an input power level of $P_{IN} = 14\ dBm$ the requested shoulder distance of 20 dB and an efficiency of 50 % are expected at an output power level of $P_{OUT} = 34\ dBm$. For back-off condition the requested shoulder distance of 30 dB cannot be reached in simulation. The $IMDD$ value range for which this problem occurs is equal to the range where the transistor model for the EPA480CV estimated wrong values for the test amplifier presented in Chapter 4.4.6.

The intermodulation distortion distance displayed in Fig. 4.65 (two-tone simulation and measurement results of the test amplifier) was underestimated by 8 dB. Therefore, it is expected that measured $IMDD$ and, therefore, shoulder distance will be again better than simulated.

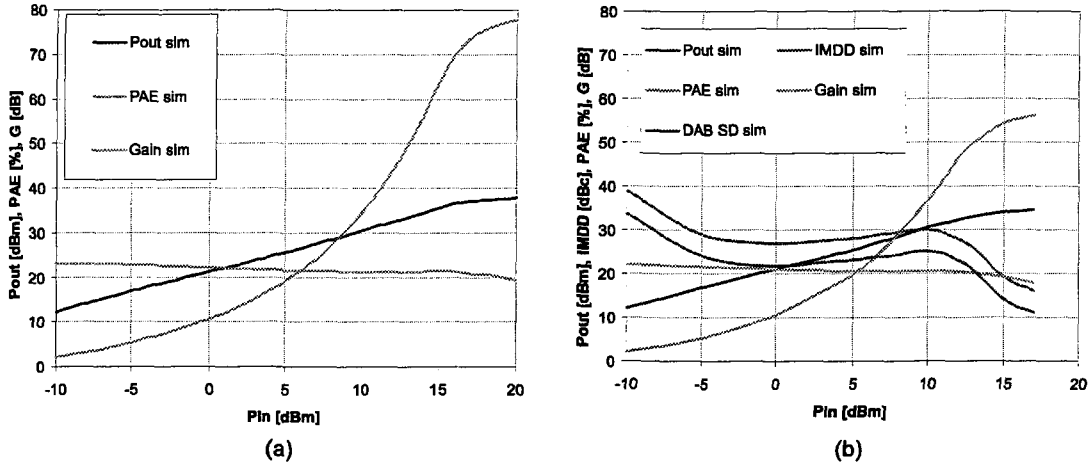


Figure 5.10: Single stage power amplifier simulated power sweep ($V_{DD} = 6V$, $V_{GG} = -1.46V$). – (a) Single-tone excitation; (b) two-tone excitation, $\Delta f = 1MHz$.

5.2.6 Implementation

The determined values for fundamental and harmonic terminations are summarized in Fig. 5.11 and are already transformed to the termination values that have to be presented to the device's external ports.

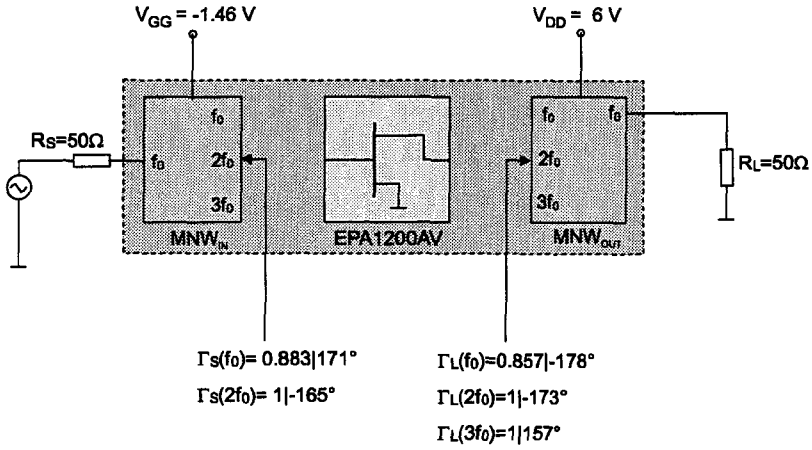


Figure 5.11: Single stage amplifier module design parameters.

For implementation is was necessary to gain knowledge on the influence of the presented

impedance values to the harmonics in comparison to the fundamental load impedance and thus investigations on this issue were made. Figure 5.12 indicates the influence of presented load resistances at the 2nd and 3rd harmonic, respectively. Simulations showed that one can define the following rule of thumb:

It is sufficient that the load resistances for a class F ouput network presented to the 2^{nd} and 3^{rd} harmonic signals are:

- *at the 2^{nd} harmonic smaller than $\frac{1}{10} \cdot R_{L,fundamental}$, and*
- *at the 3^{rd} harmonic higher than $10 \cdot R_{L,fundamental}$.*

These termination resistances are sufficient for practically optimal operation and have the advantage to be realizable.

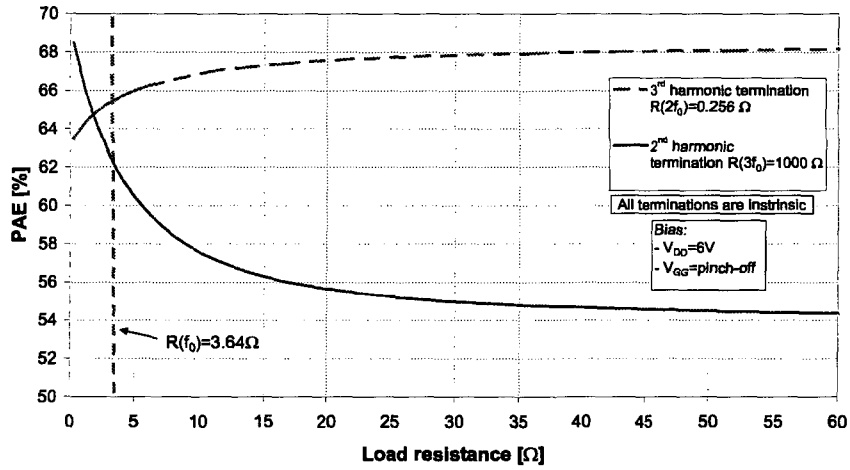


Figure 5.12: Dependency of power added efficiency on intrinsic harmonic termination impedance value. Rule of thumb: $R_{L,2f_0} < \frac{1}{10} \cdot R_{L,f_0}$, $R_{L,3f_0} > 10 \cdot R_{L,f_0}$.

The principal single stage power amplifier circuit diagram is depicted in Fig. 5.13a. The output harmonic terminations are realized by two high-Q series resonant circuits positioned with such a distance to the drain contact to offer the desired termination angles to the intrinsic transistor drain contact. A transmission line and a shunt capacitor determine the fundamental match.

The 2nd harmonic at the input is also terminated by a high-Q series resonant circuit. The input match at the fundamental frequency is realized by a capacitor – line – capacitor π – circuit. Gate and drain DC biases are fed to the circuit by external bias-Ts to check the amplifier module independently.

The high-Q series resonant circuits were realized using single layer chip capacitors (for characterization and modeling see Chapter 4.3) and thin film spiral inductors. The inductors (see also Chapter 4.3) have high Q-factor and are continuously scaleable. This scalability allows an accurate adjustment of the resonant frequency during design and offer a tuning possibility by altering the bond wire length. The developed spiral inductor model

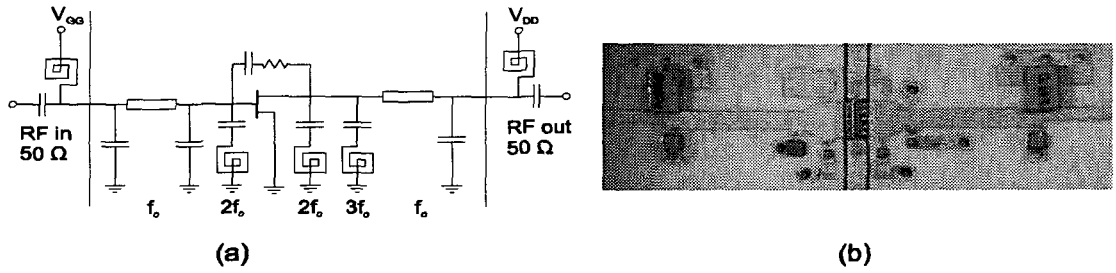


Figure 5.13: Single stage power amplifier – schematic and layout. – (a) Principal power amplifier schematic; (b) photograph of assembled single stage amplifier (original size 14x5 mm).

(Chapter 4.3) was very useful during design since the inductor's behavior is predicted very accurately with no EM simulation iterations by adjusting the inductance value only.

The final layout and the assembled amplifier is depicted in Fig. 5.13b. For solving possible stability problems the layout was precautionary extended to allow for a feedback circuit. This feedback circuit is illustrated in the amplifier schematic and is described in more detail in Chapter 5.3. During operation there was no need for the stabilizer circuitry since the amplifier showed no signs of oscillations and is furthermore unconditionally stable.

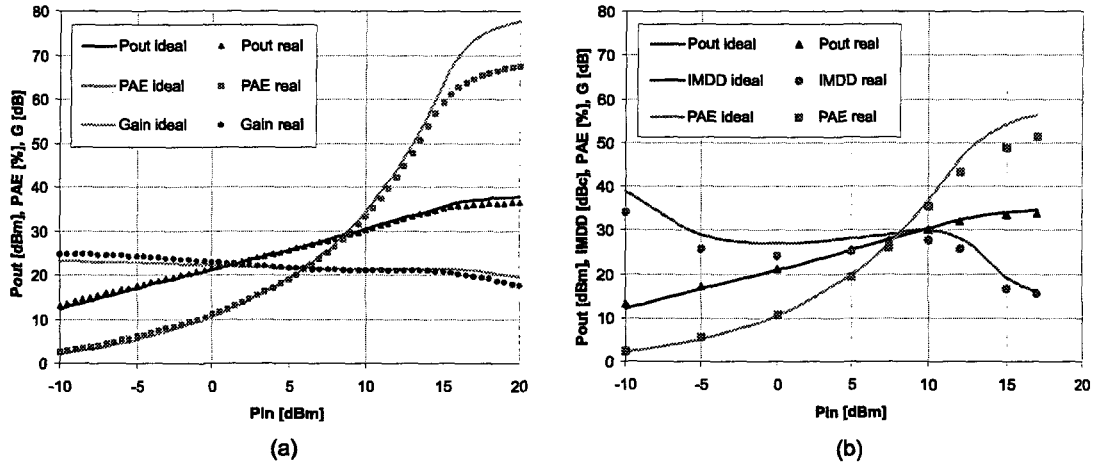


Figure 5.14: Simulation based comparison of ideal and real terminations. – (a) Single-tone excitation; (b) two-tone excitation, $\Delta f = 1MHz$.

Simulations with real components show a slight reduction in output power and, therefore, a reduction in power added efficiency also. Furthermore, intermodulation distortion distance is reduced by some 2 dB as well (Fig. 5.14).

5.2.7 Measurement Results

Several single stage amplifier modules were finally assembled and tuned for optimum intermodulation distortion distance while still achieving good power added efficiency. The tuning process was done by bond wire tuning of the thin film spiral inductors only. For each amplifier module the correct gate bias voltage was determined since the pinch-off voltage of the active devices may vary in a wide range.

Figures 5.15 to 5.17 present the measurement results for single-tone excitation, two-tone excitation and DAB mode II excitation. Single-tone results are in a good agreement with simulation results with real components (Fig. 5.14a).

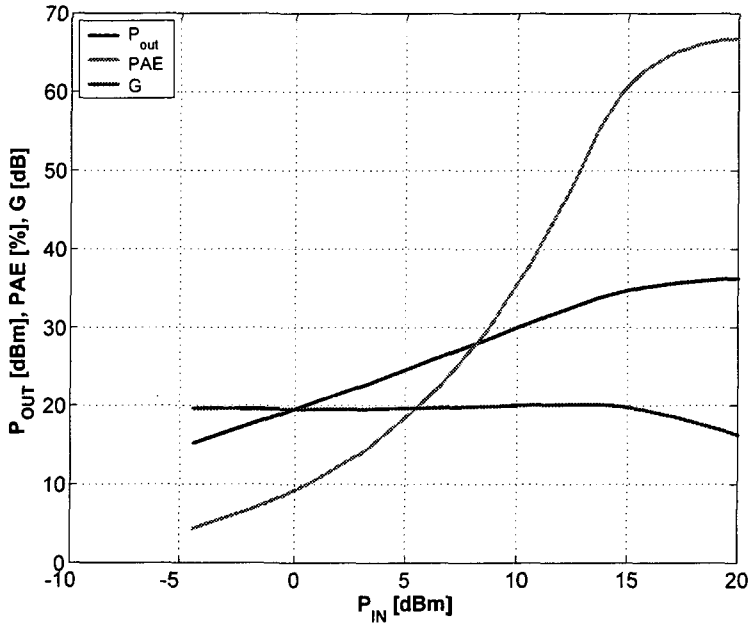


Figure 5.15: Tuned single stage amplifier measurement results at single-tone excitation ($V_{DD} = 6V$, $V_{GG} = -1.55V$).

Two-tone results for high input drive are also in good agreement with the simulation results with real components (Fig. 5.14b). As expected, the intermodulation distortion performance is better than simulated. This was already recognized at the test amplifier results (model of EPA480CV) and is also true for this amplifier (model of EPA1200AV). Since the EPA1200AV model is an upscaled model of the EPA480CV device this had to be expected.

Figure 5.17 illustrates that with the built amplifier a shoulder distance of 30 dB is realizable at a power added efficiency of 30 % while a shoulder distance of 20 dB is achievable at a power added efficiency of 48 %.

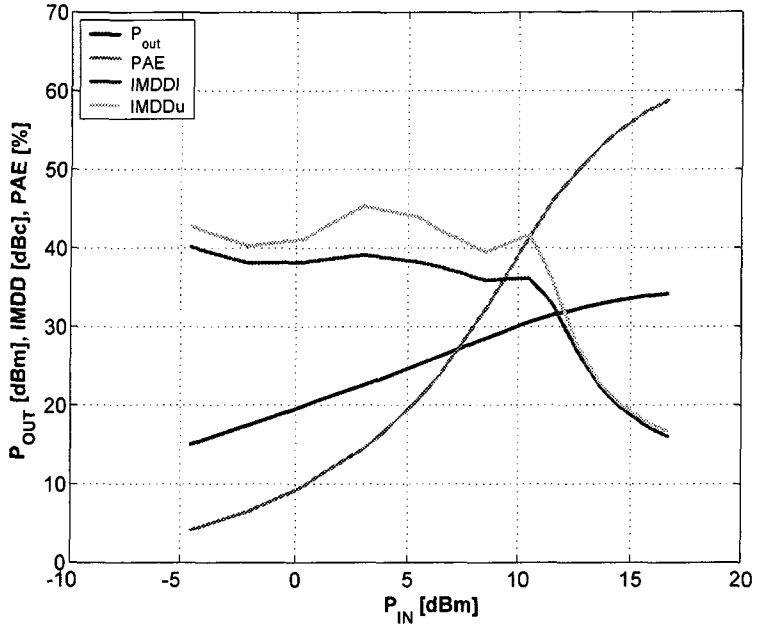


Figure 5.16: Tuned single stage amplifier measurement results at two-tone excitation ($V_{DD} = 6V$, $V_{GG} = -1.55V$, $\Delta f = 1MHz$).

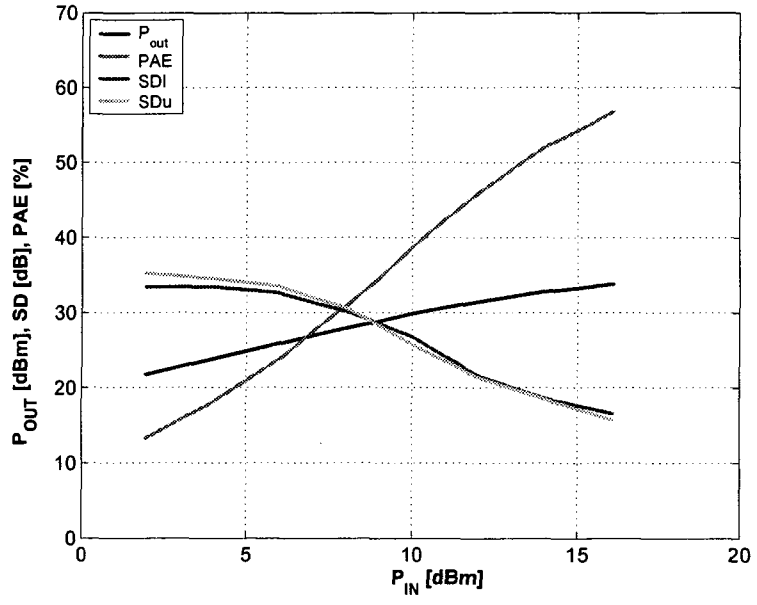


Figure 5.17: Tuned single stage amplifier measurement results at DAB mode II excitation ($V_{DD} = 6V$, $V_{GG} = -1.55V$).

5.3 Stability Issues

RF PA oscillation problems can be broadly categorized into two kinds. Bias oscillations occur at very low frequencies, in the megahertz to VHF range, and are caused by inappropriate and unintentional terminations at those frequencies by the bias networks. These oscillations have little to do with details of the RF matching circuitry. RF oscillations, on the other hand, typically occur either inband or out of band but still quite close to the design bandwidth, typically on the LF side [10]. Both kinds of instability can be analyzed quite effectively using k-factor[1] analysis. Although k-factor analysis assumes a linear two-port device, it usually is a satisfactory assumption that RF oscillations in power amplifiers will be more likely when the amplifier is backed off into its linear region where k-factor analysis is valid. A simple strategy is to run the entire circuit on a linear simulator.

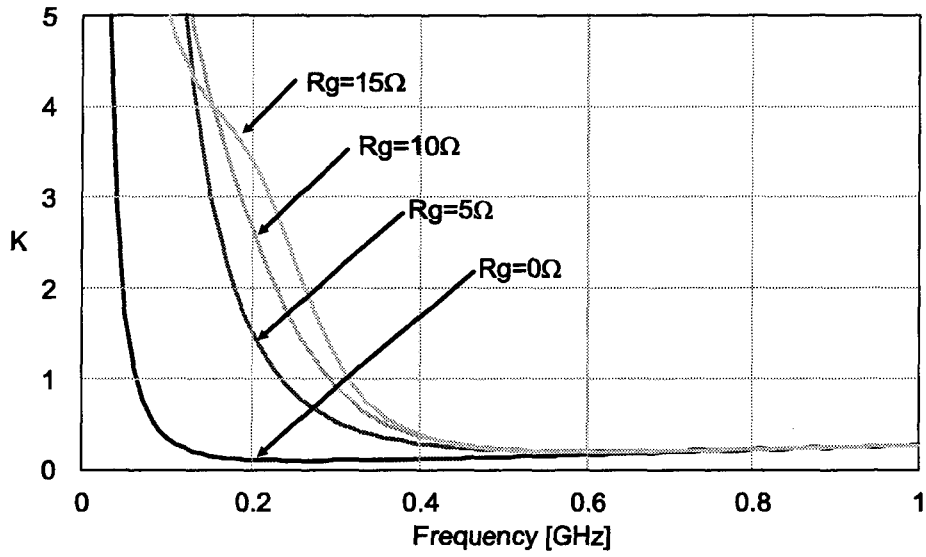


Figure 5.18: Dependency of Rollet stability factor k on DC gate series resistance R_g.

Figure 5.18 depicts the k-factor analysis results for the low frequency range in dependency on the DC series gate resistance R_g. As can be seen that stability is significantly improved in the few 100 MHz range by introducing a series resistance. The according stability circles at the in- and output of the active device are shown in Fig. 5.19 for different values of R_g. A choice of $R_g = 10\ \Omega$ offers the largest area (area encircled by the stability circles) for low band matching and was therefore chosen as optimum value. Stability is also improved at the device output by introducing a DC series resistance at the device input as can be seen in Fig. 5.19 as well.

Investigating RF stability of the single stage amplifier developed in Chapter 5.2 k-factor analysis leads to the results presented in Fig. 5.20. As can be seen at the output Smith Chart the output stability circles are quite close to the required load impedances for optimum matching. In the analysis the circuit is still stable but with manufacturing

[1]The k-factor is the Rollet stability factor. $k > 1$ indicates unconditional stability while $k < 1$ indicates potential instability; i.e. oscillation may occur.

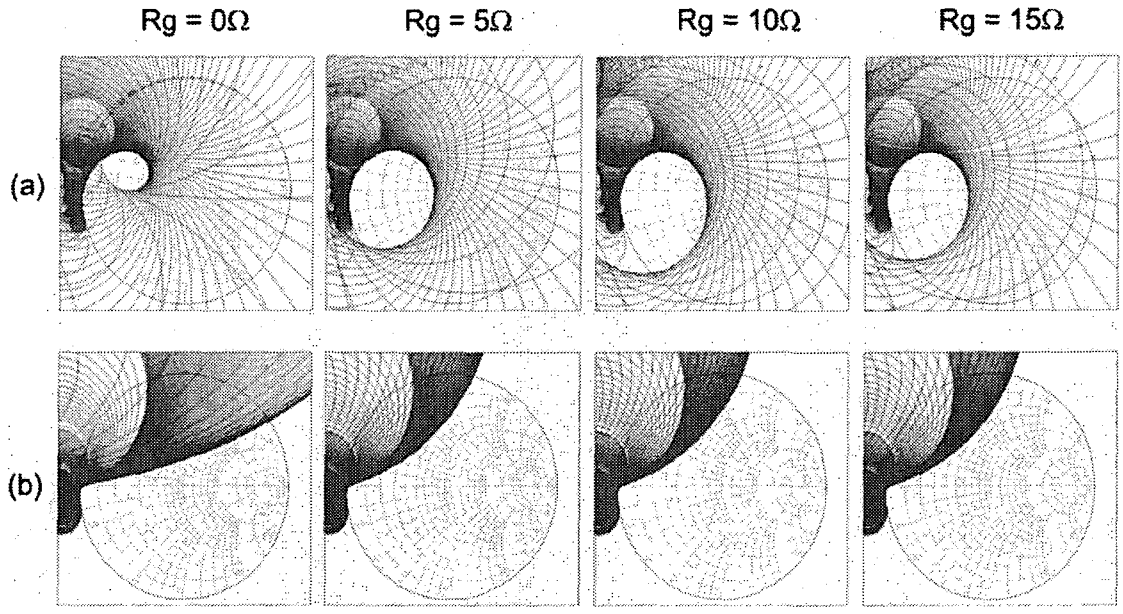


Figure 5.19: Dependency of stability circles on DC gate series resistance R_g. – (a) Input stability circles; (b) output stability circles.

tolerances oscillations can occur easily.

To prevent oscillations a simple feedback circuit was developed. Figure 5.22 displays the schematic and the RC feedback circuitry. This voltage feedback limits the transconductance of the device and thus improves stability. Figure 5.21 shows the resulting stability circles at the in- and output of the device presenting the improvement in distance from the stability circles to the load impedances. However, introducing feedback and improving stability has its price. The gained stability will reduce gain and thus ouput power and efficiency will be reduced. Table ?? sums up the performance parameters for single tone drive.

Single stage performance	P_{OUT} [dBm]	G [dB]	PAE [%]
Without stability improvement	37.7	18.7	75.0
With stability improvement	36.8	17.8	69.5
Performance degradation	**-0.9**	**-0.9**	**-5.5**

Table 5.1: Performance degradation by stability improvement. $P_{IN} = 19dBm$.

It is most likely that the RC stability circuit doesn't have to be used at all because of stable operation and thus performance is not degraded. However, the final balanced amplifier will have much better stability due to the wideband isolation and resistive terminations of the couplers. This is a major benefit of balanced amplifier designs.

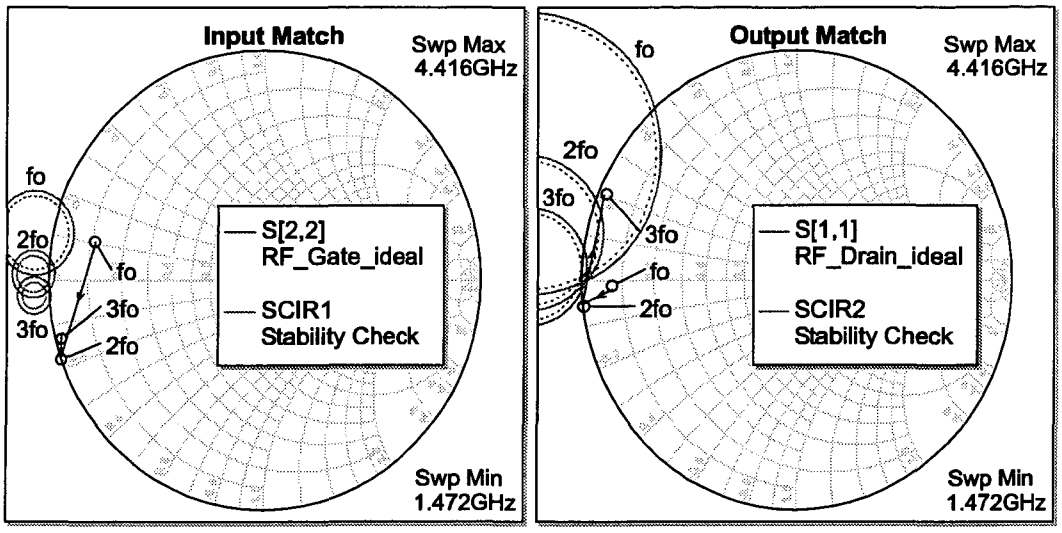


Figure 5.20: RF stability analysis without stability improvement.

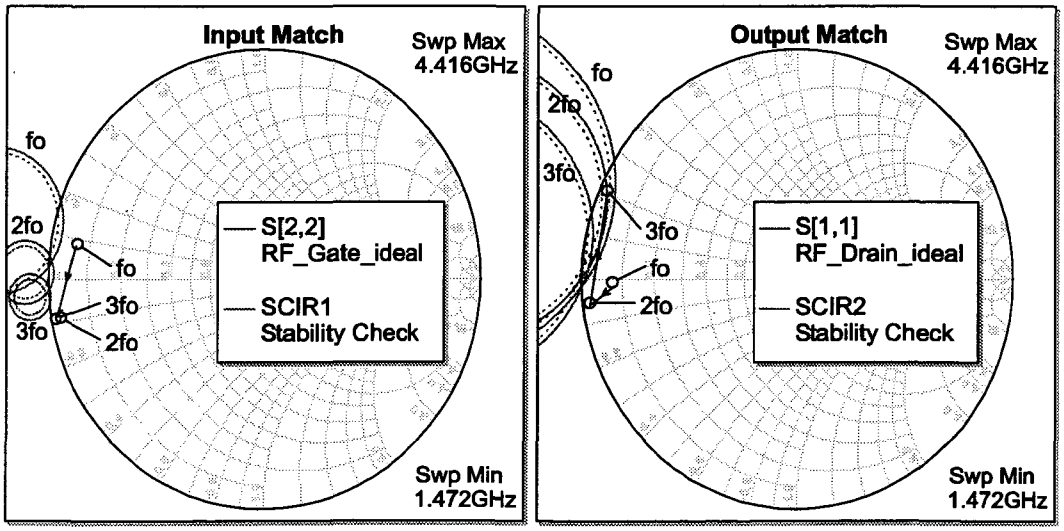


Figure 5.21: RF stability analysis with stability improvement.

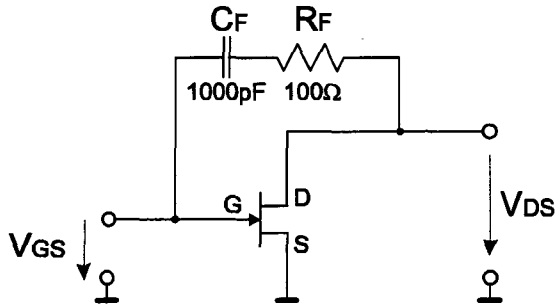


Figure 5.22: Stability improvement by voltage feedback.

5.4 Bias Networks

For DC power supply and quiescent point adjustment bias circuits are needed. As mentioned in chapter 5.3 the circuit stability can be significantly enhanced by proper biasing. Therefore, the circuit design of the so called "bias-Ts" has to be done carefully.

5.4.1 Drain Bias

At the amplifier output two issues are of great importance. Firstly, the insertion loss has to be low. High insertion loss would cause a reduction of output power and, therefore, also a reduction of efficiency. Secondly, the DC series resistance has to be low. High DC series resitance would cause a modulation of the transistor's supply voltage by the envelope of the RF signal. This modulation is induced by the voltage drop on the series resistance caused by the varying DC power supply current.

Figure 5.23 shows two different bias circuits for the amplifier output. The circuit shown in Fig. 5.23a is a classical bias circuit using $\frac{\lambda}{4}$ stubs for RF blocking. The $\frac{\lambda}{4}$ stub connected to the $DC + RF$ input transforms the short circuit provided by the open circuited $\frac{\lambda}{4}$ stub and the grounded capacitor to an open circuit and, therefore, blocks the RF signal from leaking to the DC supply. Since only a transmission line is connected between the DC supply and the transistor, the DC series resitance is fairly low thus reducing modulation effects. To achieve minimum insertion loss a capacitor with its series resonance at the fundamental frequency and a low internal series resistance (ESR=0.1 Ω) was chosen for blocking DC from the RF output.

To minimize circuit size a second design (Fig. 5.23b) was made with an inductor to block RF from leaking to the DC supply. The inductance value of 24 nH offers an impedance of 220 Ω will only marginally influence the amplifier output. Furthermore, the chosen inductor offers a low series resistance of 0.1 Ω.

The measurement results displayed in Fig. 5.23 show good agreement with simulation results. With an insertion loss of 0.08 dB (version with lumped elements) and a return loss of better than 20 dB the drain bias circuit is well suited for biasing the amplifier.

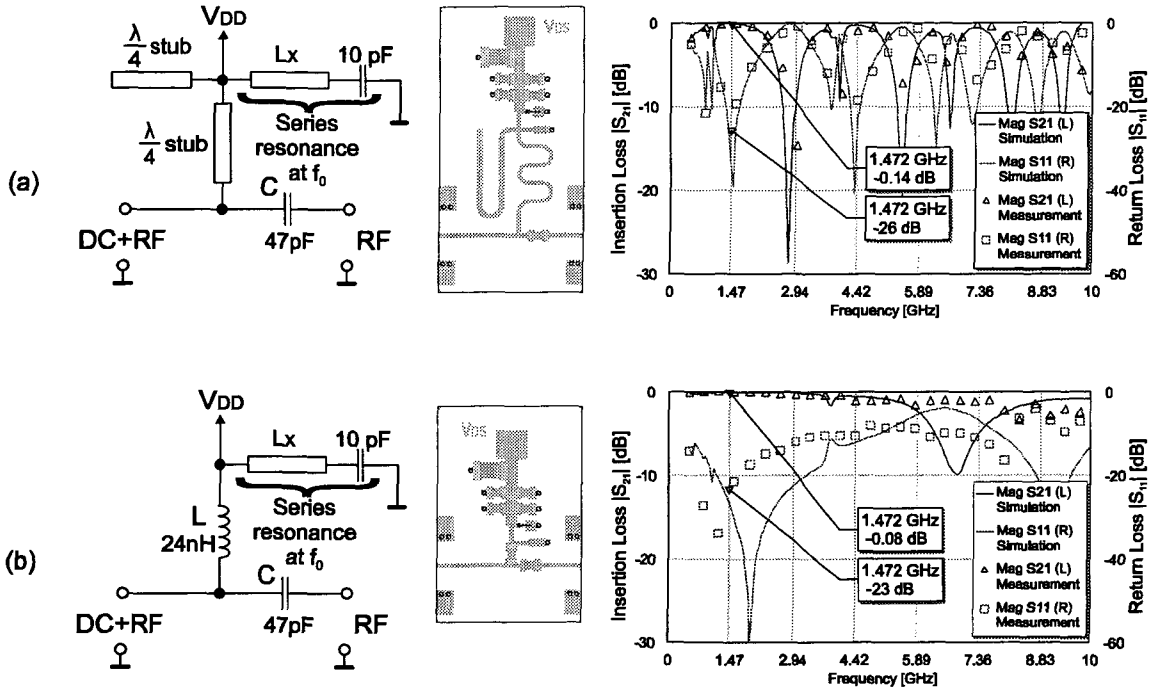


Figure 5.23: Output bias-T. – (a) Design with distributed elements, layout (size: 14.5 x 29 mm) and simulation and measurement results; (b) design with lumped components, layout (size: 14.5 x 22 mm) and simulation and measurement results.

5.4.2 Gate Bias

As presented in Chapter 5.3 the DC gate series resistance R_g can be optimized to minimize stability problems. However, attention has to be paid that the resistance value is small enough not to influence bias modulation. For high input power levels the DC gate current will vary with the RF envelope and thus will modulate the DC gate bias when a series resistance is present.

The maximum of R_g is further limited by device thermal runaway [83]. The runaway mechanism can be explained as: $V_{gs} = V_{gg} - R_g I_{gs}$ is negative without RF drive. When the temperature rises, I_{gs} decreases and and V_{gs} increases. This rise in V_{gs} increases the drain current I_{ds}, which increases the power dissipated in the device and, consequently, the channel temperature. An increase in channel temperature results in a decrease in I_{gs}, a consequent increase in I_{ds}, and so on. Fortunately the maximum value required to avoid thermal runaway is higher than the maximum value for bias modulation.

Figure 5.24 again shows two designs for gate bias circuits. One design is using $\frac{\lambda}{4}$ stubs for RF blocking while the second design is using a thin film spiral inductor for RF to DC leakage prevention. The resistance R_g is provided by a NiCr thin film resistor.

With low drive level, the DC gate current is negative for depletion FETs and has a low absolute value. Under large drive conditions, the gate current is positive with a relatively large value (up to tens of mA). As a result, the gate power supply must be able to supply positive and negative current. To guarantee proper function resistance R_p is connected in

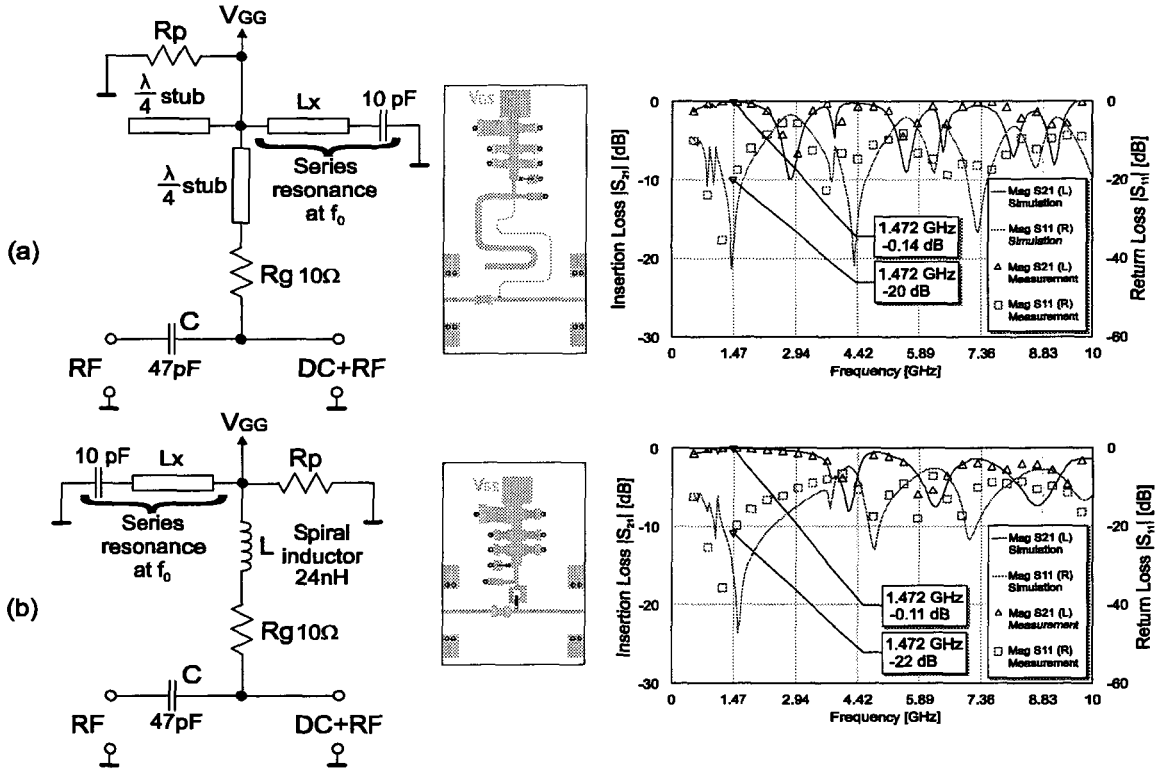


Figure 5.24: Input bias-T. – (a) Design with distributed elements, layout (size: 14.5 x 29 *mm*) and simulation and measurement results; (b) design with lumped components, layout (size: 14.5 x 22 *mm*) and simulation and measurement results.

parallel with the gate power supply terminals. To ensure that the internal current in the power supply will flow from the negative to the positive terminal, R_p should be:

$$R_p < \frac{-V_{p,\max}}{2I_{gs,\max}}, \tag{5.8}$$

where $V_{p,\max}$ is the maximum pinch-off voltage and $I_{gs,\max}$ is the maximum gate current under normal conditions. For the EPA1200AV this results in $R_p < 50\ \Omega$.

The measurement results displayed in Fig. 5.24 show good agreement with simulation results. With an insertion loss of 0.11 *dB* (version with lumped elements) and a return loss of better than 20 *dB* the gate bias circuit is well suited for biasing the amplifier.

5.5 Quadrature Couplers

For power splitting at the input and power combining at the output of the balanced amplifier configuration quadrature hybrids are needed. These couplers have to provide a phase difference of 90° between the decoupled output (input) ports and a symmetrical coupling of 3 dB between the common input (output) port and the decoupled output (input) ports. An important requirement is that especially the output quadrature coupler

has very low insertion loss to minimize the degradation of output power and efficiency (see also 3.6).

Two different quadrature hybrids were designed for the input and output of the amplifier. At the input a Lange coupler was chosen due to its broadband frequency response which allows noncritical design. Since a Lange coupler realized on alumina substrate consists of very narrow transmission lines this is not a reasonably good choice at the output of an amplifier where high power has to pass the coupler. The resistance of the narrow transmission lines would result in significant insertion loss thus reducing output power and efficiency. Therefore, at the output a branchline coupler was chosen. Branchline couplers have the disadvantage that they are very narrowband. So a careful design is needed to achieve good performance.

5.5.1 Lange Coupler

Figure 5.25a depicts the principle layout of the designed Lange coupler. The geometrical dimensions in this picture were adapted for demonstration since line width is 33 μm, line spacing is 30 μm, and $\frac{\lambda}{4}$ is 20500 μm. The transmission lines connected to ports 1 to 4 are 50 Ω lines. The bridges in the layout were realized by wire bonding. To ease the bonding procedure the bridge structure was changed compared to the standard implementation (see Fig. 3.33a).

Figure 5.25b displays the simulation and measurement results of the realized Lange coupler. The graphs show good agreement between simulation and measurement. The coupler features at a center frequency of 1.472 GHz an operating bandwidth higher than 500 MHz with 3.3 dB coupling and an isolation close to 30 dB.

5.5.2 Branchline Coupler

Figure 5.26a portrays the layout of the branchline coupler. To reduce size the structure was folded. To achieve a symmetric coupling of the folded structure the width of the transmission lines at the center of the structure had to be decreased. The measurement results, presented in Fig. 5.26b, show exceptionally good agreement with the simulation results due to careful EM based simulation.

The branchline coupler provides symmetric coupling of 3.3 dB at a center frequency of 1.472 GHz and a bandwidth of 40 MHz at an isolation better than 30 dB. For isolation better than 20 dB the bandwidth increases to 150 MHz.

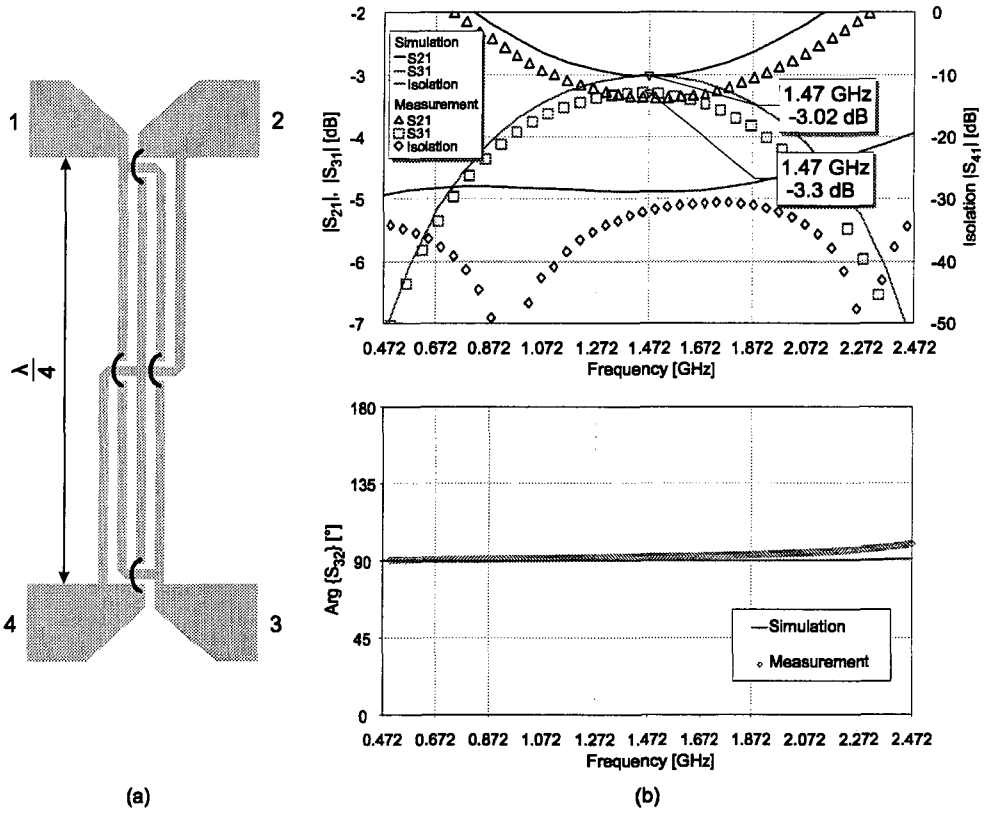


Figure 5.25: Lange coupler. – (a) Layout: The geometrical dimensions in this picture are adapted to show the principle since line width and spacing are extremely small compared to $\frac{\lambda}{4}$; (b) simulation and measurement results.

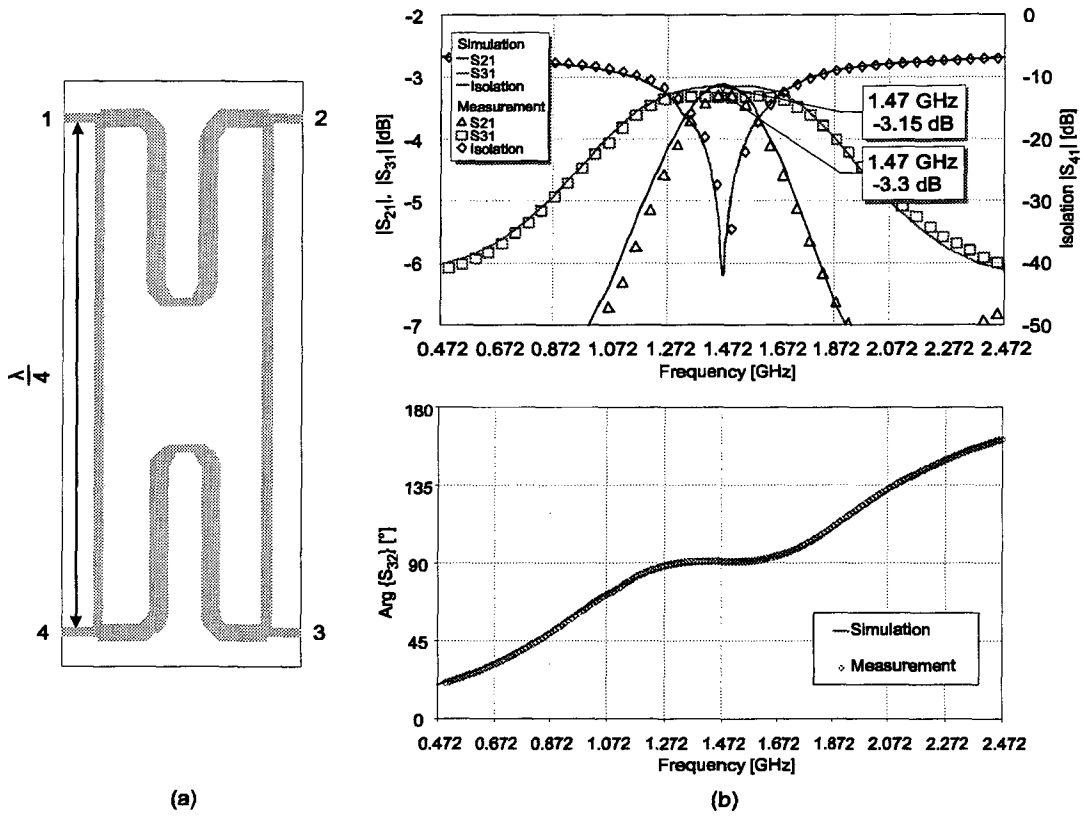


Figure 5.26: Branchline coupler. – (a) layout; (b) simulation and measurement results.

5.6 Balanced Amplifier

The final amplifier is implemented as a balanced architecture to benefit of its above mentioned advantages. The layout of the two basic single stage amplifier modules is shown in Fig. 5.27. The 2^{nd} harmonic termination at the input and and the output can be connected in this layout by wire bonding directly to ground (single stage operation) or can be connected to the according 2^{nd} harmonic termination of the second amplifier module (harmonic reaction operation). A comparison of these two operation modes will be given below.

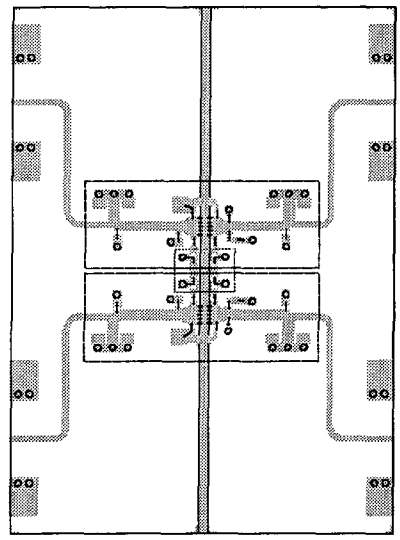


Figure 5.27: Balanced amplifier layout excluding bias-Ts and couplers. The boxes outlined in black indicate the single stage amplifiers, the red colored box marks the 2^{nd} harmonic ground connection.

As mentioned earlier, the amplifier is divided into submodules to be able to characterize each module separately and for easy exchange of single modules (e.g. testing the influence of the different bias-Ts). One configuration is depicted in Fig. 5.28.

Connecting the submodules causes a loss at the output of the amplifier modules. This loss comprises the insertion loss of the drain bias-T ($\approx 0.1\ dB$), the insertion loss of the Q-hybrid ($\approx 0.3\ dB$), and estimated loss of the bond wire connections and of the connector transition ($\approx 0.1\ dB$). The total loss sums up to $0.5\ dB$ which reduces the power added efficiency by a factor of 0.89 (Fig. 3.30) and the output power level by $0.5\ dB$ while the gain is reduced by $1\ dB$ since the total loss of the amplifier input is equal to the output loss. Figure 5.29 displays these reductions for the complete amplifier compared to a single stage amplifier with ideally doubled power levels. It can be further seen that balancing the amplifier improves linearity by improved symmetry.

Figure 5.30 shows the comparison results for 2^{nd} harmonic terminations directly connected to ground (single stage operation) to harmonic reaction operation. The transmission line used for connection of the 2^{nd} harmonic terminations has equivalent electrical length as the via connections to ground. It can be seen that due to a compensation mechanism the

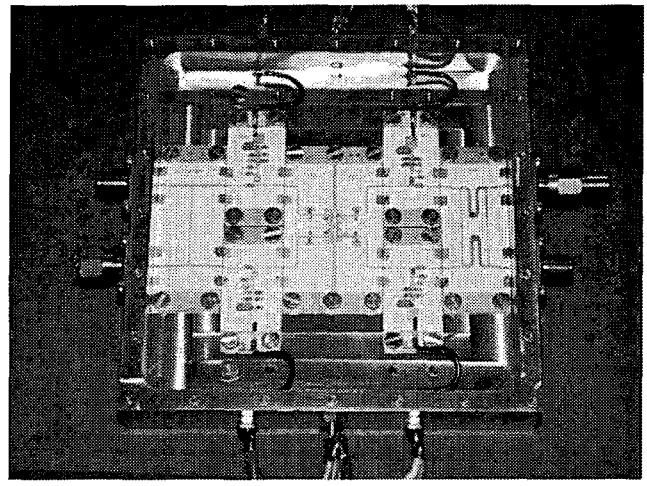


Figure 5.28: Photograph of complete amplifier. The amplifier is assembled out of single modules.

harmonic reaction amplifier has better intermodulation performance. But this only appears at a sweet spot where the linearity of the single stage operation is high enough anyway. The improvement in linearity has to be paid by slightly reduced power added efficiency. Thus 2^{nd} harmonic terminations were bonded directly to ground since an improvement for the final DAB amplifier was not achieved with harmonic reaction. Figure 5.30 depicts measurement results of untuned 2^{nd} harmonic terminations. Only with short bond wires (not extended to an unknown length as it is true for tuning) a reproducable comparison is possible.

For optimum amplifier performance and to meet the requirements a bias search was performed by an automated measurement setup. For this purpose the drain and gate bias of both single stage amplifiers were swept in a wide range and an RF power sweep was performed at each bias combination. This power sweep started at maximum input power and was swept to lower values. For each power level the shoulder distance SD was measured and decided whether this value was beyond the required shoulder distance (30 dB or 20 dB). If so, the according input power level, output power level, and power added efficiency were stored. Figure 5.31 illustrates the search results for the two required shoulder distances. Every measured point in these subplots is closely beyond the required shoulder distance, except the white colored area for P_{OUT} at $SD = 30dB$ (and the equivalent area in the PAE subplot). In this area it was not possible to achieve a shoulder distance better than required.

The areas encircled by the cyan colored dotted lines indicate the required power levels and the desired power added efficiencies. As can be seen the power levels can be only achieved for reduced gate bias voltage and increased drain bias voltage. As optimum bias values (marked by the cyan colored pyramides) $V_{DD} = 8V$, $V_{GG1} = -1.6V$, and $V_{GG2} = -1.425V$ was determined. The start values for the gate bias voltages were $V_{GG1} = -1.55V$ and $V_{GG2} = -1.375V$.

The resulting measurement results are presented in the next chapter.

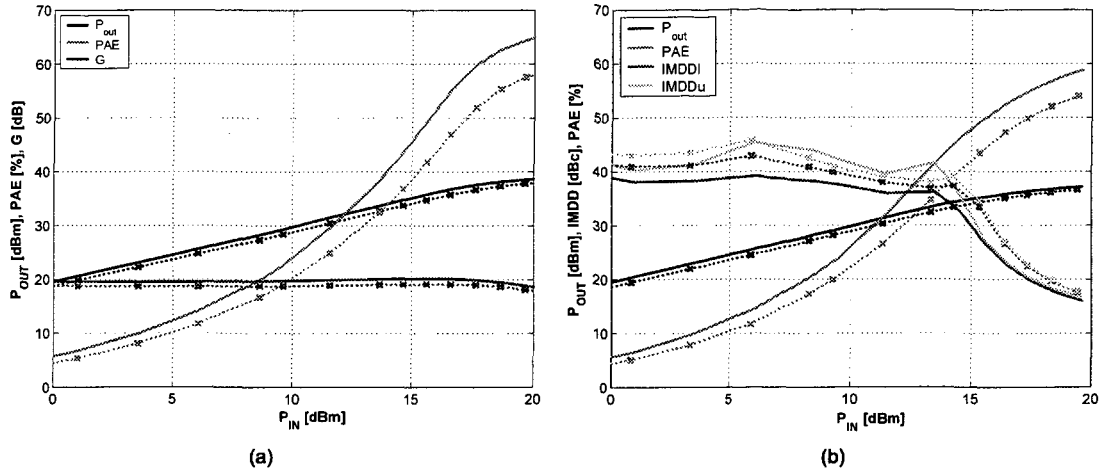


Figure 5.29: Comparison of balanced amplifier to single stage amplifier performance ($V_{DD} = 6V$, $V_{GG1} = -1.55V$, $V_{GG2} = -1.375V$, $f_0 = 1.472GHz$). – (a) Single tone excitation; (b) two-tone excitation. – Dotted line: balanced amplifier; solid line: single stage amplifier + 3 dB.

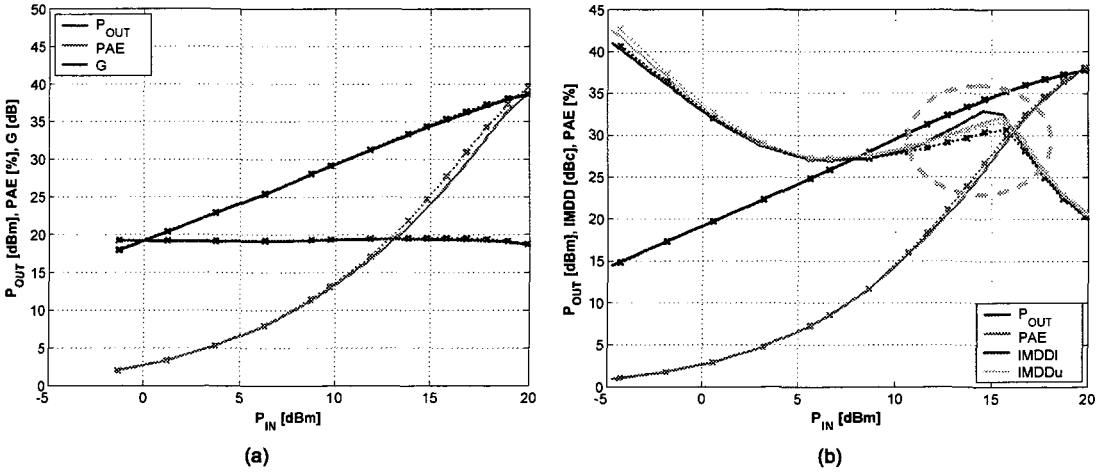


Figure 5.30: Comparison of 2^{nd} harmonic terminations connected for single stage operation to harmonic reaction termination ($V_{DD} = 8V$, $V_{GG1} = -1.6V$, $V_{GG2} = -1.425V$, $f_0 = 1.472GHz$). – (a) Single tone excitation; (b) two-tone excitation, $\Delta f = 1\ MHz$. – Dotted line: balanced amplifier; solid line: harmonic reaction amplifier.

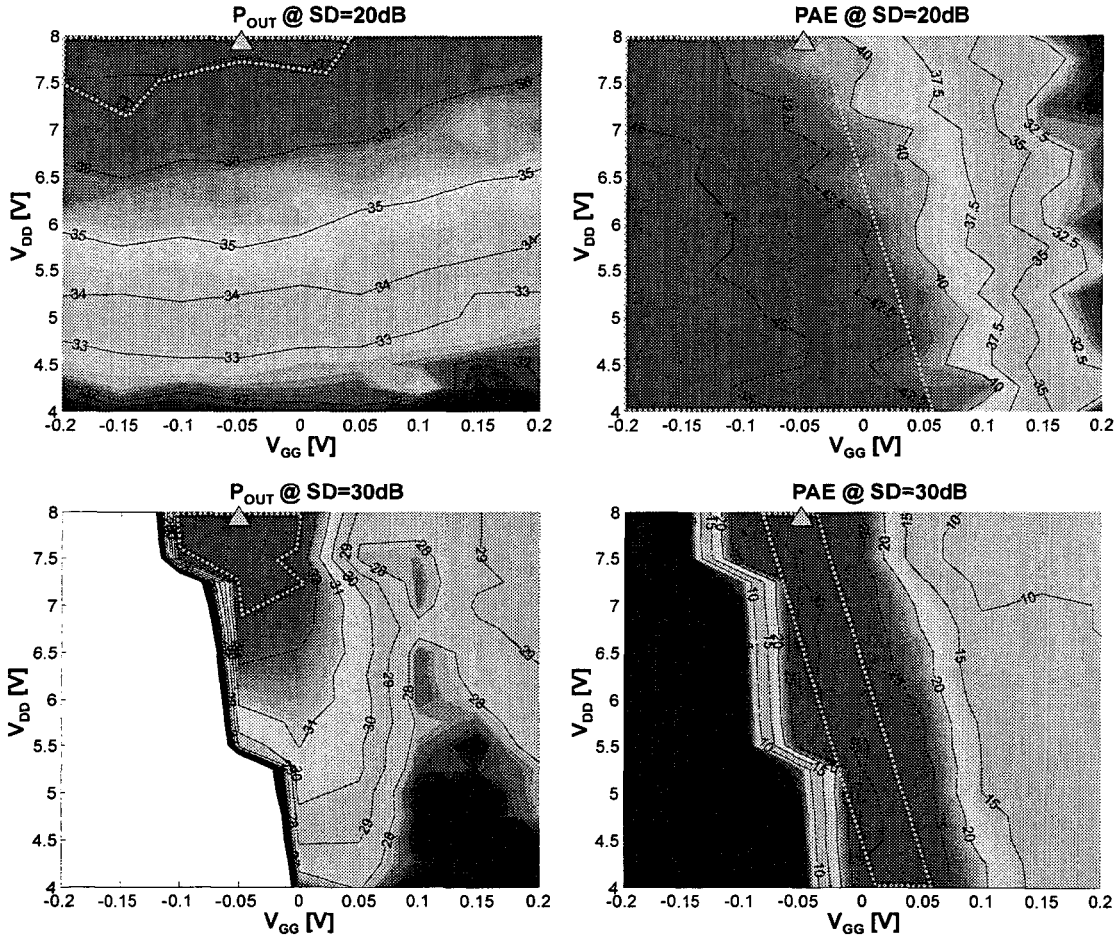


Figure 5.31: Optimum amplifier bias search (V_{GG} Offset=0: $V_{GG1} = -1.55V$, $V_{GG2} = -1.375V$).

5.7 Measurement Results

The final amplifier was characterized to verify its performance with respect to the requirements. Figure 5.32 presents the amplifier performance on swept power level at single-tone and two-tone excitation, respectively. Since the drain bias voltage had to be increased to get the required power level for DAB operation the power added efficiency was reduced. At single-tone excitation an output power level of 40 dBm at a power added efficiency of 50 % is achieved. Two-tone characterization shows a distinctly recognizable sweet spot causing the intermodulation distortion distance rising very quickly over 40 dBc causing shoulder distance to rise quickly above the 30 dB threshold.

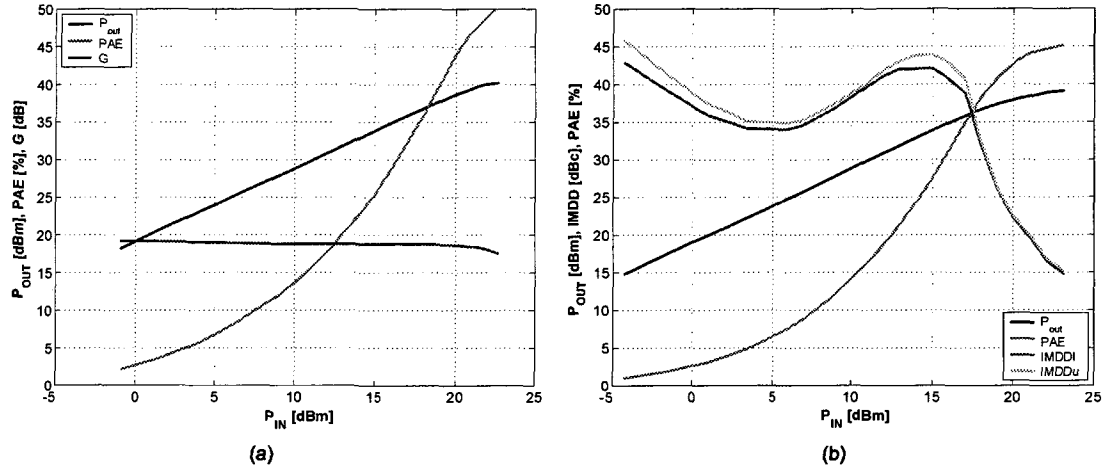


Figure 5.32: Final amplifier performance ($f_0 = 1.472GHz$). - (a) Single-tone excitation; (b) two-tone excitation, $\Delta f = 1\ MHz$.

The amplifier performance with respect to swept input power for DAB mode II excitation is depicted in Fig. 5.33. At shoulder distance 20 dB and 30 dB the required output power levels of 33 dBm and 37 dBm, respectively, are well reached. The according power added efficiency values are 31 % and 41 %, respectively. These values could be increased by lower cominbing losses to a maximum of 34.8 % and 46 %, respectively. The relation $SD = IMDD_{2-tone} - 5.5\ dB$ mentioned at the beginning of this chapter is only true for the range where no sweet spot occurs. Comparing Fig. 5.32 to Fig. 5.33 reveals that intermodulation distortion distance has to rise much steeper in the sweet spot range to achieve improvement in shoulder distance. Sweet spots occur at intermodulation cancellation of different odd order products which is quite easily achieved by a two-tone signal but not by a quasi-random signal with a Crest factor of 13 dB.

Frequency sweep analysis is presented in Fig. 5.34 showing DAB performance for two different power levels. At the lower power levels it is seen that the matching is a good compromise between power added efficiency and intermodulation distortion distance. The strong frequency dependency of shoulder distance is due to the phase dependency of the distortion cancellation mechanism of the sweet spot formation. For higher power levels the frequency dependency of shoulder distance is reduced since this is beyond the sweet spot

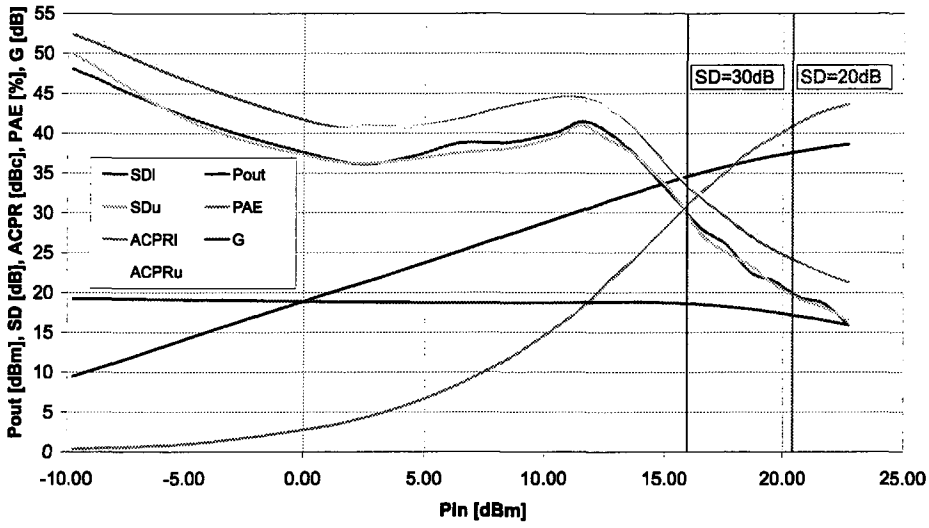


Figure 5.33: Final amplifier DAB mode II power sweep performance ($f_0 = 1.472GHz$).

range. Power added efficiency is well centered for higher power levels.

To characterize amplitude and phase distortion an AM/AM and AM/PM characterization using a vector network analyzer was performed in a wide range of frequency. The results are depicted in a 3D view in Fig. 5.35. Maximum of gain magnitude is well centered at the center frequency and shows only low variation with swept input power. The phase is also very constant with respect to swept input power and varies proportionally with frequency as expected.

A closer look on the gain performance is done in Fig. 5.36. Figure 5.36a shows flat gain and only small AM/PM distortion. Figure 5.36b shows a well centered gain performance and flat phase. To have an even closer look on phase variation group delay was derived and plotted in Fig. 5.37. A variation of $\pm 0.4\ ns$ is observed in the full 40 MHz range while the worst deviation for one DAB channel ($BW = 1.536\ MHz$) is better than $\pm 0.025\ ns$.

A summary of the results is given in the next chapter.

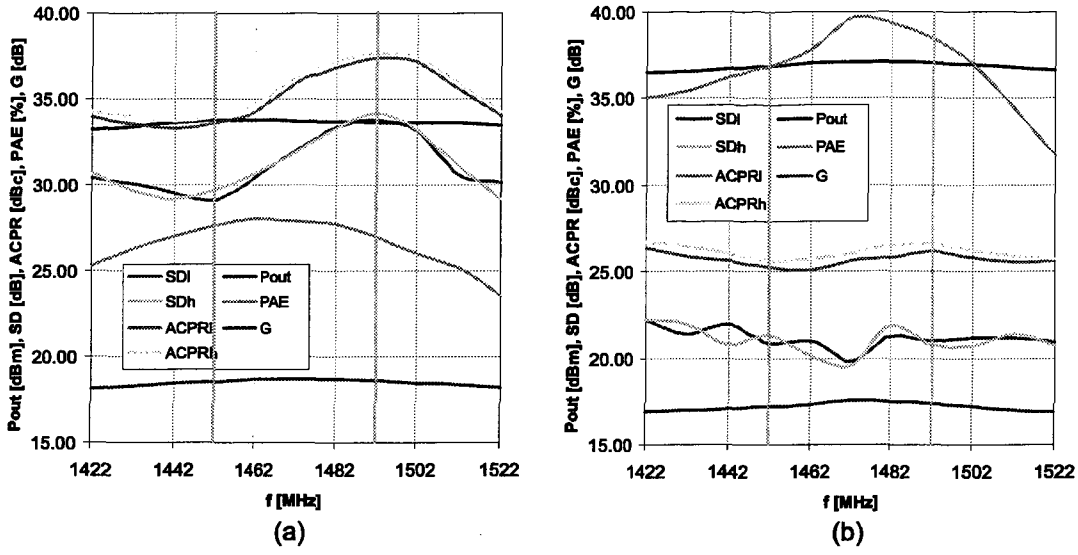


Figure 5.34: Final amplifier DAB mode II frequency sweep performance. – (a) $P_{IN} = 15dBm$; (b) $P_{IN} = 19.7dBm$.

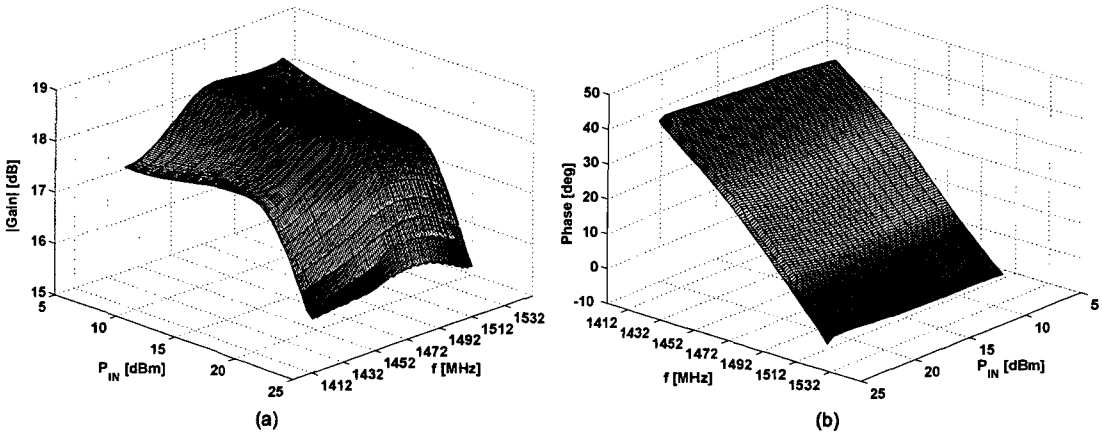


Figure 5.35: Complex gain characterization results. – (a) Magnitude of gain; (b) angle of gain.

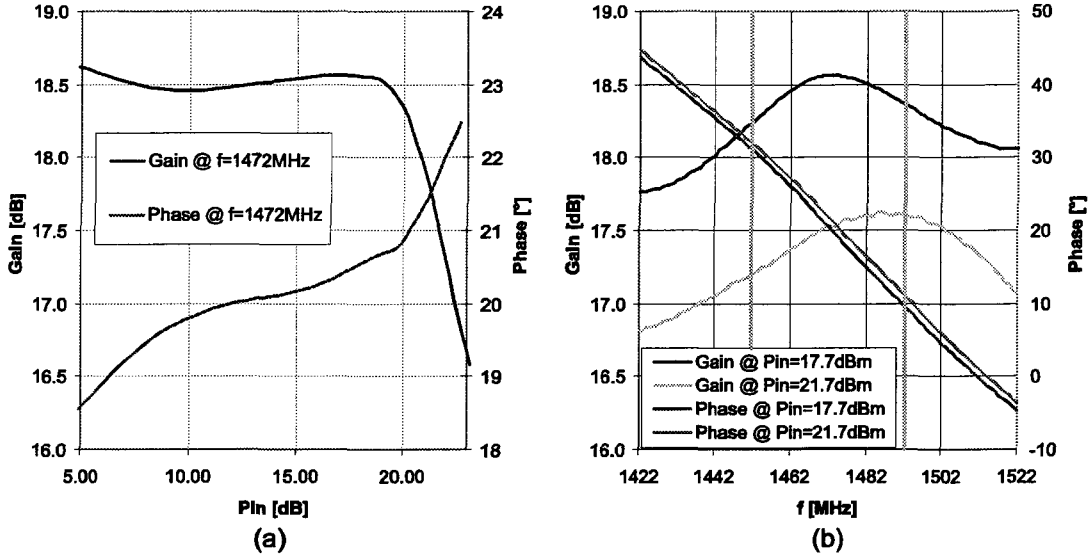


Figure 5.36: Complex gain power sweep and frequency sweep. – (a) AM/AM, AM/PM characterization; (b) gain frequency sweep at two different power levels.

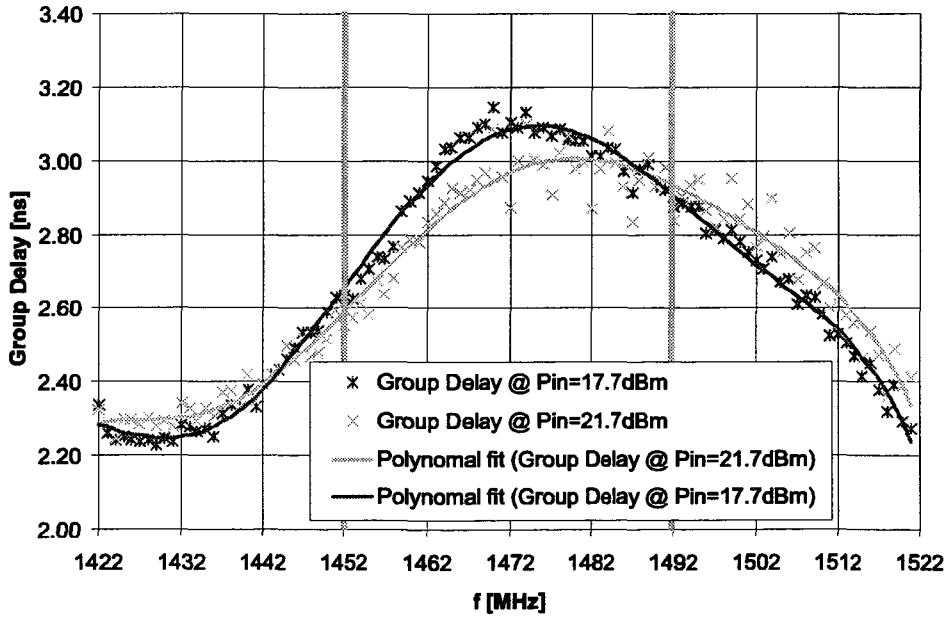


Figure 5.37: Final amplifier group delay variation at two different power levels.

Chapter 6

Conclusion

In this concluding chapter a comparison of the measured amplifier performance with the specified requirements (Tab. 1.1) is given. Further, a short summary of the research work is given including a comparison table of achieved results reported in literature and of the realized amplifier. Finally, an outlook concludes this doctoral thesis.

6.1 Table of Compliance

Table 6.1 contains a comparison of the performance of the realized amplifier with the requirements given in Chapter 1 and one can find good agreement with all specifications.

The amplifier module delivers at nominal DAB drive an output power of 37.3 dBm at the requested shoulder distance of 20 dB at a power added efficiency of 41 %. At reduced output power level (back-off condition) the module delivers at DAB excitation an output power of 34.5 dBm at the requested shoulder distance of 30 dB at a power added efficiency of 31 %. The power added efficiencies could be increased by lower combining losses to a maximum of 46 % and 34.8 %, respectively, which is close to the required goal.

Designing the amplifier in a modular concept is with respect to insertion loss and, therefore, with respect to PAE suboptimal. A further increase in PAE could be gained by an optimization of connecting transmission line lengths and by a unified design on one substrate. Higher values for power added efficiency at nominal drive can be reached at the requested output power level and shoulder distance only at reduced linearity at back-off condition by shifting gate bias voltage into class C near class B operation mode.

6.2 Summary

Linear and efficient small size amplifiers are needed for gap-filler transmitters for DAB broadcast in high quantity. Thin film technology is one miniaturization route which is for a medium number of units more cost effective than MMIC technology. The main goal of this thesis was to develop a solid state power amplifier (SSPA) module fulfilling DAB requirements in thin film technology showing conceptional feasibility for achieving simultaneously good linearity and good DC-power conversion rate.

The improvement of power added efficiency of microwave solid state power amplifiers has been investigated by many researcher in the last 20 years. With the introduction of

complex digital modulation schemes with a non constant envelope (e.g. OFDM, CDMA, ...) interest in high linearity power amplifier design increased in the last 5-10 years. The sources of nonlinearities were investigated and effective linearisation techniques have been invented by several researchers. Improving linearity of the amplifier circuit was mostly done by an improvement in device technology and by careful bias selection but rarely by an optimization of the amplifier circuit itself.

Class F mode of operation is well known for high efficiency. But investigations on linearity of class F termination have been reported rarely and the optimum termination angles of the harmonic loads in terms of linearity were not reported at all. In this thesis class F operation mode was investigated in terms optimization of linearity and efficiency based on nonlinear simulations. To improve linearity further, harmonic termination at the input was investigated on its capability to improve linearity and efficiency. To reach the required output power a balanced amplifier configuration was chosen since it offers many advantages, such as minimized input VSWR and increased stability. For easy characterization and flexibility the amplifier was designed in a modular way.

As no experience with thin film technology was available at the institute the thin film process of the selected foundry was evaluated to ensure the validity of the used component models. For multiharmonic amplifier termination passive components with high Q-factor are needed. Since no accurate model for spiral thin fim inductors was available in the simulation software used, a new spiral inductor model was developed being capable of predicting all parasitic elements and being scalable in a wide range of inductance values. This model is a fundamental tool in the design of harmonic terminations since it eliminates an iterative spiral inductor design process. All selected lumped components were characterized and scaleable models were made for those also. To ensure high reliability the bonding technique of the active devices was investigated and optimized.

To design and optimize a harmonic controlled amplifier, reliable large-signal transistor models are necessary. As no such models were available in our harmonic balance simulation software, computer models were generated from transistor DC and multiple bias small-signal scattering parameter measurements. The generated models agree well with measurements even at those regions which are crucial for high efficiency applications.

Simulation results of the 3rd order multiharmonic terminated transistor showed that with a non-ideal device the theoretical maximum of class F efficiency of 81.65 % is closely achievable only reduced by the knee voltage factor $\varkappa = \frac{V_{DD}-V_K}{V_{DD}} = 0.92$. The assumption that linearity and efficiency is maximized simultaneously with class F termination was proven by non-linear circuit simulations. Termination of the 2nd harmonic at the output was found to be crucial for linearity and efficiency optimization. Linearity and efficiency was further improved by a 2nd harmonic termination concept at the device input to compensate for the 2nd order nonlinearities of the gate-source capacitance.

The final amplifier results fulfil the given requirements for DAB operation. Table 6.2 summarizes some achievements in high efficiency and high linearity power amplifier design reported in literature. The results of this work are listed in the bottom line of the table for comparison. The developed amplifier module shows average results with respect to efficiency mainly due to suboptimal output combiner design. With respect to linearity at compression point and particularly at back-off condition the developed amplifier module achieves excellent results.

The results of selected parts of the work done during this doctoral thesis are published in several publications ([60], [61], [62], [65], and [82]).

6.3 Outlook

It was shown in this work that the class F operation concept is well known and understood in terms of optimum efficiency and linearity. From the scientific point of view it doesn't offer much room for further investigations. Hence, further improvement to reach the theoretical maximum efficiency is only possible by reducing the knee voltage factor $\varkappa = \frac{V_{DD}-V_K}{V_{DD}}$. As the equation shows this can be either done by reducing the knee voltage V_K or/and by increasing the drain bias voltage V_{DD}. There is still improvement in knee voltage possible as it is shown in [87] (tunnel collector GaInP/GaAs HBT, $V_K = 0.3V$). Wide bandgap devices (GaN: 3.49 eV, SiC: 3.26 eV) offer very promising results for future amplifier modules [88], where GaN technology achieves best transit frequencies (25 GHz, [89]). With such wide bandgap devices high breakdown voltages and, therefore, high drain bias voltages of about 50 V are possible and enable high efficient amplifier design with low Q components since the optimum load resistance is much closer to 50 Ω. Additionally, due to exceptional good thermal conductivity (power density is about 10 W/mm gate width for GaN devices fabricated on a SiC carrier substrate) and high operating temperatures (300 °C) those devices are well suited for reliable high power amplifiers at small size.

Improvement in linearity is possible by the use of a more linear device per se (recent research results showed linearity improvement by GaAs HBT collector doping design [90]) or by a linearization system approach. Without the access to the digital baseband signal adaptive digital predistortion, which is the most promising method, is not possible. Analog predistortion can be achieved by a diode- or FET-based predistorter which distorts the input signal in such a way that the main amplifier saturation is compensated. As it was shown in Chapter 3.5 a promising method is harmonic injection of 2^{nd} harmonic low frequency (baseband) and high frequency ($2f_0$) signals. The advantage of injecting both signals is that the sensitivity of the linearity improvement on the proper phase angle of the injected signals is decreased as compared to injecting only one signal [39].

	Requirements	Amplifier Performance
Signal Characteristics:		
- Type of signal:	continuous wave, multi-carrier	continuous wave, multi-carrier
- Frequency range:	1.452 – 1.492 GHz	1.452 – 1.492 GHz
- RF-output Power:	see output performance	see output performance
- VSWR (in/out):	$\leq$ 1.2 / minimized (50 Ω load, no isolators)	$\leq$ 1.3 / minimized
Gain Performance:		
- Power gain:	$\geq$ 15 dB (20 dB as a goal)	18.5 dB
- Amplitude ripple:	$\leq$ 0.5 dB	$\leq$ 0.4 dB
- Phase ripple:	$\leq$ 10 deg	$\leq$ 4 deg
- Group delay variation:	$\leq$ 0.2 ns	$\leq$ 0.05 ns
Spurious Response:		
- Harmonics ($2f_0$, $3f_0$):	-20 dBc / -30 dBc	fulfilled
- Non Harmonics:	-70 dBc	fulfilled
- Other	-60 dBc	fulfilled
Output Performance:		
DAB signal (nominal drive)		
- Output power:	$\geq$ 37 dBm	37.3 dBm
- Linearity (SD):	20 dB	20 dB
- Efficiency:	to be maximized (50 % as a goal)	41 %
DAB signal (back-off condition)		
- Output power:	$\geq$ 33 dBm	34.5 dBm
- Linearity (SD):	30 dB	30 dB
- Efficiency:	to be maximized (35 % as a goal)	31 %
DC Supply Voltage:	depending on semiconductors	$V_{DD} = 8V$, $V_{GG1} = -1.6V$, $V_{GG2} = -1.425V$
Operational Stability:	unconditionally stable under different load conditions with isolator at output (input/output)	unconditionally stable under different load conditions without isolator at output (input/output)

Table 6.1: Table of compliance.

Reference (Year)	Class (Bias)	Device (Style)	f [GHz]	G [dB]	Power Level	P_{OUT} [dBm]	PAE [%]	IMDD [dBc]
Bouthillette 1996 [13]	AB	PHEMT	1.6	18	1 dB CP	33.5	58	20
					4 dB BO	30	43	34
Iwai 2000 [18]	B	HBT (MMIC)	1.95	30.5	1 dB CP	27	42	38
					4 dB BO	–	–	–
Grebennikov 2003 [23]	E	HBT	1.8	22.6	1 dB CP	–	–	–
					3 dB BO	27	38.3	42
Iso 1990 [84]	F	FET	2.5	–	1 dB CP	41	47	22
					4 dB BO	–	–	–
Duvanaud 1996 [85]	F	FET	7.5	–	1 dB CP	26.6	50	18
					4 dB BO	–	–	–
Ingruber 1998 [32]	hHCA	MESFET	1.62	27.2	1 dB CP	23	65	21
					4 dB BO	20	35	21
Ingruber 1999 [86]	hHCA	MESFET	1.47	27	1 dB CP	25	50	30
					4 dB BO	22	34	34
Colantonio 2001 [81]	G	MESFET	5	21	1 dB CP	22.3	50	17
					4 dB BO	19	32	32
This work:	F	PHEMT	1.47	18.5	1 dB CP	38	43	22
					4 dB BO	35	30	42

Table 6.2: Comparison of high efficiency and high linearity amplifiers reported in literature. CP ... compression point; BO ... back-off condition.

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