DISSERTATION

An Integrated 17 GHz Receiver in 0.13 μm CMOS for Wireless Applications

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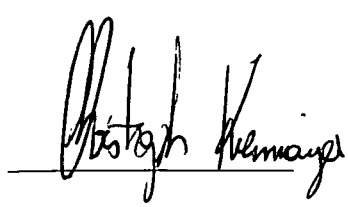

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List of Abbreviations

ADC	Analog-Digital Converter
AP	Access Point
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
BRAN	Broadband Radio Access Networks
C_L	Load capacitance in F
C_{CB}	Channel-bulk capacitance in F
C_{DB}	Drain-bulk capacitance in F
C_{GC}	Gate-channel capacitance in F
C_{gd}	Parasitic gate-drain capacitance in F
C_{gs}	Parasitic gate-source capacitance in F
C_{ox}	Oxide capacitance per unit area in F/m^2
C_{OV}	Gate overlap capacitance in F
C_{SB}	Source-bulk capacitance in F
σ	Conductivity
C11N	Infineons 0.13 μm CMOS technology
CA	Collision Avoidance
CAD	Computer-Aided Design
CEPT	Conference of Postal and Telecommunication
CMOS	Complementary Metal Oxide Semiconductor
CSMA	Carrier Sense Multiple Access
D	Data
DC	Direct Current
DECT	Digital Enhanced Cordless Telecommunications
DSSS	Direct Sequence Spread Spectrum
ε_{ox}	Dielectric constant of oxide in As/Vm
ε_r	Relative permittivity in 1
EDGE	Enhanced Data for GSM Evolution
ESD	Electrostatic Discharge
ERC	European Resuscitation Council
ETSI	European Telecommunications Standards Institute
f_{max}	Maximum oscillation frequency in Hz
f_t	Transit frequency in Hz
FHSS	Frequency Hopping Spread Spectrum
FIB	Focused-Ion Beam
γ	Bias-dependent parameter
GaAs	Gallium-Arsenide
GBW	Gain Bandwidth Product
GSM	Global System for Mobile communication
GPIB	General Purpose Interface Bus

GPRS	General Packet Radio Service
g_m	Transconductance in S
g_{mn}	Transconductance of nMOS device in S
g_{mp}	Transconductance of pMOS device in S
HB	Harmonic Balance
HF	High Frequency
I_d	Drain current in A
i_g	Gate current in A
I	Inphase Output
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate Frequency
IMD	Intermodulation Distortion
ISDN	Integrated Services Digital Network
ISI	Intersymbol Interference
ISM	Industrial, Scientific and Medical band
J_D	Drain current-density per drain width in A/m
k	Boltzmann's constant in J/K / Coupling coefficient in 1
λ	Channel length modulation parameter in V^{-1}
L	Transistor gate length in m
L_{eff}	Effective transistor gate length in m
L_{min}	Minimum transistor gate length in m
LAN	Local Area Network
LDD	Lightly Doped Drain
LO	Local Oscillator
LNA	Low Noise Amplifier
μ_n	Mobility of electrons in m^2/Vs
μ_p	Mobility of holes in m^2/Vs
MAN	Metropolitan Area Network
MBS	Mobile Broadband System
Mbps	Megabits per second
MIM	Metal-Insulator-Metal capacitor
MS-FF	Master-Slave Flip-Flop
OTA	Operational Transconductance Amplifier
PAN	Personal Area Network
PC	Personal Computer
PCB	Printed Circuit Board
PDA	Personal Digital Assitant
PIP	Poly-to-Poly capacitor
Q	Quadrature output
QI-Divider	Frequency divider with inphase and quadrature component
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
r_D	Drain resistance of a MOS in Ω

r_{DS}	Drain-Source resistance of a MOS in Ω
r_G	Gate resistance of a MOS in Ω
r_i	Channel charging resistance of a MOS in Ω
r_o	Drain output resistance of a MOS in Ω
R_o	Output resistance of current source in Ω
r_S	Source resistance of a MOS in Ω
RO4003	Rogers microwave substrate
S	Scaling factor
Si	Silicon
SIG	Bluetooth Special Interest Group
$SiGe$	Silicon-Germanium
SOI	Silicon-On-Insulator
SiO_2	Silicon-dioxide
SMA	Sub-miniature A connector
SNR	Signal-to-Noise Ratio
SRD	Short Range Devices
STI	Shallow trench isolation
t_{ox}	Gate oxide thickness in m
T	Temperature in K
TiN	Titanium-Nitride
UMTS	Universal Mobile Telecommunication System
USB	Universal Serial Bus
UWB	Ultra Wide-Band
VCO	Voltage Controlled Oscillator
VCVS	Voltage-Controlled Voltage-Source
V_{ds}	Drain-source voltage in V
V_{dsat}	Drain-source saturation voltage in V
V_{gs}	Gate-source voltage in V
V_T	Threshold voltage in V
W	Transistor width in m
WAN	Wide Area Network
WLAN	Wireless Local Area Network
ω_t	Transit angular frequency in Hz
ω_{max}	Maximum oscillation angular frequency in Hz

Notation

Throughout the thesis, signals (voltages and currents) are denoted in accordance with:

- Constant voltages and currents: with capital letters and capital indices (e.g. V_{SS})
- Total instantaneous voltages and currents: with capital letters and small indices (e.g. I_d)
- Small-signal voltages and currents in the time domain: with small letters and small indices (e.g. i_d)
- MOS transistors with a bulk-V_{SS} connection are drawn as three-terminal device in the circuit diagrams.

Abstract

This work presents the design and implementation of a fully integrated receiver in 0.13 μm CMOS for the 17.2 GHz WLAN/ISM band. The main challenges are the high frequency of operation, high integration level and low power consumption. This thesis explores possible solutions for these challenges by careful active and passive component design, circuit design and receiver partitioning to achieve an optimum result.
The receiver has been designed using the 0.13 μm CMOS process from Infineon Technologies AG. By avoiding the mandatory external filters of classical heterodyne receivers, a so-called "sliding-IF" double-conversion architecture offers more flexibility for the integration of a complete receiver on a single chip. As introduction, several receiver architectures are presented and the wave propagation effects at 17 GHz are discussed. Different levels of abstraction, starting with receiver specifications to building blocks are documented. Understanding the behaviour of a MOS transistor is important for high frequency circuit design. Integrated passive components are even more crucial to the performance of the building blocks and are described in depth. Design and measurement results of single building blocks, such as low noise amplifiers (LNA), mixers, dividers and voltage-controlled oscillators (VCO), demonstrate the functionality.
The fabricated testchip advances the state-of-the-art of receiver design. It has an area of only 1.2 mm^2, and a power consumption of 188.4 mW from a 1.5 V supply. The receiver includes a low-noise amplifier, a first down-conversion mixer, an IF-amplifier, I/Q-mixers, a fully integrated VCO, a 4:1 I/Q-divider and baseband amplifiers to drive the 50 Ω I/Q-outputs.
The main improvements over the state-of-the-art are a very high-level of integration, operation at a radio frequency of 17 GHz, and outstanding low power consumption.

Chapter 1

Introduction

Drawing on the expertise of hundreds of engineers from the communications industry, a hierarchy of complementary wireless standards has been established. Figure 1.1 shows the hierarchy, starting with the Personal Area Network (PAN), the next standard is the Local Area Network (LAN), followed by the Metropolitan Area Network (MAN) and the proposed standards for the Wide Area Network (WAN). Each standard represents the optimized technology for a distinct market and usage model and is designed to complement the others.

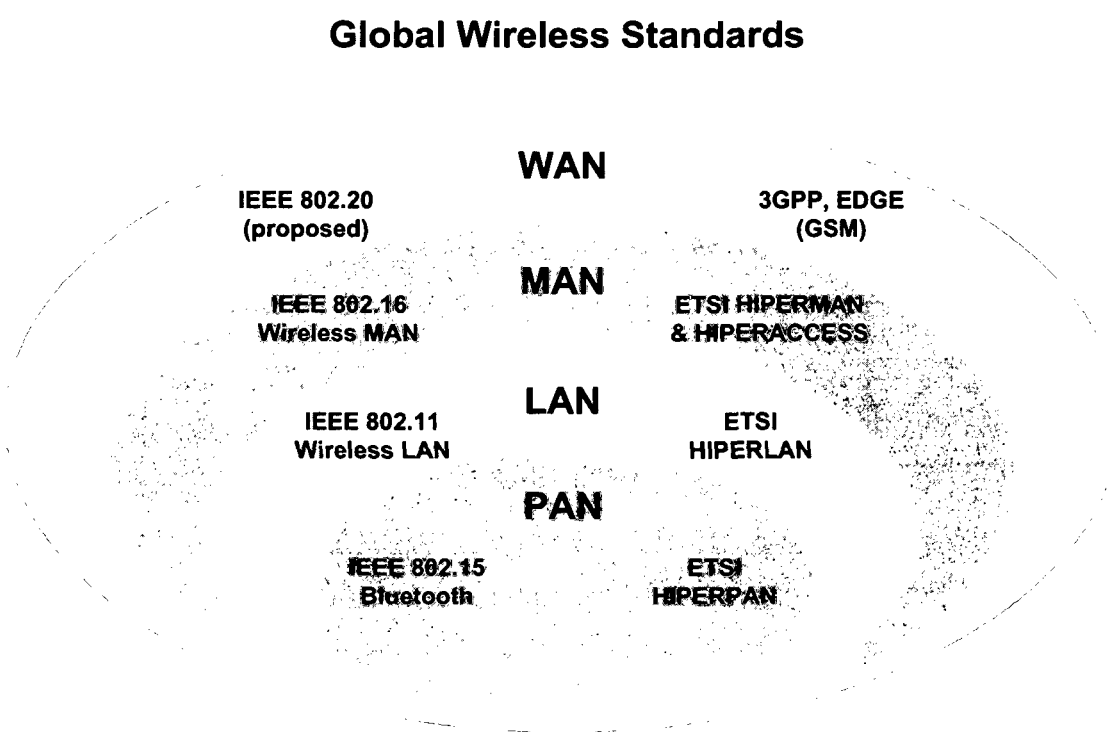

Figure 1.1: Global wireless standards to ensure interoperability.

The trend towards smaller equipments, portability and mobility in consumer electronics devices has led to the emergence of new classes of products. These products have rich functionality, multimedia capabilities, and require connection to other devices. Within the home, for instance, a family may have a digital video camcorder, digital camera, portable MP3 player, personal digital assistant (PDA), wireless speakers and tablet personal computer (PC). Each of these portable devices needs to be connected to other devices such as PCs or stationary consumer electronics products, i.e. stereos, televisions, video records, or the like. Figure 1.2 shows such a scenario with clusters for short range connection but also a long range backbone network.

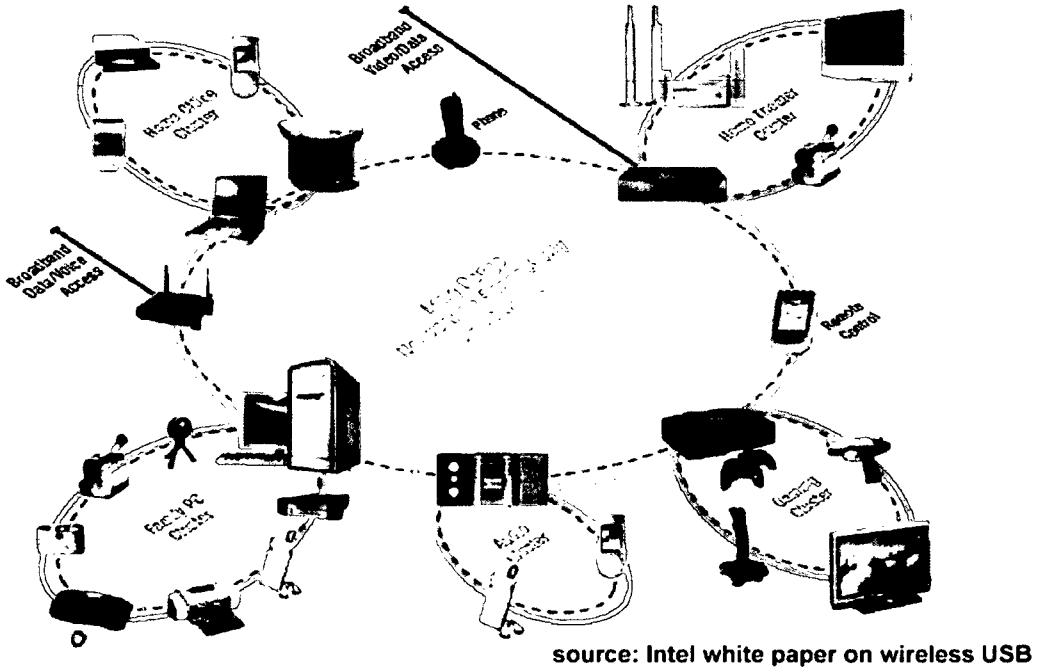

Figure 1.2: Home usage scenarios that could be wired or wireless.

Wireless Local Area Networks (WLAN) systems are increasingly used in offices, hotels and public places to provide high-speed wireless access for portable computers and other mobile devices. Wireless LANs are relatively cheap, easy to install and require no license for network operation. Current systems mostly use the 2.4 or 5 GHz frequency bands, where propagation conditions yield large cells and hence allow considerable area coverage with only a few Access Points (APs). If wireless traffic grows and network becomes congested, either the cell size must be reduced or an overlay network at another frequency band has to be deployed so that the increased capacity demand can be met.
In this work the second alternative is considered and a fully integrated 17 GHz CMOS receiver has been implemented and the performance was tested. The band between 17.1 and 17.3 GHz is suggested in [CEPT/ERC Rec 04] for the operation

of unlicensed Wireless LANs. In addition to provide larger bandwidth, operation at the 17 GHz band is also intended to be used as backbone for 2.4 or 5 GHz access points over a distance up to 100 m. Furthermore the 17 GHz link can be used as a short range high data rate wireless link. This is exactly the same application as the recently emerged wireless standard Ultra Wide-Band (UWB) [Intel 04]. Both applications are compared in Table 1.1.

Table 1.1: 17 GHz WLAN versus UWB.

	UWB	17 GHz WLAN
Frequency	3-5 GHz	17.1-17.3 GHz
Data Rate	up to 480 MBit/s	up to 155 MBit/s
Application	wireless USB (short range, high speed)	standard WLAN & high speed - short range
Standardization	open	open, but similar to WLAN at 2.4 and 5 GHz
Chip Size	small (5 GHz)	very small (17 GHz)

1.1 Current State-of-the-Art

The Integrated Circuit (IC) technology for most of the transceivers is CMOS. The fundamentals of Radio Frequency (RF) CMOS are still a topic of research with a substantial work on the building blocks and modeling as well as technology characterization [Kienmayer 04,c]. Radio frequency receiver integrated circuits require a combination of expertise in the areas of circuit design and system architecture along with the choice of a suitable process technology for the various applications. Table 1.2 presents some recently published transceiver work.

Table 1.2: Published state-of-the-art work.

	Technology	Level of Integration	Power consumption
Chapter 6	0.13 μm CMOS	17 GHz RX	188.4 mW
[Ahola $^{+}$04]	0.18 μm CMOS	2.4/5 GHz RX/TX	436 mW
[Yue 04]	0.18 μm SiGe-BiCMOS	17 GHz Down-converter	63 mW
[Bevilacqua 04]	0.18 μm CMOS	3.1 - 10.6 GHz LNA	9 mW
[Guan 04]	0.18 μm CMOS	24 GHz front-end	30 mW
[Girlando 04]	0.8 μm SiGe	12 GHz RX	540 mW
[Hashemi 04]	0.18 μm SiGe	24 GHz RX	910 mW

As can be seen from the Table 1.2, the RX power consumption of the current receiver is comparable to the 5 GHz receiver from [Ahola $^{+}$04]. Further, other

ICs for such high frequency applications make use of Silicon-Germanium (SiGe) technologies or use Silicon-on-Insulator (SOI) CMOS processes.

Chapter 2

Wireless LAN Systems

Wireless networks have enjoyed an increased demand from the general public as well as from business and other professional users. Section 2.1 introduces different wireless applications, especially WLAN. An overview of possible receiver architectures is presented in section 2.2 while propagation effects are discussed in Section 2.3.

2.1 Introduction

The IEEE 802.11 Wireless LAN specification was published to extend the functionality provided by the IEEE 802.3 Wired LAN standard. A radio interface for wireless communications adds considerable complexity. However, advances in highly integrated radio circuitry have made it possible to bring the cost of wireless devices down to affordable levels.
An alternative specification for WLAN is from the European Telecommunications Standards Institute (ETSI) suggested Broadband Radio Access Network (BRAN) HiperLAN/2, with more extensive services, but diminishing commercial support (Table 2.1). The operation of the radio frequency part is in a similar way to 802.11a standard. Numerous techniques have already used for wired LAN to deal with multiple users who have access to the central server, additional steps must be taken in order to deal with the sudden breaddown of WLAN links. A WLAN link has many less-than-ideal transmission characteristics, such as the dependency of signal errors on physical position and the possibility of nearby RF devices to "eavesdrop" or interfere. As the name implies, WLAN was designed to extend the data transfer function of a wired LAN. Table 2.1 shows an overview of current BRAN wireless system types and definitions. Mobility, data rates and power consumption will be the main requirements to WLAN systems. Figure 2.1 shows a comparison of technologies, mobility and data rates.

Table 2.1: Summary of current BRAN system types and definitions.

BRAN System	Use	Expected majority use	Frequency Band	Mobility	Range	Rate Mbit/s
HIPERLAN 1	wireless LAN	indoor	5.15 to 5.25 GHz [5.25 to 5.3] GHz	ambulant	50 m	20
HIPERLAN 2	wireless access, ATM or IP	indoor	around 5 GHz	ambulant	50 m	25
HIPERLINK	wireless infrastructure	indoor private networks, outdoor	17.1 GHz to 17.3 GHz	fixed	150 m	155
HIPERACCESS/E HA/E (Exempt)	wireless access, ATM or IP	outdoor, private networks	around 5 GHz	fixed	0.5 km to 5 km	25
HIPERACCESS/U HA/U (Urban)	urban fixed access, ATM or IP	outdoor, public operator	>10 GHz	fixed	0.5 km to 5 km	25
HIPERACCESS/R HA/R (Rural)	rural fixed access, ATM or IP	outdoor, public operator	<10 GHz	fixed	0.5 km to 5 km	25

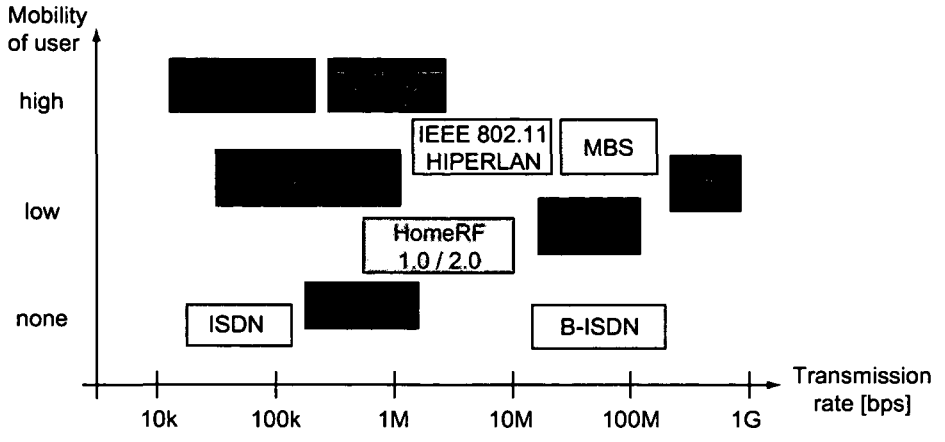

Figure 2.1: Technology, mobility and data rates of communication systems.

One can observe several applications in parallel:

- *Bluetooth*: A standard technology for low-cost, low power short range wireless communications. First specified in 1999 (Version 1.0) several promoter companies build up the Bluetooth Special Interest Group (SIG) [SIG 01]. The actual Bluetooth specification Version 1.1 uses the frequency range location of $f = (2402 + k)\,MHz$, $k = 0, \ldots, 78$ for the majority of the countries around the world. Bluetooth uses frequency hopping spread spectrum (FHSS) technique with 1 MHz of frequency spacing. Furthermore, it features a maximum data throughput up to 1 Mbit/s.

- *Wireless LAN*: There exist several Wireless LAN standards, all starting with IEEE 802.11x. In the 2.4 GHz band, the most popular WLAN standard is IEEE 802.11b. It features a maximum throughput of 11 Mbit/s and uses a Direct Sequence Spread Spectrum (DSSS) modulation. Like coaxial cable based Ethernet IEEE 802.3 (10Base-2), it uses Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA). 802.11b operates between 2.4 and 2.483 GHz with 3 channels of each 11 Mbit/s allowing a maximum of 192 users.

- *UWB*: Wireless USB has a targeted bandwidth of 480 Mbps at launch, which is comparable to the current wired USB 2.0 standard, and will feature wireless high-data throughput with low power consumption for distances less than 10 meters. The Wireless USB interface will deliver the benefits of high-speed wireless connectivity, security, ease-of-use and backward compatibility to customers.

- *WiMAX*: WiMAX, or 802.16, is a fast-emerging wide-area broadband technology that shows great promise as the "last mile" solution for bringing high-speed Internet access into homes and businesses. It can provide data

rates up to 75 Mbps per base station with typically cell sizes of 2 to 10 kilometers.

- *Cordless Phones*: In U.S. DECT-like cordless phone standards are found in the 2.4 GHz frequency band with similar requirements as in the European counterpart.
- *GSM/UMTS*
- *Wireless Audio/Video Connection Systems*
- *Movement Detection Systems*

2.2 Receiver Architectures

A wireless receiver is typically composed of two sections: an analog front end and a baseband digital processor. The analog section receives the modulated RF signal and the down-converted signal can be either demodulated in the analog domain or converted to a digital signal by means of an analog-to-digital converter (ADC) and then demodulated. In order to improve the sensitivity of the receiver, the RF signal is amplified before down-conversion. For the suppression of interferers, the baseband signal is applied to a channel-select filter before detection.
In this section, three different receiver architectures are compared. When designing RF receivers, the choice of architecture is primarily determined by criterias including complexity, aspects of the design, power dissipation, noise and the number of external components.

2.2.1 Homodyne or Zero-IF Receiver

In a homodyne or direct conversion receiver, the incoming RF signal is directly down-converted to zero-IF in one step by mixing with an local oscillator (LO) output (see Figure 2.2 and 2.3). Therefore, in this type of the receiver, the LO frequency is equal to the RF. The baseband signal is then filtered with a low-pass filter to select the desired channel. This is illustrated in the block diagram in Figure 2.2.

For frequency- and phase-modulated signals, the down-conversion must provide quadrature outputs in order to avoid loss of information. The main advantage of a homodyne receiver is that it does not possess the image problem as the incoming RF signal is down-converted directly to baseband without any IF stage. Another advantage is its simplicity. The major disadvantage is that severe DC offsets can be generated at the output of the mixer when the leakage from the local oscillator is mixed with the local oscillator signal itself. This effect could saturate the following stages. Equally critical is the flicker noise of the mixer since the mixer output is a baseband signal and can be easily corrupted by large noise.

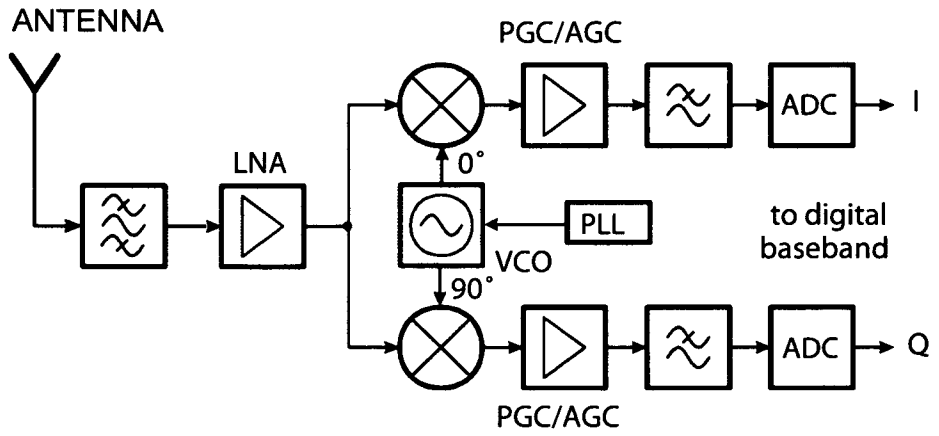

Figure 2.2: Block diagram of a homodyne I/Q receiver.

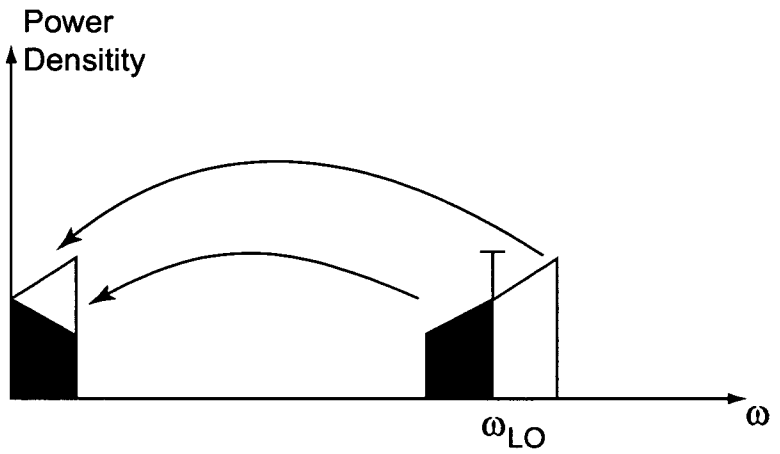

Figure 2.3: Frequency translation in a zero-IF receiver.

2.2.2 Heterodyne or IF Receivers

The most straightforward architecture for implementing a cellular receiver front-end is evidently the heterodyne receiver (see Figure 2.4 and 2.5). Its main feature is the use of an intermediate frequency (IF). For this reason the heterodyne receiver is often also called the IF receiver.

The RF signal from the antenna is first filtered by a band select filter that removes out-of-band signals. These signals could saturate the following stages. An LNA amplifies the signal, which is then filtered by an image-reject filter to remove the image. The image has an offset of twice the intermediate frequency (IF) from the desired channel signal, before being down-converted to the intermediate frequency by the mixer. A channel-select filter performs the channel selection of the IF and demodulation or detection is carried out to retrieve the desired information.

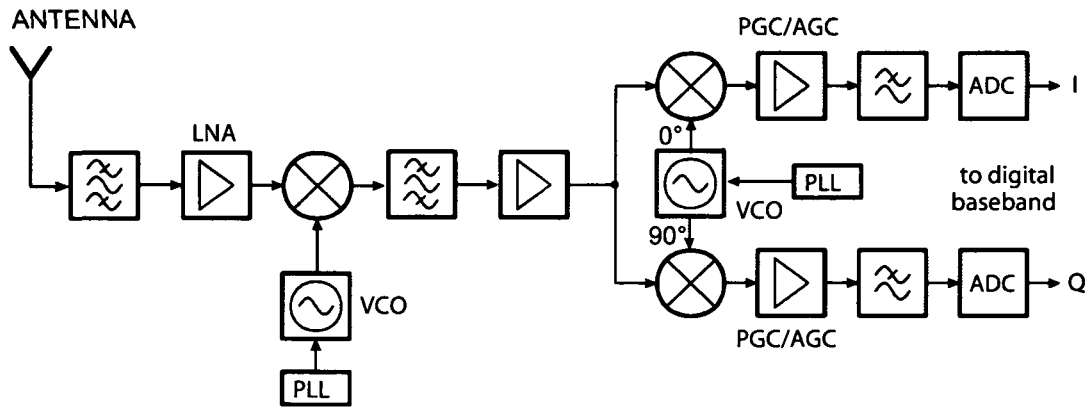

Figure 2.4: Block diagram of a heterodyne receiver.

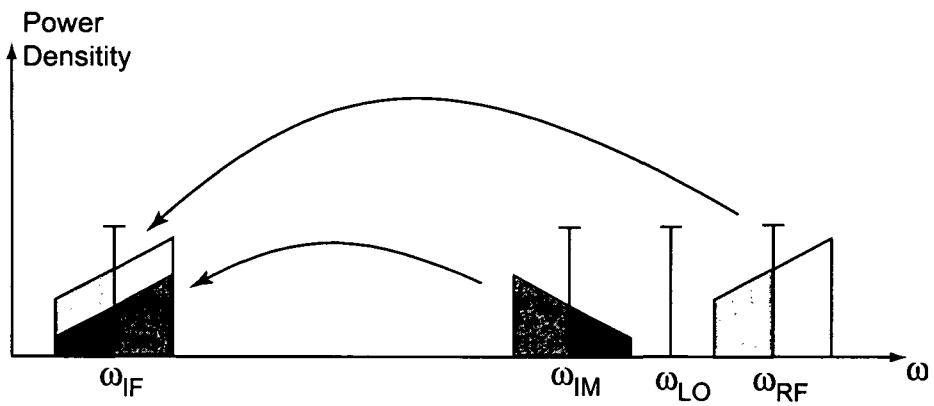

Figure 2.5: Frequency translation in an IF receiver.

The image has to be suppressed before it is mixed down to the IF. This is done by the means of a high frequency (HF) filter. Such a HF filter can only be realized when the IF is high enough because the wanted signal must be relatively far away from the mirror frequency. However, the HF filter and the channel selection filter requires a very high Q-factor, which is defined as the ratio of the center frequency to the 3 dB bandwidth. If the IF is low, the channel selection has a more relaxed requirement, but proper image suppression becomes harder to achieve. HF filters are therefore always realized as discrete off-chip components, but these are very expensive and vulnerable in use. Off-chip components require extra handling, extra board space and an increased pin-count and come along with reduction of board yield.

2.2.3 Sliding IF Receiver

In a heterodyne architecture, the IF is fixed because of the external high quality filters. A sliding IF receiver makes use of only one oscillator for both mixing stages. In this case, the IF is no longer fixed and the signal is *sliding*. In Figure 2.6 a block diagram of such a sliding IF architecture is shown which is reported by [Tadjpour 01].

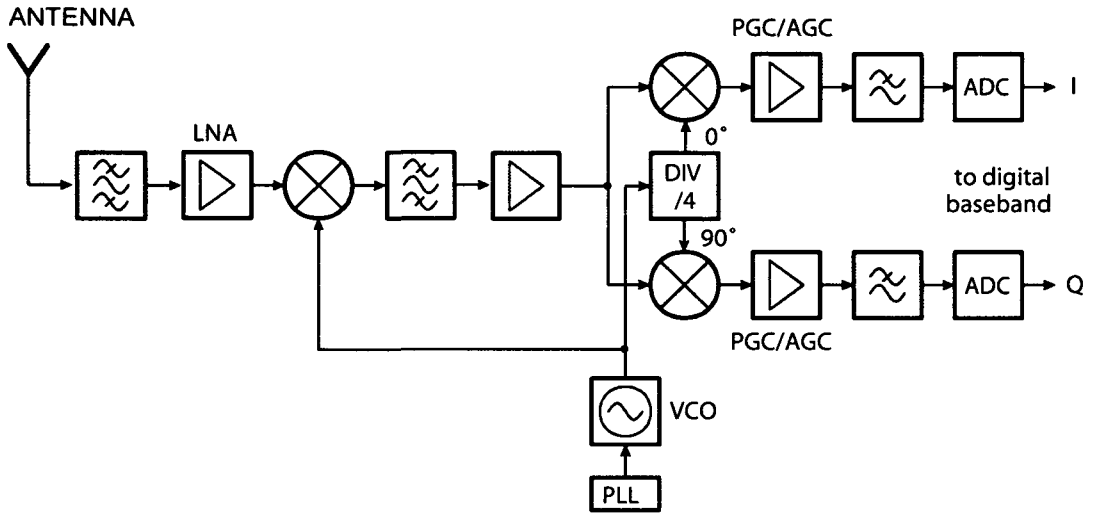

Figure 2.6: Block diagram of a sliding IF receiver.

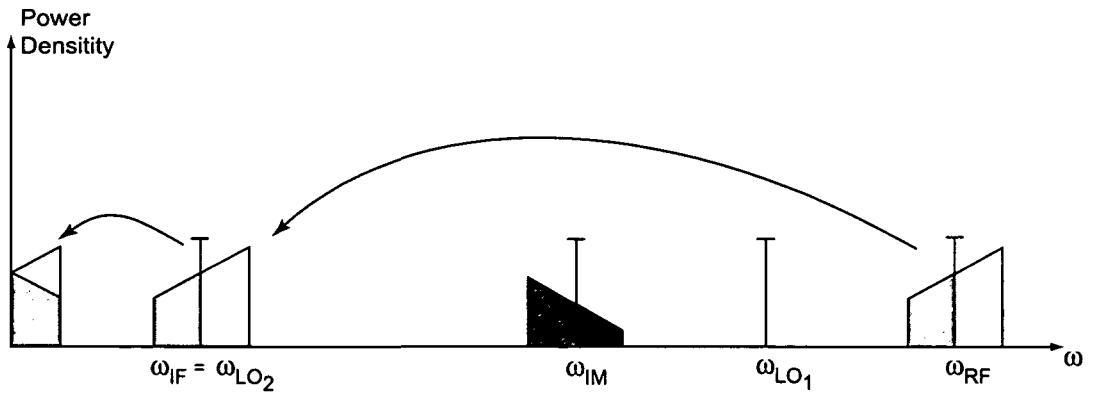

Figure 2.7: Frequency translation in a sliding IF receiver.

The diagram shows a special case using a 4:1 divider, but in general any ratio for the second mixing stage can be chosen. As shown, innovation of only one VCO increases the integrity. Furthermore, the usage of two mixers suppresses the effects of flicker noise because the first and second down-converting mixers can be optimized for high gain and low flicker noise respectively.

2.3 Propagation Effects

Signal propagation is an external phenomenon that does not occur in the receiver but its effects have significant impact on the receiver signal integrity. In addition, better understanding of the overall system from the transmitter, through the propagation medium and to the receiver can provide the designer with very useful insight [Vaughan 03].

2.3.1 Path Loss

In general, the path loss, as a deterministic parameter, is defined in the following way. Let P_T be the power delivered by the transmitter with antenna gain G_T while P_R is the received power with G_R, gain of the receiving antenna. The relation between the received power P_R and the transmitted power P_T is given the Friis transmission equation

$$\frac{P_R}{P_T} = G_T G_R \frac{1}{L_P}. \tag{2.1}$$

The path loss L_P in free space is given by the expression

$$L_P = \left(\frac{4\pi d}{\lambda}\right)^2 = \left(\frac{4\pi df}{c}\right)^2. \tag{2.2}$$

where d is the distance between transmitter and receiver, f the frequency, λ the wavelength and c is the speed of light in vacuum ($3 \cdot 10^8 m/s$). The frequency of operation and the distance in a wireless communication link determine the path loss. The relationship 2.1 that describes the propagation of a signal from the transmitter, through the air to a receiver is also well known in its logarithmic form as

$$P_R = P_T + G_T - L_P + G_R\,[dBm]. \tag{2.3}$$

2.3.2 Multipath and Fading

The signal from the transmitter arrives at the receiver not only along the direct path but also via various other paths as a result of reflection and diffraction caused by obstacles in the signal path.
Propagation conditions on these additional paths differ from those on the direct path. For instance, we can expect signals traveling via additional paths to exhibit:

- longer travel times because of increased path length
- various strengths
- different Doppler shifts

Because of the different travel times, the signals arrive with a different phase at the receiving antenna. Depending on this phase, components may be canceled or added to a high-quality signal which is received in a relatively short span of time. Figure 2.8 shows such a scenario, where multiple reflections of the same signal arrive at the receiving antenna with different phase and amplitude.

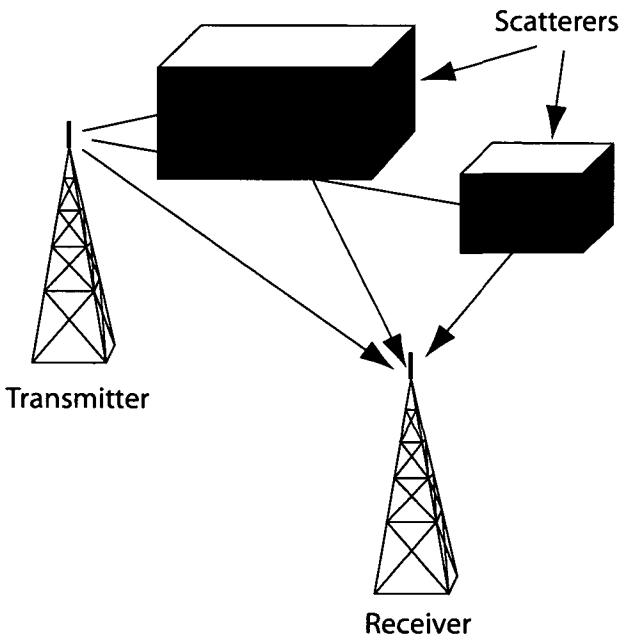

Figure 2.8: Outdoor scenario for a multipath link.

2.3.3 Equalization

Equalization is used to reduce intersymbol interference (ISI) caused by multipath propagation within the channels. This form of interference occurs when the radio channel bandwidth truncates the signal modulation bandwidth, resulting in time spreading of modulation pulses.
To reduce ISI in a mobile environment, adaptive equalization is used to track the time-varying characteristics of the channel. Typically, a known training sequence is transmitted to characterize the channel. The received information is then manipulated to calculate and set the proper filter coefficients for equalization in the receiver back-end. The data is transmitted following the training sequence while the received data is corrected by the equalizer. In an adaptive equalizer, the filter coefficients of the equalizer are constantly optimized to compensate the changing radio channel.

2.3.4 Diversity

An alternative way to reduce severity of fading is diversity. There are several diversity techniques available such as polarization, time and frequency diversity, but the most common diversity technique is spatial diversity. In this technique, multiple receiver antennas are strategically placed at different locations which allows the antennas to receive different versions of the transmitted signal, thus providing the receiver with a choice of which version to use.

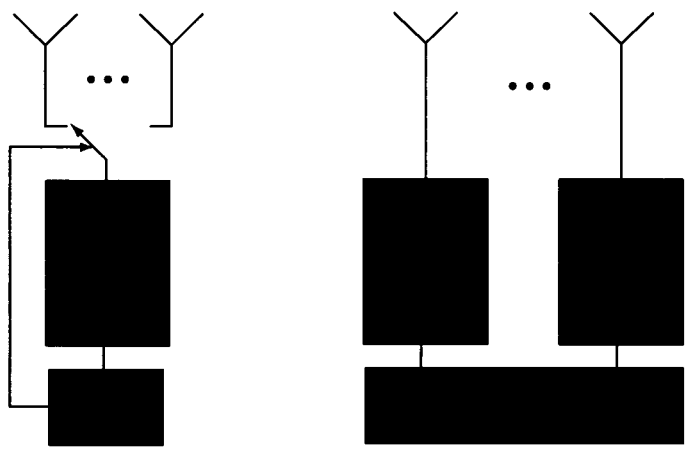

Figure 2.9: Block diagram of a receiver using antenna diversity (a), and a complete receive-chain diversity (b).

As shown in Figure 2.9, there are two different methods to implement a spatial diversity receiver. In one method, the receiver can switch between multiple antennas. This requires the receiver to first test each connected antenna and then make a decision. This is method is called antenna diversity. In the second method, multiple independent receiver paths with their own antennas are used. In this case, the receiver back-end has both signals available simultaneously and is able to choose the better one.

2.3.5 Coding

Another method to improve the performance of the communication link is channel coding. In this technique, redundant data bits are added to the original message prior to modulation and transmission of the signal. These added bits follow specific code sequences that help the receiver to detect and correct some or all of the error created by the radio channel. The addition of coding bits however reduces the overall channel capacity but is very effective in reducing errors.

Chapter 3

CMOS Technology

The C11N fabrication process is a CMOS 0.13 μm generation foundry technology, designed for SRAM, logic, mixed signal and mixed-voltage I/O applications. It provides a platform technology for embedded DRAM. This chapter gives a short overview of the implemented CMOS technology.

Section 3.1 shows the behaviour of the nMOS transistor. Section 3.2 discusses the passive devices used for the circuit design. Section 3.3 presents an overview of the C11N CMOS technology, in particular.

3.1 The nMOS Transistor

A typical cross-section of commonly used sub-μm CMOS technology transistor is presented in Figure 3.1. On the left side, an NMOS-transistor is depicted and

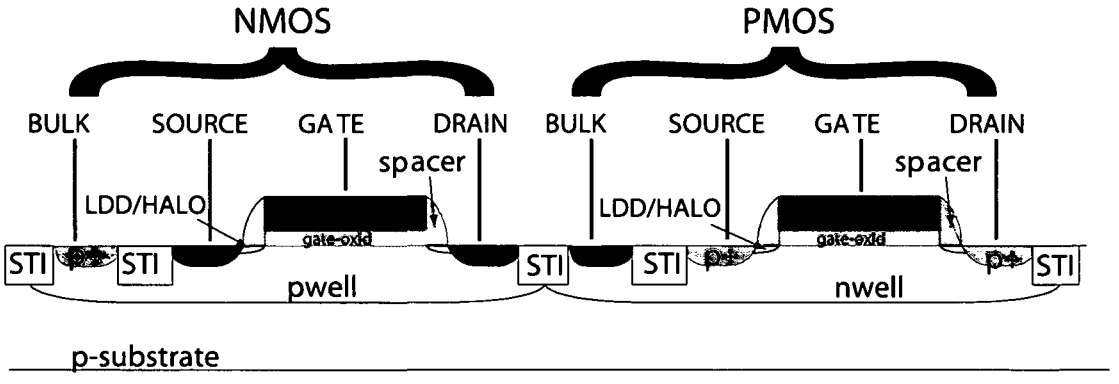

Figure 3.1: Typical sub-μm CMOS technology transistor cross-section.

on the right side a PMOS-transistor, respectively. For both transistors, all four terminals including their backgates (bulks) are shown. Fabricated on a p-type substrate (also called the "bulk" or the "body"), the NMOS-device consists of

two heavily-doped n regions forming the source and drain terminals. A heavily-doped (conductive) piece of polysilicon (often simply called "poly") is operating as the gate while a thin layer of silicon dioxide (SiO_2) insulates the gate from the substrate. The desired action of the device occurs in the substrate region under the gate oxide. Note that the structure is symmetric with respect to source and drain. The PMOS-device consists of heavily-doped p regions instead of n regions. Current technologies use shallow trench isolations (STI) to isolate transistors enabling a higher transistor density. A lightly doped drain (LDD) extension is inserted to avoid hot electron effects which cause reliability and lifetime degeneration. Further, short channel device optimization is obtained through the HALO-extension.

A typical 0.13 μm standard CMOS transistor layout for high frequency operations is shown in Figure 3.2. Instead of one single transistor with a width W of 21 μm, the transistor consists of 6 parallel connected 3.5 μm wide transistor gates. This folded structure exhibits substantially less drain junction capacitance while providing the same width-length ratio (W/L) [Razavi 99].

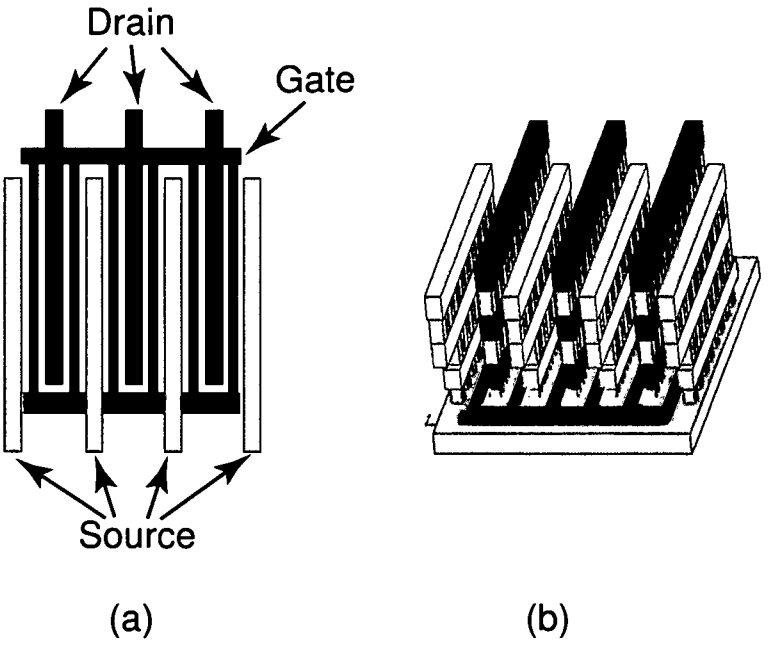

Figure 3.2: Layout of a folded MOS transistor (a) planar cut (b) 3D view.

Furthermore, the effective gate series resistance is reduced by the folding factor n squared:

$$R_{Gate} = \frac{R_g/sq}{3} \cdot \frac{W}{n^2 L}, \tag{3.1}$$

where R_g/sq denotes the sheet resistance of the gate material (typically 7 Ω/sq), W is the total width and L the total length of the transistor. For RF analog

circuits, however, the capacitances associated with the devices must also be taken into account. These relevant capacitances are shown in a three dimensional figure (Figure 3.3) of an NMOS device embedded in a p-substrate.

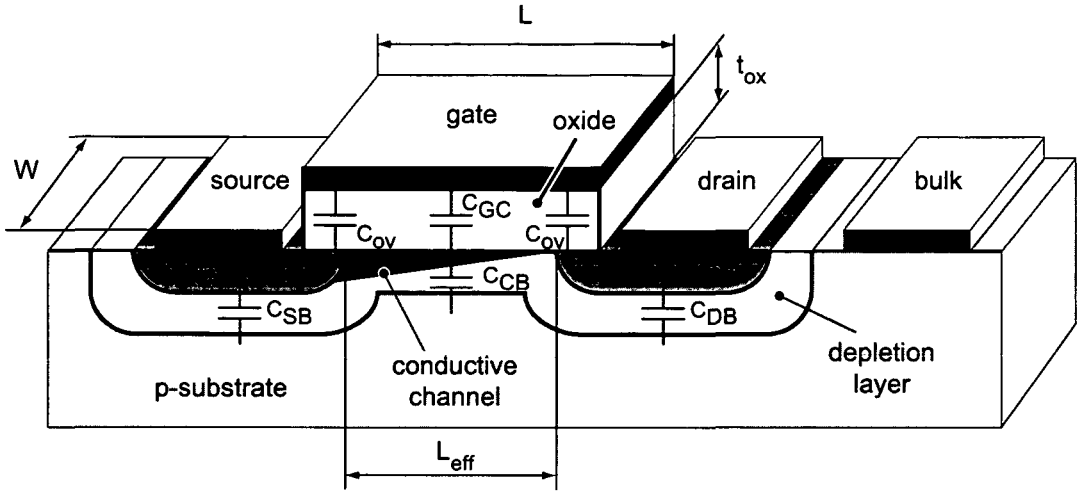

Figure 3.3: n-channel MOSFET with parasitic capacitances.

The conductive channel is drawn at the boundary between linear and saturation region. Each parasitic capacitance may depend on the bias conditions of the transistor. From the Figure, the following capacitances can be identified:

Oxide Capacitance: The contribution of *gate-to-channel* capacitance C_{GC} to the terminal capacitances depends on the operation region of the device. Total value C_{oxt} equals $C_{ox}\mathrm{W}L_{eff}$.

Depletion Capacitance: The *channel-bulk* junction capacitance C_{CB} is the controlling capacitance of the device. The *source-bulk* and *drain-bulk* junction capacitances C_{SB} and C_{DB} consist of a bottom-plate capacitance associated with the bottom of the junction, and a side wall capacitance due to the perimeter of the junction.

Overlap Capacitance: The overlap capacitance C_{OV} is a result of the gate overlapping with source and drain area by an amount of $L - L_{eff}$.

nMOS in Linear Region

The linear region of operation is defined as one in which V_{gs} is large enough to guarantee an inversion layer from source to drain. The boundary between linear and saturation region is defined by

$$V_{ds} = V_{gs} - V_T = V_{dsat}. \tag{3.2}$$

As long as V_{ds} is smaller than V_{dsat}, the device will be in the linear region of operation. The drain current is proportional to charge times velocity. The derived expression for the drain current in linear region is

$$I_d = \mu_n C_{ox} \frac{W}{L} \left[(V_{gs} - V_T) V_{ds} - \frac{V_{ds}^2}{2} \right]. \tag{3.3}$$

where W is the width of the device, L is the length of the gate and μ_n represents the mobility of electrons in the channel. C_{ox} is the total gate oxide capacitance per unit area

$$C_{ox} = \varepsilon_{ox} / t_{ox} \tag{3.4}$$

where ε_{ox} is the dielectric constant and t_{ox} the thickness of the oxide. The relationship between drain current and drain-to-source voltage is nearly linear for small voltages V_{ds}. An nMOS in the linear region behave like a voltage controlled resistor.
The transconductance of such a device in linear region is easily found by differentiating the expression of Eqn. 3.3 for drain current:

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{ds}. \tag{3.5}$$

nMOS in Saturation Region

When V_{ds} is high enough so that the inversion layer does not extend all over from the drain to source, the device is in saturation. In this case, the channel charge stays constant. The drain current is also constant while V_{ds} is rising.
The drain current in saturation region can be derived from Eqn. 3.3 by substituting V_{ds} by V_{dsat}.

$$I_d = \mu_n C_{ox} \frac{W}{L} \left[(V_{gs} - V_T) V_{dsat} - \frac{V_{dsat}^2}{2} \right]. \tag{3.6}$$

Using Eqn. 3.2, this expression simplifies to

$$I_d = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_T)^2. \tag{3.7}$$

In saturation, the drain current has a square-law dependence on the gate-source voltage and is independent of the drain-voltage. Again, the transconductance of the device in saturation is easily found by differentiating the expression Eqn. 3.7 for drain current

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{ds} - V_T). \tag{3.8}$$

which can also be written as

$$g_m = \sqrt{2 \mu_n C_{ox} \frac{W}{L} I_d}. \tag{3.9}$$

In order to represent the behavior of transistors in circuit simulations, an accurate model of the NMOS-device is required. For RF-simulations the subcircuit model of Figure 3.4 is preferred which goes in hand with the industry-standard *Berkeley BSIM model* [UC Berkeley 04].

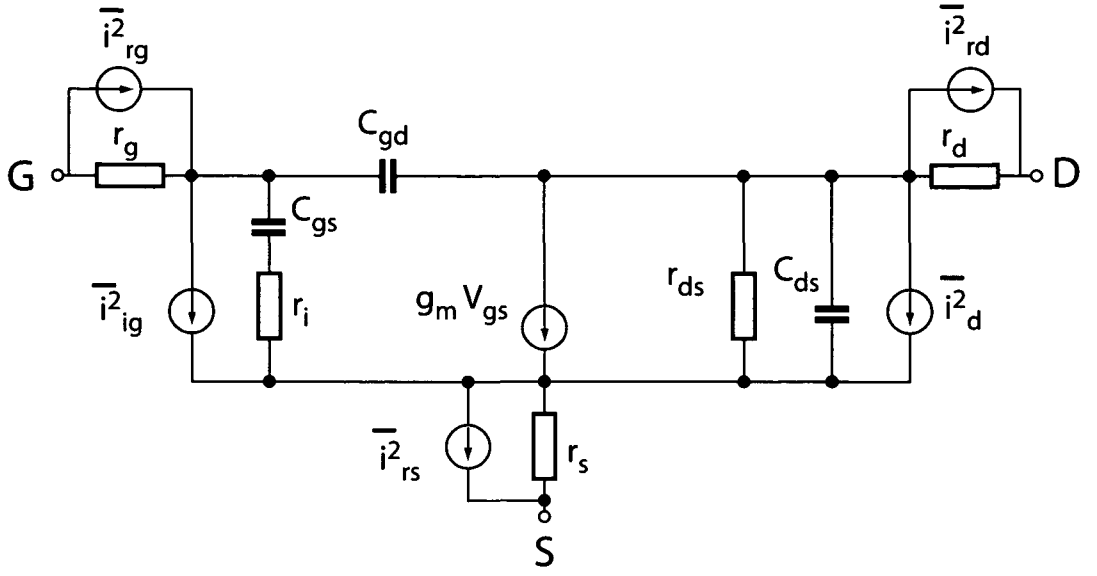

Figure 3.4: Small signal model including the noise sources.

The series resistances of gate, source and drain can not be neglected at high frequencies due to the low-pass poles and the contributed white noise ($\overline{i_{rg}^2}$, $\overline{i_{rd}^2}$, $\overline{i_{rs}^2}$). The channel charging resistance r_i models the phenomenon that the channel can not instantaneously respond to changes of the gate-source voltage [Manku 99]. The channel charging resistance is given by

$$r_i = \frac{1}{5g_m}, \tag{3.10}$$

which has been theoretically proven. In Equation 3.10 g_m represents the transconductance of the transistor. The drain channel noise consists of flicker noise and thermal noise generated by carriers in the channel. The drain channel noise is typically given as

$$\overline{i_d^2} = 4kT\gamma g_m \triangle f. \tag{3.11}$$

Here, γ is a bias-dependent parameter, where $\gamma = 2/3$ for long channel devices, k is the Boltzmann's constant, T is the temperature of the carriers in the channel, and $\triangle f$ is the noise bandwidth. In deep sub-micron processes γ might rather equal to 1 for relevant analog RF operating points [Brederlow 02]. Further, the induced gate noise is generated in the channel standard flicker noise and coupled through the gate as a gate current. At low frequencies this gate induced noise

current can be neglected. Nevertheless, at high frequencies it must be taken into account and is expressed as

$$\overline{i_{ig}^2} = 4kT\delta g_g \triangle f \tag{3.12}$$

with $\delta = 2\gamma$ and

$$g_g = \frac{(\omega C_{gs})^2}{5g_m}. \tag{3.13}$$

Since the drain channel noise and induced gate noise arise from the same source, they are correlated with a factor c [Manku 99].
Additionally, in the case of high-frequency performance two figures of merit are popular. These are f_t and f_{max}. The transit frequency is defined as the frequency where

$$\left|\frac{i_d}{i_g}\right| \equiv 1, \tag{3.14}$$

where i_d is the drain current and i_g is the gate current. Perhaps more relevant than f_t is the frequency at which the maximum available power gain is extrapolated to fall to unity. However, computing f_{max} is in general quite difficult and we will take an expression from [Lee 98] for the maximum oscillation frequency

$$f_{max} \approx \sqrt{\frac{f_t}{8\pi r_g C_{gd}}}, \tag{3.15}$$

where r_g is the series gate resistance and C_{gd} is gate-drain capacitance.
The manufactured nMOS transistors in 0.13 μm CMOS have a cutoff frequency f_t of 100 GHz and a maximum oscillation frequency f_{max} of 50 GHz respectively [Schiml 01]. The devices have typically a qualified maximum supply voltage of 1.5 V.

3.2 Passive Devices

Passive devices are of main interest in analog RF-circuit design. These include inductors, capacitors, resistors and varactors. This subchapter gives an overview of the main properties of these devices.

3.2.1 Inductors

Inductors are widely used in RF circuits, e.g. as inductive load or matching element in LNA or as part of the frequency determining LC-tank in voltage-controlled oscillators. Integrated inductors can be realized as planar structures using metal layers. Modern CMOS processes offer 4 to 9 metal layers which are intended for circuit wiring and used for inductor design. Various layout structures for integrated inductors have been discussed and presented in literature

[Ashby 96][Yue 98][Niknejad 00]. For conducting metal layers copper (conductivity $\sigma = 57.14\,\mathrm{S/m}$) or aluminum ($\sigma = 37.7\,\mathrm{S/m}$) are used. The metal layers reside on top of the substrate and are usually embedded in silicon dioxide SiO_2 (relative permittivity $\varepsilon_r \approx 4$). The substrate has a typical conductivity of $\sigma = 20\,\mathrm{S/m}$ and

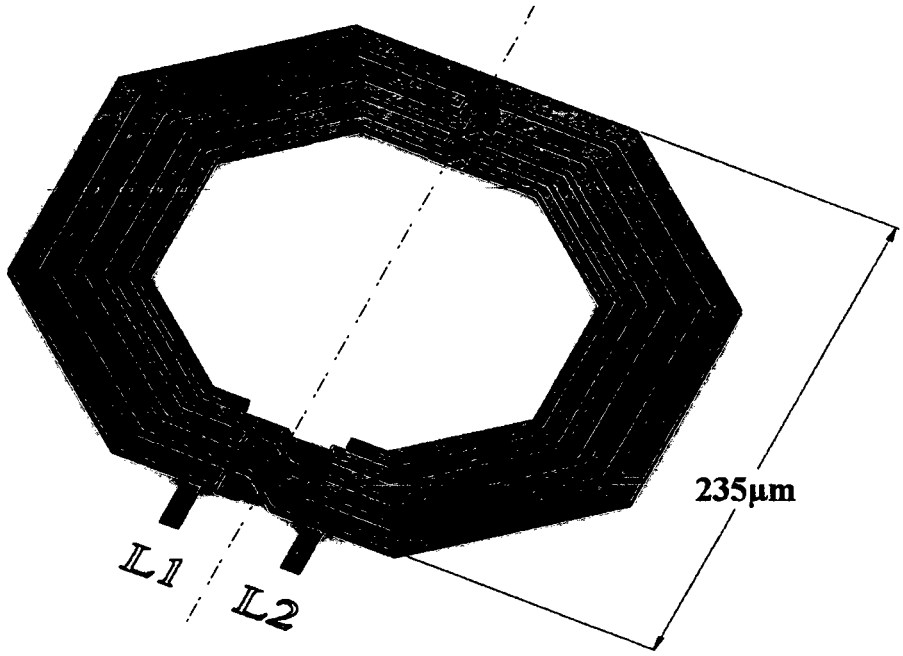

Figure 3.5: Cross-coupled symmetrical inductor for a resonant frequency of 3.4 GHz.

a relative permittivity of $\varepsilon_r \approx 12$. Usually two metal layers are shunt connected using VIA bars as intermetallic stripes along the winding. Thereby, the series resistance of the windings is reduced up to 60%.
Figure 3.5 shows an example of a cross-coupled symmetrical integrated inductor. Desiring highly integrated receivers, the symmetrical inductor layout is generally preferred for its inherently better insensitivity to substrate noise.

Main disadvantage is the more complicated layout and modeling. A center tap to the inductor is easily realized as common-mode access point or as direct current (DC) biasing connection. At least two metal layers are needed for the turns else it would be impossible to connect the turns to each other. Figure 3.6 shows how the crossing of the individual turns is realized by the metal layers.

For electrical characterization, several models exist, which differ in their complexity. The aim of a lumped, lower order model is to characterize the integrated

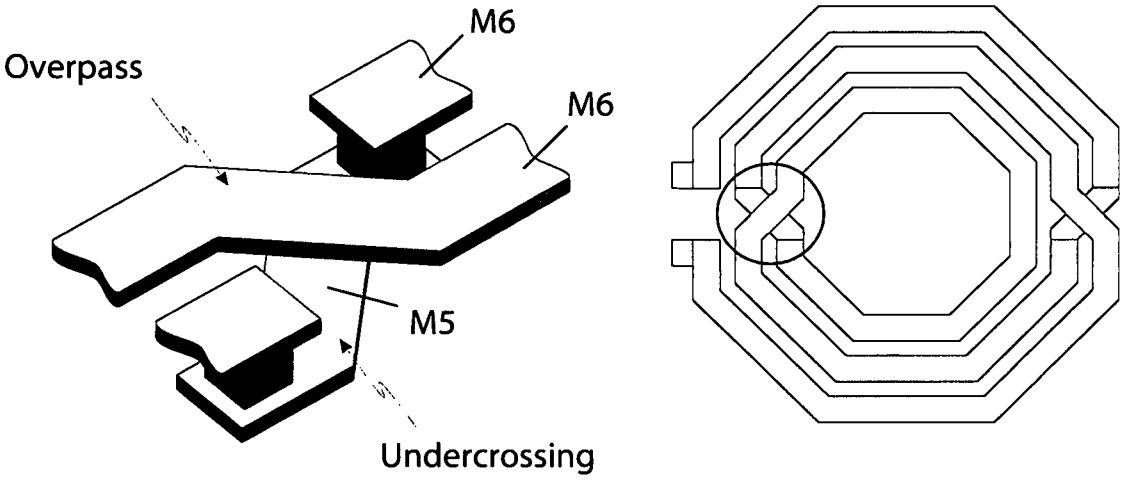

Figure 3.6: Symmetrical inductor

inductor with a minimum number of discrete components. A detailed derivation of the lumped low order model for inductors can be found in [Thüringer 02]. Here, only a brief insight into the modeling process is given. Figure 3.7 shows the cross-section of an integrated inductor together with discrete elements to model the various parasitics.

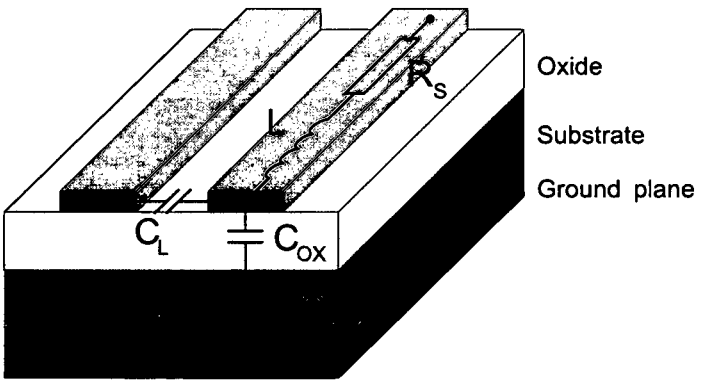

Figure 3.7: Inductor cross-section and parasitic components

What follows is a short explanation of the various components found in the lumped low order model:

- L: The inductance is caused by the magnetic flux density $\vec{B}$ of the electromagnetic field.
- R_{Sub}: The resistance R_{Sub} is used to model the ohmic losses in the substrate.

- R_S: The resistance R_S characterizes the series resistance of the metal traces with finite conductivity as well as the skin-effect and current crowding. For all inductors in this work, the metal series resistance is dominant due to the thin metal layers in standard CMOS. Therefore R_S equals to the DC series resistance, neglecting skin effects and current crowding.
- C_L: The capacitive coupling between the turns of the inductor is modeled with the lateral coupling capacitance C_L.
- C_{OX}: Models the capacitance between inductor and substrate.
- C_{Sub}: The capacitance C_{Sub} is used to characterize the capacitance in the substrate. Due the highly conductive substrates typically used in standard CMOS processes (1 to 6 Ωcm), C_{Sub} is neglected.

It is important to note that the whole inductor is modeled with these components, hence a minimum number of discrete elements is used in the modeling process. The resulting electrical circuit is now easily obtained. The use of a π-circuit is appropriate, since the inductor is a two-port device. The series branch of the π-circuit corresponds to the winding of the inductor, so the inductance L and series resistance R_s are placed here as well as the lateral coupling capacitance C_L. Since we assume static parasitic components, the overall resistances and capacitances to the substrate can be split into two equal parts to complete the equivalent electrical circuit. The values are divided as follows:

$$C_{ox1} = C_{ox2} = \frac{C_{ox}}{2} \tag{3.16}$$

$$R_{sub1} = R_{sub2} = 2 \cdot R_{sub} \tag{3.17}$$

$$C_{sub1} = C_{sub2} = \frac{C_{sub}}{2} \tag{3.18}$$

Figure 3.8 shows the resultant electrical circuit. In [Wohlmuth 00], [Kehrer 01], [Thüringer 02] and [M. Engl 03] detailed methods and algorithms for the calculation of these lumped components can be found. For simple spiral coils, C_L can be neglected as the voltage difference between neighboring windings is small.

For symmetrical inductors (Figure 3.6) the single-π lumped model must be extended to the double π model as presented in Figure 3.9. The double π-model allows an accurate modeling of the coil, in balanced as well as in single-ended operation mode. E.g. in balanced mode the capacitor at the middle node completely disappears, causing a totally different self-resonance frequency. The meaning of the model parameters is the same as for the single-π model, only a form factor f is introduced to distribute the overall parasitics to each branch. This form factor depends on the winding staggering. For coils without winding staggering $f = 0.25$. In contrast to simple spiral coils, the lateral winding to winding capacitance C_L cannot be neglected as the voltage difference between neighboring

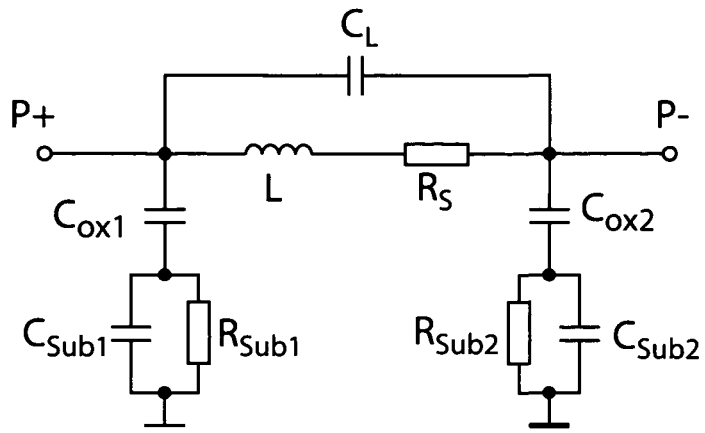

Figure 3.8: Low order equivalent circuit

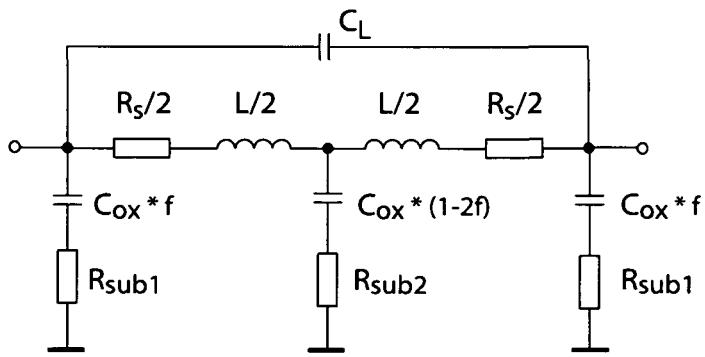

Figure 3.9: Differential inductor lumped model.

windings is maximal due to the differential winding scheme.
Alternatively, commercial 3D electromagnetic simulators like HFSS [HFSS 04] or Agilent MOMENTUM [Momentum 04] can be used to estimate the behaviour of the inductors. These simulators require long simulation times hence run-times are too long to optimize the coils. For a fast and acceptable model estimation, the public domain M.I.T. simulators FASTHENRY [M.I.T. 04,b] and FASTCAP [M.I.T. 04,a] can be combined to provide the magnetical and electrical parts of the lumped model which is described in more detail in [Kehrer 01]. The shorter calculation time of this approach allows a qualitative optimization of integrated inductors.

3.2.2 Capacitors

Considering highly integrated transceivers in CMOS, linear capacitors are mainly needed for filtering, for AC-coupling and for inductor-capacitors tanks. Addition-

ally, a capacitor in combination with a MOS-switch can be used to switch the center frequencies of VCOs [Kral 98] or LNAs [Darabi 00]. Linear RF-capacitors can be modeled by the lumped π-model presented in Figure 3.10.

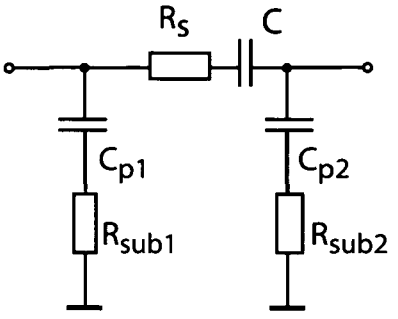

Figure 3.10: RF-capacitor lumped model.

There are two main design parameters for RF-capacitor design, the quality factor Q and ratio C/C_p, respectively. The quality factor, which is given as

$$Q_c = \frac{1}{j\omega R_s C}, \tag{3.19}$$

is dominated by the series resistance. The ratio of wanted to parasitic capacitance C/C_p. This ratio is best for Metal-Insulator-Metal (MIM) capacitors situated on the top metal layers. Poly-Interpoly-Poly (PIP) or standard metal layer based capacitors feature worse values for C/C_p of about 10% to 20%.

3.2.3 Varactors

MOS varactors are variable, voltage-controlled capacitors based on the MOS structure. The use of a MOS-device as varactor has been published before [Panasonic 82] and is well known [Porret 00]. Their main application is LC-voltage controlled oscillators (VCOs).

Figure 3.11 shows a cross section of an NMOS varactor and a general small-signal model for varactors: a variable capacitance in series with a variable resistance. For the NMOS device, source and drain are n^+-doped. The substrate (or well) region between and around source and drain is of opposite doping, i.e. p^--type while the polysilicon gate is of the same doping as source and drain, i.e. n^+-type. A PMOS device is obtained when all regions have opposite doping as in the NMOS.
Unlike a MOS transistor, a MOS varactor is a three-terminal device. The source and drain regions are shorted to apply the voltage V_{tune} that tunes the variable capacitance. The p^- body is grounded and the voltage V_{gate} is applied to the gate node.
The variable capacitance C_v appears between the gate node and all other nodes

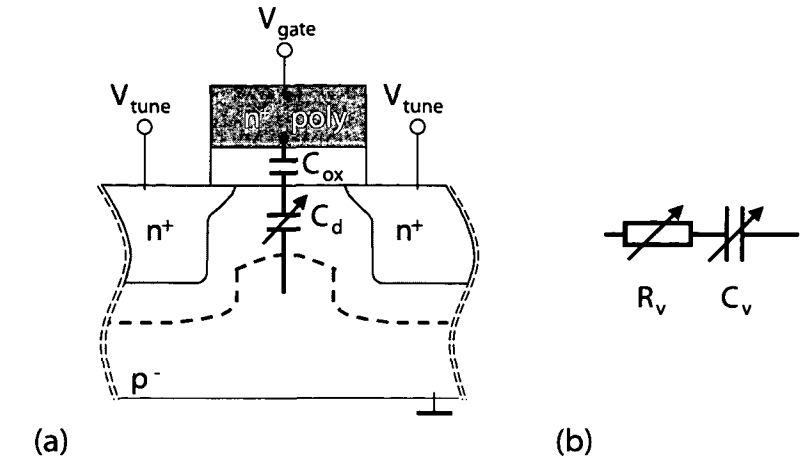

Figure 3.11: Cross-section of a conventional NMOS varactor in depletion (a) and the generally assumed model (b). The dashed line indicates the border of the depletion region.

at AC ground. Essentially it is the series connection of the gate oxide capacitance C_{ox} and the variable depletion region capacitance C_d

$$\frac{1}{C_v} = \frac{1}{C_{ox}} + \frac{1}{C_d}. \tag{3.20}$$

Figure 3.12 depicts the small-signal capacitance of an NMOS varactor at zero tuning voltage. The corresponding charges and the relevant lumped elements in the device are also included.

Negative gate voltages result in surplus of holes at the surface of the semiconductor: the device is in accumulation. Charge variations at the gate are balanced by changes in the accumulation layer charge. A large capacitance determined by the gate oxide is effective.
With increasing gate voltage, flat-band situation is reached. The semiconductor beneath the gate is neutral and fixed oxide while the interface charges balance the gate charge. The flat-band voltage V_{FB} is usually negative but the oxide charges are comprised of positively charged alkali-ions inevitably introduced during processing. Further, for a particular value of V_{FB}, different work functions of the gate and well have to be considered. Flat band voltage is close to 0 V, when same type of doping is present in gate and well. Different doping shifts the V_{FB} by approximately 1 V.
Just above the flat-band voltage holes are repelled from the surface and the negatively charged ions of fixed dopant atoms (acceptors) form the depletion region. Charges at the gate are balanced by widening (more negative dopants) or narrowing (less negative dopants) the depletion region. The capacitance in this case is a series connection of the gate oxide capacitance C_{ox} and the variable depletion region capacitance C_d.

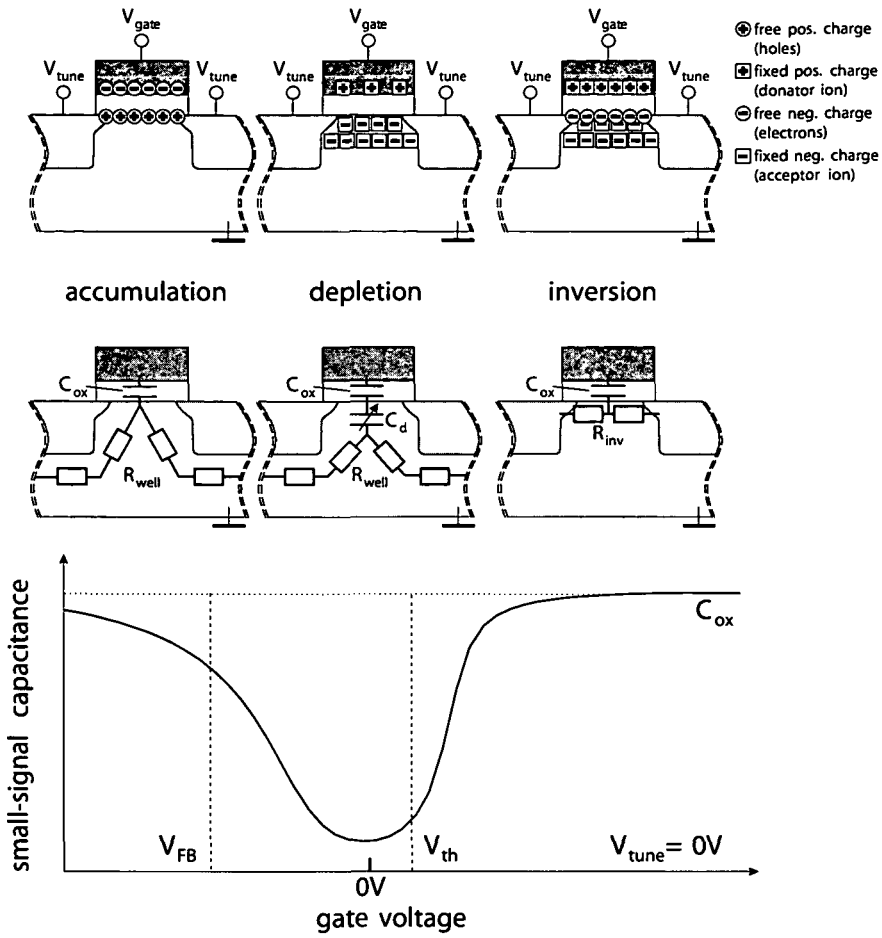

Figure 3.12: Typical measured small-signal capacitance characteristic of a NMOS varactor (bottom), the corresponding charges (top) and the relevant lumped elements (middle) at zero tuning voltage. Oxide, interface charges and charges at *pn* junctions are not shown.

Gate voltages above a certain threshold voltage V_{th} result in a surplus of electrons at the semiconductor surface, i.e. the device is in inversion. In this situation the depth of the depletion region remains constant and changes in the gate charge are balanced by changes in the electron inversion layer. Again the effective capacitance is determined by the gate oxide capacitance. The necessary electrons can be provided by thermal generation in the depletion region. However, at voltages leading to inversion, the electric field between the gate and the source/drain lowers the barrier between the source/drain and semiconductor's surface considerably. Therefore, the main source of electrons are the n^+-doped source and drain regions.

Part of the resistance is always the gate resistance determined by the polysili-

con line. The gate area and thus the gate width have to be large to achieve the necessary capacitance values ($\approx 500\,\mathrm{fF}...2\,\mathrm{pF}$) for VCOs in wireless communication systems. With a regular straight transistor design the corresponding gate resistance

$$R_{gate} \propto N_{\square} R_{\square} \tag{3.21}$$

is large. $N_{\square}$ and $R_{\square}$ are the number of squares and the resistance per square of the gate, respectively. To avoid this large undesired resistance, RF transistors as well as varactors are laid out in so called multifinger structures (Figure 3.13).

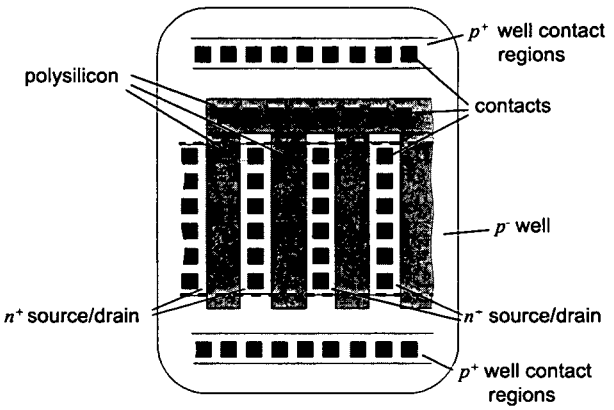

Figure 3.13: Typical multifinger structure of RF varactors. Dashed line indicates area of thin oxide.

Many short fingers (often less than 10μm) connected in parallel resemble a device with large total gate width

$$W_g = L_f N_F \tag{3.22}$$

with N_F the number of parallel fingers and L_f the length of each finger. Thereby, the gate resistance is considerably reduced to

$$R_{gate} \propto \frac{F_{\square} R_{\square}}{N_F} \tag{3.23}$$

with $F_{\square}$ the number of squares per finger. A typical value for R_{gate} is around $300\,\mathrm{m}\Omega$ for a $600\,\mu$m wide device (at $0.25\,\mu$m gate length). Further reduction of the gate resistance by a factor of $\frac{1}{4}$ is achieved when contacting the gate fingers at both ends.

In accumulation, the gate resistance is in series with the resistance extending from the accumulation layer to substrate (well) contacts presents outside the device, see Figure 3.13. This resistance is strongly layout dependent.

In depletion, the resistance is usually lower than accumulation, as the resistive path, in this case extend from the border of the depletion region to the substrate (well) contacts, is shorter. Above V_{th} the resistance is determined by the inversion layer. Thus, a peak in the resistance is observed at the onset of inversion as the

semiconductor surface is only weakly inverted with few electrons. At higher gate voltages and strong inversion the resistance drops to a relatively low value. The resistance in inversion is proportional to the gate length of the varactor.
The transition from depletion to inversion is determined by the voltage difference between gate and source/drain and the threshold voltage. Therefore the transition voltage would be increased with increasing tuning voltage (Figure 3.14).

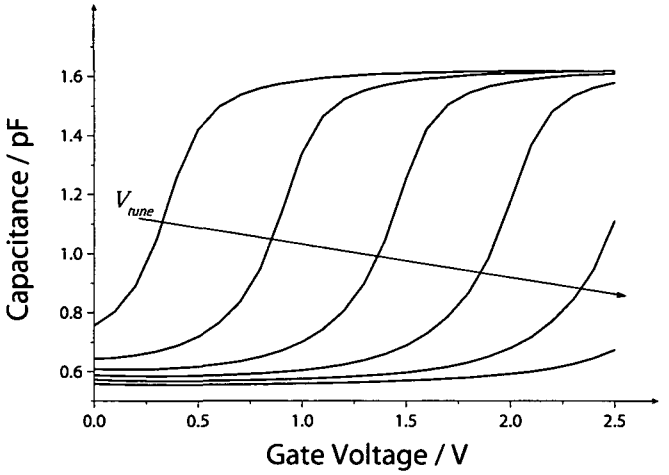

Figure 3.14: Typical measured small-signal capacitance characteristic of a conventional NMOS varactor at various tuning voltages (0V...2.5V; 0.5V steps).

The threshold voltage depends on the voltage between source/drain and substrate (bulk effect) and contributes additionally to the shift of the transition.

3.3 C11N CMOS Technology

The C11N technology offers low-k dielectric copper metallization with up to six levels of interconnect at dense pitches (M1: 0.32 μm, Mx: 0.40 μm). The two upper metal layers are thick metals. The dielectric is silicon-oxide ($\varepsilon = 3.9$). A simplified cross section of the C11N-metallization is shown in Figure 3.15.

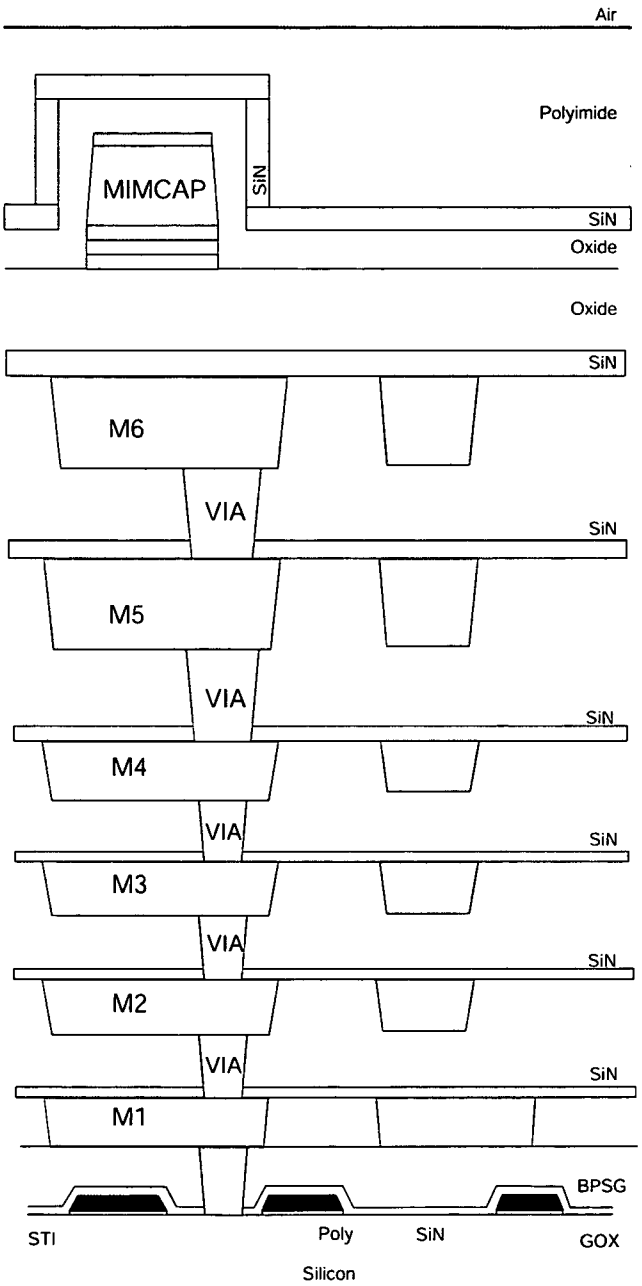

Figure 3.15: Cross section of the C11N metallization.

Chapter 4

Receiver Architecture and Specifications

4.1 Introduction

The BRAN family of standards includes HIPERLAN Type 1 (high speed wireless LANs) and HIPERLAN Type 2 (short range wireless access to IP, ATM and UMTS networks) operating in the 5 GHz band along with HIPERACCESS (fixed wireless broadband point-to-multi-point) and HIPERLINK (wireless broadband interconnection) operating in the 17 GHz band. This is represented in Figure 4.1 together with the operating frequencies and achievable data transfer rates over the air interface.

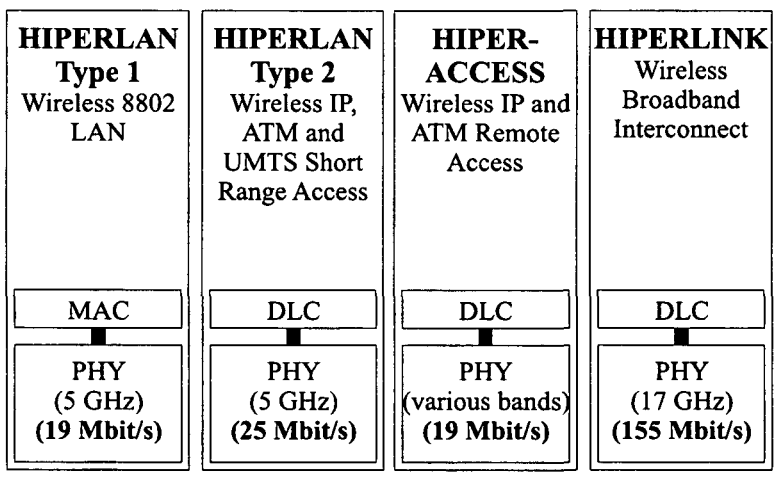

Figure 4.1: Overview of HIPERLAN Types, HIPERACCESS and HIPERLINK.

4.2 Block Diagram

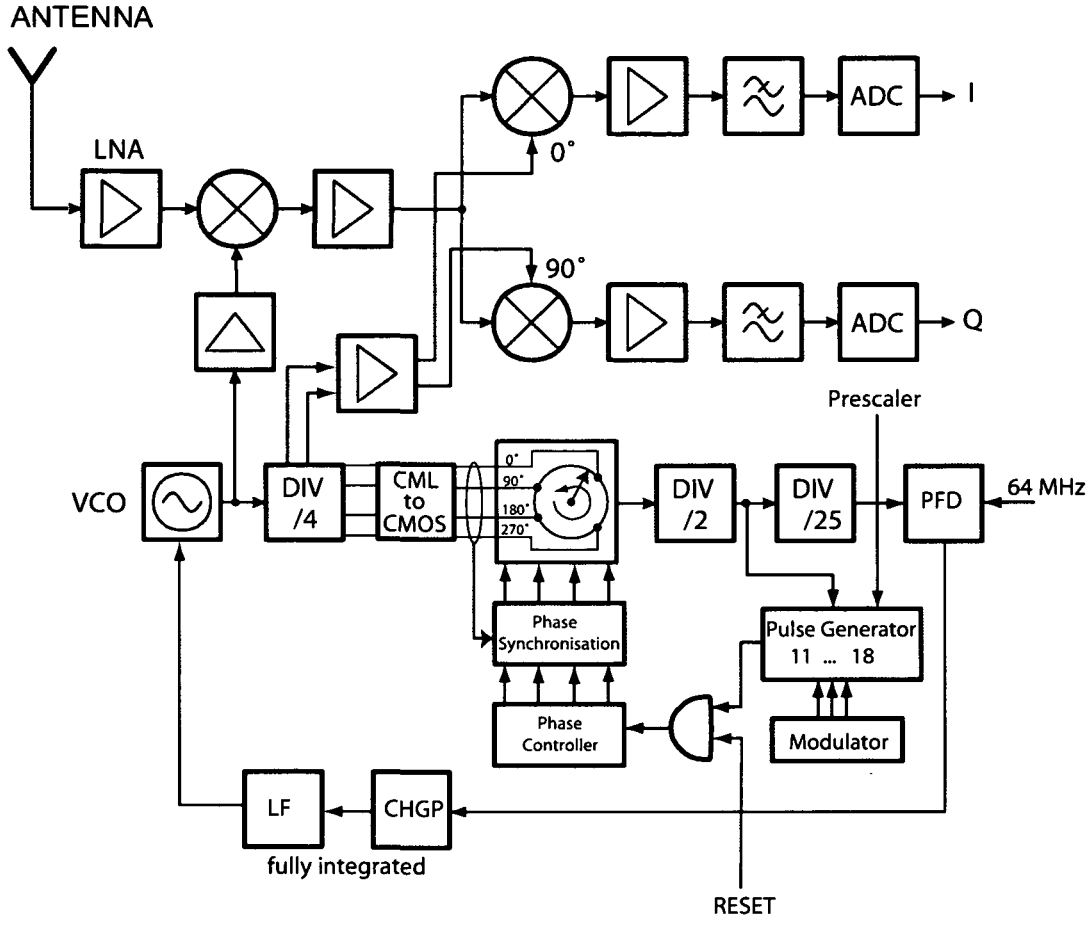

Figure 4.2: Block diagram of a double conversion receiver.

The block diagram depicted in Figure 4.2 shows a double conversion receiver with an appropriate phased-locked loop (PLL). In this implementation, the bandpass filters of the receiver (see Figure 2.6 in Chapter 2) can be neglected and external filters are not required because filtering is implemented in the LNA and the first mixer. This can be realized with inductor-capacitor tanks which provides a second-order bandpass filtering.

4.3 Frequency and Level Plan

As shown in Figure 4.2, there are only two frequency down-conversions, one from RF to IF and one from IF to baseband I and Q, respectively.

4.3.1 Sensitivity and Bit-Error Rate (BER)

The sensitivity of a receiver is defined as the minimum input signal power level that is detectable assuming a given signal-to-noise ratio (SNR). The required SNR depends on the application. In case of an ideal, noiseless system the sensitivity is only determined by the background noise that comes with the signal, i.e. the noise of the signal source. However, since a practical system always adds noise, the effective input noise floor is higher in contrast to the ideal case. The sensitivity thus critically depends on the noise contribution of the different building blocks in the receive path. In reality however, the sensitivity and the reception quality of a complete digital communication system are not defined in terms of signal-to-noise ratios. Instead is used the bit-error rate (BER). The BER is the percentage of bits that are affected by errors relative to the total number of bits received in a transmission. Hence, in order to be able to derive the specifications for the RF analog part of a digital receiver, the required BER needs to be mapped onto an equivalent minimum SNR. For a given modulation method, the BER values can be directly translated into corresponding SNRs.
As an example, Figure 4.3 shows the theoretical BER of different quadrature-modulated (QAM) signals in an additive white gaussian noise (AWGN) channel as a function of E_b/N_0, where E_b is the energy per bit and N_0 is the noise density. Table 4.1 depicts the minimum sensitivity power for a 5 GHz WLAN system for different data rates [IEEE 99]. For a 17 GHz WLAN system, there is no standard available yet, therefore important system and design parameters are assumed from the IEEE 802.11a standard. The highest sensitivity of -82 dBm must be achieved for a 6 Mbit/s transmission. This is a challenging value because the propagation loss for a wave in free space is defined as

$$L_p = 20 \cdot \log\left(\frac{4\pi f d}{c_0}\right), \tag{4.1}$$

where c_0 is the speed of light ($3 \cdot 10^8$ m/s), d is the distance and f the frequency. Figure 4.4 shows the propagation loss over frequency. A value of $L_p = 97.15\,dB$ is found for a transmission over a distance of 100 m.
If one assumes a transmit power of about 30 dBm (= 1 W transmit power) and a maximum propagation loss of 97.15 dB, the receiver should have a sensitivity of about -67.15 dB, which is similar to the IEEE standard shown in Table 4.1. Using Figure 4.3, a BER for example of 1% translates into a required E_b/N_0 for a 256 QAM of about 16.4 dB. Assuming a bit-rate of 155 Mbps and taking into account the channel spacing of 200 MHz, this requires a minimum SNR of 15.3 dB in a single channel.

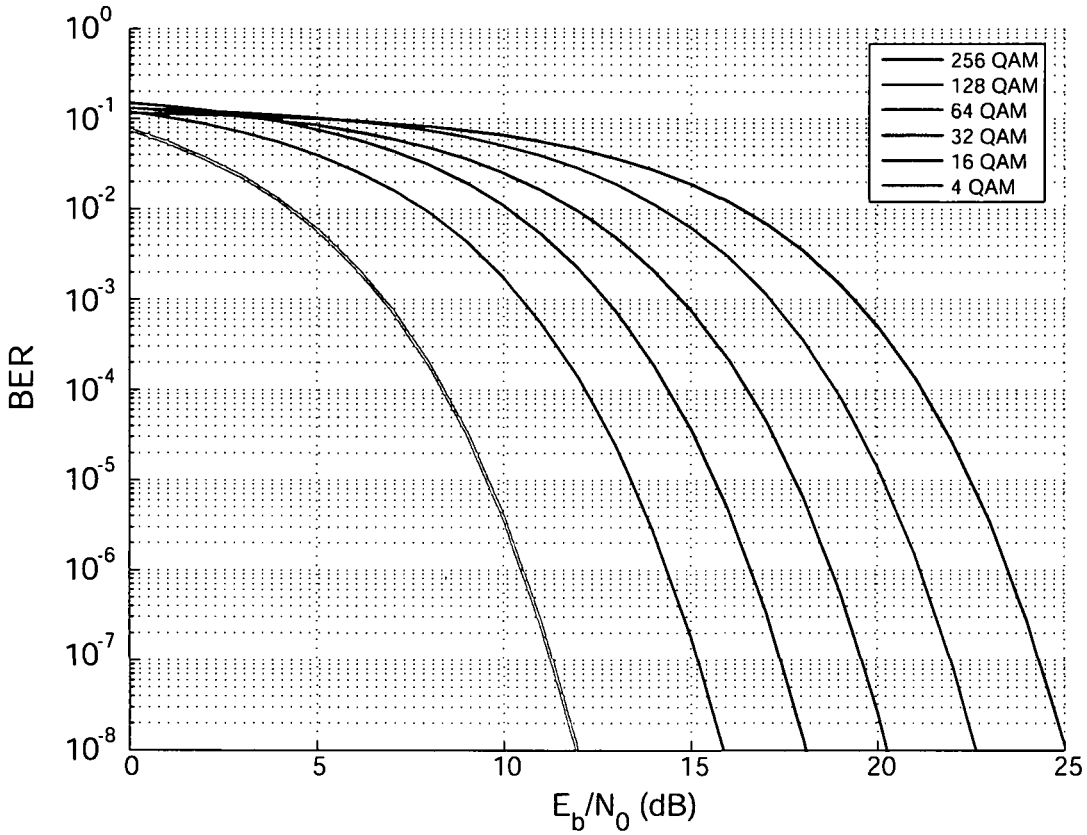

Figure 4.3: Bit-error rate of uncoded QAM-signals as a function of E_b/N_0.

Table 4.1: Receiver performance requirements for a 5 GHz WLAN system

Data rate (Mbit/s)	Minimum sensitivity (dBm)	Adjacent channel rejection (dB)	Alternate adjacent channel rejection (dB)
6	-82	16	32
9	-81	15	31
12	-79	13	29
18	-77	11	27
24	-74	8	24
36	-70	4	20
48	-66	0	16
54	-65	-1	15

4.3.2 Noise Figure

The relative decrease of SNR due to system noise and hence the degradation of sensitivity is quantified by the noise figure NF [Friis 44], which is defined as

$$NF = 10 \cdot \log\left(\frac{SNR_{IN}}{SNR_{OUT}}\right). \tag{4.2}$$

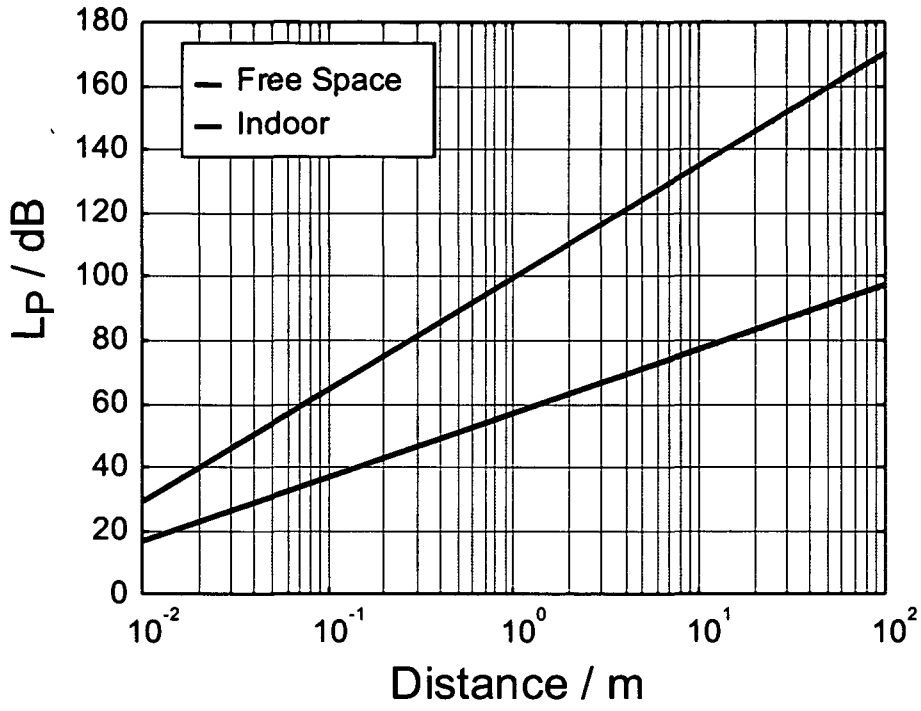

Figure 4.4: Propagation loss at 17.2 GHz for indoor and free space waves.

The noise figure requirement can be derived from the required receiver sensitivity (see previous subsection). The equivalent input noise power at the antenna must be lower than

$$-68\,dBm - 15.5\,dBm = -83.5\,dBm. \tag{4.3}$$

The thermal noise floor at 1 Hz bandwidth at room temperature can be calculated by

$$P_n\,(1\,Hz) = 10 \cdot \log(kT) + 10 \cdot \log(1\,Hz), \tag{4.4}$$

where k is the Boltzmann's constant ($k = 1.38e^{-23}\,JK^{-1}$) and T is the room temperature in kelvin (300 K). This results in a thermal noise floor of about $-173.87\,dBm$ at 1 Hz. In the same manner, the thermal noise floor for a bandwidth of 200 MHz is calculated by

$$P_n\,(20\,MHz) = -173.87\,dBm/Hz + 10 \cdot \log(200\,MHz) = -90,87\,dBm. \tag{4.5}$$

The noise figure required at the antenna thus becomes

$$-83.5\,dBm - (-90.87) = 7.37\,dBm. \tag{4.6}$$

4.3.3 LO Leakage

In addition, leakage of the LO signal to the antenna and radiation therefrom creates interference in the band of other receivers using the same standard. In the standards, there exists an upper bound of in-band LO radiation which is typically between -50 dBm and -80 dBm.

4.3.4 Image Rejection Ratio

The image rejection ratio quantifies the factor by which the mirror signal, i.e. the parasitic signal or adjacent channel which is folded onto the wanted signal, is suppressed.
The image rejection specification can be derived from the reference interference specification in the standard. The standardization have not been declared, so this specifications are not available. For other systems, the so-called reference interference performance which is basically a minimum BER must be guaranteed in the presence of co-channel and adjacent channel interference.

4.3.5 Blocking Signals

Large unwanted signal can block the desired signal. This happens when the desired signal is small while the undesired signal is large in amplitude. Due to this, the receiver is overloaded and the desired signal cannot be retrieved. This situation is known as *blocking*.

The effects of interfering signals, distant from the wanted signal are specified by the blocking signal characteristics. As mentioned before, this information is not available from the standardization committee but different blocking levels for the 5 GHz WLAN can be assumed (Figure 4.5).

4.3.6 Intermodulation Performance

The third order intermodulation products (IM3) are located in the vicinity of the two input tones. The magnitude of the two IM3 products is given by

$$IM3_{low} = \frac{3}{4} a_3 S_1^2 S_2 \cos(2\omega_1 t - \omega_2 t) \tag{4.7}$$

and

$$IM3_{high} = \frac{3}{4} a_3 S_1 S_2^2 \cos(2\omega_2 t - \omega_1 t), \tag{4.8}$$

where S_1 and S_2 denote the amplitudes of the input signal. The input-intercept point of 3^{rd} order (IIP_3) is the theoretical point where the extrapolated amplitude of the fundamental tone intersects the extrapolated IM3 product. This is illustrated by Figure 4.6).

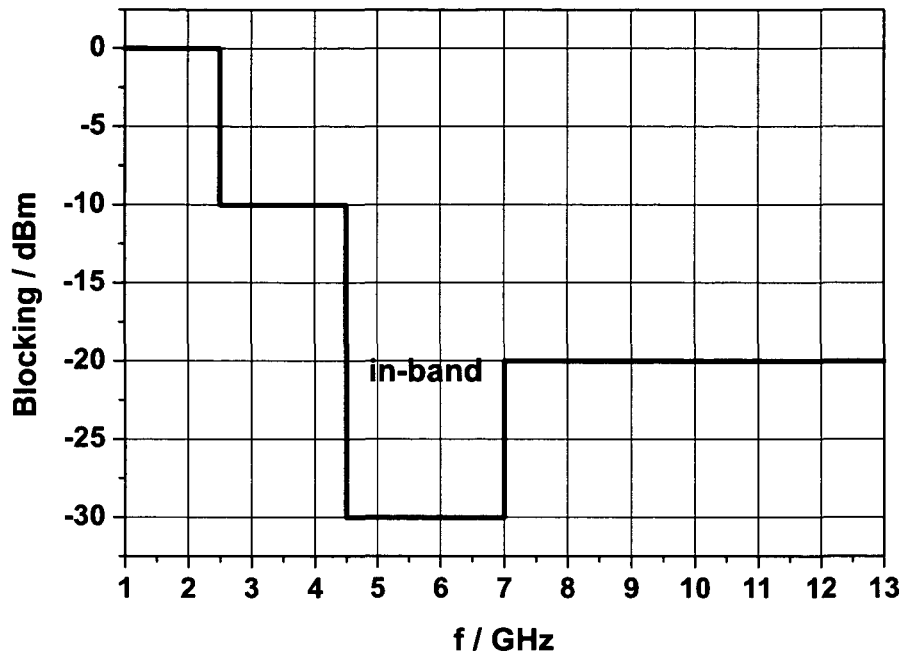

Figure 4.5: The allowed blocking signal levels for a 5 GHz WLAN system.

It can be shown by simple analysis that the IIP_3 can be calculated as

$$IIP_3 = P_{in} + \frac{IMD}{2}. \tag{4.9}$$

The IIP_3 can also be calculated using Equation 4.7. By setting $S_1 = S_2$ and solving

$$\frac{3}{4} a_3 S_{1,IIP_3}^2 S_{2,IIP_3} = a_1 S_{1,IIP_3}, \tag{4.10}$$

the IIP_3 in voltage is obtained as

$$V_{IIP_3} = \sqrt{\frac{4a_1}{3|a_3|}}. \tag{4.11}$$

Since in RF systems signals are processed by cascaded stages (Figure 4.7), the intercept point can be determined

$$IIP_3 = \frac{1}{\frac{1}{IIP_{3,1}} + \frac{G_1}{IIP_{3,2}} + \ldots + \frac{G_1 \ldots G_n}{IIP_{3,n}}}, \tag{4.12}$$

where $IIP_{3,1} \ldots IIP_{3,n}$ denote the input third order intercept point of each stage and $G_1 \ldots G_n$ denotes the gain of the corresponding stage.
With the above formulas the intermodulation performance for any specification

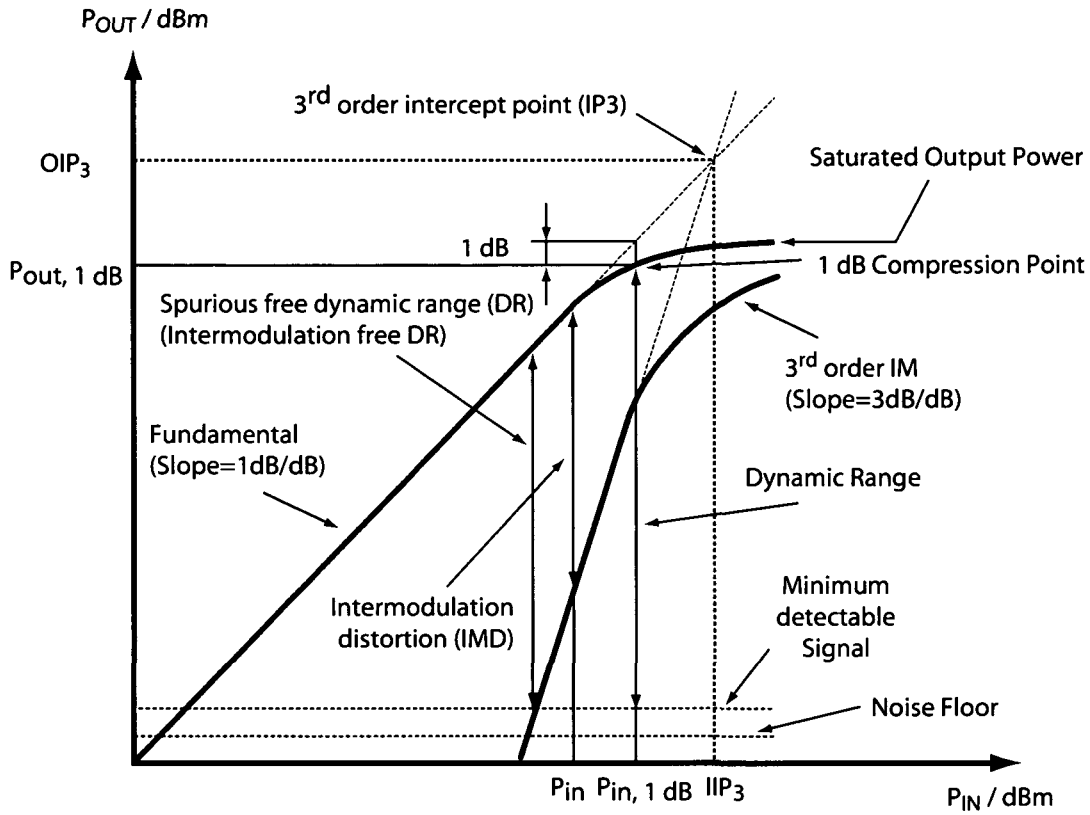

Figure 4.6: Output power of fundamental and IM_3 versus input power.

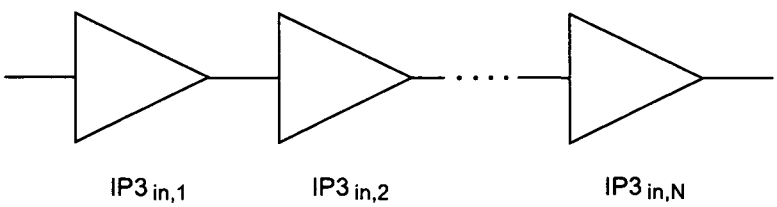

Figure 4.7: System input IP_3 calculation.

can be calculated. Combining the results, the derived IIP_3 can be calculated if two interferers with different amplitudes and the allowed interference level are given (in dB):

$$IIP_3 = \frac{2 \cdot P_1 + P_2 - IM3_{low}}{2}. \tag{4.13}$$

4.4 Circuit Specification

In this section, the receiver specifications are enforced to the different building blocks. Minimum power consumption is one of the main criteria for wireless applications. These results are summarized in Table 4.2. The mapping of these specifications is often subject to change.

4.4.1 Low Noise Amplifier

The LNA gain should fulfill the following criteria:

- The gain needs to be large enough to amplify the smallest possible wanted signal sufficiently above the noise floor.
- The gain must be low enough to ensure that the down-converters are not saturated by the amplified blocking signal.

Assuming a realistic value of -10 dBm for the mixer input capability, the allowable gain is set to 20 dB. This results in an in-band blocking of about -30 dBm.
The LNA noise figure must be low and hence 3.5 dB as target noise figure for the LNA was chosen.

4.4.2 1^{st}-Mixer

The required noise figure of the complete receive path is 7.37 dB, of which 3.5 dB has already been assigned to the LNA. Taking into account the 20 dB gain of the LNA, the required noise figure for the first mixer becomes 24.4 dB.

4.4.3 IF Amplifier

In the receiver architecture the intermediate frequency amplifier is responsible to separate the first mixer and the I/Q-mixers. So, a high third-order intercept point is desirable for the amplifier as the noise is not a problem in a cascaded system.

4.4.4 2^{nd}-Mixer

The only demand on the 2^{nd}-mixer stage is to have a high enough intercept point and low I/Q-mixer mismatch. Furthermore a flat gain characteristic would be necessary for the whole baseband bandwidth.

4.4.5 Operational Amplifier

The operational amplifier (OP-amp) has to make sure that the output can drive 50 Ω. Additionally, this is an important building block because it is the last stage in receiver path to ensure a high intercept point.

4.4.6 Voltage Controlled Oscillator

A low phase noise voltage controlled oscillator (VCO) is an essential building block for the receiver. The phase noise specification is determined by the unwanted down-conversion of adjacent channels.

4.5 Specification Summary

Table 4.2 summarizes the specifications of the receiver building blocks.
Finally Figure 4.8 shows the level diagram of the proposed receiver architecture. At the end of the receiver an A/D converter is placed. This block is very critical

Table 4.2: Summery of the derived specifications for the receivers building blocks

LNA	Reflection Coefficient (S_{11})	< -10 dB	
	Noise Figure (NF)	< 3.5 dB	4.4.1
	Gain	20 dB	4.4.1
1^{st}-Mixer	IF Frequency	3.4 GHz	4.2
	Conversion Gain	10 dB	
	SSB Noise Figure	< 24.4 dB	4.4.2
	Third-order Intercept Point (IP_3)	> - 5 dBm	4.4.2
IF-Amplifier	Gain	5 dB	
	Third-order Intercept Point (IP_3)	> - 5 dBm	4.4.3
2^{nd}-Mixer	IF Frequency	0-200 MHz	4.2
	Gain	5 dB	4.4.4
	Third-order Intercept Point (IP_3)	> - 5 dBm	4.4.4
OP-Amplifier	Gain	0 dB	4.4.5
	Third-order Intercept Point (IP_3)	> - 5 dBm	4.4.5
VCO	Resonance Frequency	13.76 GHz	4.2
	Tuning Range	> 1.2%	4.2
	Phase Noise	-120 dBc/Hz @ 10 MHz	

and determines the performance of the complete system. Hence, the A/D converter parameters are at first, e.g. bit resolution, dynamic range and bandwidth. Also the implementation of A/D converters can be different for example a sigma-delta converter [Zheng-Yu 04][Hung-Chih 04]. In particular, the propagation of the following set of signals is shown:

(a) The minimum detectable signal.

(b) The largest input signal for the LNA.

(c) The largest wanted signal.

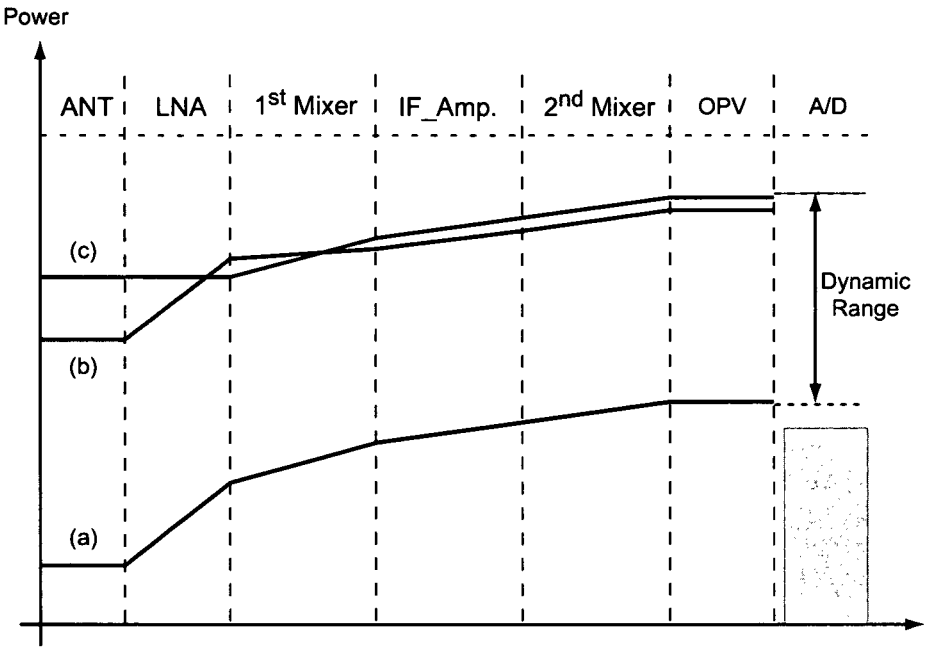

Figure 4.8: Level diagram of the receiver.

4.6 Conclusion

The chapter has treated the theoretical high-level design of a future WLAN receiver front-end. First, the system level requirements have been derived for different assumptions. At the end, these specifications are allocated to the individual blocks.
As mentioned in this chapter, the standardization for a 17 GHz WLAN communications system has not started yet. This is the reason why many of the specifications in the previous chapters are only a first assumption for a communication link. For further applications, the target values are subject to change. For example, the BER can be set to values that implicates tougher specifications of the complete receiver path. Furthermore, the design is strongly coupled to the data rate of the system link. In this case, a decrease of the data rate goes in hand with a decrease of the receiver sensitivity.
Finally, this chapter gave a theoretically overview, how a future communication system can be described. Additionally, it showed the general design process to get building blocks specifications from receiver specifications.

Chapter 5

Receiver Implementation

5.1 Introduction

During the design, the practical problems and constraints that are encountered when arranging building blocks together will be explained in detail. In Figure 5.1 a block diagram of the implemented receiver topology is presented. A sliding IF architecture with small changes are used for the on-chip implementation. The image rejection of the first mixing operation is ensured by the antenna which works like a bandpass with small bandwidth. For example, a patch antenna for 17.2 GHz has a bandwidth of typically 1 GHz [Bahl 80][James 81]. The bandpass filter between the LNA and the first mixer is neglected because the output of the LNA has a second-order bandpass characteristic as explained in Chapter 5.4. Pragmatic for this design is the large frequency separation between the RF input and the local oscillator. Additionally, this receiver does not have a channel selection filter at the IF because the first mixer output provides a bandpass characteristic achieved by the implemented integrated LC-tank.

A complete receiver schematic including the schematics of all building blocks, which are explained in detail in chapter 4, is presented in Figure 5.2. The anatomy of the design is same as the block diagram from Figure 5.1 but with schematics as overlay. The plot depicts the complexity of the receiver in an impeccable way. Starting with a differential RF input at the LNA, followed by the first mixer and an IF-amplifier. At this point the signal splits up in two branches, one for the inphase signal and the other for the quadrature signal. After the I/Q-mixers the two differential baseband signals are buffered with an operational amplifier to drive the 50 Ω outputs. On his part, the VCO allocates the LO signal to the first mixer and the 4:1 divider.

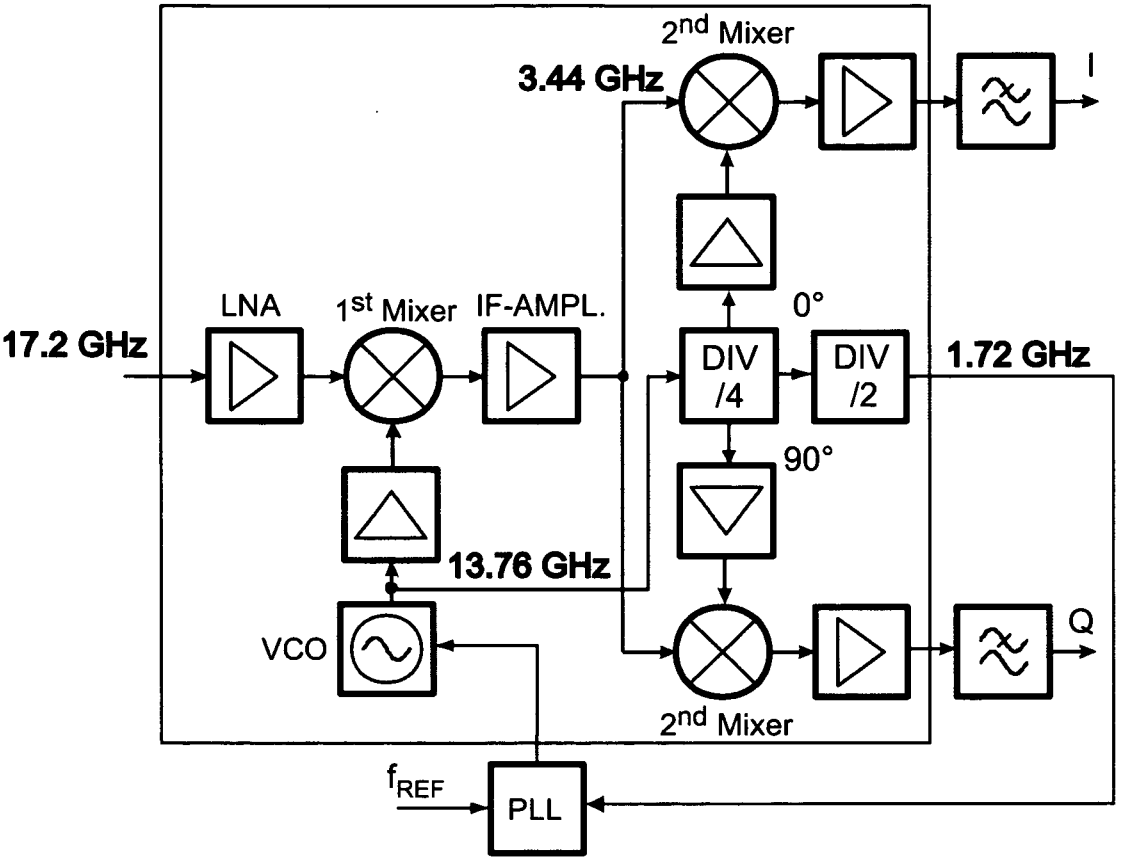

Figure 5.1: Block diagram of the integrated receiver.

5.2 Simulation Techniques

Circuit simulation is a very important tool for designing integrated circuits. Circuit simulators are used to evaluate new designs before they are fabricated, which is costly and time consuming. It is of paramount importance to optimize a circuit design before production, because there is little room for changes once the IC is manufactured. The only possibility for a design modification is disconnection of on-chip interconnects or the addition of a few short interconnects using Focused-Ion Beams (FIB).
Simulation of RF communication circuits pose problems due to the special requirements of the building blocks such as oscillators and mixers along with complex signals used for digital communications [Kundert 99][Mayaram 00].

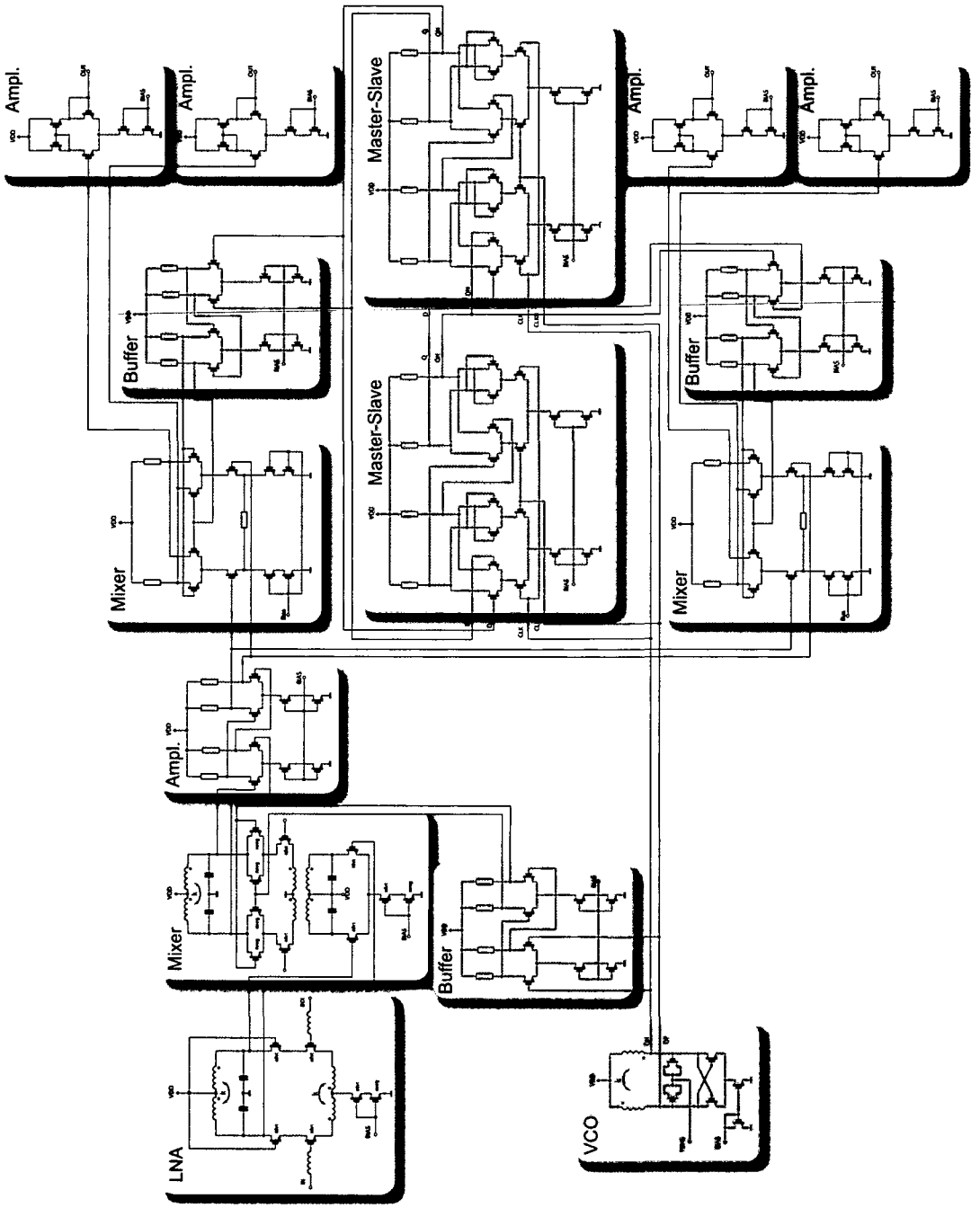

Figure 5.2: Schematic of the receiver (signal and LO path are colored).

AC Analysis

The AC analysis computes the small-signal behaviour of the circuit. First, the DC operating point is calculated and further the circuit is linearized at particular operating point using a Taylor series expansion. Since AC analysis is a linear time-invariant calculation, the results cannot exhibit distortion and frequency translation. This type of simulation is implemented in all derivations of SPICE [SPICE 04].

Transient Analysis

Transient analysis computes the response of a circuit to various stimuli as a function of time. A nonlinear differential equation cannot be solved numerically, the best solution is to solve for a finite-dimensional approximation to the actual solution, such as a finite sequence of points. In transient analysis, the simulation interval is broken into small individual steps, and is simplified in a way that the signal trajectory follows a low-order polynomial over a time step. The transient simulation is used for a variety of tests on the circuit such as IP_3, which is performed in conjunction with the Fourier transform. This kind of simulation is used in nearby all derivations of SPICE [SPICE 04].

Periodic Steady-State Analysis

For communications circuits it is important to simulate nonlinear noise (like in mixers and VCOs) and intermodulation distortion. Transient analysis is capable of calculating intermodulation distortion by using Fourier transformation. However, long time-constants in the circuits can be problematic during transient analysis, because the solution has to reach a steady-state before the spectrum can be calculated. Further, the transient analysis is not capable of calculating noise. With periodic analysis like shooting a steady-state response is computed and it is used as a periodic point for subsequent small-signal analysis like noise. The periodic steady-state analysis is not embedded in all simulation tools. TITAN, Infineons inhouse circuit simulator, and SPECTRE [SPECTRE 04] provide this type of analysis.

Harmonic Balance

The Harmonic Balance (HB) method is a well-known frequency-domain technique for periodic and quasi-periodic steady-state analysis of nonlinear circuits.
In HB, the nodal equations are formulated in the frequency domain, thus the differentiation in the time domain is replaced by algebraic multiplication. Since all nonlinear device models are formulated in the time domain, i.e. where the voltage node spectrum is transformed into the time domain by a Fourier series

representation. The corresponding current is calculated and converted back into the frequency domain by Fourier transform. Harmonic balance simulation needs special software tools like Infineons TITAN, Agilents Advanced Design Sytem [ADS 04] or Menthor Graphics ELDO [ELDO 04].

5.3 Current Source

A current source is used in each of the receiver building blocks. Ideally, the output impedance of a current source is infinite. It should be able to deliver a constant current over a wide voltage range. However, real current source circuits have limited output impedance and voltage range. Typically, the voltage range is determined by a lower bound, which should be high enough to keep the device in saturation and an upper bound, the break-down voltage of the device.
Figure 5.3(a) shows a conventional current mirror. The gates of transistor M1 and M2 and the drain of M1 are connected together. Since the gates of M1 and M2 are shorted, the gate-source voltages for both devices are the same

$$V_{gs1} = V_{gs2}. \tag{5.1}$$

A current I_1, which flows through M1, is given by

$$I_1 = \frac{\mu_n C_{ox}}{2} \frac{W_1}{L_1} (V_{gs1} - V_T)^2. \tag{5.2}$$

While I_2, assuming that M2 is in saturation, is

$$I_2 = \frac{\mu_n C_{ox}}{2} \frac{W_2}{L_2} (V_{gs2} - V_T)^2. \tag{5.3}$$

Since $V_{gs1} = V_{gs2}$ Eqn. 5.1, the ratio of the drain currents is given by

$$\frac{I_2}{I_1} = \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} = \frac{W_2 L_1}{W_1 L_2}. \tag{5.4}$$

If the length of all devices have the same size, Eqn. 5.4 simplifies to

$$\frac{I_2}{I_1} = \frac{W_2}{W_1}. \tag{5.5}$$

Typically, when designing current mirrors, the values for V_{gs1} and L_1 are given and W_1 and R_1 can be derived from

$$I_1 = \frac{V_{DD} - V_{gs1}}{R_1} = \frac{\mu_n C_{ox}}{2} \frac{W_1}{L_1} (V_{gs1} - V_T)^2. \tag{5.6}$$

The output resistance of the current mirror is simply given by the output resistance of the device M2

$$r_o = \frac{1}{\lambda I_2}. \tag{5.7}$$

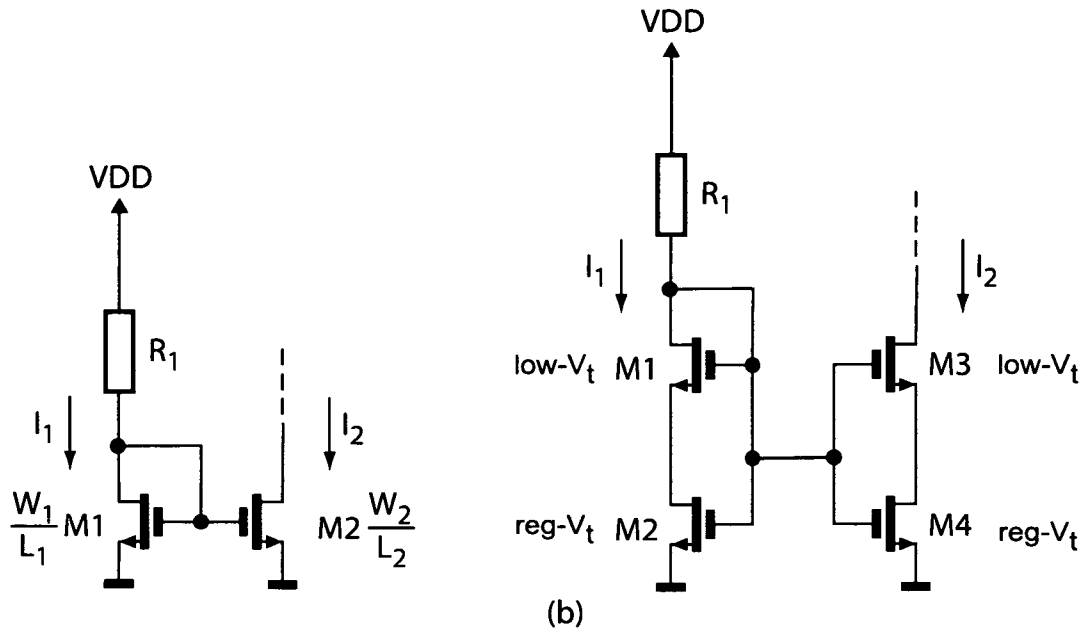

Figure 5.3: Schematic of a conventional current mirror (a) and stacked current source (b).

where λ is the channel length modulation parameter. Longer channel length results in a lower λ hence a higher r_o but in a higher parasitic capacitance.
Setting V_{gs} close to the threshold voltage V_T results in large device width W and in a larger capacitance at the drain node. Setting V_{gs} significantly larger than V_T causes the transistor to enter the linear region.
Figure 5.3(b) shows a stacked current mirror. All gates and the drain of M1 are connected together. A regular-V_t device and a low-V_t device (cascode) are connected in series. This configuration increases the output resistance of the current source. Neglecting the body effect, the output resistance of the stacked current source can be written as

$$R_o = r_{o3} + r_{o4}(1 + g_m r_{o3}), \tag{5.8}$$

where r_{o3} and r_{o4} are the output resistance of the devices M3 and M4. If the output resistance of M3 and M4 are equal, Eqn. 5.8 simplifies to

$$R_o = r_o + r_o(1 + g_m r_o) = 2r_o + g_m r_o^2 \approx g_m r_o^2 \tag{5.9}$$

The stacked current source has much higher output impedance compared to the conventional current mirror. Figure 5.4 shows the drain current I_D versus drain-source voltage V_{DS}. The stacked current source shows flat current source behaviour. The main disadvantage of stacked current sources is the higher operating voltage to keep the devices in saturation. The low-V_T device in the receiver

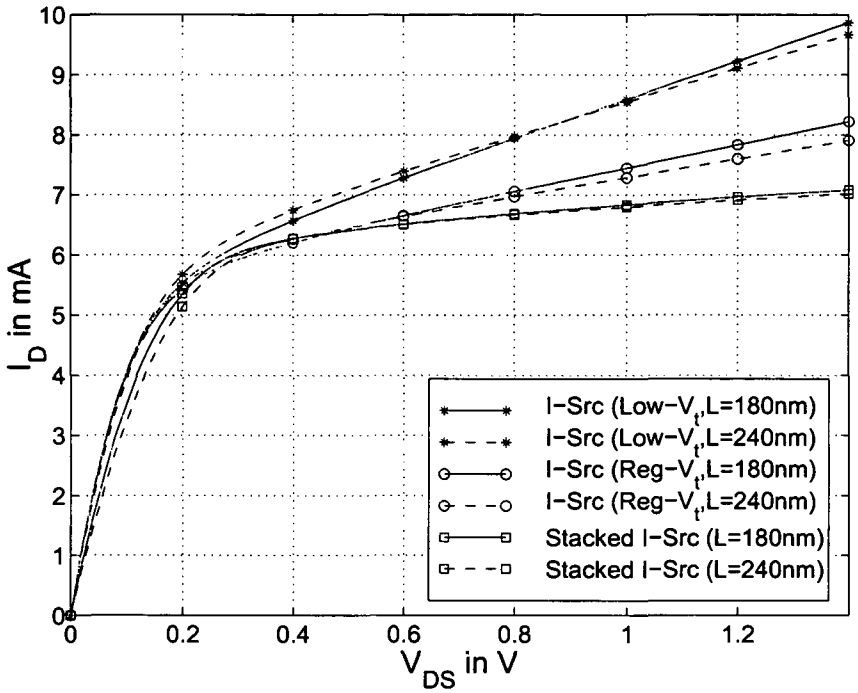

Figure 5.4: Current source characteristic of conventional current mirror with low-V_T and regular-V_T devices and the stacked current source.

stacked current source minimizes the operating voltage. The minimum operating voltage is very close to the minimum operating voltage of the conventional current mirror.

5.4 Low Noise Amplifier

Since the LNA is the first component in the receiver chain, the input of the LNA must be matched to 50 Ω. Many methods for matching the input using passive circuit elements are possible with varying bandwidths and degrees of complexity. However, one of the most elegant method is described in [Shaeffer 97] and [Paparisto 01]. This method requires two inductors to provide the power and noise match for the LNA, as shown in Figure 5.5.

A straightforward analysis of the input matching shows that

$$Z_{in} = \frac{-j}{\omega C} + j\omega L_{IN} + \frac{g_m L_S}{C} + j\omega L_S. \tag{5.10}$$

The LC-tank, consisting of the inductances L_S and L_{IN} and the transistor capacitance C, is in resonance if the imaginary part is equal to zero. The resonance

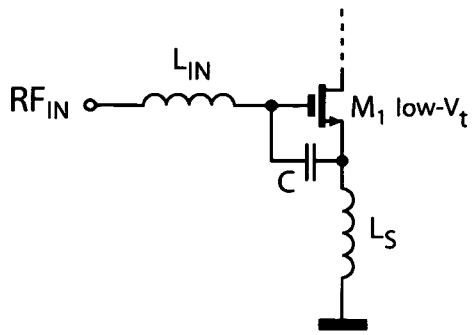

Figure 5.5: Input matching of a LNA with two inductors.

frequency ω_0 is

$$\omega_0^2 = \frac{1}{(L_S + L_{IN}) \cdot C}. \tag{5.11}$$

Also for matching, the real part of the input impedance Z_{in} must be equal to the source resistance R_S so that

$$R_S = \frac{g_m L_S}{C}. \tag{5.12}$$

Eqn. 5.12 can be written as,

$$L_S = \frac{R_S C}{g_m} = \frac{R_S}{\omega_T}. \tag{5.13}$$

whereas ω_T is the angular frequency of the transistor. Also the imaginary part of the input impedance must be equal to zero. Therefore, the appropriate choice of the transistor parameters and values of the inductors determine resonance frequency as well as the input matching.

For the receiver implementation, a fully differential common-source type LNA with on-chip inductive degeneration was chosen. The LNA is one of the main challenges in the front-end design, since this circuit determines the total noise figure of the receiver. The LNA core in Figure 5.6 consists of a cascoded, inductively degenerated common source input stage which converts the available power into current.

The differential pair at the input mainly consists of two equal transistors. An example of such a differential pair is shown in Figure 5.7. It consists of two equal transistors and a current source with value I_B, which biases both transistors M_1 and M_2 at the same current $I_B/2$. As a result, two input and two output terminals are available. The differential-mode input voltage v_{Id} and the common-mode input voltage v_{Ic}, are derived from the applied input voltages v_{I1} and v_{I2}, as defined by

$$v_{Id} = v_{I1} - v_{I2} \tag{5.14}$$

$$v_{Ic} = \frac{v_{I1} + v_{I2}}{2}. \tag{5.15}$$

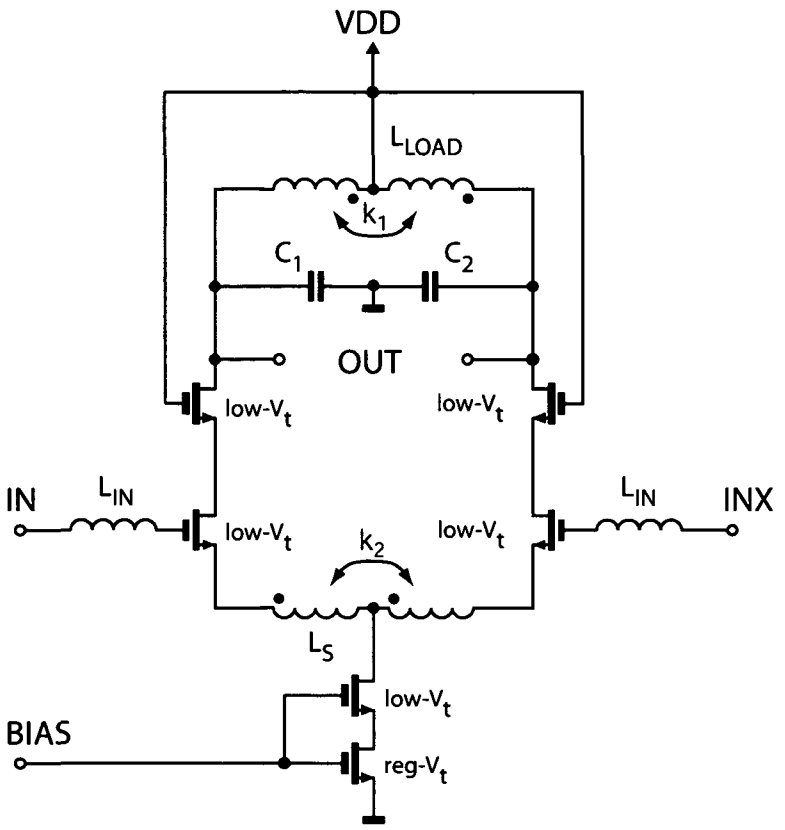

Figure 5.6: Schematic of the LNA.

In a similar way, the output voltages are defined as

$$v_{Od} = v_{O1} - v_{O2} \tag{5.16}$$

$$v_{Oc} = \frac{v_{O1} + v_{O2}}{2}. \tag{5.17}$$

Now, the value of v_{Od} is given by

$$v_{Od} = -R_L i_{Od} \tag{5.18}$$

where

$$i_{Od} = i_1 - i_2 \tag{5.19}$$

$$I_B = i_1 + i_2. \tag{5.20}$$

The currents i_1 and i_2 can be extracted from the two expressions above. They can given by written as:

$$2i_2 = I_B + i_{Od} \tag{5.21}$$

$$2i_2 = I_B - i_{Od}. \tag{5.22}$$

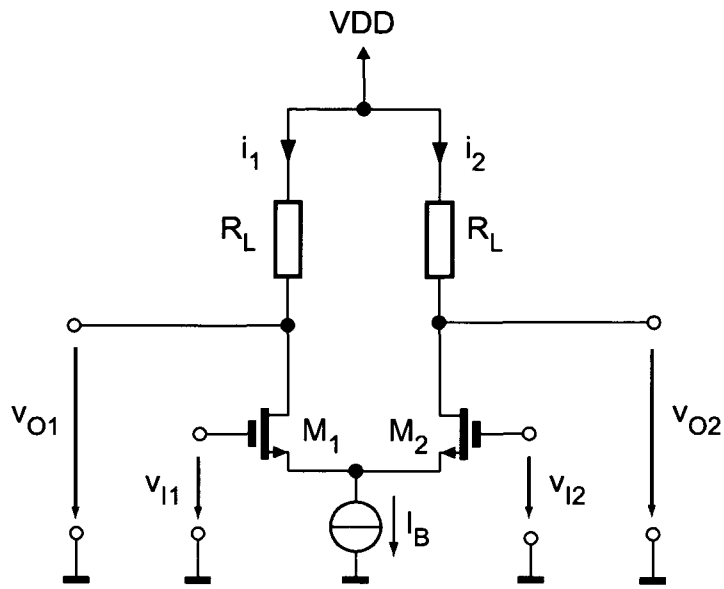

Figure 5.7: MOS differential pair.

On the other hand, the input voltages are related by:

$$v_{Id} = v_{GS1} - v_{GS2} \tag{5.23}$$

$$v_{GS1} = V_T + \sqrt{\frac{i_1}{(W/L)_1 K'_n}} \tag{5.24}$$

$$v_{GS2} = V_T + \sqrt{\frac{i_2}{(W/L)_2 K'_n}} \tag{5.25}$$

where $(W/L)_1 = (W/L)_2 = (W/L)$ and $K'_n = \frac{\mu_n C_{ox}}{2}$. Eqn. 5.24 and Eqn. 5.25 are obtained by use of the simple quadratic i_{DS} versus i_{GS} relationship of a MOS. Substitution of v_{GS1} and v_{GS2} from Equation 5.24 and Equation 5.25 in Equation 5.23 then

$$v_{Id} = \frac{1}{\sqrt{(W/L)K'_n}} \left(\sqrt{i_1} - \sqrt{i_2}\right). \tag{5.26}$$

Finally, substitution of i_1 and i_2 from Equation 5.21 and Equation 5.22 in Equation 5.26 yields

$$\sqrt{1 + \frac{i_{Od}}{I_B}} - \sqrt{1 - \frac{i_{Od}}{I_B}} = \sqrt{\frac{2K'_n(W/L)}{I_B}} v_{Id}. \tag{5.27}$$

This equation has the form

$$\sqrt{1+y} - \sqrt{1-y} = x \tag{5.28}$$

where

$$y = \frac{i_{Od}}{I_B} \tag{5.29}$$

and

$$x = \sqrt{\frac{2K'_n(W/L)}{I_B}} v_{Id} = \frac{v_{Id}}{V_{GS} - V_T}. \tag{5.30}$$

The solution is given by

$$y = x\sqrt{1 - \frac{x^2}{4}}. \tag{5.31}$$

This is the result for the DC transfer characteristic of the differential pair. This means that for $x = \pm\sqrt{2}$, $v_{Id} = \pm\sqrt{I_B/K'_n(W/L)}$, or $\pm\sqrt{2}(V_{GS} - V_T)$, all current flows in one transistor only. The other transistor is off.
For small values of v_{Id} or x, $y \approx x$, or by using Equations 5.31, 5.28 and 5.27:

$$v_{Od} = -R_L\sqrt{2K'_n(W/L)I_A}v_{Id} \tag{5.32}$$

which can be written as

$$v_{Od} = -g_m R_L v_{Id}. \tag{5.33}$$

The small signal gain thus becomes the same as that of a single transistor operating at the same current $I_B/2$, as each of the transistors of the differential stage.

The cascode transistor on top of the amplifying device in Figure 5.6 is inserted for a number of reasons:

- The cascode device lowers the output conductance by a factor $g_m r_0$, so that the gain is completely controlled by the load network
- The cascode device reduce the Miller effect on the capacitance C_{gd} by ensuring a low impedance at the drain of the amplifying device.
- The cascode improves the reverse isolation of the LNA, thus highly reducing the LO leakage when the LNA is embedded in a receiver.

The integrated series inductors at the input improves the matching in a robust way compared to external matching or bond wire matching. In order to improve the gain, the LNA-output is loaded by an integrated LC-tank, resonating at 17.2 GHz.

A detailed chip photograph of the LNA is presented in Figure 5.8. The inductors L_{IN} and L_S for the input matching and the inductor L_{LOAD} at the output are visible while the circuit is hidden by fill structures. For illustration purposes the CAD layout of the circuit is overlayed (see Figure 5.8).

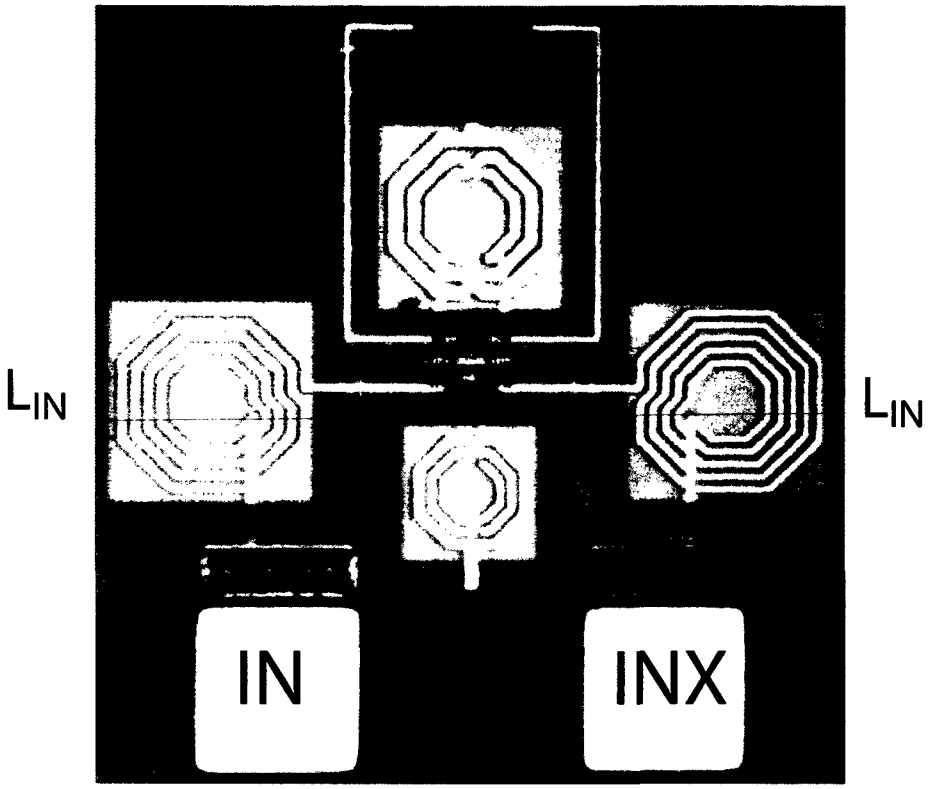

Figure 5.8: Chip photograph of the LNA.

Additionally, new concepts for LNA design were introduced and patented:

- LNA with tunable resonance frequency [Kienmayer 04,a]
- Bandpass ESD protection for LNAs [Kienmayer 04,b].

For high frequency LNAs, inductors are necessary to achieve feasible high gain. Such inductors offers high quality factors but narrow bandwidth. However, future wireless applications require more bandwidth. Up to now, MIM-capacitors were connected in parallel to the inductors and thus decreasing the quality factor and increasing the bandwidth. To tune the center frequency of this circuit, MOS switches are connected in series to the capacitance. Thereby, the MIM-capacitances can be switched on and off which changes the resonance frequency. The disadvantage of this structure is that it consumes much chip area.
This concept can be improved using MOS-varactors instead of MIM-capacitors and MOS-switches. Now, the resonance frequency is tunable by the gate voltage of the varactors. In this case, capacitance and switch are one single component. Figure 5.9 illustrates the implementation with a differential, source degenerated

LNA. MOS-varactors are merged to two rows consisting of two varactors. The LNA output can be shifted by tuning the varactors.
Electrostatic discharge (ESD) for high frequency circuits is a complex technical

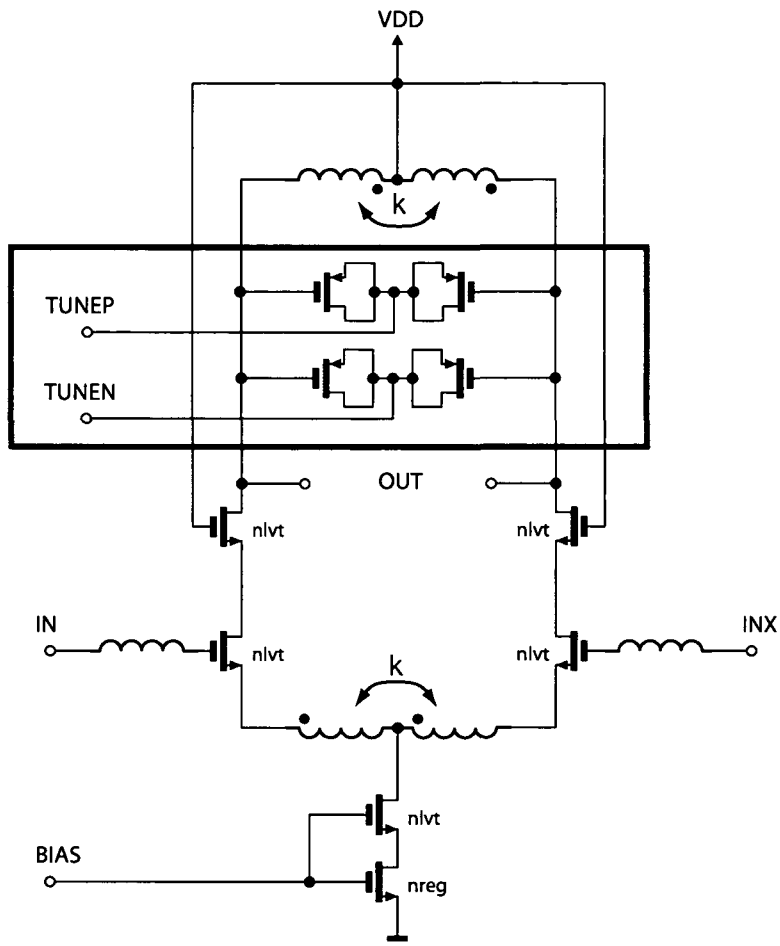

Figure 5.9: Implementation example of a LNA with varactors.

problem because the large parasitic capacitances of the ESD protection components (e.g. diodes, thyristors, grounded NMOS transistors,...) strongly reduce the maximal achievable frequency. Smaller ESD components allow higher frequencies but the protection cannot be entirely fulfilled.
A special case is the protection of differential input or output circuits because ESD discharge can easily destroy the gate oxide of the transistors. Conventionally, additional ESD components are connected for protection which yields extra capacitance.
The main idea is to decouple ESD components with the help of integrated LC tanks, shown in Figure 5.10. Advantage of this method is the usability for high frequencies. Disadvantageous is the consumption of more chip area. Both input pins are connected together by an inductor and capacitances. Employing the cor-

rect design, the two input pins are still isolated against each other. As shown in Figure 5.10(a), at the center tap of the inductor which represents a virtual ground, ESD protection components can be connected without influence. Additionally, matching elements as shown in Figure 5.10(b) can help to improve the impedance matching without disturbing the protection effect.

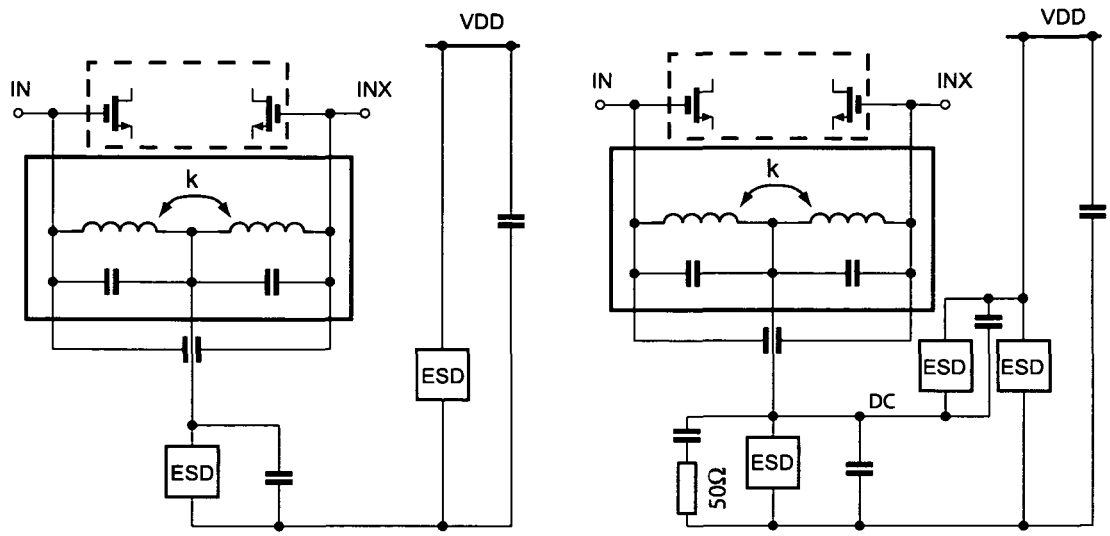

Figure 5.10: Proposed ESD protection for differential input stages.

5.5 1^{st} Down-conversion Mixer

The amplified signal of the LNA output is down-converted to an intermediate frequency of 3.4 GHz for further application, filtering and detection. The first mixer is an integral part of the RF receiver.

Single Balanced Differential Pair Mixer

A single-balanced mixer is basically a differential pair whose bias current is modulated by the RF input, illustrated by the circuit in Figure 5.11.

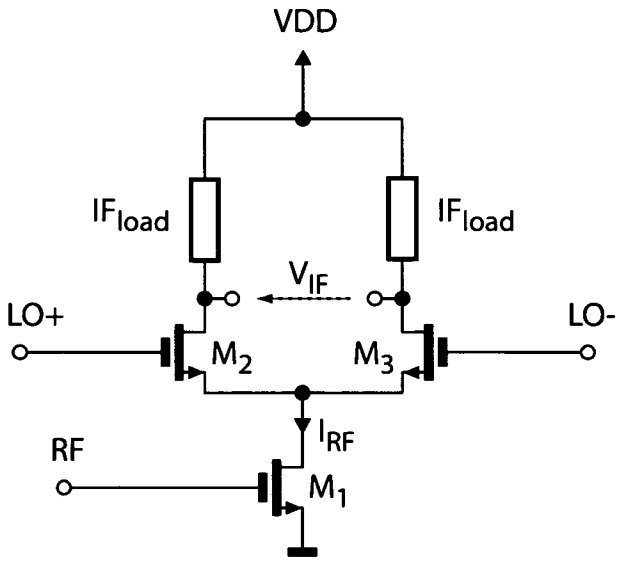

Figure 5.11: Single-balanced mixer.

Due to LO to IF feedthrough, the single-balanced mixer is only used in communications circuits where extremely low noise figures or low power consumption requirements are desired. The more common mixer topology is the double-balanced mixer but it is relatively simpler to illustrate the functionality by the single-balanced equivalent.
For the single-balanced mixer shown in Figure 5.11, the transistor M_1 acts as a transconductor which converts the input RF voltage into a current I_{RF}. This current is fed to M_2 and M_3 (the switching pair) and thus a differential output signal at IF is obtained at the drain of M_2 and M_3. If transistors M_2 and M_3 are driven with a small signal LO, the circuit forms an analog multiplier, where the nonlinearity of the differential pair will provide frequency translation. However, for mixing purposes it is more desirable for transistors M_2 and M_3 to act as switches controlled by the local oscillator signals [Gilbert 96]. LO+ and LO- are two anti-phase large signals that act as the clock for the switching pair of transistors formed by M_2 and M_3. Figure 5.12(a) and (b) depict the single-balanced

mixer in the LO+ and LO- phases.
Therefore, the effect of the switching operation is to multiply I_{RF} with a square

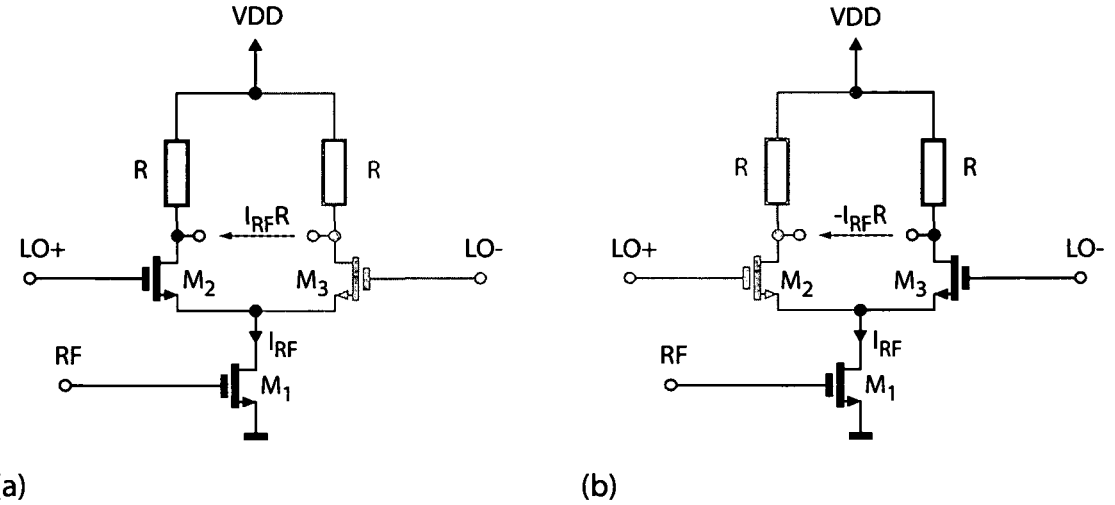

Figure 5.12: Mixer in (a) LO+ phase: M_2 ON, M_3 OFF, (b) LO- phase: M_2 OFF, M_3 ON.

wave signal alternating between +1 and -1 at the frequency of the local oscillator. This can be described mathematically [Rofougaran 96] as:

$$v_{IF} = v_{RF}\cos(\omega_{RF}t) \cdot g_{m1} \cdot R \cdot square(\omega_{LO}t), \tag{5.34}$$

where g_{m1} is the transconductance of M_1.
Substituting for the Fourier series expansion of the square wave gives

$$v_{IF} = v_{RF}g_{m1}R\cos(\omega_{RF}t) \cdot \frac{4}{\pi}[\cos(\omega_{LO}t) + \frac{1}{3}\cos(3\omega_{LO}t) + \ldots] \tag{5.35}$$

$$= \frac{2V_{RF}g_{m1}R}{\pi}\cos(\omega_{IF}t) + \ldots \tag{5.36}$$

In Equation 5.35, multiplication of the ω_{LO} and the ω_{RF} harmonics gives rise to the frequency down-conversion. The preceding analysis suggests that mixers have two main stages:

- a transconductance stage or gain stage
- a switching stage.

The transconductance stage converts the RF input to current and provides the mixer conversion gain together with the IF load. If the switching stage can be assumed to have switching behaviour, the transconductance stage sets the limit on the mixers linearity. Hence it is important to design an input transconductance

that is as linear as possible.
A double-balanced mixer is an extension of the single-balanced mixer using a Gilbert Cell [Gilbert 68] as the mixer core. In Figure 5.19 the implemented mixer schematic diagram with a classical Gilbert cell as core is presented. Transistors M_1 and M_2 form a differential transconductance pair that converts the RF input to a current. This current is then commutated by the switching action of the mixer core formed by transistors M_3-M_6. If all transistors are well matched, then LO feedthrough of M_3 will be canceled by that of M_5, and any feedthrough of M_6 will be canceled by that of M_4. This requires carefully balanced LO switching and a well constructed layout.
The gain of the double-balanced mixer is similar to that for the single-balanced mixer:

$$v_{IF} = v_{RF}G_mZcos(\omega_{RF}t) \cdot \frac{4}{\pi}\left[cos(\omega_{LO}t) + \frac{1}{3}cos(3\omega_{LO}t) + \ldots\right] \quad (5.37)$$

$$= \frac{2V_{RF}G_mZ}{\pi}cos(\omega_{IF}t) + \ldots \quad (5.38)$$

where the IF load is an inductor with impedance Z, v_{RF} is the differential input voltage and G_m is the transconductance of the RF input differential pair [Toumazou 02].

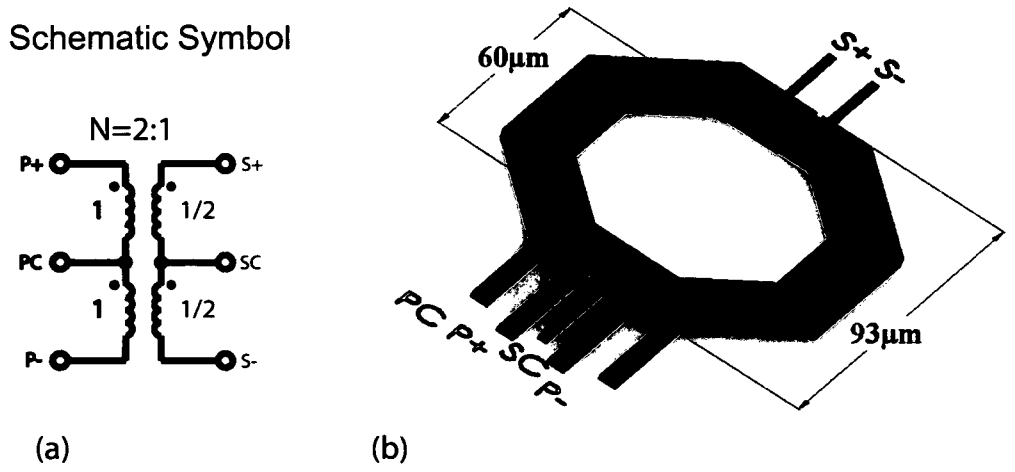

Figure 5.13: Mixer transformer: (a) winding scheme (b) schematic symbol.

To overcome the problems caused by the low supply voltage of 1.5 V for the 0.13 μm CMOS process, a fully differential integrated transformer [Kehrer 01] was inserted between the transconductance stage and the switching pairs.

Figure 5.13 shows the used input transformer and its winding scheme. In the mixer a transformer with a winding ratio of two was implemented, the primary side has two windings and the secondary only one. This results in a 2:1 transformer. The dimensions of the transformer are quite small. A comparison of the symbol with the layout in Figure 5.13 shows the same pins, but due to different winding turns, the secondary center tap lies on the other side. The two top most metal layers were deployed and lower metal layer were used for undercrossings. The size of the transformer is operating at 17.2 GHz 93 $\times$ 93 μm^2.
The total coupling coefficient k is 0.72 at 17.2 GHz. A SPICE low-order equivalent circuit can be found in Figure 5.14. The modeling issues of monolithic transformers are presented in [Kehrer 01] and [Long 00]. The simulation results of the

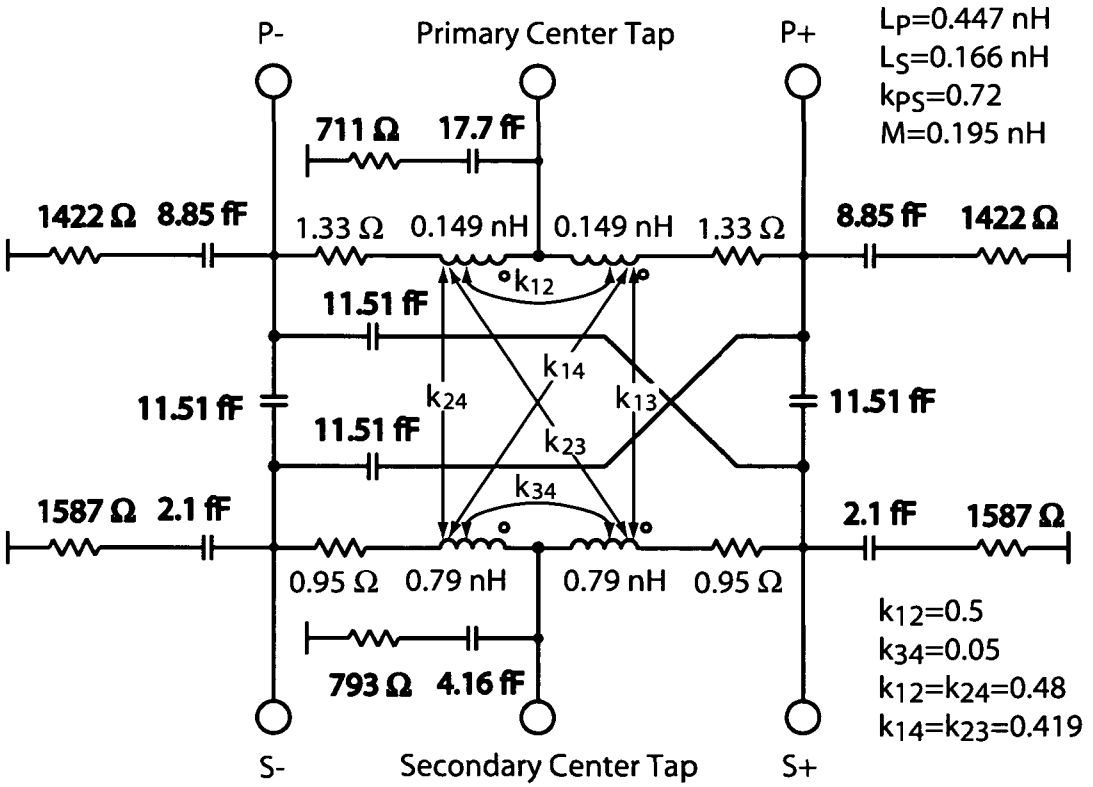

Figure 5.14: Mixer transformer equivalent circuit.

transformer modeling tool FastTrafo [Thüringer 02] are presented in Figure 5.15, 5.16 and 5.17. The resulting SPICE model is shown in Figure 5.14.

As shown in the mixer schematic (Figure 5.19), the supply voltage is connected to the primary center tap while the secondary center tap is grounded. This topology effectively doubles the voltage headroom available for the circuit design, and enables the insertion of cascode transistors to improve the linearity and to control

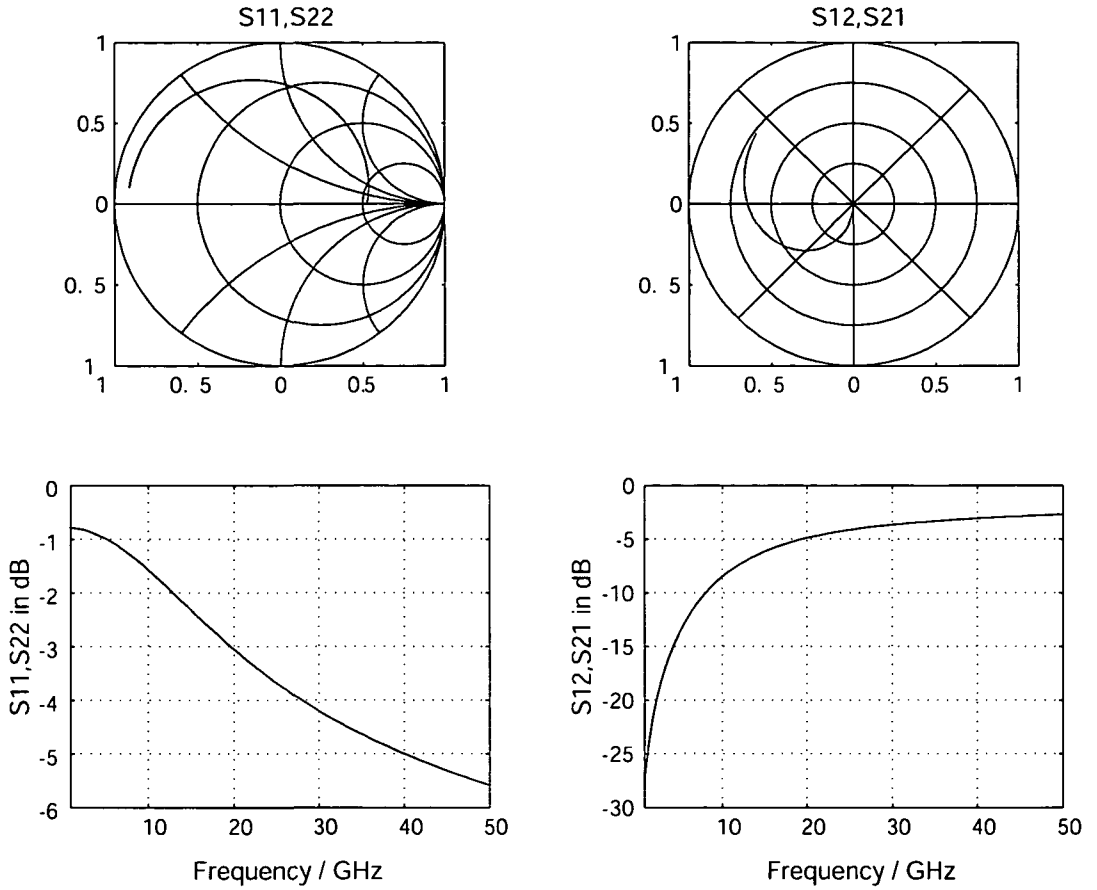

Figure 5.15: S-Parameter simulation results of the input transformer using Fast-Trafo.

the current in the mixer switching stage. To achieve the highest coupling between the two stages the transformer should work in resonance. This is realized by inserting two NMOS-capacitances connected to the primary winding. Due to these capacitances the transformer is tuned to the desired center frequency of 17.2 GHz. Further, the mixer is loaded by an integrated LC-tank to enhance the gain and to provide a second order bandpass filtering. In order to achieve the maximum inductance per chip area, the inductor is realized as cross-coupled fully differential inductor which makes usage of the coupling factor in order to increase the inductance.

The total capacitance seen by the inductor in the circuit is realized by the inherent capacitance of the inductor (inner winding and to substrate) and the capacitance of the connected transistors (drain, gate). Furthermore, the parasitics of the interconnections, especially between two stages, must be taken into account. The inductor of the tank circuit consists of a fully differential integrated 6.6 nH inductor. Figure 5.18 shows the double π-model of the used inductor.
A detailed chip photograph of the transformer-mixer is shown in Figure 5.20. The

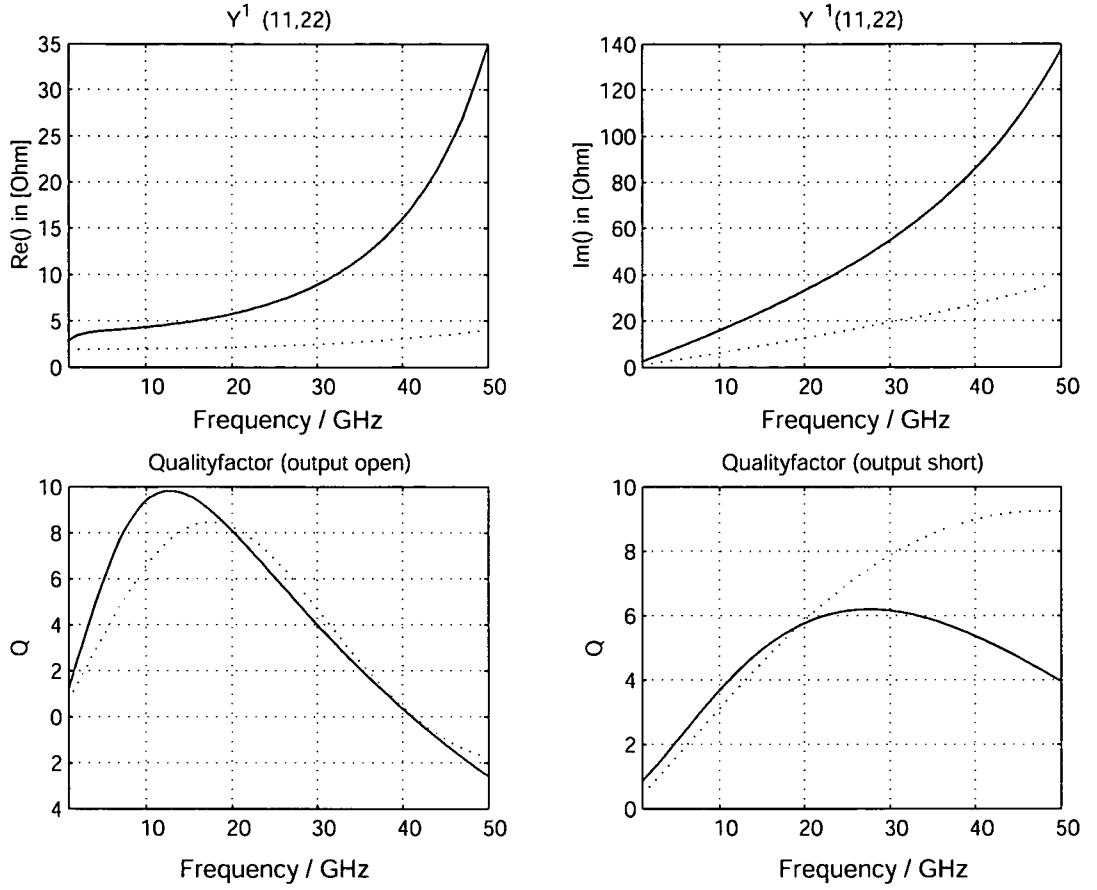

Figure 5.16: Y^{-1}-Parameter simulation results of the input transformer using Fast-Trafo.

die photograph gives quite good relation between the 17.2 GHz monolithic transformer and an inductor for 3.4 GHz. Additionally, the layout of the transistors is drawn to give a better illustration.

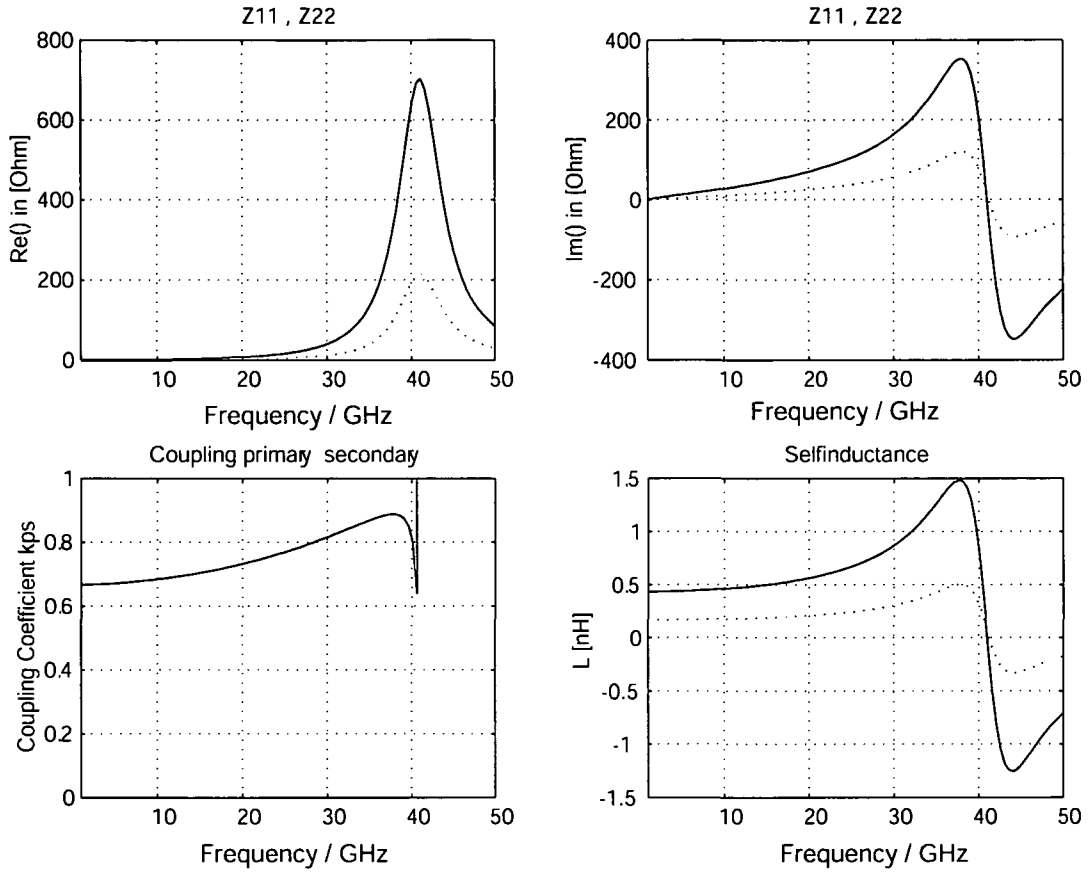

Figure 5.17: Z-Parameter simulation results of the input transformer using Fast-Trafo.

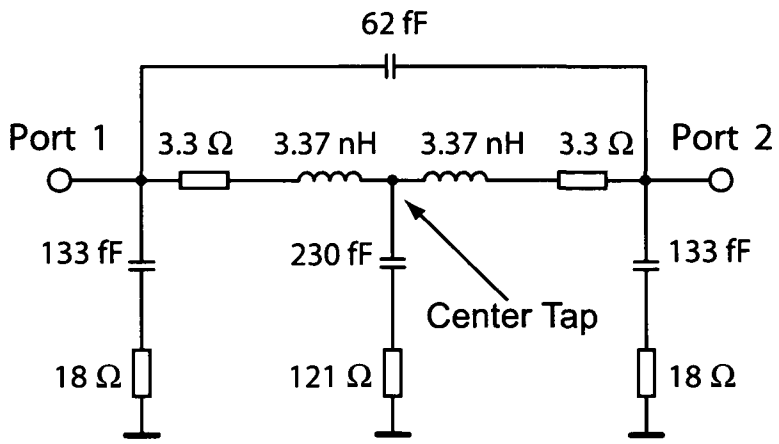

Figure 5.18: Schematic of the 6.6 nH inductor.

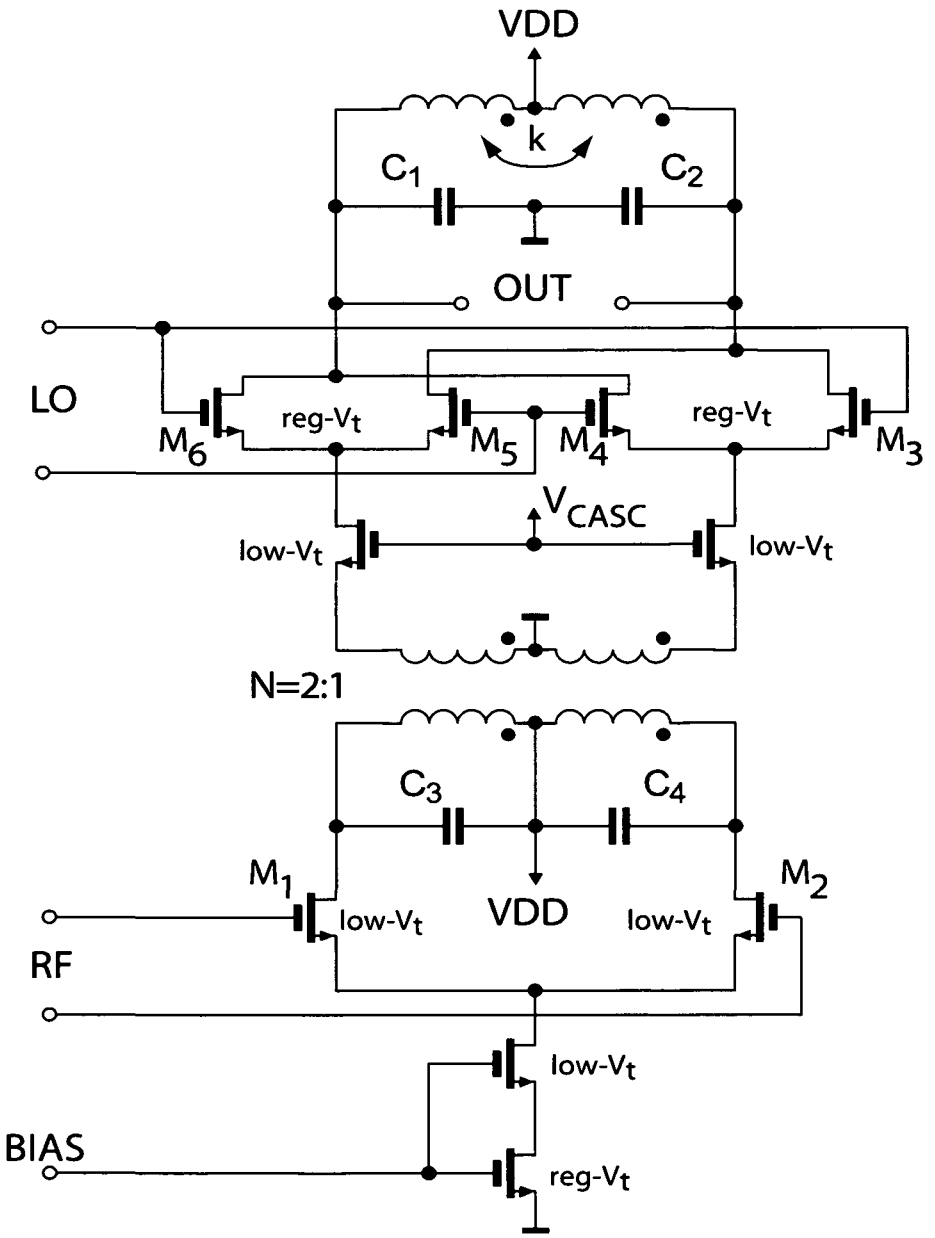

Figure 5.19: Schematic of the first down-conversion mixer.

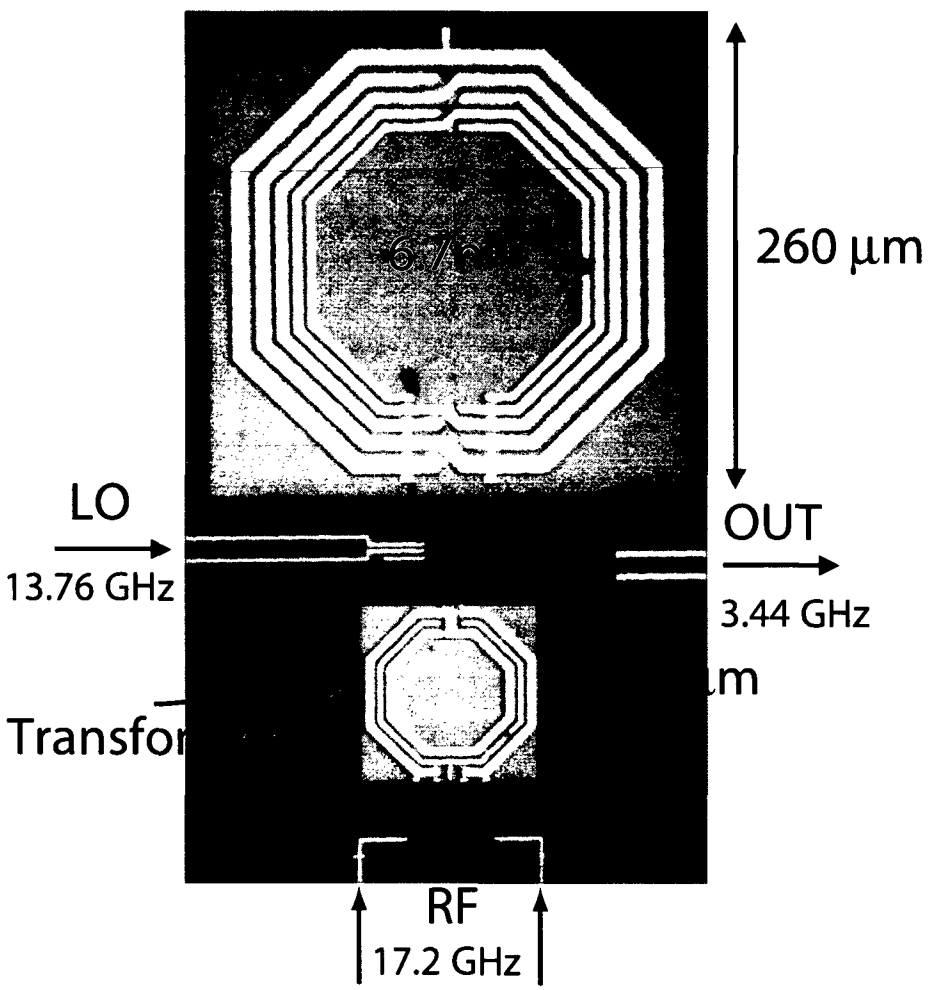

Figure 5.20: Chip photograph of the first down-conversion mixer.

5.6 Intermediate Frequency Amplifier

The first mixer output couples to an intermediate frequency (IF) amplifier. The advantages of the IF amplifier are that the input transistors are very small and therefore provide small capacitances to the resonance circuit at the output of the mixer. Further, the mixer output DC voltage is shifted down to drive the input stages of the following I/Q-mixers. Consequently, a low gain was achieved which is a critical design criteria. Figure 5.21 shows the implementation of the two stage differential amplifier. The first differential amplifier stage has a tail current of

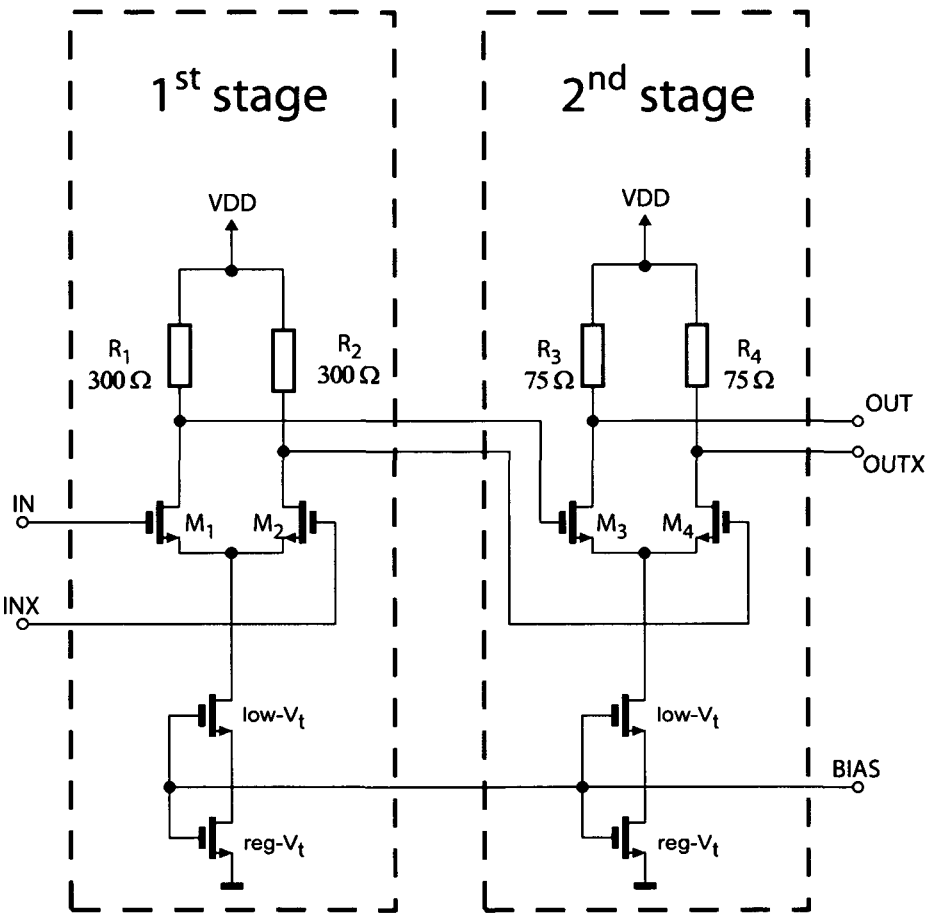

Figure 5.21: Schematic of the intermediate frequency amplifier.

$I_{tail,1} = 1.1\,mA$. The voltage swing of the first stage is

$$V_{swing,1} = R_1 I_{tail,1}. \tag{5.39}$$

The load resistors R_1 and R_2 have a resistance of $300\,\Omega$. Consequently, the first stage offers a high voltage swing of $V_{swing,1} = 330\,mV$. This high voltage swing drives the second stage.. The width $W_{1,2} = 20\,\mu m$ of transistor M_1 and M_2 is

relatively small. Therefore, the input capacitance is small which is important for the LC-tank of the first mixer output.
The second stage drives the input of the I/Q-mixers and therefore large transistor widths with low resistances ($R_3 = R_4 = 75\,\Omega$) are implemented. If output swing ($V_{swing,2}$) is chosen to be 560 mV, a tail current (I_{tail}) of 15 mA is obtained which is about 7 times greater than the first stage tail current.

The bias voltages of the two stage IF-amplifier are nearly fixed. The bias voltage of the first stage is given by the output swing of the first mixer. The first stage output voltage swing V_{swing} is the input voltage swing $V_{bias,2}$ of the current stage i.e. second stage of IF-amplifier. The bias voltage of the second buffer stage is

$$V_{bias,2} = VDD - V_{swing,1} = VDD - I_{tail,1}R_1. \tag{5.40}$$

The voltage swing $V_{swing,1}$ of the first buffer stage becomes $330\,mV$, hence the bias voltage of the second stage is $V_{bias,2}$ is $1.17\,V$.

A complete 17 GHz front-end which includes an inductive source-degenerated LNA, a transformer based Gilbert mixer and an IF amplifier, was published and presented on the *IEEE Symposium on Very Large Scale Integration Circuits 2004* [Kienmayer 04,d]. The front-end was characterized by including bond wires and the measurement board. The measurement results of gain and noise figure as a function of the RF input frequency with a LO frequency of 3.4 GHz apart is presented in Figure 5.22. The two-tone intermodulation results are presented in Figure 5.23. Figure 5.24 shows the power transfer characteristic of the receiver front-end.

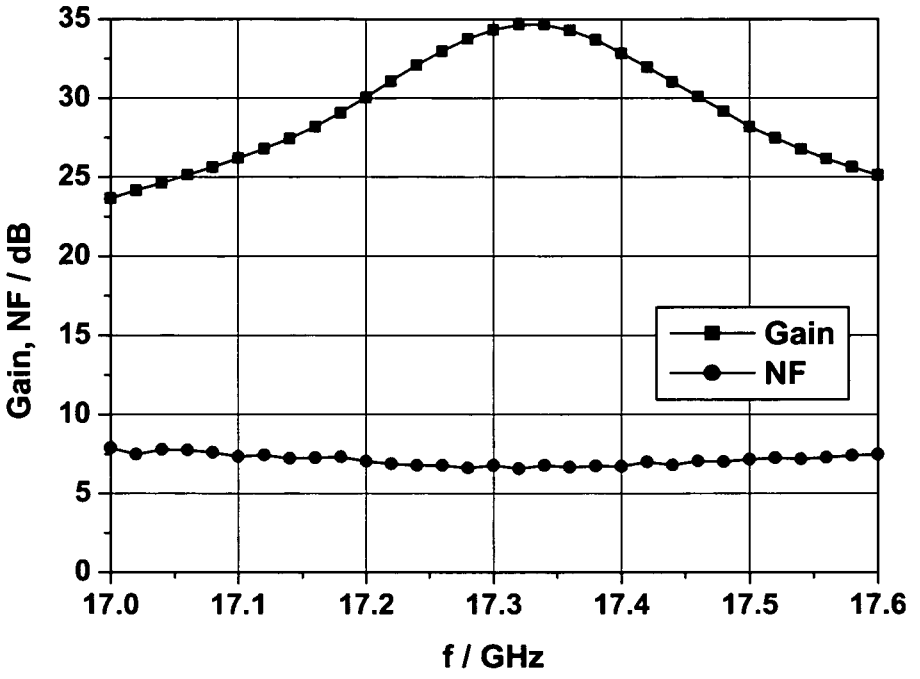

Figure 5.22: Gain and noise figure versus frequency at a fixed IF of 3.4 GHz

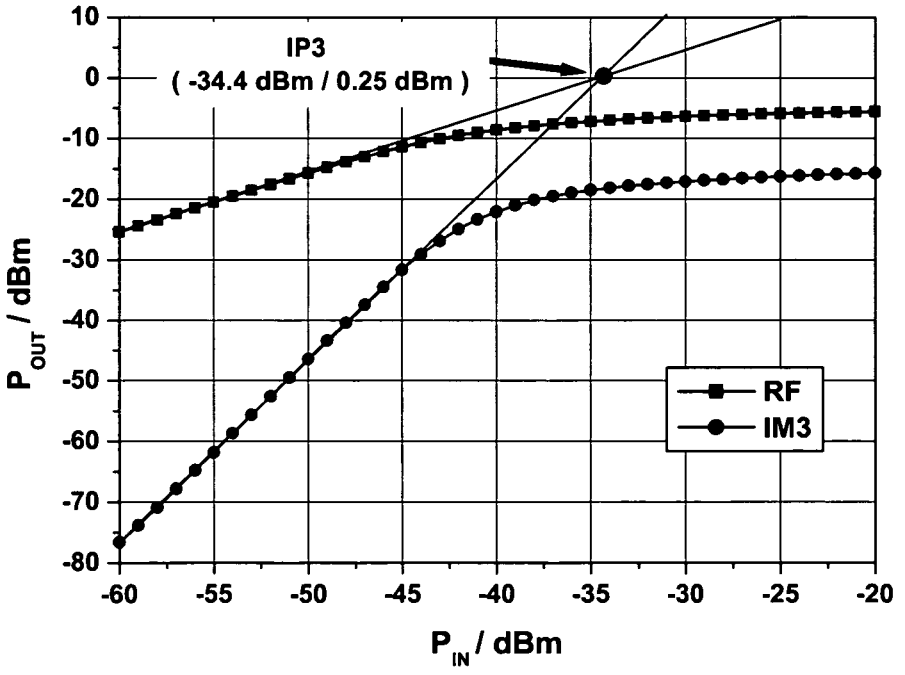

Figure 5.23: Measured front-end two tone test.

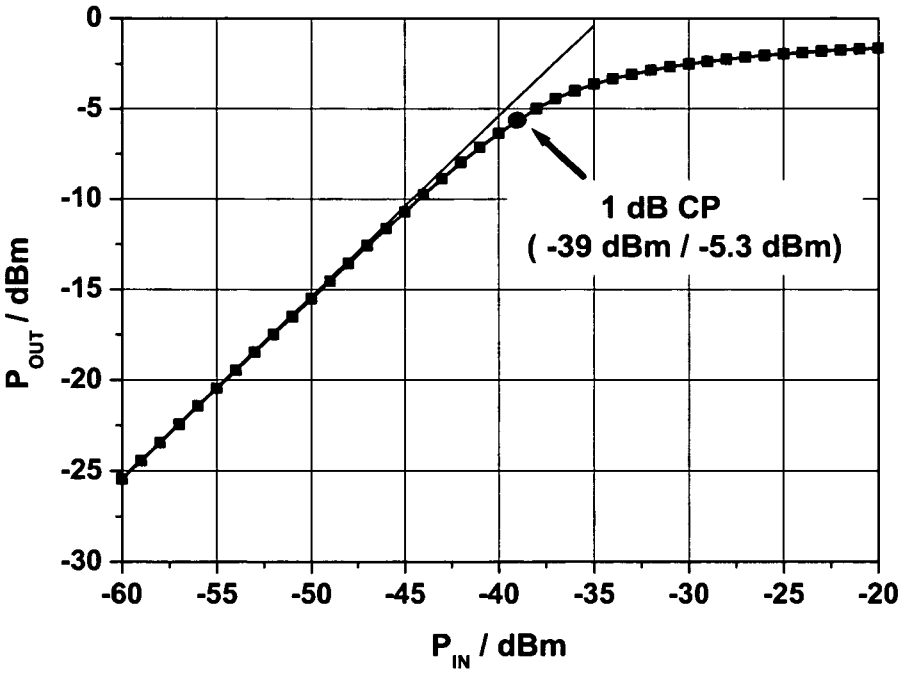

Figure 5.24: Measured power transfer characteristic of the receiver.

5.7 2^{nd} Down-conversion Mixer

The output of the IF amplifier is down-converted by the second mixer stage to the baseband frequency. To get the inphase- and quadrature-outputs, two equal mixers must be connected to the output of the IF amplifier. The mixer is a Gilbert cell mixer with a differential NMOS transistor pair at the input that converts the RF input to a current. This current is then commutated by the switching action of the mixer core. If all transistors are well matched, then LO feedthrough is negligible. This requires vigilant balanced LO switching and an optimized layout as well. The schematic is shown in Figure 5.25.

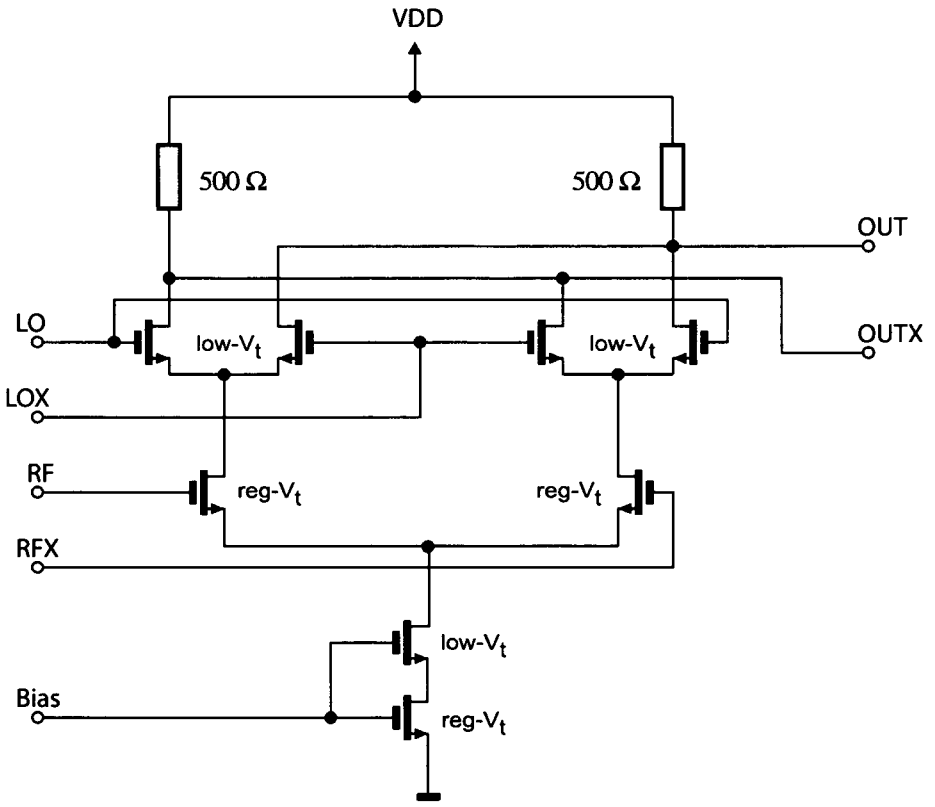

Figure 5.25: Schematic of the second down-conversion mixer.

The bias voltage of the RF input is determined by the IF-amplifier. As stated, the voltage swing is $V_{swing,2} = 560\,mV$,

$$V_{bias,RF} = VDD - V_{swing,2} = VDD - I_{tail,2}R_3. \tag{5.41}$$

So the bias voltage $V_{bias,RF}$ of the input becomes $0,94\,V$. The bias voltage of the Gilbert cell is determined by the buffer of the 4:1 divider. The voltage swing

V_{swing} at the buffer is 460 mV, therefore the bias voltage is $V_{bias,LO} = 1.04\,V$. The derivation of the gain of a double-balanced mixer is similar to that for the single-balanced mixer:

$$v_{IF} = v_{RF} G_m R_L cos(\omega_{RF} t) \cdot \frac{4}{\pi} \left[cos(\omega_{LO} t) + \frac{1}{3} cos(3\omega_{LO} t) + \ldots \right] \quad (5.42)$$

$$= \frac{2 v_{RF} G_m R_L}{\pi} cos(\omega_{IF} t) + \ldots \quad (5.43)$$

where the IF load is a resistor R_L, v_{RF} is the differential input voltage and G_m is the transconductance of the RF input differential pair [Razavi 99]. A testchip was designed to verify the correct operation of the mixer.

The two-tone test results for third-order intermodulation distortion are shown in Figure 5.27. The test was performed at 3.44 GHz. Input IP_3 is -4.5 dBm and the input referred 1dB-compression point from Figure 5.26 is -13 dBm. In Figure 5.28, the power gain versus input frequency at 1 MHz output frequency is reported while in Figure 5.29 the power gain in the baseband is shown. The maximum power gain of the second down-conversion mixer is 5.3 dB and the -3 dB bandwidth is 300 MHz.

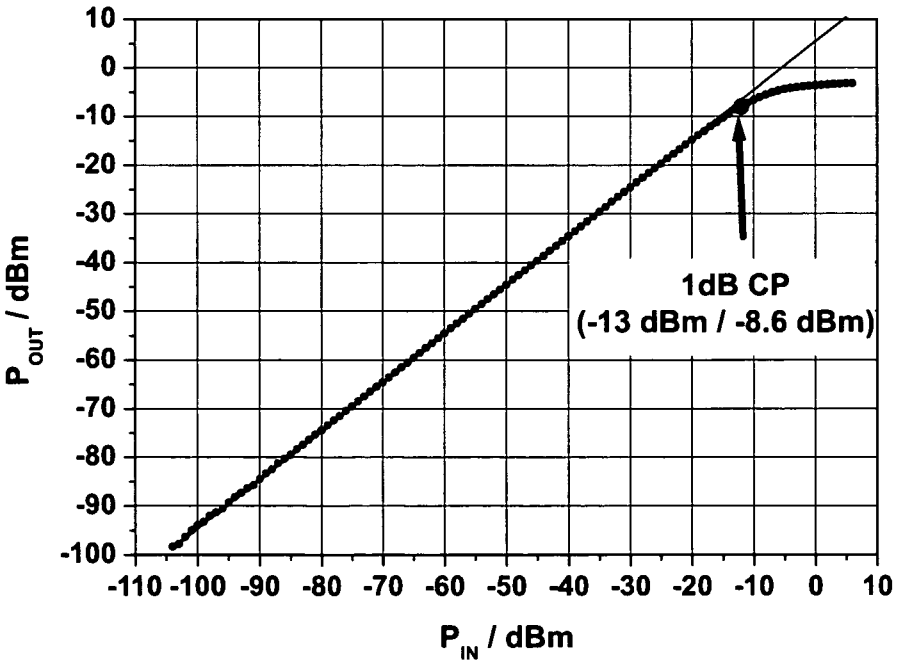

Figure 5.26: Measured single-tone compression point.

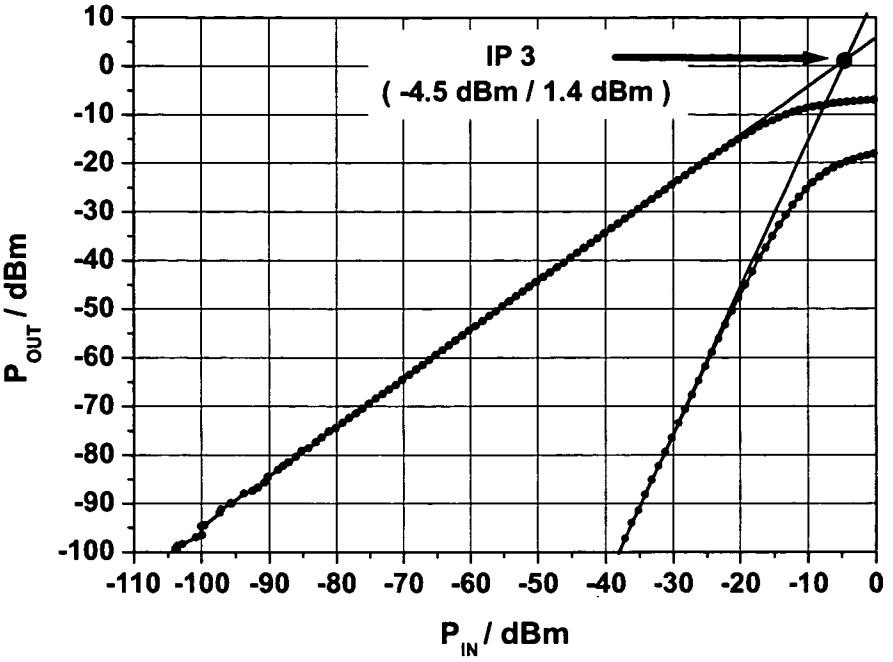

Figure 5.27: Linearity measurement of the second down-conversion mixer.

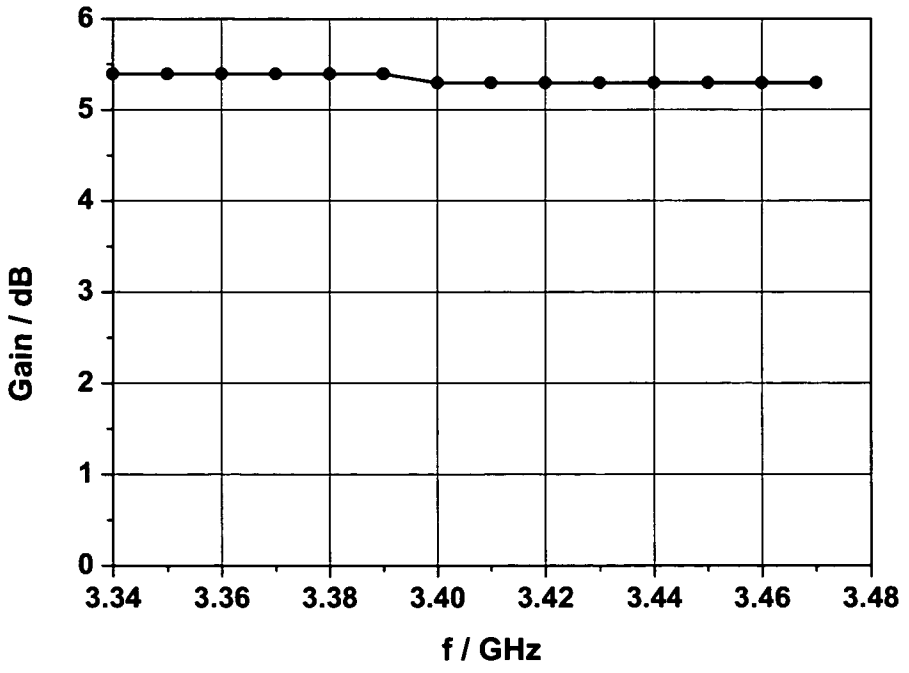

Figure 5.28: Mixer gain versus input frequency at 1 MHz output frequency.

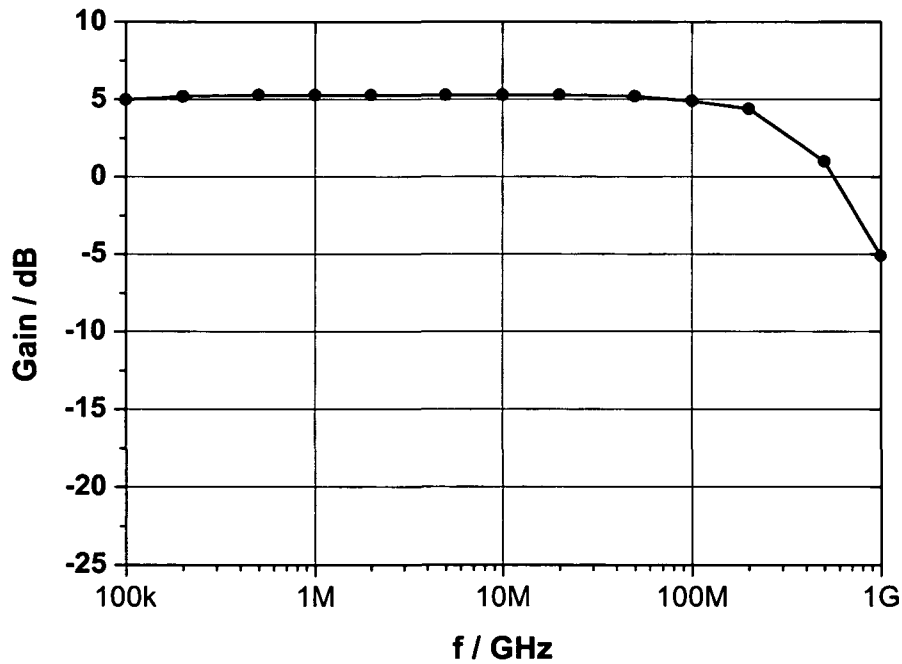

Figure 5.29: Gain versus baseband frequency.

5.8 Voltage Controlled Oscillator

Fully integrated VCOs operating at frequencies in the millimeter wave bands are to date mainly realized in III-V or SiGe technologies. The recent ongoing shrinking of CMOS technologies to deep-submicron dimensions enabled the design of CMOS oscillators at frequencies in the range of 10 to 50 GHz [DeRanter 01][Wu 01] [Wang 01] [Hung 00].
A general LC-VCO can be symbolized as in Figure 5.30. The oscillator consists of an inductor L and a capacitor C, building a parallel resonance tank, and an active element -R, compensating the losses of the inductor as well as of the capacitor (R_L and C_L in Figure 5.30). Angular center frequency of the oscillator is given by:

$$\omega_c = \frac{1}{\sqrt{LC}}. \tag{5.44}$$

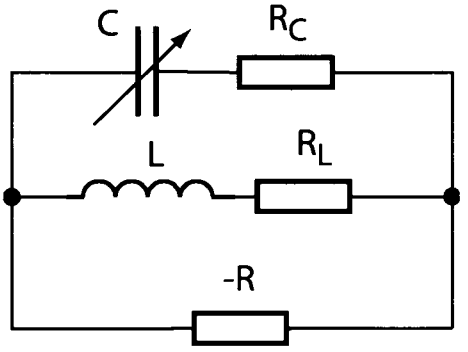

Figure 5.30: Basic inductor-capacitor (LC) VCO.

Typically, the capacitance C is realized as varactor. Its value depends on the tuning input voltage. So the circuit works as a voltage controlled oscillator. The capacitor C in Figure 5.30 not only includes the variable capacitor to tune the oscillator, but it also includes the layout parasitics or fixed capacitances of the inductor, the active elements and of any load connected to the VCO (mixer, prescaler, etc.).
The ideal sinusoidal oscillator is described as

$$v_{out}(t) = V_0 \cos(2\pi f_c t + \phi) \tag{5.45}$$

with constant amplitude V_0, center frequency f_c and ϕ as a fixed phase. In the frequency domain the spectrum of this oscillator only shows a Dirac impulse at frequency $\pm f_c$. A nonideal oscillator is generally given by

$$v_{out}(t) = v_0(t) y(2\pi f_c t + \phi(t)), \tag{5.46}$$

where y denotes a periodic function. The fluctuations introduced by $v_0(t)$ and

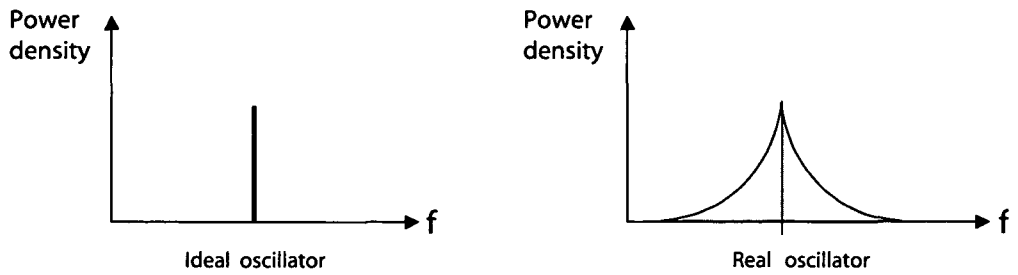

Figure 5.31: Frequency spectrum of ideal and real oscillators.

$\phi(t)$ - now functions of time - result in spectral sidebands with symmetrical distribution around center frequency f_c (Figure 5.31). The frequency fluctuations correspond to jitter in the time-domain which is random perturbation of zero-crossings of a periodic signal (Figure 5.32).

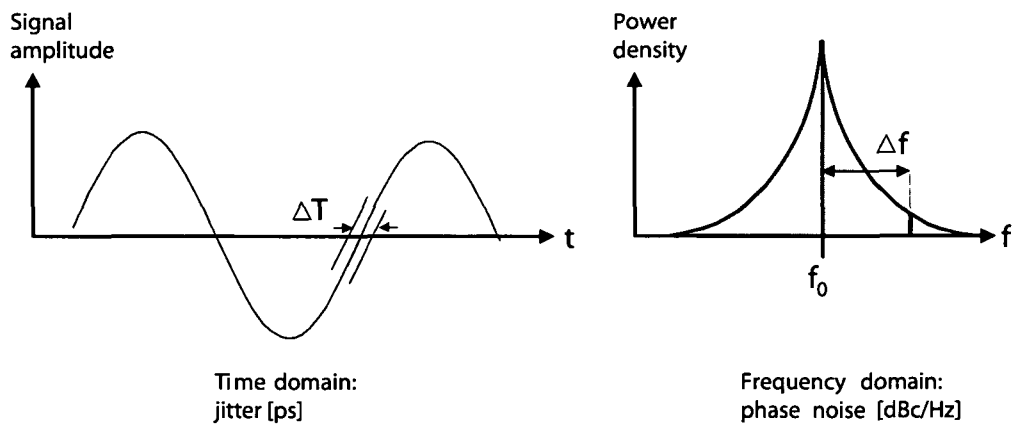

Figure 5.32: Jitter in the time domain relates to phase noise in the frequency domain.

Frequency fluctuations are usually characterized by single sideband noise spectral density normalized to the carrier signal power. It is defined as

$$L_{total}(f_c, \Delta f) = 10 \cdot log \left[\frac{P_{sideband}(f_c + \Delta f, 1\,Hz)}{P_{carrier}} \right] \tag{5.47}$$

and has units of decibel below the carrier per Hertz (dBc/Hz). $P_{carrier}$ is the carrier signal power at the carrier frequency f_c and $P_{sideband}(f_c + \Delta f, 1\,Hz)$ denotes the single sideband power at the offset Δf from the carrier f_c at a measurement bandwidth of 1 Hz.

The schematic of the oscillator is presented in Figure 5.33. For this topology only NMOS transistors are chosen because the speed of NMOS transistors ($f_t \approx$

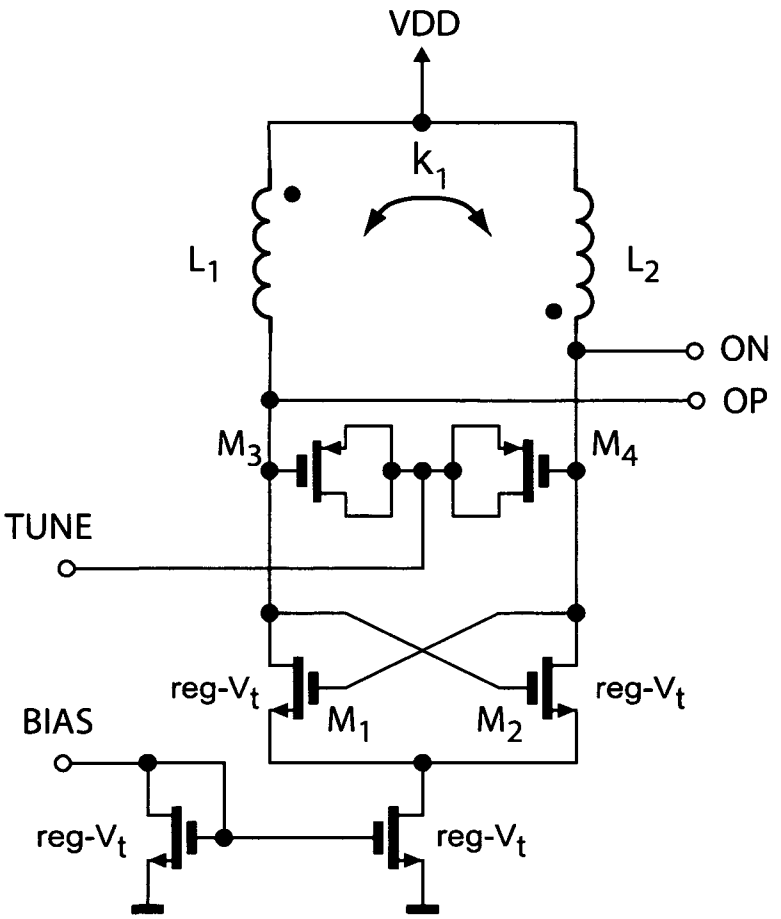

Figure 5.33: Schematic of the 13.76 GHz VCO.

$100\,GHz$) is much higher than for PMOS ($f_t \approx 50\,GHz$). As the voltage swing of this topology exceeds the power supply voltage, the voltage is reduced from nominal 1.5 V to 1 V for reliable operation within the technology limits. The general LC-VCO consists of coupled inductors (L_1, L_2 coupled by k_1) which are laid out as one fully symmetrical inductor with middle tap. The coupling factor of about 0.8 (FastHenry [M.I.T. 04,b] simulation) nearly doubles the effective inductance. The differential layout generally makes the oscillator less sensitive to substrate noise when co-integrating it with other circuits. The symmetrical coil is operated in balanced mode and is modeled by a double-π model as presented in Figure 5.34.

For the tuning of the oscillator conventional 4-terminal NMOS transistors are used as varactors (see Section 3.2.3). The measured tuning-characteristic of the VCO is presented in Figure 5.35. The measured VCO resonance frequency is a little bit to low. Further the inductor of the VCO was adapted before it was implemented in the receiver. For the use in a receiver, the output voltage swing as well as the phase noise power are an important design criteria. A high voltage

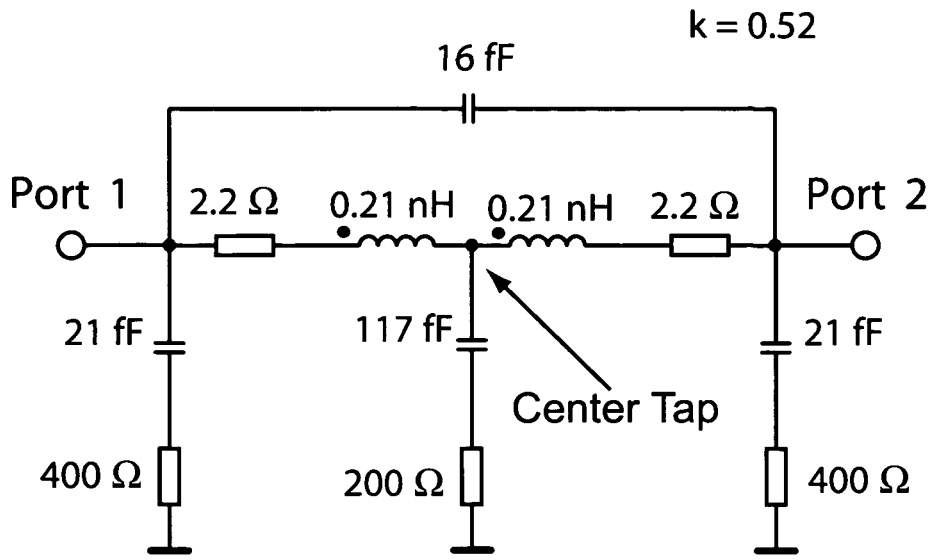

Figure 5.34: VCO inductor equivalent circuit.

swing of the VCO is required for input of the mixers. The measured output power and phase noise power versus tuning voltage is shown Figure 5.36. Further, the phase noise of free running VCO is presented in Figure 5.37.

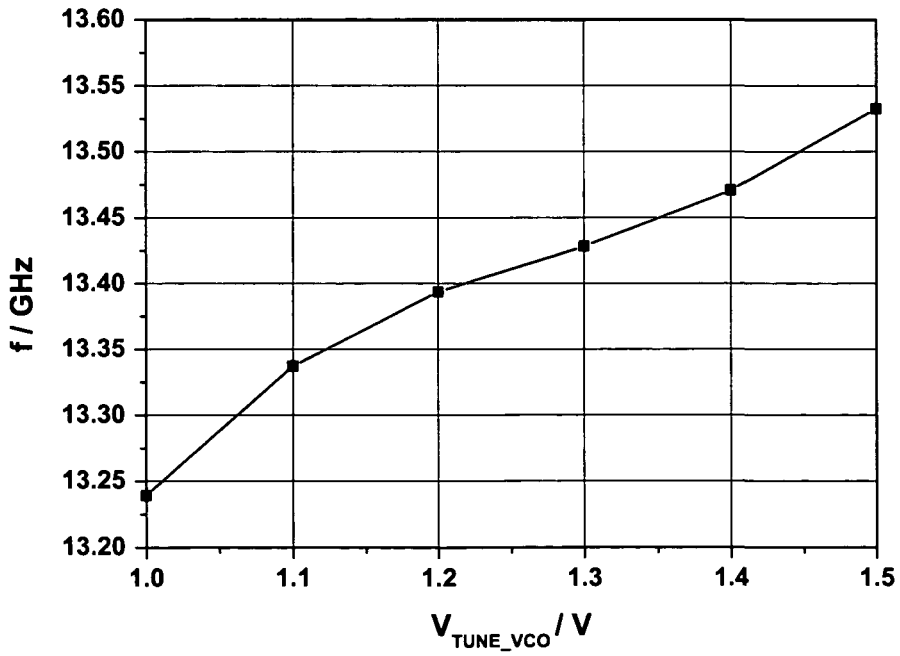

Figure 5.35: VCO frequency versus tuning voltage.

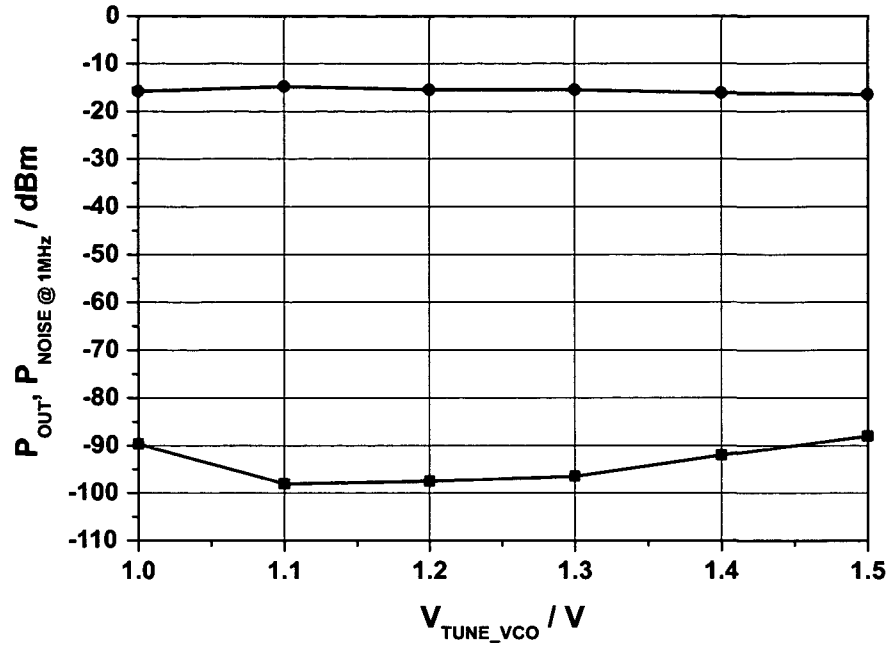

Figure 5.36: Measured output power and phase noise power versus tuning voltage.

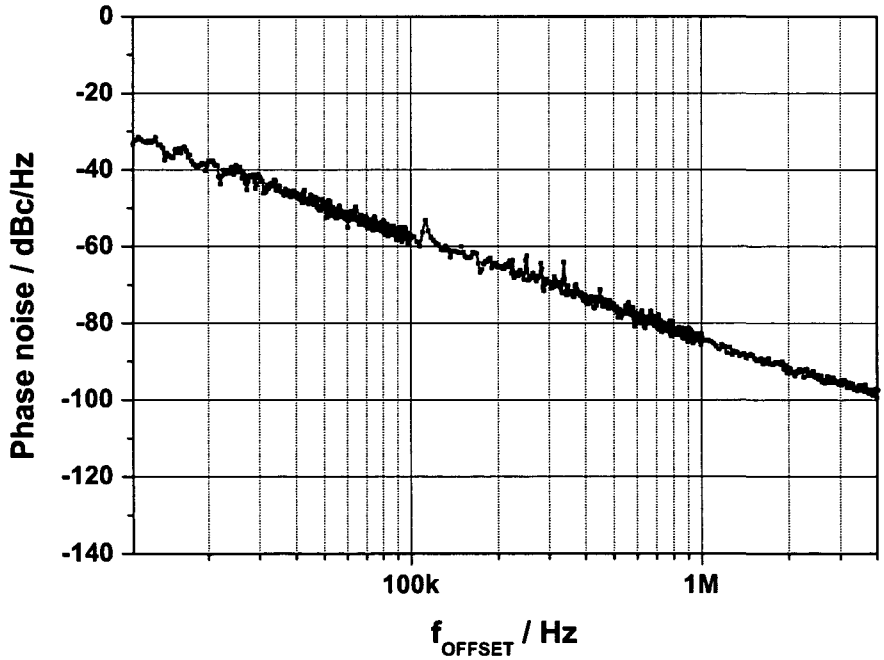

Figure 5.37: Measured VCO phase noise at V_{TUNE_VCO} of 1.5 V.

5.9 I/Q-Divider

The block diagram in Figure 5.38 shows how the VCO output signal is divided to produce the LO-signals for the second mixers and the PLL-output. A feedback exists from the inverted output of the fourth latch to the input of the first latch, which provides the static 4:1 synchronous divider functionality. The output is a square wave with 50% duty cycle and a frequency which is fourth the frequency applied to the clock input $VCO-CLK$. The waveforms of the outputs are exactly 90° phase-shifted, which is further used for the inphase and quadrature mixer stage in the receiver. The PLL reference signal, which is half of the frequency of the LO for the mixers, is generated by a static 2:1 divider. As shown in Figure 5.38, therefore, two additional latches with a separate feedback are connected to the chain. For testing the functionality of the clock generation shown in Figure 5.38, a separate testchip was fabricated. The testchip consists of a static 2:1 divider, to characterize and evaluate the speed of the D-latches. In the following, the 2:1 divider is explained in detail. Recently, operating frequencies up to

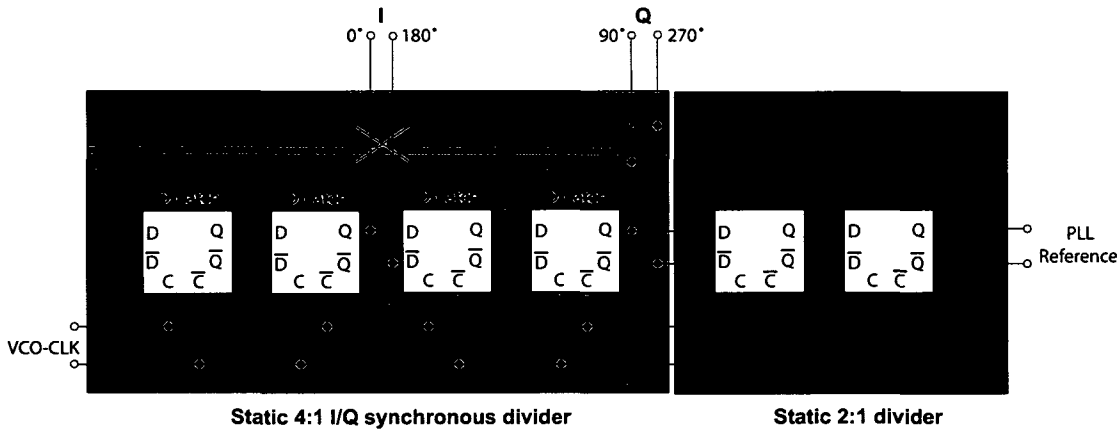

Figure 5.38: Block diagram of clock generation with latches.

30 GHz of 2:1 divider in CMOS have been reported [Knapp 02][Wohlmuth 02,a]. Frequency dividers with higher functionality like prescalers reach frequencies up to 16 GHz in CMOS [Wohlmuth 02,b].
Figure 5.39 shows the block diagram of a static 2:1 frequency divider used in the receiver. The internal dividing function is based on a Master-Slave Flip-Flop (MS-FF) by connection the inverted slave outputs to the master inputs. For high speed operation, the well-proven common mode logic (CML) principle is used, which decreases the internal voltage swing and therefore guarantees high operation frequencies. In Figure 5.40 the schematic of a CML D-latch is shown which is used to form a MS-FF. In the high frequency part low-V_T NMOS devices are used due of their higher speed compared to PMOS transistors. 100 Ω Poly-silicon resistors are used as low capacitive loads for the latches. Due to a differential

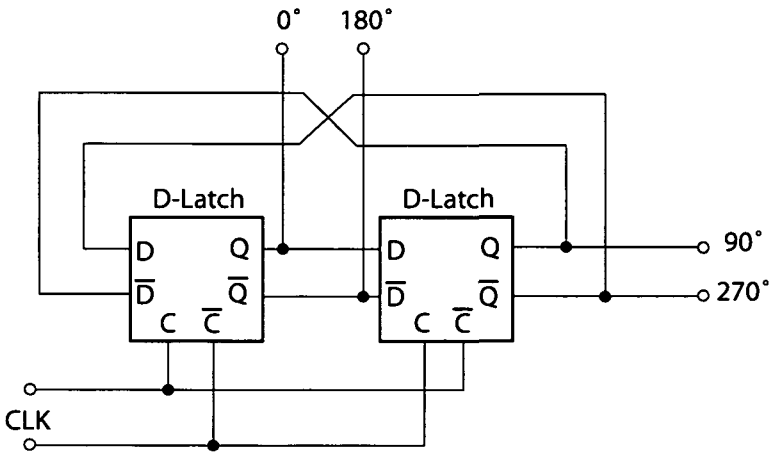

Figure 5.39: Block diagram of a static frequency 2:1 divider.

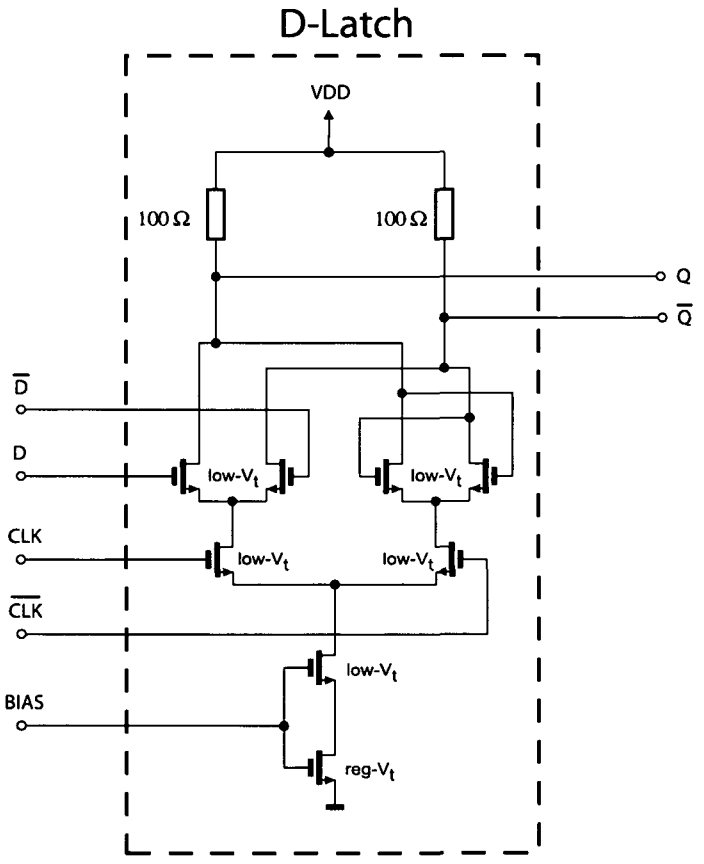

Figure 5.40: D-latch circuit diagram.

design is applied, the layout is kept as symmetrical as possible. Furthermore, all interconnects are kept as short as possible. Especially the lines between slave

outputs and master inputs affect the maximum operation frequency due of their propagation delay and capacitive load.
To evaluate the circuit performance and its applicability to the receiver, the chip was mounted on a $30 \times 30\,mm^2$ 0.51 mm RO4003 microwave substrate ($\varepsilon = 3.38$) with SMA connectors for input and output signals. The measured data from Figure 5.41 and 5.42 represents the performance of the divider and includes the loss caused by the bond wires, microstrip lines on the test board, RF connectors an the 180°-hybrid coupler. The differential input signal was generated by a 180°-hybrid coupler.
Figure 5.41 gives the input sensitivity versus input frequency. The circuit shows broadband performance up to operating frequencies of 22 GHz with input levels less than 0 dBm. The highest input sensitivity is measured at 18 GHz. The loss

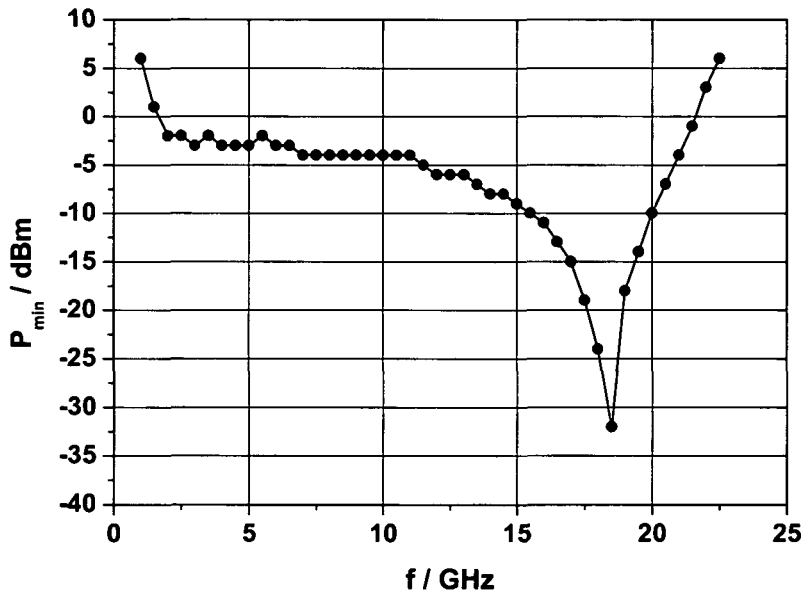

Figure 5.41: Measured divider sensitivity versus input power.

of sensitivity below 2 GHz is caused by the lower cut off frequency of the hybrid coupler and the limited slew rate of the sinusoidal input signal. Operation at lower frequencies requires a square-wave input signal. Figure 5.42 shows the input waveform (top) and output transient signals (middle and bottom) at 15 GHz input frequency. The measured single-ended output voltage swing on an external 50 Ω load is two times $150\,mV_{pp}$ at 15 GHz. The divider supply current is 30 mA at 1.5 V supply voltage.

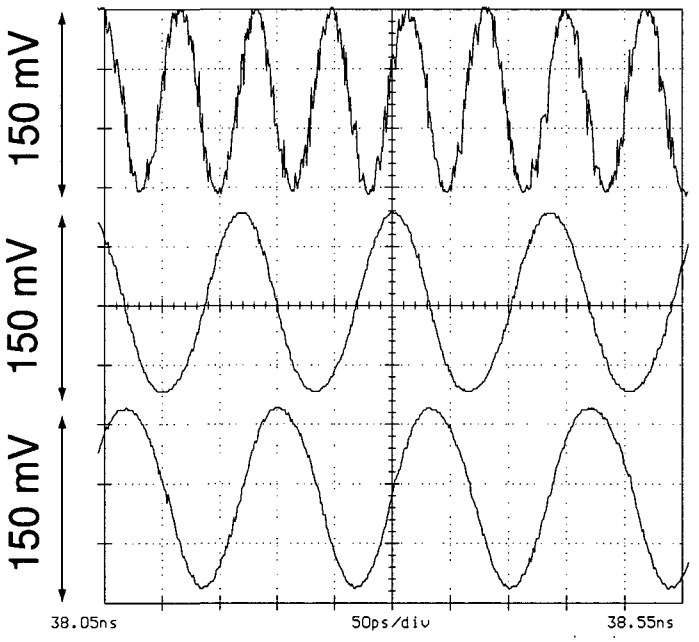

Figure 5.42: Measured single ended input and output waveforms at the input frequency of 15 GHz.

5.10 LO-Buffer

As shown in the block diagram presented in Figure 5.1, the VCO and the output of the 4:1 divider have a buffer to drive the mixers in the receiver. The input of the buffers is a relatively small transistor pair, which provides a small load capacitance C_L for the previous stage. First, this is important for the VCO because the LC-tank is not so much out of tune. Secondly, the bandwidth of the 4:1 divider is increased.
Figure 5.43 shows the schematic diagram of the used LO-buffer. The buffer consists of two differential stages. The first differential amplifier stage has a tail current of $I_{tail,1} = 1.1\,mA$. The voltage swing of the first stage is

$$V_{swing,1} = R_1 I_{tail,1}. \tag{5.48}$$

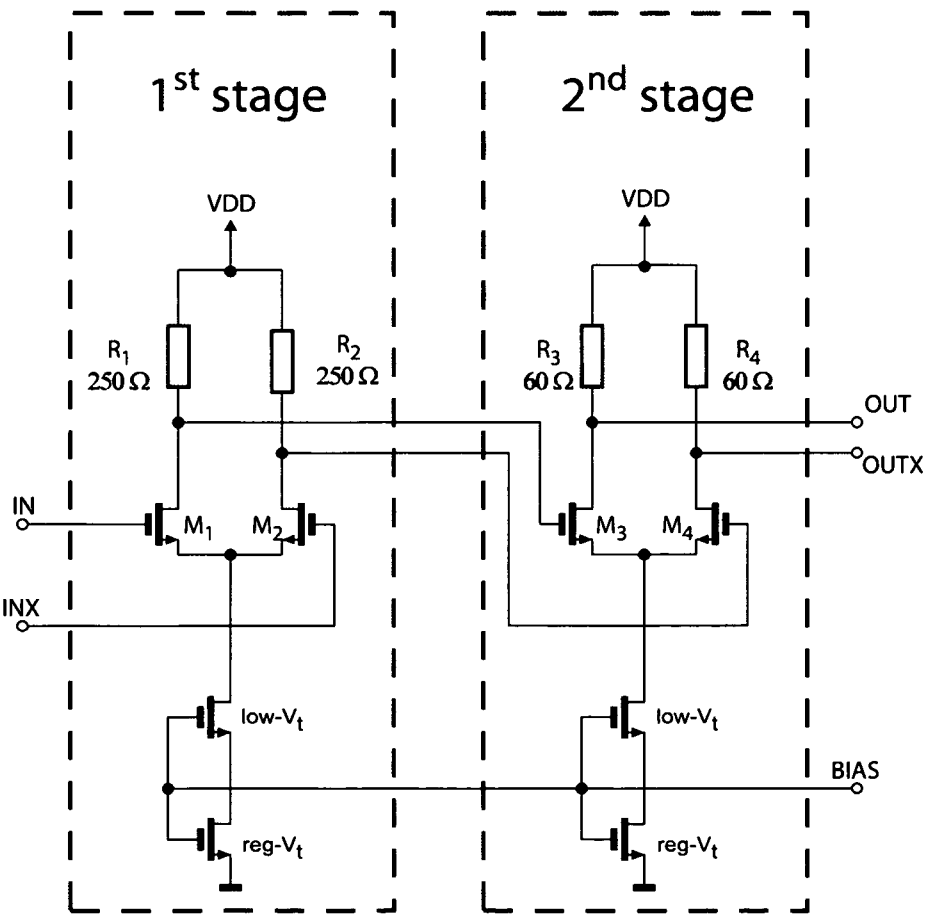

Figure 5.43: Schematic diagram of the two stage LO-buffer.

The load resistors R_1 and R_2 have a resistance of 250 Ω. The first stage offers a high voltage swing of $V_{swing,1} = 275\,mV$. This voltage swing drives the second stage of the amplifier. The gate width $W_{1,2} = 12\,\mu m$ of transistors M_1 and M_2 is

chosen to be relatively small to get a small capacitance.
The second stage drives the input of the mixers and therefore uses $R_3 = R_4 = 60\,\Omega$ load resistors. The low resistance is important to drive the following input stages with relatively large transistor widths.
An output swing of $V_{swing} = 460\,mV$ is chosen, a tail current of $I_{tail} = 15.2\,mA$ is set. The tail current of the second stage is about 7 times greater than the tail current of the first stage.
The bias voltages of the two stage buffer are nearly fixed. The bias voltage of the first stage is given by the output DC levels of the VCO and the 4:1 divider. The output voltage swing V_{swing} of the previous stage is the input voltage swing $V_{bias,2}$ of the current stage. The bias voltage of the second buffer stage is

$$V_{bias,2} = VDD - V_{swing,1} = VDD - I_{tail,1}R_1. \tag{5.49}$$

The voltage swing $V_{swing,1}$ of the first buffer stage becomes $275\,mV$. Consequently, then the bias voltage of the second stage is $V_{bias,2}$ is $1.225\,V$.

5.11 Operational-Amplifier

For the output buffer an operational transconductance amplifier (OTA) is used as an operational amplifier (op amp). Generally, an OTA has a large open-loop output resistance at low frequencies. The noninverting amplifier shown in Figure 5.44(a) is obtained by connecting the output to the negative input of the OTA. This topology forms a so called *unity gain amplifier*. The advantage of this circuit being its unity gain and behaviour as an ideal voltage-controlled voltage-source (VCVS) over a wide range of frequencies. In Figure 5.44(b) the schematic of the simple CMOS OP-amplifier is shown with a self-biasing NMOS differential stage with active load. Transistors M_1 and M_2, with equal $(W/L)_1$ ratios, form a matched transistor pair, while M_3 and M_4 also have equal $(W/L)_4$ ratio. All current levels are determined by current source I_B. Half of current I_B flows through M_1 and M_3 and the other half through M_2 and M_4, respectively.

According to specification, an implementation of a simple CMOS OTA with a certain gain-bandwidth product (GBW) for a given load capacitance C_L is mandatory. The GBW is given by

$$GBW = \frac{g_{m1}}{2\pi C_L}. \tag{5.50}$$

[Laker 94] yields

$$(W/L)_1 = (W/L)_2 \left(\frac{C_{13}}{C_L}\right)^2. \tag{5.51}$$

C_{13} is the node capacitance between transistor M_1 and M_3. Hence, it is necessary to determine three variables: I_B, $(W/L)_1$ and $(W/L)_4$.
Finally, the design procedure presented by [Laker 94] leads to the following op-amplifier parameters:

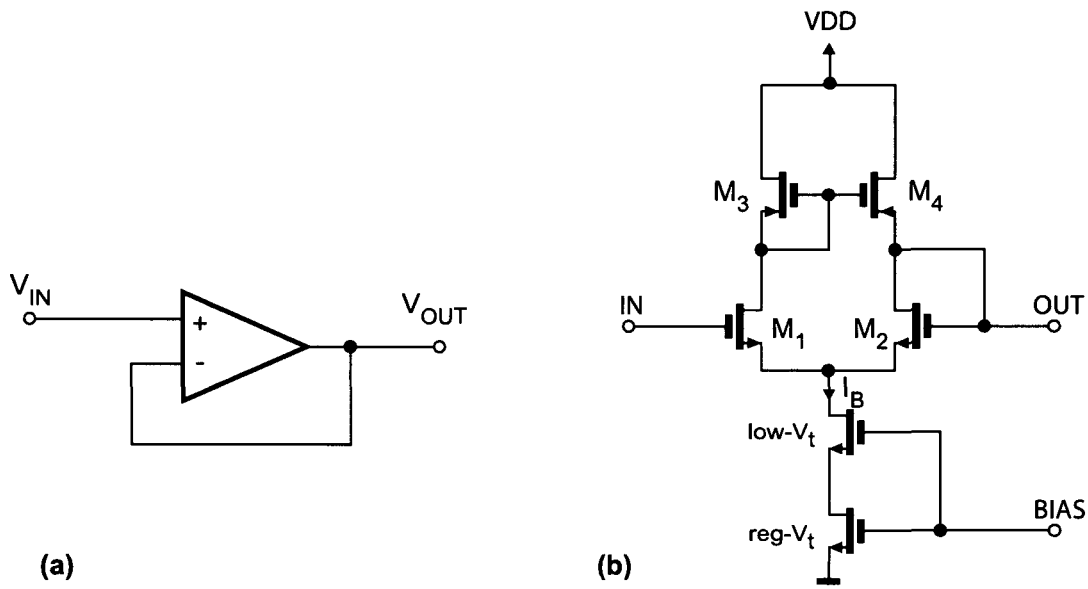

Figure 5.44: Symbol (a) and schematic (b) of the operational amplifier.

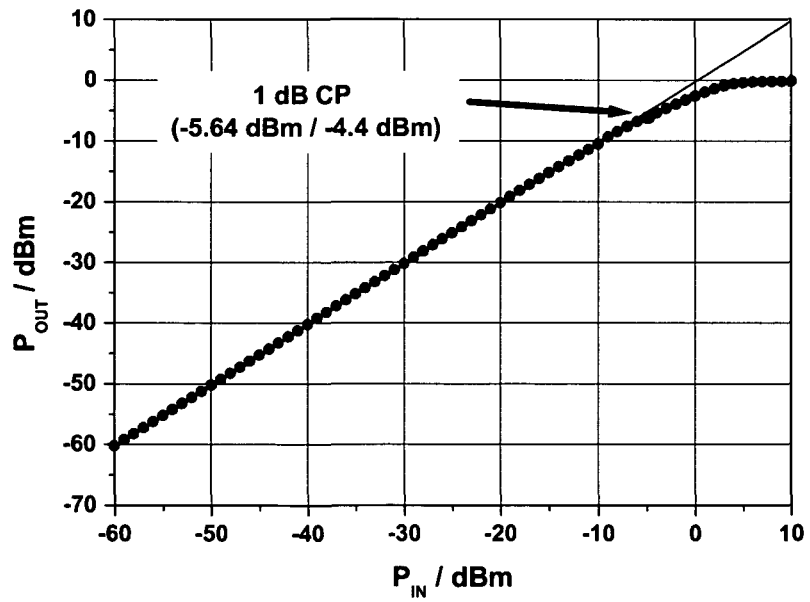

Figure 5.45: Linearity plot of the operational amplifier.

Figure 5.45 shows the measured single-tone compression point of the developed op-amplifier. For different input DC voltages, the gain is plotted in Figure 5.46.

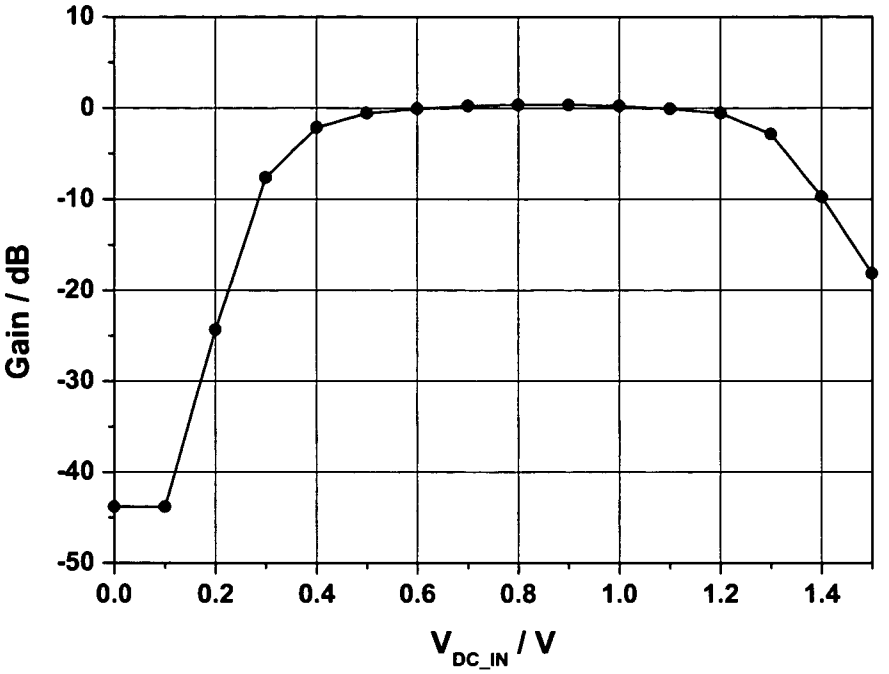

Figure 5.46: Gain versus DC bias voltage of the operational amplifier.

$(W/L)_1$	(300 μm/500 nm)
$(W/L)_4$	(450 μm/500 nm)
I_B	6.43 mA
Gain	0 dB

Hence, the op-amplifier can be used in the range of 0.5-1.2 V of input DC voltages.

Chapter 6

Receiver Experimental Results

6.1 Introduction

In this chapter, different RF building blocks as described in Chapter 5, are combined to implement a sliding-IF 17 GHz receiver front-end manufactured in 0.13 μm CMOS technology [Tiebout 05]. A micrograph of the receiver IC is shown in Figure 6.1. The outer dimensions of the chip are $1 \times 1.2\,mm^2$. The inductors of the LNA, the mixer and the VCO are visible (see Figure 6.1). The symmetrical layout of the LNA and mixers reduces the LO feed-through. A large area of the chip area is covered by on-chip NMOS-capacitors for blocking of the supply voltages.

6.2 Testboard

The chip was mounted on a Rogers RO4003 microwave substrate test-board for evaluation. The substrate has a thickness of $0.51\,mm^2$ and a dielectric constant of $\varepsilon = 3.38$.

The receiver shown in Figure 6.2 is bonded to the microwave substrate by a wedge-wedge bonder. The IC has a thickness of about 180 μm and is mounted on the surface in the middle of the microwave substrate. The bond wires have a diameter of 25 μm. Signal is guided through coupled microstrip lines to the microwave substrate. SMA connectors are mounted at the end of the microstrip lines.
A simplified schematic of the test-board with all connections is shown in Figure 6.3. All on-chip grounds are connected to the off-chip ground on the RO4003 substrate using multiple bondwires. The same applies to the power supply lines. Additionally, the power supply lines are blocked by off-chip capacitors. For measurements of the receiver testchip, the integrated VCO is locked by an external PLL with a reference signal $f_{REF} = f_{VCO}/8$ (see Figure 6.3). At the RF input, a 180°-hybrid is used to provide a differential signal from a single-ended input

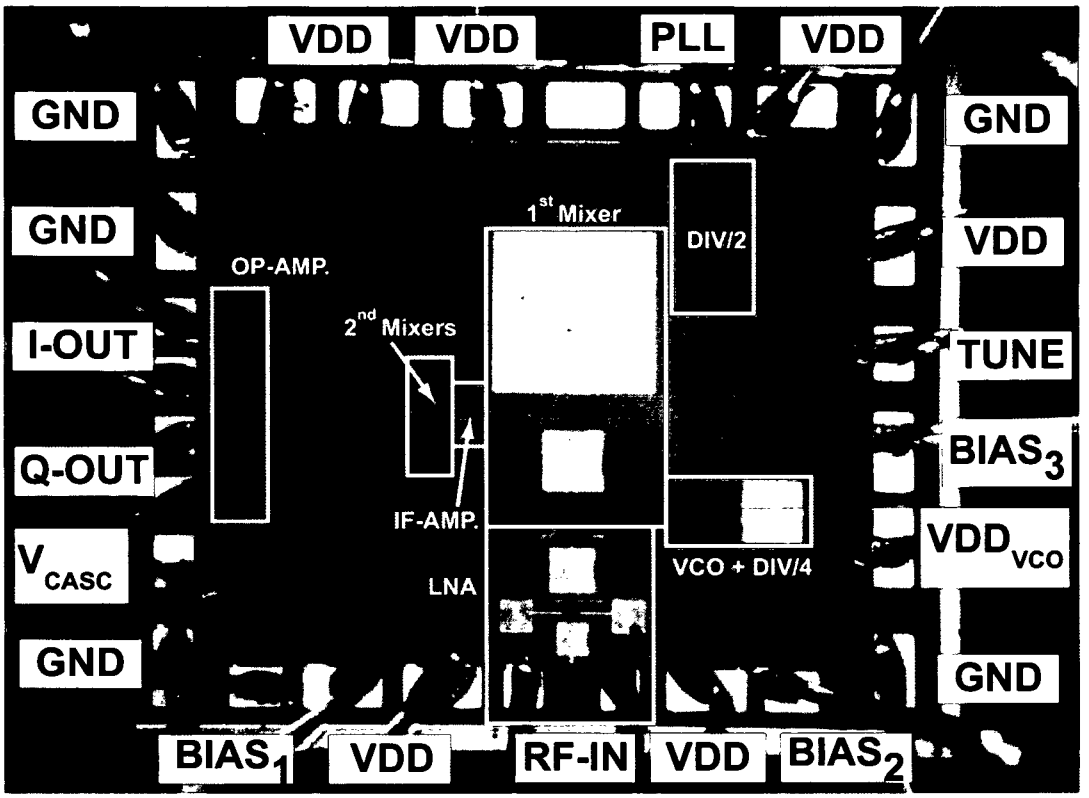

Figure 6.1: Chip photograph of the receiver testchip (chipsize $1 \times 1.2 mm^2$).

signal. BIAS-pins are not only the test points for DC measurements, but also have influence on the behaviour of the receiver. Additionally, the voltage of the cascode stage in the first mixer can be changed externally, which provides extra influence on the operating receiver chip.

Some of the presented measurement results are provided by the software tool *CIG-Measure V1.0* [Pöllendorf 04] which enables an automated measurement of power gain, single tone compression and two tone intermodulation of the receiver using the GBIP bus.

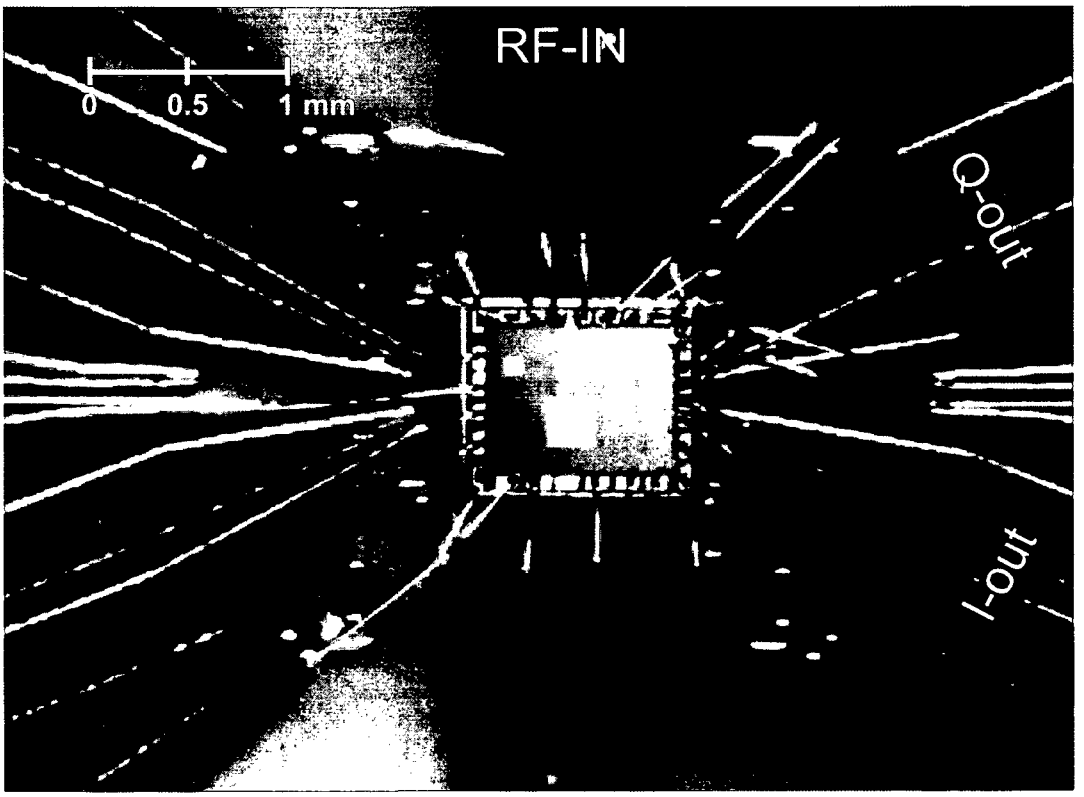

Figure 6.2: Photograph of the bonded chip on a test-board (chipsize $1 \times 1.2\,mm^2$).

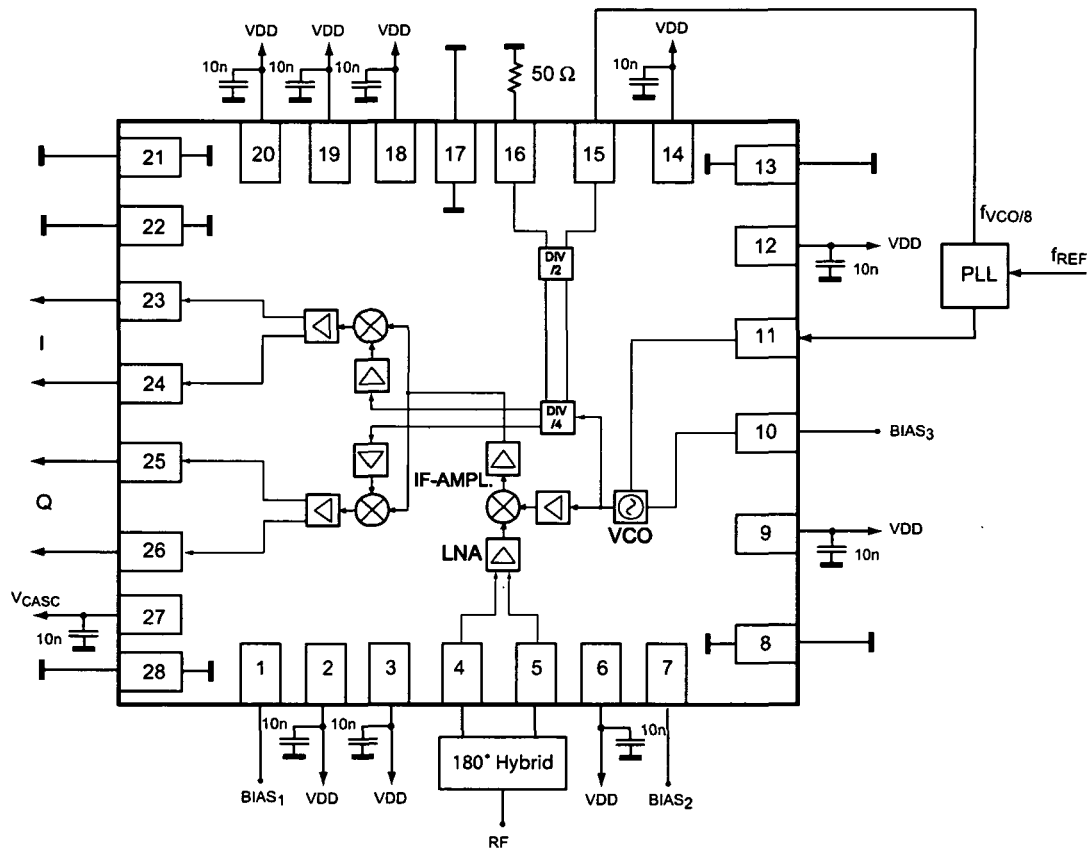

Figure 6.3: Application circuit of the receiver.

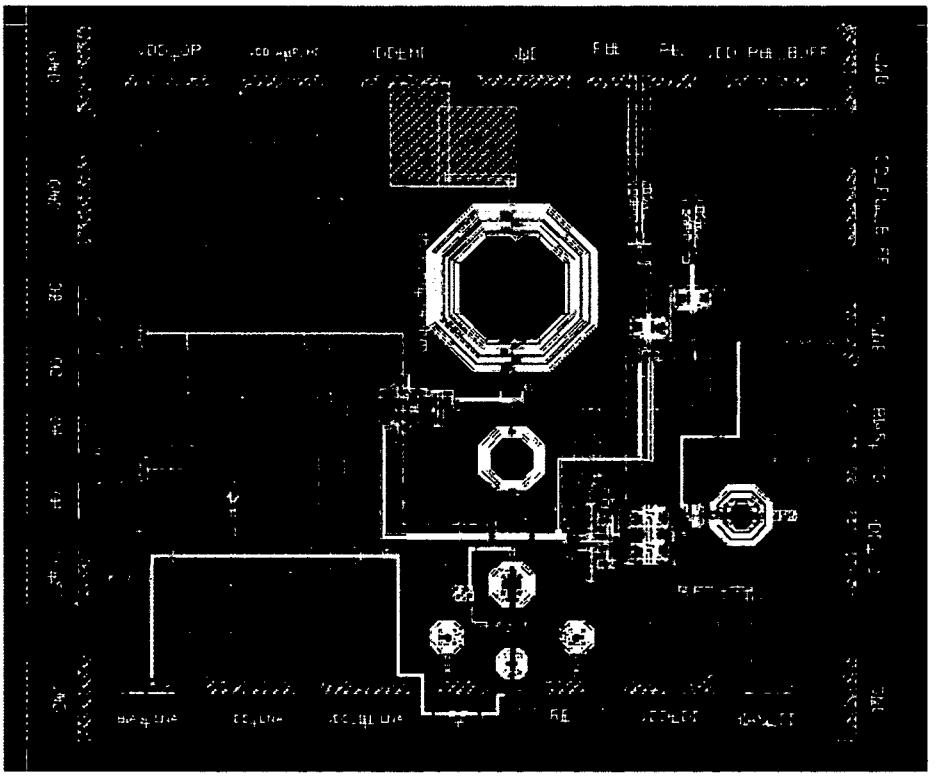

Figure 6.4: Layout of the receiver.

6.3 DC Power Consumption

Table 6.1 shows the measured current and power consumption of the entire chip. The receiver is designed for a supply voltage of 1.5 V, while the VCO runs on 1 V. The divider circuit and the buffers for the LO signal path dominate the total power consumption of the receiver.

Table 6.1: DC power consumption of receiver

	Current	Power
total power consumption RX	188.4 mW	127.7 mA
VCO	6.2 mW	6.2 mA
LNA	5.2 mW	3.5 mA
IF-amplifier	26.3 mW	17.5 mA
1^{st}-mixer	23.7 mW	15.8 mA
I/Q-mixers	5.5 mW	3.7 mA
VCO-buffer	11.5 mW	7.7 mA
I/Q-divider	32.2 mW	21.5 mA
I/Q-buffers	44.7 mW	29.8 mA
operational amplifiers	33.1 mW	22 mA

6.4 Input Reflection Coefficient at the RF-Input

The measured input reflection coefficient of the receive path is shown in Figure 6.5. This result includes the parasitics of the SMA connectors, bondwires and pads. The commonly accepted specification of -10 dB input reflection is met over the whole band.

6.5 Single-Tone Compression Measurement

For measurement of the single-tone compression, a 17.201 GHz signal is applied to the RF input. The frequency of the LO is set to 13.76 GHz with the help of an external PLL. By sweeping the power of the signal source, the 1dB-compression point is extracted from the measured baseband output signal. The result is presented in Figure 6.6. The receiver front-end shows excellent linearity up to -120 dBm input power. In the region of the compression-point, there is no sharp bend as the curve is smooth because the compression point is mostly determined by the cascade of the receiver building blocks, which are not perfectly adjusted. The simulated single-tone compression result is also plotted in Figure 6.6. A good match between simulation and measurement can be observed.

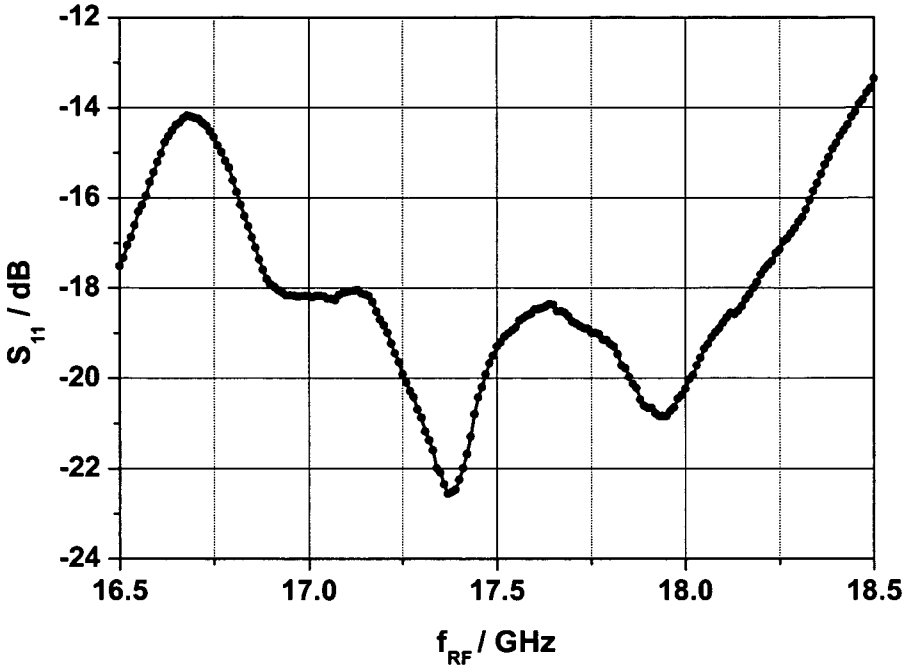

Figure 6.5: Input reflection coefficient (S_{11}).

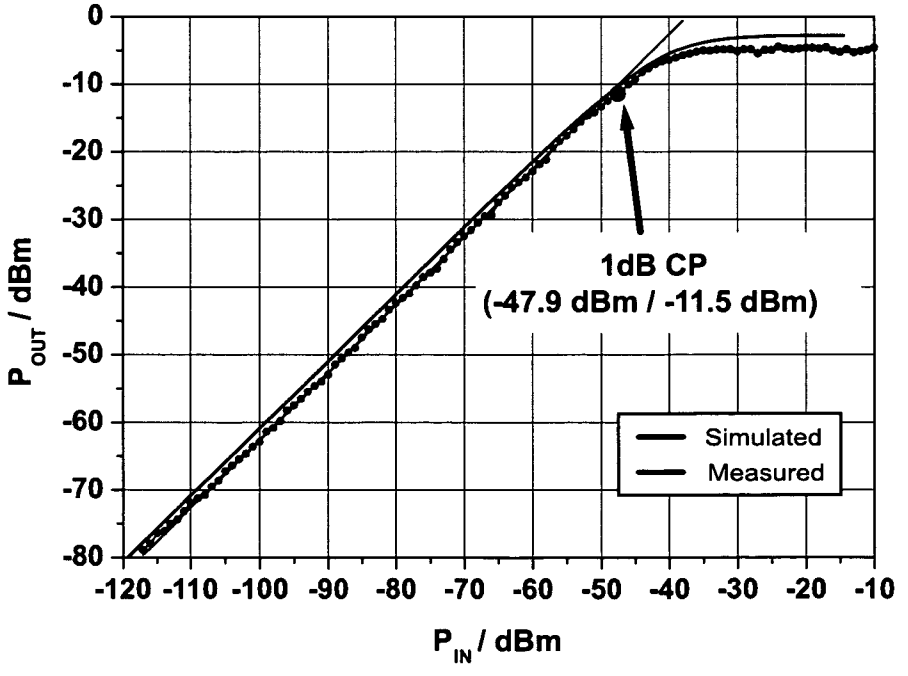

Figure 6.6: 1 dB compression point at 1 MHz output frequency.

6.6 Conversion Gain

Conversion gain of the receiver is measured by adjusting the VCO reference voltage with the external PLL to generate a 13.68 GHz LO signal. A 17.1 $GHz+x\,kHz$ signal is applied to the input terminal and further converted to baseband. Figure 6.7 shows the measured conversion gain versus frequency offset. The conversion gain is about 37.5 dB in a 200 MHz band.

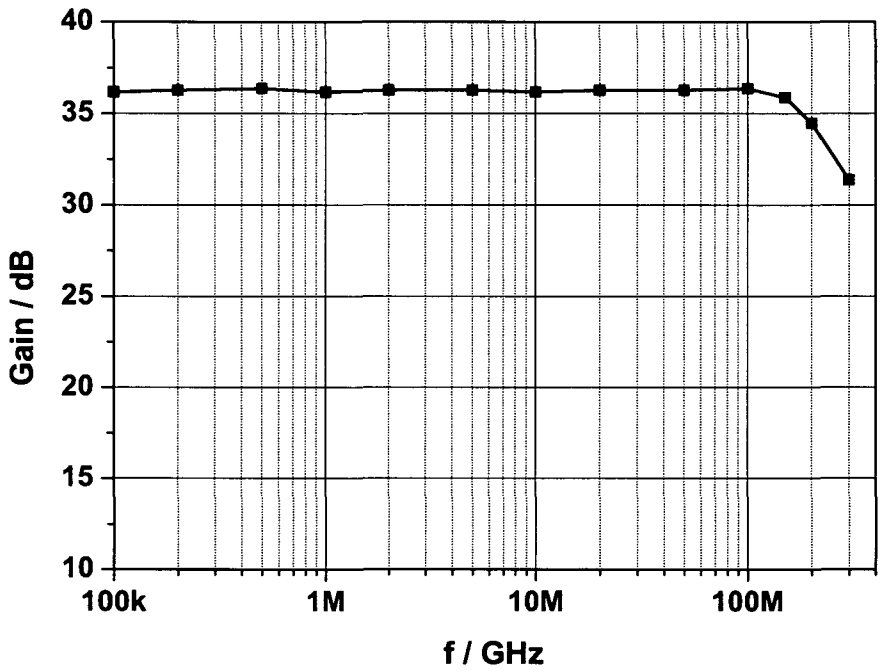

Figure 6.7: Conversion gain in the baseband.

The conversion gain at the WLAN/ISM band is measured by supplying a -67 dBm input signal, which is swept over the 17.2 GHz receive band. Each time the local oscillator is adjusted to track the RF signal with a frequency offset of 1 MHz. The power of the 1 MHz output signal is subsequently measured by a spectrum analyzer. The extracted conversion gain of the I-channel is shown in Figure 6.8. The center frequency of the receiver path clearly lies in the middle of the 17.2 GHz band.

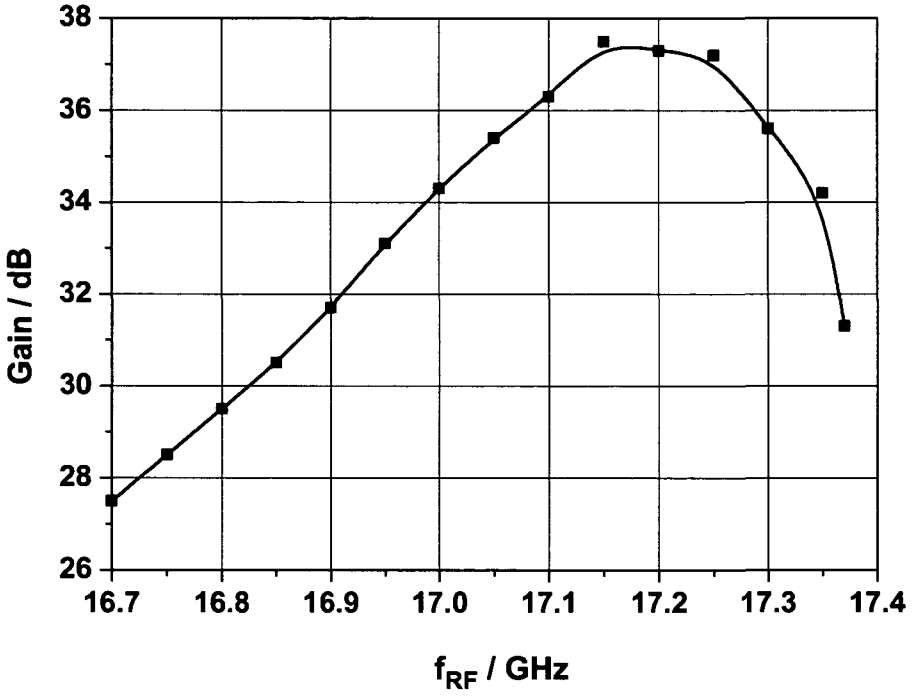

Figure 6.8: Conversion gain in the 17.2 GHz ISM band.

6.7 VCO Performance

As shown in the block diagram (see Figure 5.1 in Chapter 5), an additional 2:1 divider is implemented to provide an output for an external PLL. For measurements, an external mixer was used with a signal generator providing a reference signal. For the loop filter, a small test-board with a PI-characteristics was developed.

Figure 6.9 shows the tuning range of the locked PLL, using the on-chip varactors. A tuning from 13.35 GHz up to 13.87 GHz is possible, which is equivalent to a bandwidth of 0.52 MHz and a tuning range of 3.8%. The phase noise of the integrated VCO and external PLL is plotted in Figure 6.10. Additionally, the simulation result of the phase noise of an unlocked free running VCO is drawn. A comparison of the two results clearly indicates the locking of PLL.

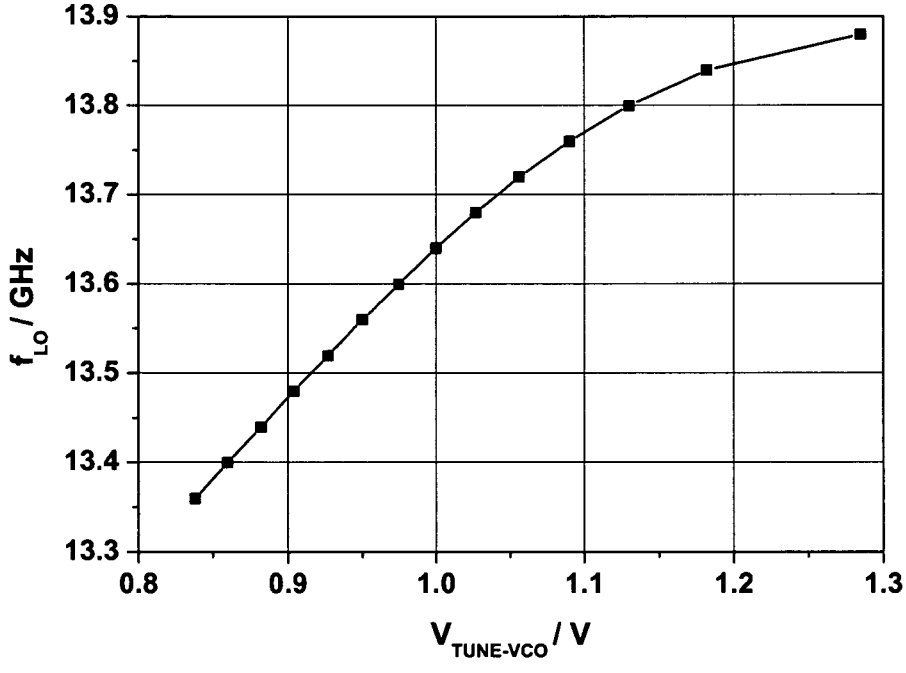

Figure 6.9: Measured frequency tuning of locked VCO.

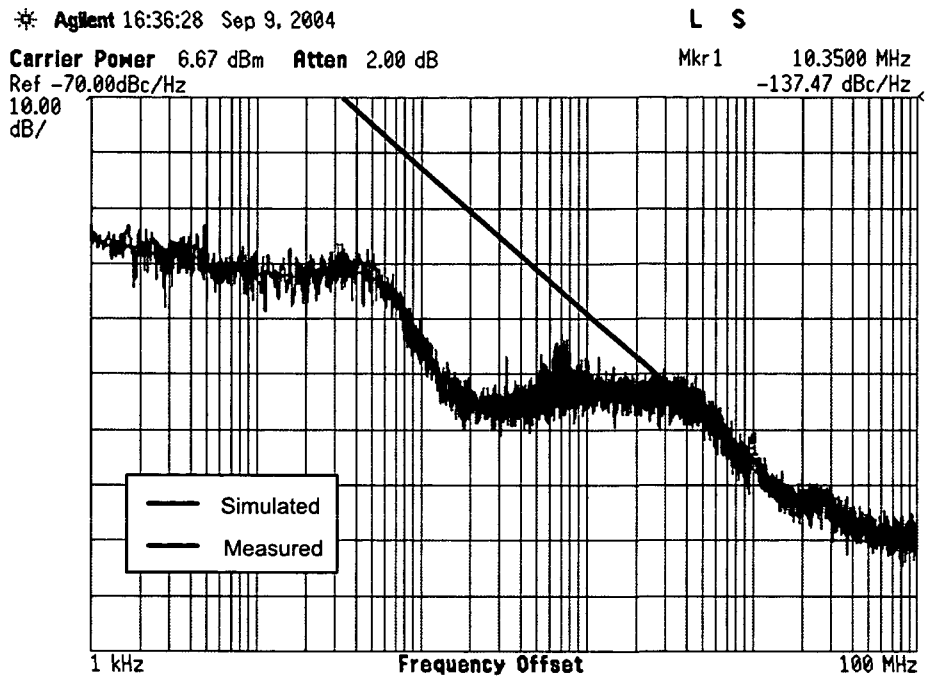

Figure 6.10: Measured phase noise of locked VCO compared to simulation of free running VCO.

6.8 Two-Tone Third-Order Intermodulation

Sensitivity to RF interferers is characterized by measuring the IP_3 value. The measurement setup includes two large interferers in the ISM band. The interferers are applied as RF input to the receive path using two calibrated RF sources, attenuators and a power combiner. The two interferers at 17.201 GHz and 17.2012 GHz generate an in-band third-order intermodulation product that is down-converted by multiplication with a 17.2 GHz local oscillator. By sweeping the power of the interferers, the IP_3 is extracted which is shown in Figure 6.11. The receiver features a measured input IP_3 of -37.4 dBm.

6.9 Noise Figure

The noise figure is measured by applying a 50 Ω noise source at the receiver input, measuring the output noise power with a spectrum analyzer and referring it back to the receiver input. At 1.5 V, the measured noise figure of the total receiver is 9.4 dB.

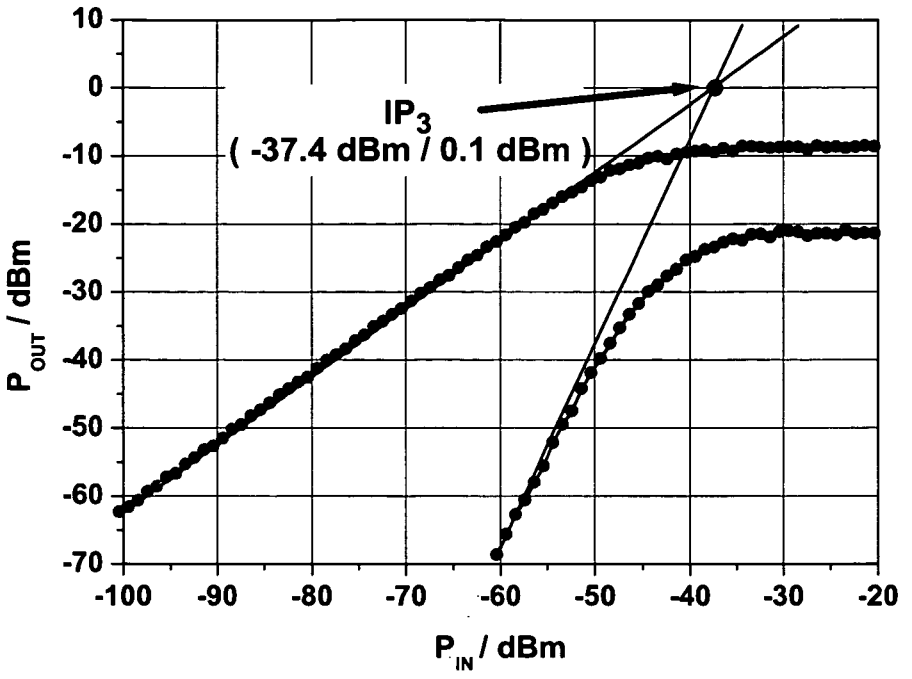

Figure 6.11: Measured IP_3 compression point performance.

6.10 LO Leakage Radiation at the RF-Input

To measure the LO leakage towards the antenna, the LNA input is directly connected to the spectrum analyzer. The local oscillator is swept from 13.35 GHz to 13.9 GHz by adjusting the VCO reference voltage by the external PLL. Figure 6.12 plots the LO power, which is measured by the spectrum analyzer. From Figure 6.12 can be observed that the LO power injected into the antenna is always below -60 dBm. As the receiver will use a narrow band antenna at 17.2 GHz which additionally helps to attenuate the LO leakage signal.

6.11 Performance Summary

The measured performance of the complete receiver is summarized in Table 6.2. The integrated 17 GHz receiver with a die areo of only $1.2\,mm^2$ in standard $0.13\,\mu$m CMOS technologies consumes 188.4 mW by a supply voltage of the receiver of 1.5 V and 1 V for the VCO, respectively. The maximum gain of 37.5 dB is achieved in the frequency range of 17.02-17.33 GHz. A noise figure of 9.4 dB was achieved along with an input 1dB-compression point of -47.9 dBm and an input IP_3 of -37.4 dBm, respectively. The phase noise of the locked PLL at 1 MHz offset frequency obtains to -123 dBc/Hz. The LO leakage for LO-frequencies is always

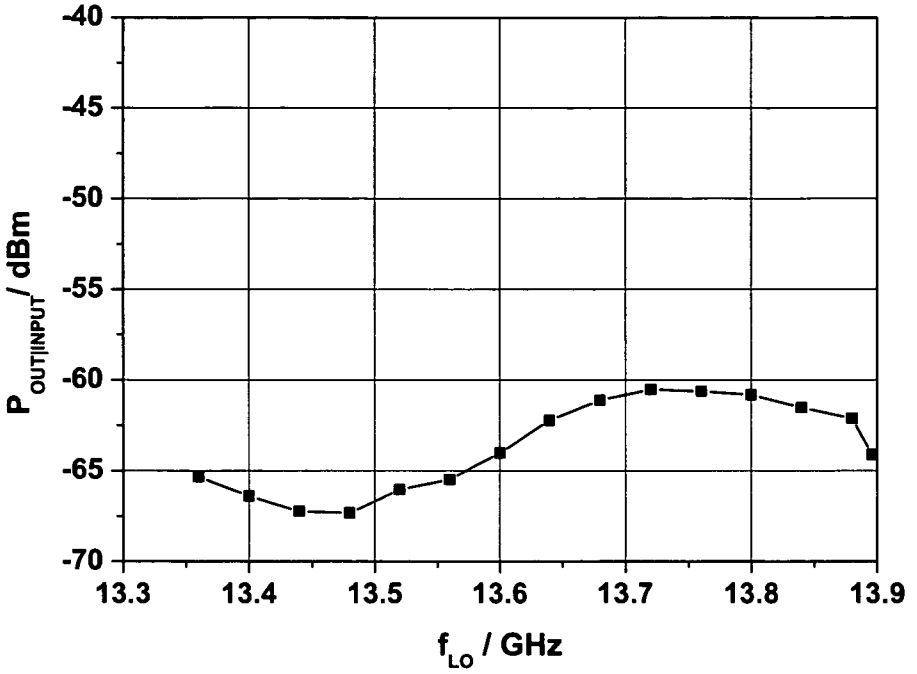

Figure 6.12: LO leakage radiation at the input port.

below -60 dBm. Measurements were performed using a 50GHz Agilent E4448A spectrum analyzer with noise figure option along with a preamplifier.

Table 6.2: Performance summary of complete receiver.

supply voltage RX	1.5 V
supply voltage VCO	1 V
3 dB bandwidth	17.02 - 17.33 GHz
S_{11}	<-12 dB
gain	37.5 dB
noise figure (SSB)	9.4 dB
RX input 1dB-CP	-47.9 dBm
RX input IP_3	-37.4 dBm
phase noise @ 1 MHz offset	-123 dBc/Hz
LO_1 leakage to RF	<-60.6 dBm
LO_2 leakage to RF	<-75.9 dBm
total power consumption	188.4 mW
die area	$1.2\,mm^2$
technology	standard 0.13 μm CMOS

Chapter 7

Conclusion and Outlook

The goal to integrate a complete receiver at 17.2 GHz in 0.13μm CMOS has been fulfilled. Detailed knowledge of the optimized passive and active integrated components, combined with careful circuit design and optimum architecture choice led to a demonstrator chip with excellent performance. The measured receiver is fully functional and is able to achieve sufficient gain and linearity to enable complex modulation schemes for WLAN communications. The receiver features a measured gain of 37.5 dB, an input 1 dB compression point of -47.9 dBm, an SSB noise figure of 9.4 dB and an input IP_3 of -37.4 dBm. At a power supply of 1.5 V, the receiver consumes only 188.4 mW, which is substantially low compared to 2 and 5 GHz receiver chips (Table 1.2). New circuits concepts were introduced and patented: LNA with tunable resonance frequency [Kienmayer 04,a] and bandpass ESD protection for LNAs [Kienmayer 04,b]. The next step will be the integration of the receiver presented here, together with a transmitter [Thüringer 03] and a frequency synthesizer [Tiebout 04].
The 17 GHz receiver presented in this work clearly demonstrates the feasibility of highest frequency RFIC design in standard 0.13 μm CMOS with existing products till 5 GHz along with research applications, i.e. short-range radar at 24 GHz for automotive applications. Due to the huge digital processing power required, system-on-chip integration in CMOS is very attractive and cost-efficient.

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